United Monolithic Semiconductors

CHA5266-FAB

10-16GHz Medium Power Amplifier

GaAs Monolithic Microwave IC in SMD Ceramic Hermetic package

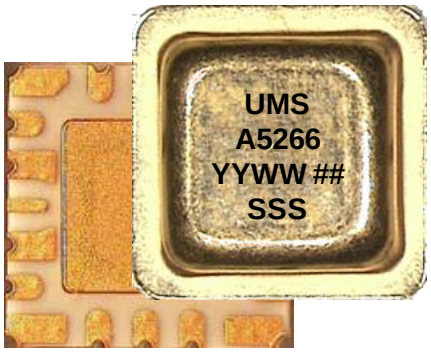
Description

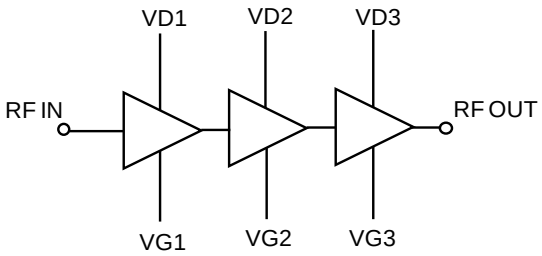
The CHA5266-FAB is a three stage monolithic GaAs medium power amplifier in leadless surface mount hermetic metal ceramic 6x6mm² package.

It is designed for a wide range of applications, from military to commercial communication systems.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

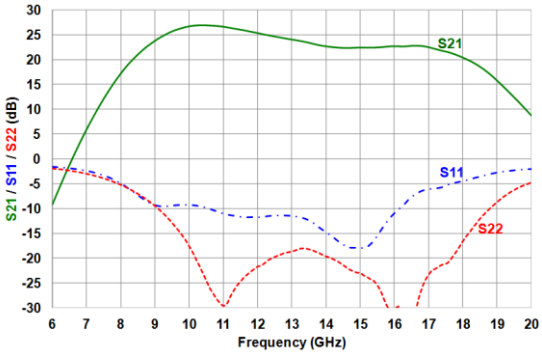
It is supplied in RoHS compliant SMD package.





Main Features

- Broadband performances: 10-16GHz
- 24dB Linear Gain
- 26dBm output power @ 1dB comp.
- 35.5dBm output IP3
- DC bias: Vd = 5.0Volt @Idq = 320mA
- 6x6mm² hermetic metal ceramic package



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	10		16	GHz
Gain	Linear Gain		24		dB
P1dB	Output power @ 1dB compression		26		dBm
OIP3	Output IP3		35.5		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +5V / Idq=320mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	10		16	GHz
Gain	Linear Gain		24		dB
RL_in	Input Return Loss		11		dB
RL_out	Output Return Loss		20		dB
P1dB	Output power @ 1dB compression		26		dBm
Psat	Saturated output power		27.5		dBm
OIP3	Output IP3		35.5		dBm
Idq	Quiescent Drain current		320		mA
Vg	Gate Voltage		-0.35		V

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	7.0V	V
Idq	Drain bias current	0.525	A
Vg	Gate bias voltage	-2 to 0	V
Pin	Input continuous power	20	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Biasing Options

Four biasing options are recommended

Biasing option 1	Standard biasing
	Vd1 = Vd2 = Vd3 = 5.0V and Vg1 = Vg2 = Vg3 tuned to get Idq = 320mA at Tamb. =25°C. Typical P1dB = 26dBm / Typical OIP3 = 35.5dBm

Biasing option 2	Reduced voltage (Vd) compensated by higher current (Idq)
	Vd1 = Vd2 = Vd3 = 4.5V and Vg1 = Vg2 = Vg3 tuned to get Idq = 360mA at Tamb. = 25°C. Typical P1dB = 25.5dBm / Typical OIP3 = 35.5dBm

Biasing option 3	Reduced current (Idq)
	Vd1 = Vd2 = Vd3 = 5.0V and Vg1 = Vg2 = Vg3 tuned to get Idq = 280mA at Tamb. = 25°C. Typical P1dB = 25dBm / Typical OIP3 = 35dBm

Biasing option 4	Reduced voltage (Vd)
	Vd1 = Vd2 = Vd3 = 4.5V and Vg1 = Vg2 = Vg3 tuned to get Idq = 320mA at Tamb. = 25°C. Typical P1dB = 25.5dBm / Typical OIP3 = 35.5dBm

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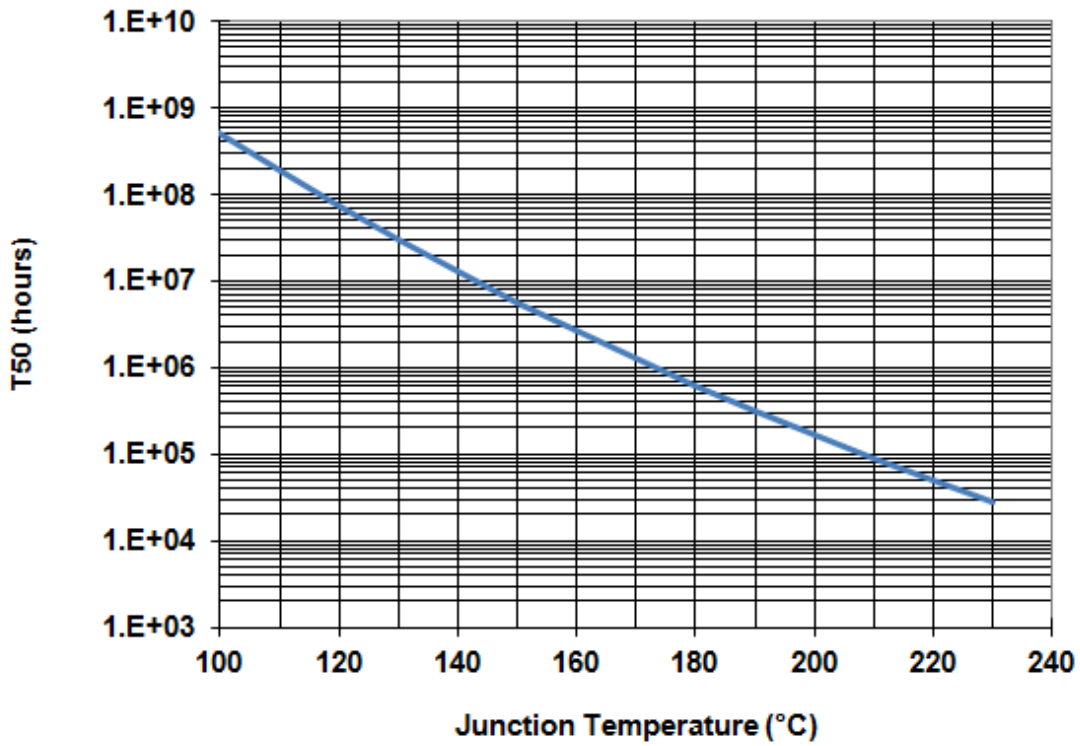
Device thermal performances

All the figures given in this section are obtained assuming that the packaged device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	Vd = 5V Idq = 290mA(2) Pdiss = 1.46W	132	32	02E+07

(1) Assuming 85°C Tcase
(2) Idq at 85°C Tcase when Vg set to get Idq = 320mA at 25°C Tcase



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Typical Package Sij parameters

Tamb.= +25°C, Vd = +5V, Id = 320mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2.0	-1.06	77.6	-66.06	-7.4	-36.32	176.2	-1.24	90.4
3.0	-1.08	31.9	-67.50	-53.4	-27.87	-38.5	-1.26	46.3
4.0	-1.14	-10.5	-73.22	-83.5	-32.79	-55.8	-1.36	0.6
5.0	-1.28	-50.4	-82.48	-111.4	-25.02	-49.3	-1.57	-46.8
6.0	-1.58	-89.7	-70.66	141.3	-9.18	-66.9	-1.95	-99.2
7.0	-2.39	-131.1	-66.11	105.9	5.96	-140.7	-3.02	-157.6
8.0	-4.94	-175.1	-59.25	64.2	17.22	117.0	-5.24	137.5
9.0	-9.32	159.5	-58.50	17.8	23.82	3.5	-9.50	64.8
10.0	-9.27	125.1	-56.02	12.7	26.74	-109.3	-17.62	-13.5
11.0	-11.04	49.9	-50.45	-33.6	26.66	147.2	-29.63	-27.7
12.0	-11.74	-34.4	-49.10	-87.2	25.38	58.2	-21.72	-61.7
13.0	-11.52	-96.4	-48.07	-141.9	24.07	-21.3	-18.66	-125.5
14.0	-14.77	-134.2	-48.46	171.8	22.70	-95.5	-19.67	168.0
15.0	-17.90	-115.9	-46.49	139.4	22.44	-166.2	-23.01	125.2
16.0	-10.93	-103.7	-43.76	80.3	22.72	116.2	-30.45	99.3
17.0	-6.09	-138.8	-45.51	13.0	22.53	26.8	-23.39	110.5
18.0	-4.46	-165.7	-48.27	17.4	20.43	-68.3	-16.60	64.6
19.0	-2.75	164.3	-48.35	-20.4	15.80	-167.4	-8.72	9.1
20.0	-2.05	128.3	-47.81	-49.4	8.78	107.0	-4.78	-44.8
21.0	-2.46	89.5	-52.98	-105.5	1.43	35.5	-2.82	-87.5
22.0	-2.76	43.0	-63.84	63.1	-5.52	-31.4	-1.88	-122.0
23.0	-3.31	-13.9	-62.88	17.0	-12.69	-94.8	-1.28	-151.0
24.0	-3.28	-74.3	-51.34	-56.4	-20.37	-153.4	-0.96	-176.5
25.0	-2.63	-126.3	-44.90	-76.9	-29.35	159.1	-0.74	161.7
26.0	-1.96	-166.4	-48.04	-62.3	-39.22	102.3	-0.51	142.1
27.0	-1.47	161.8	-49.38	-82.8	-49.55	39.0	-0.39	122.5
28.0	-1.16	134.6	-52.90	-135.9	-61.44	-30.6	-0.25	103.5
29.0	-0.90	109.4	-50.93	-166.0	-54.80	-155.5	-0.17	85.8
30.0	-0.84	85.1	-54.66	0.1	-54.18	-1.0	-0.15	68.8
31.0	-0.92	62.1	-46.56	-59.4	-46.55	-57.9	-0.22	51.9
32.0	-0.98	39.3	-49.17	-76.8	-47.97	-88.4	-0.38	34.8
33.0	-0.96	14.9	-43.55	-130.4	-43.64	-129.7	-0.38	17.4
34.0	-1.01	-11.5	-43.86	-123.3	-44.28	-120.3	-0.37	0.8
35.0	-1.09	-40.1	-43.13	-151.0	-43.28	-152.5	-0.46	-16.5
36.0	-1.22	-71.3	-42.50	-179.9	-42.32	-178.7	-0.50	-36.1
37.0	-1.37	-104.0	-45.54	177.8	-45.58	175.8	-0.51	-54.7
38.0	-1.44	-138.7	-45.04	170.6	-45.21	171.0	-0.58	-72.8
39.0	-1.46	-172.6	-44.50	146.3	-44.59	144.2	-0.59	-94.4
40.0	-1.33	153.7	-52.83	134.6	-53.51	138.0	-0.31	-116.9

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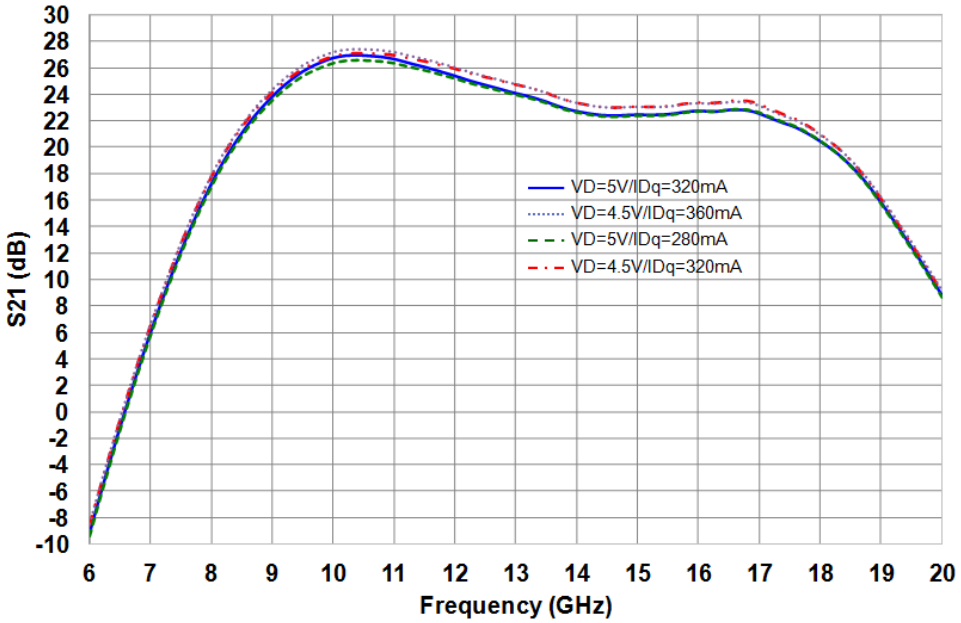
Typical test fixture Measurements

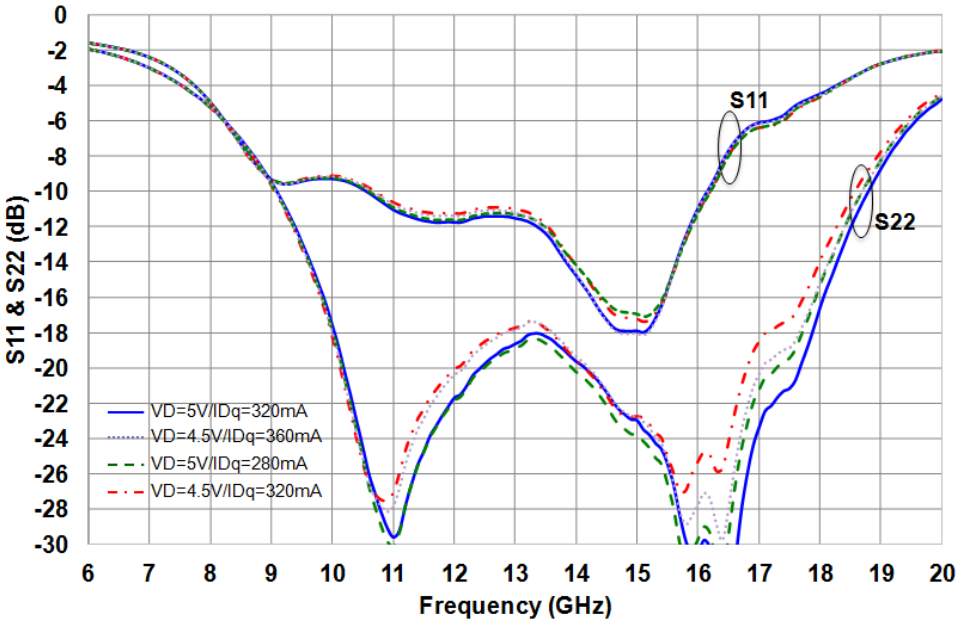
Tamb.= +25°C, Biasing conditions :

a) Vd = +5.0V, Idq = 320mA
b) Vd = +4.5V, Id = 360mA
c) Vd = +5V, Idq = 280mA
d) Vd = +4.5V, Idq = 320mA

S21 versus frequency for several biasing conditions



S11 and S22 versus frequency for several biasing conditions



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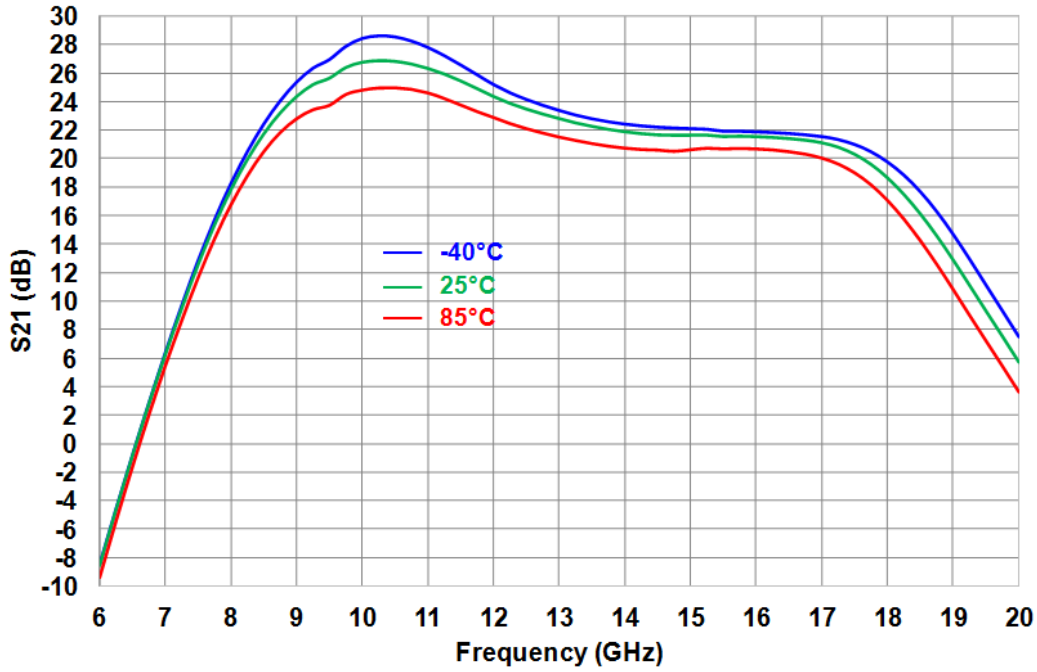
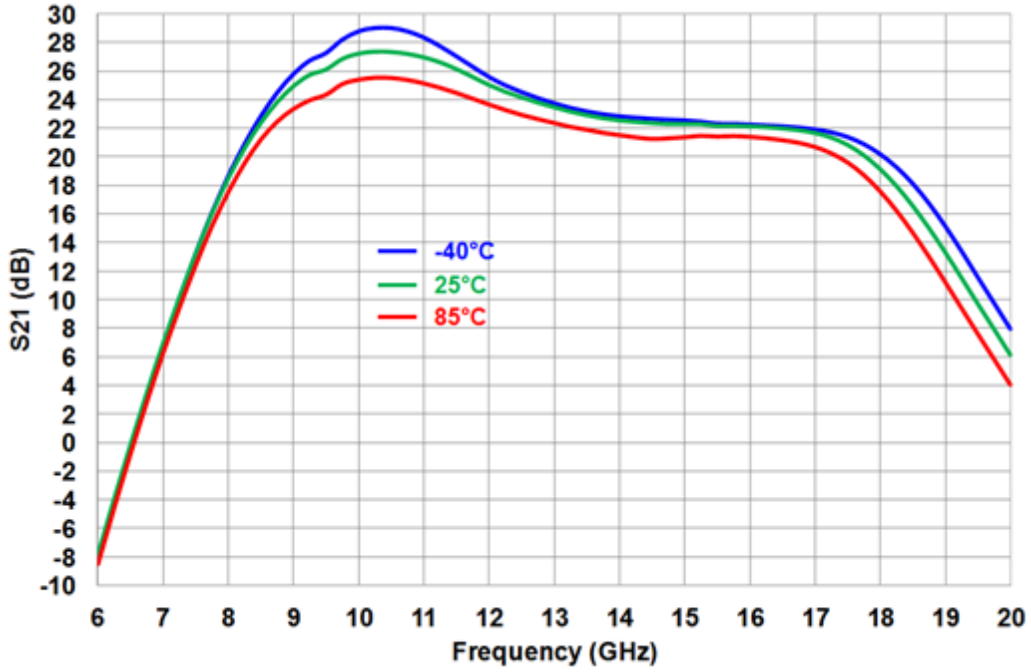
Typical test fixture Measurements

S21 versus frequency & temperature
Vd = +5V / Idq@ Tcase=25°C = 320mA



S21 versus frequency & temperature
Vd = +4.5V / Idq@ Tcase=25°C = 360mA



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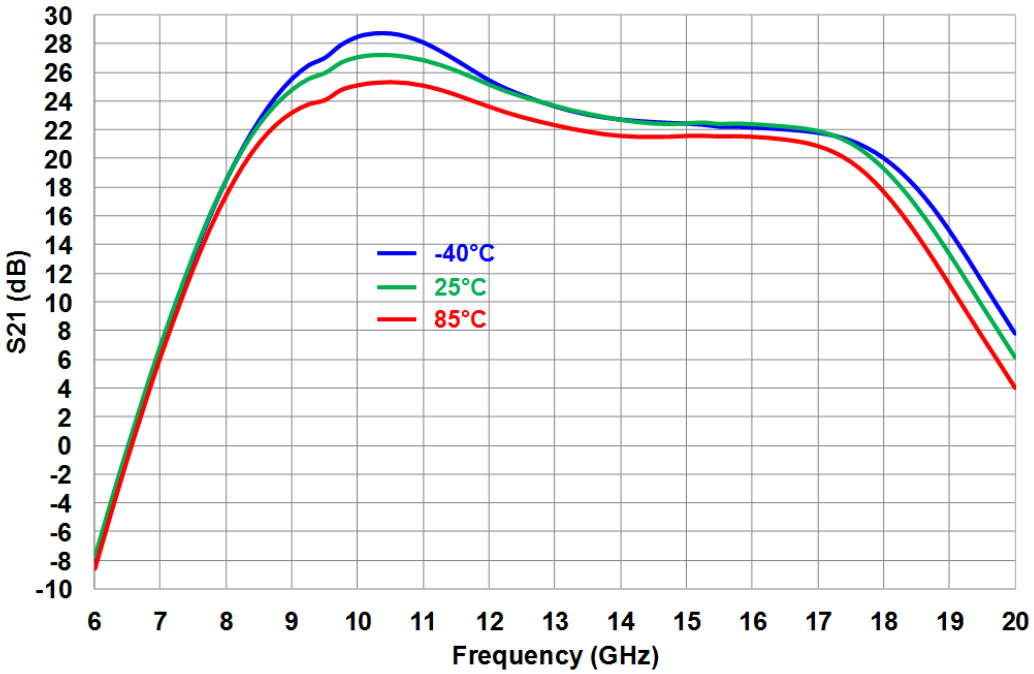
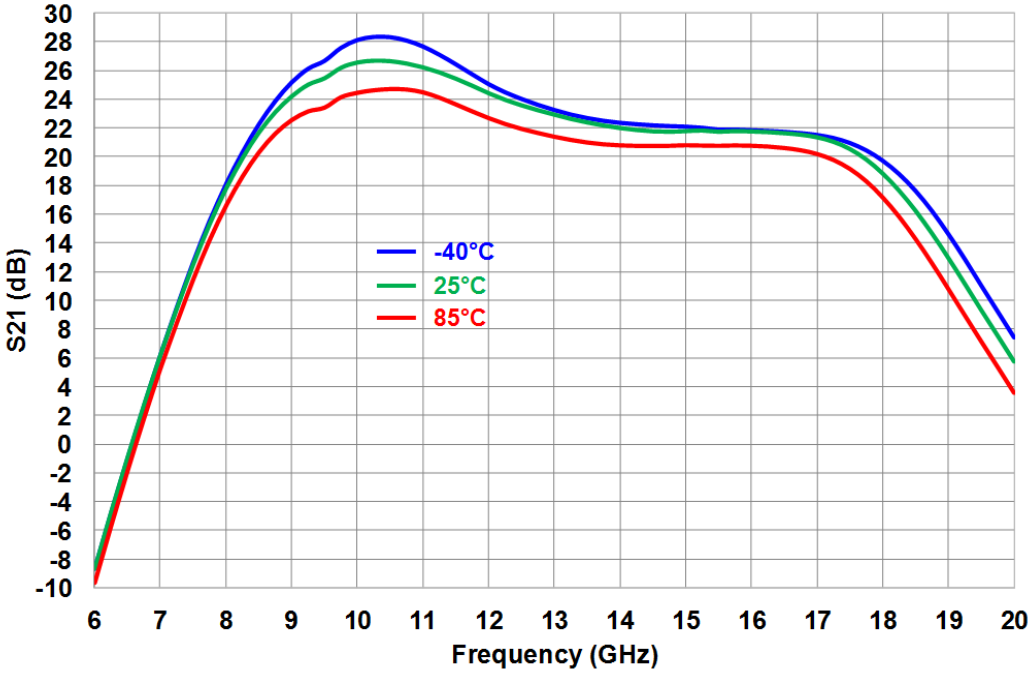
Typical test fixture Measurements

S21 versus frequency & temperature
Vd = +4.5V / Idq$_{@\ Tcase=25°C}$ = 320mA



S21 versus frequency & temperature
Vd = +5V / Idq$_{@\ Tcase=25°C}$ = 280mA



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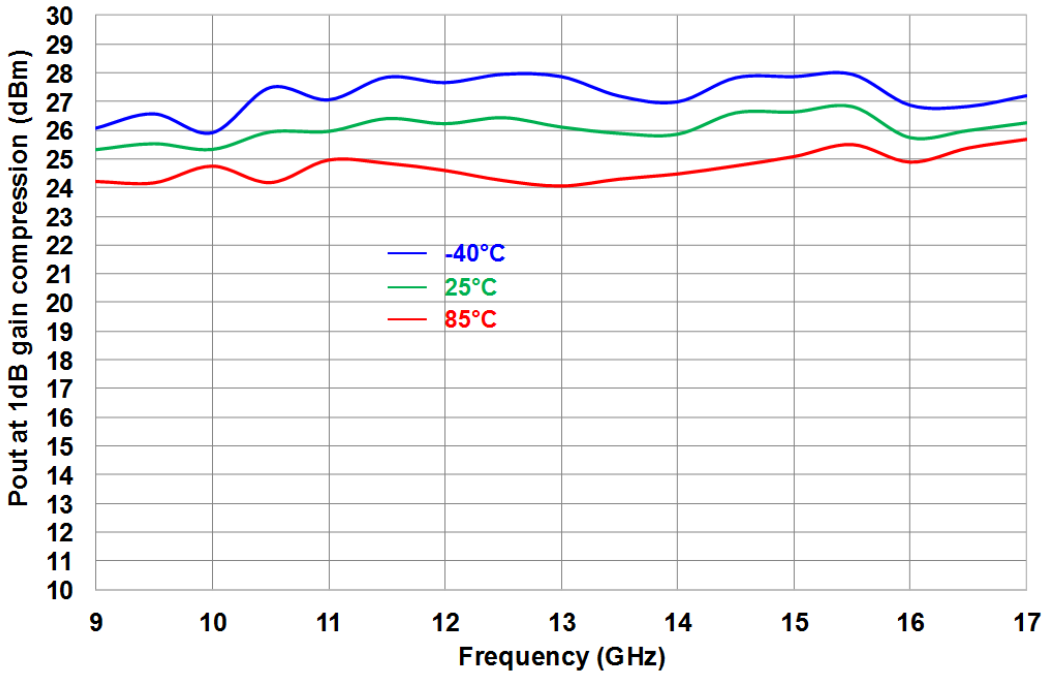
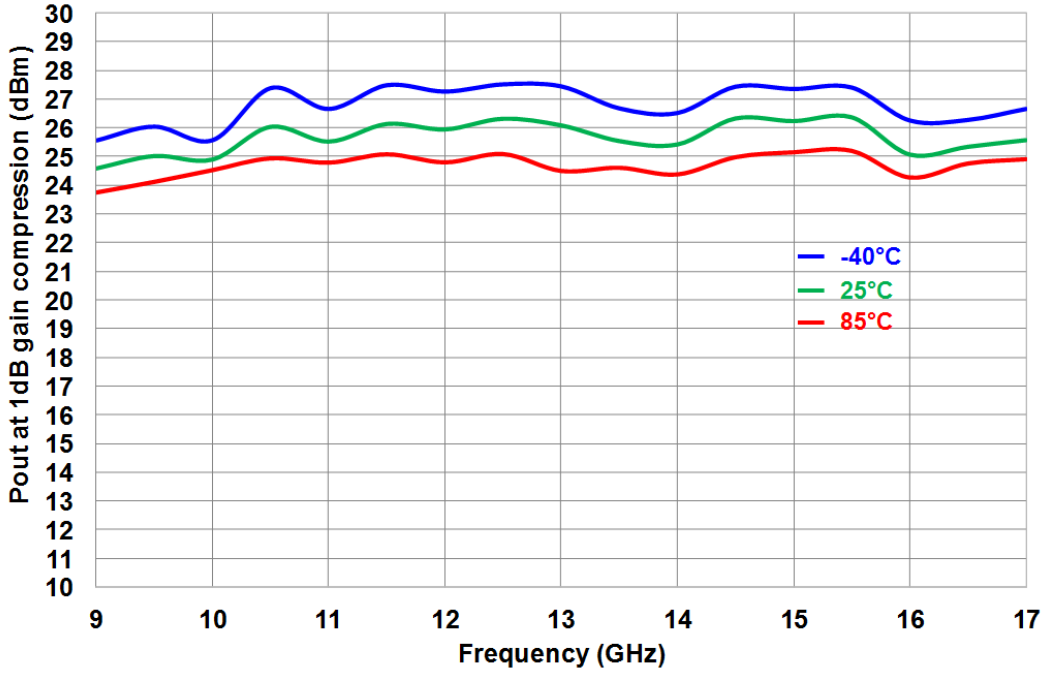
Typical test fixture Measurements

Output power at 1dB gain compression
Vd = +5V / Idq@ Tcase=25°C = 320mA



Output power at 1dB gain compression
Vd = +4.5V / Idq@ Tcase=25°C = 360mA



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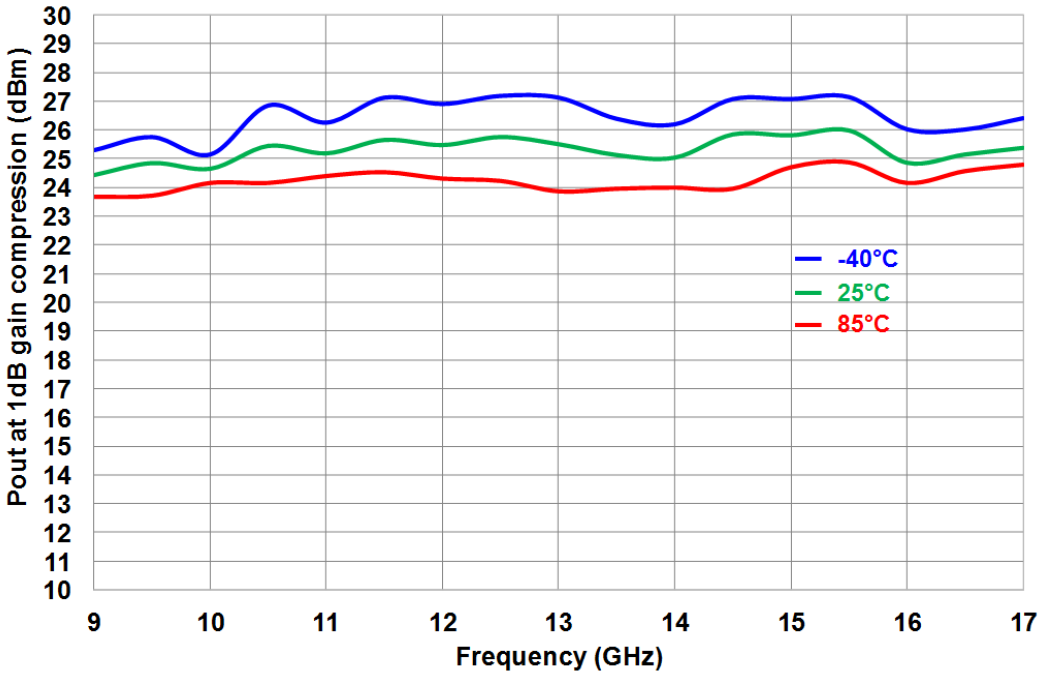
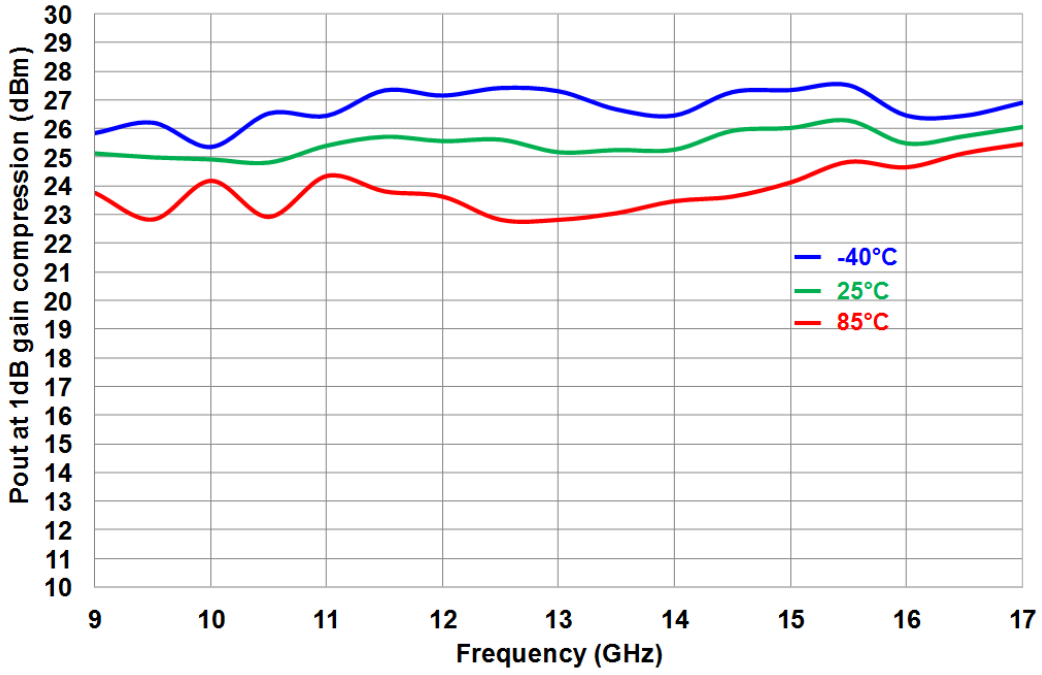
Typical test fixture Measurements

Output power at 1dB gain compression
Vd = +4.5V / Idq@ Tcase=25°C = 320mA



Output power at 1dB gain compression
Vd = +5V / Idq@ Tcase=25°C = 280mA



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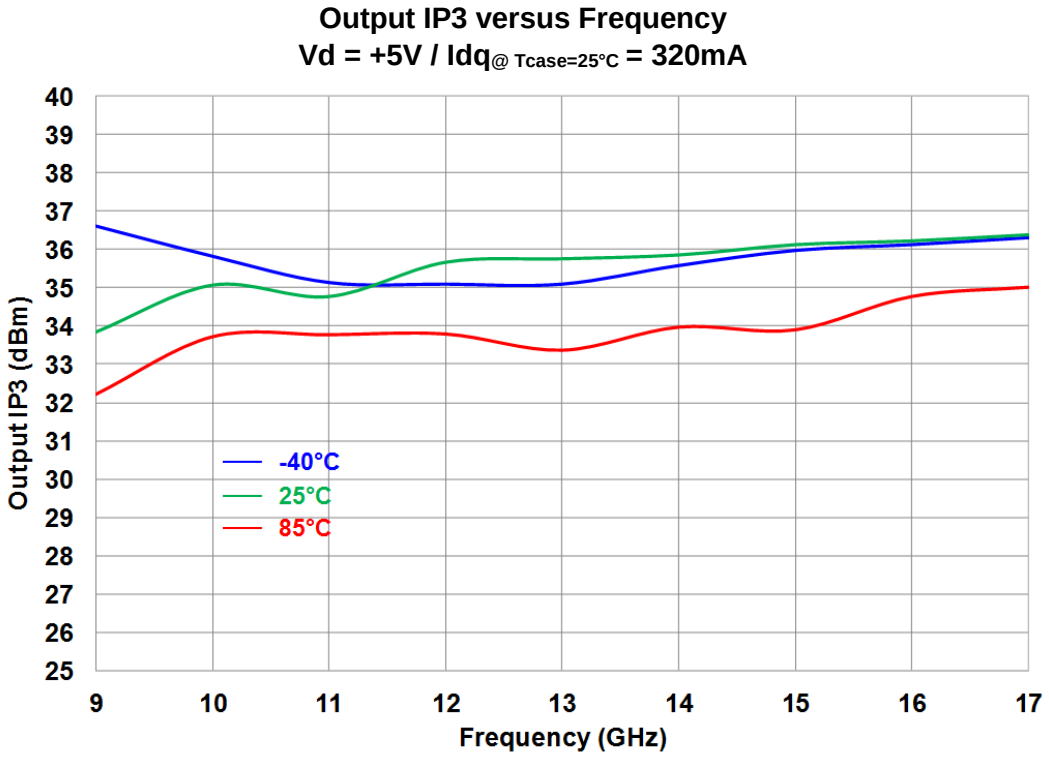
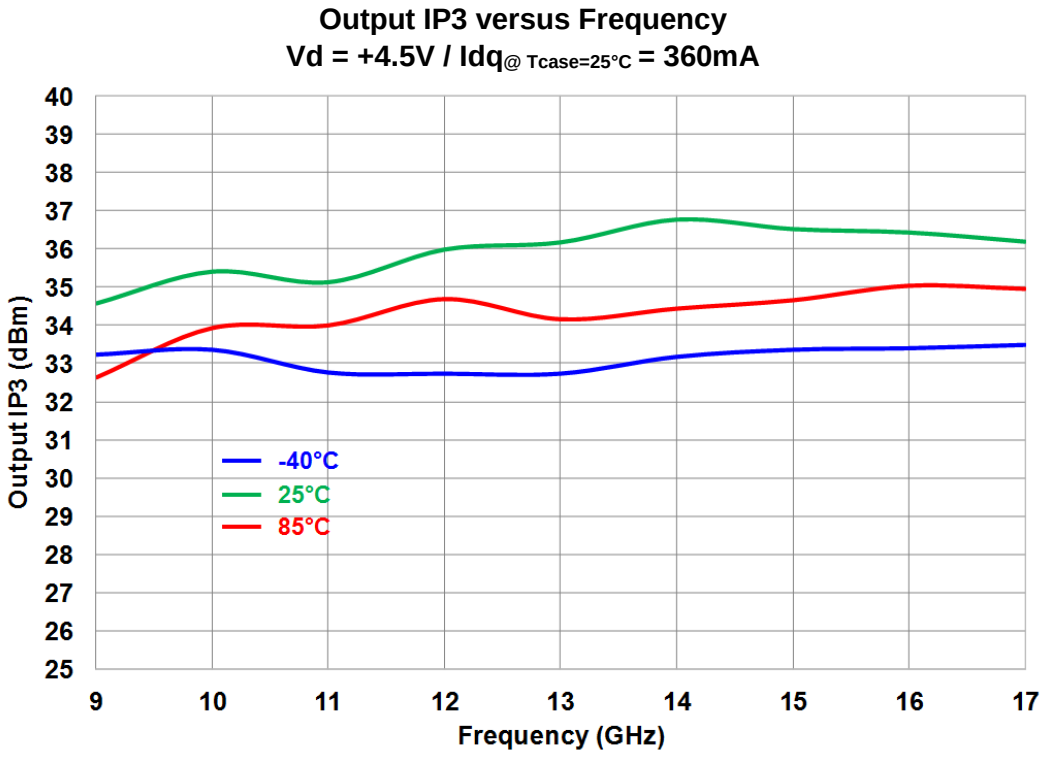
Typical test fixture Measurements





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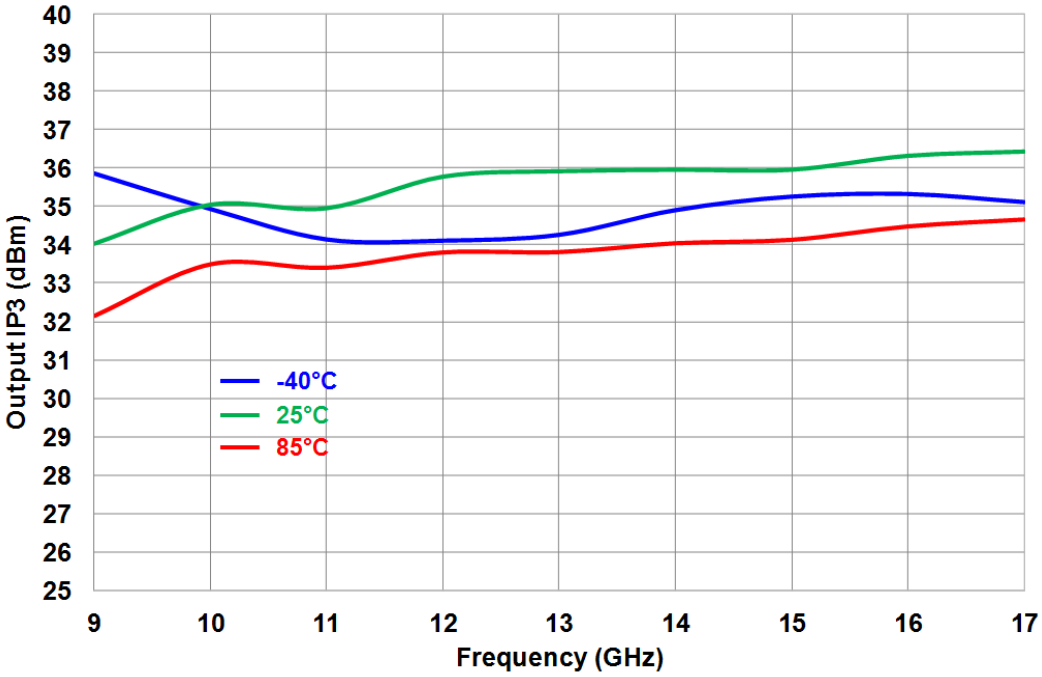
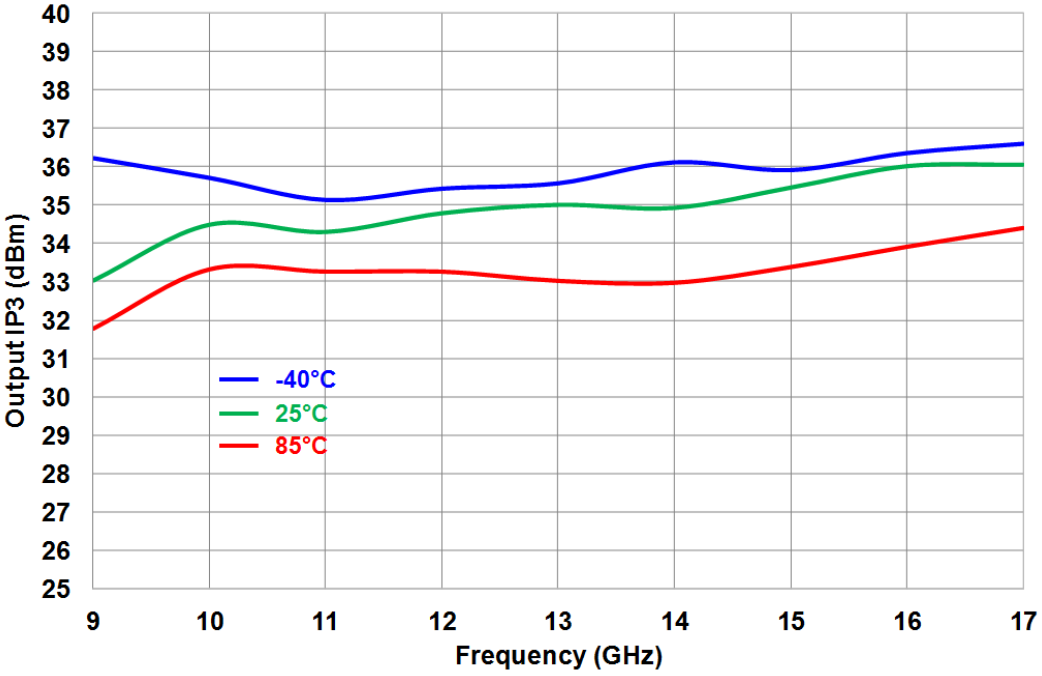
Typical test fixture Measurements

Output IP3 versus Frequency
Vd = +4.5V / Idq@ Tcase=25°C = 320mA



Output IP3 versus Frequency
Vd = +5V / Idq@ Tcase=25°C = 280mA



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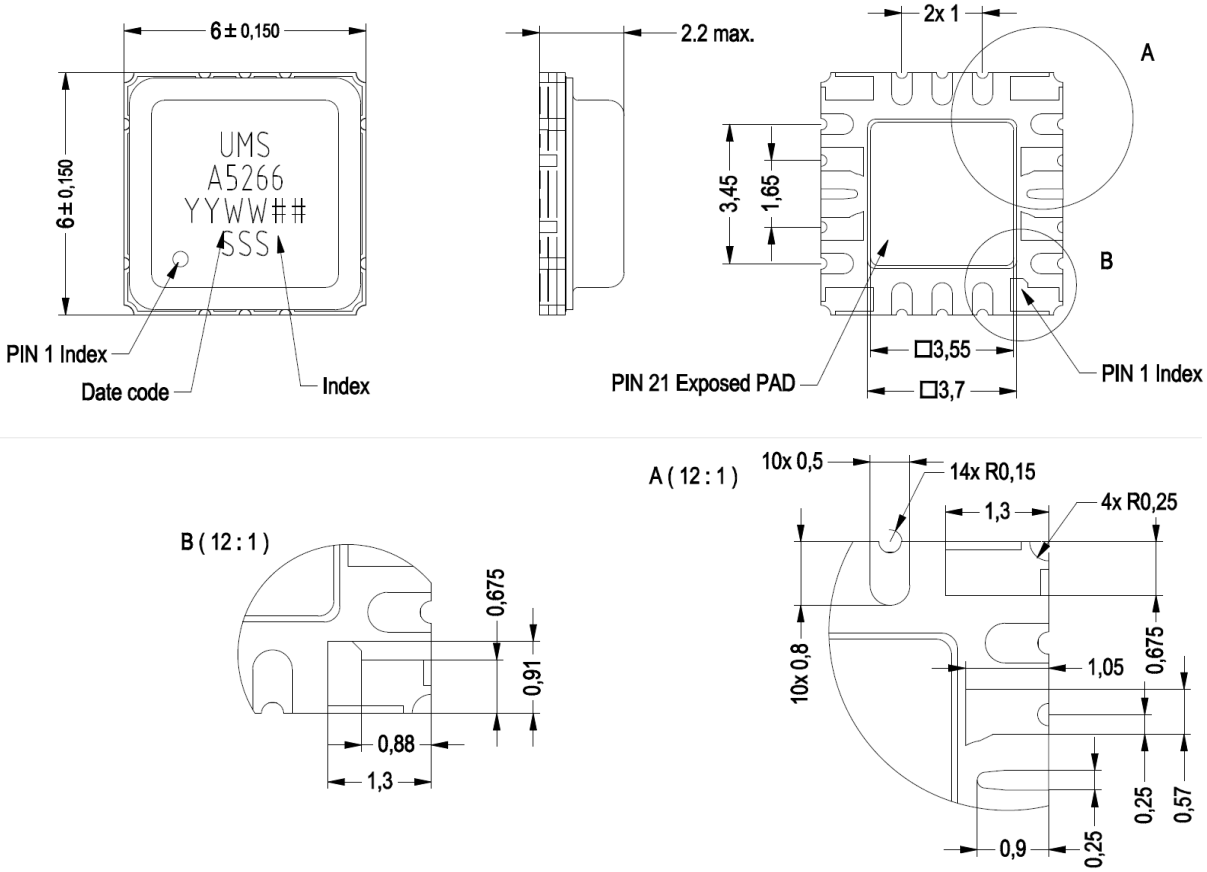
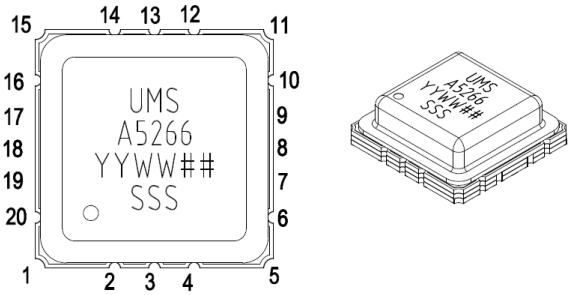
Package outline





1- GND	8- RF OUT	15- GND
2- VG1	9- GND	16- Nc
3- VG2	10- Nc	17- GND
4- VG3	11- GND	18- RF IN
5- GND	12- VD3	19- GND
6- Nc	13- VD2	20- Nc
7- GND	14- VD1	21- GND

Units : mm

It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0024 (https://www.ums-rf.com) for exact package dimensions.
(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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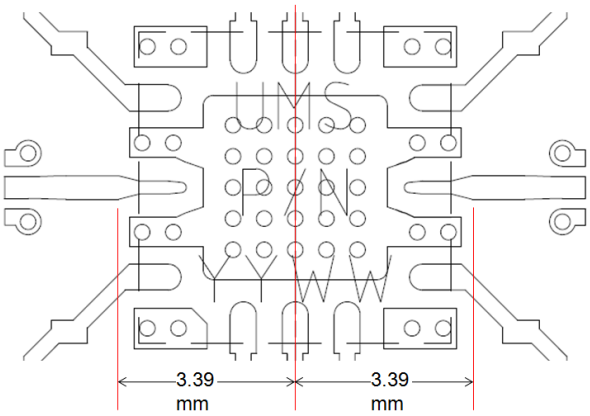
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.39mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



Package Information

Parameter	Value
Package body material	RoHS-compliant
Lead finish	Gold
Hermetic sealing (fine leak compliant Mil-Std-883 Method 1014.10 Condition A4, tracer gas He at 1atm)	$1x10^{-8}$ ccHe/s/atm

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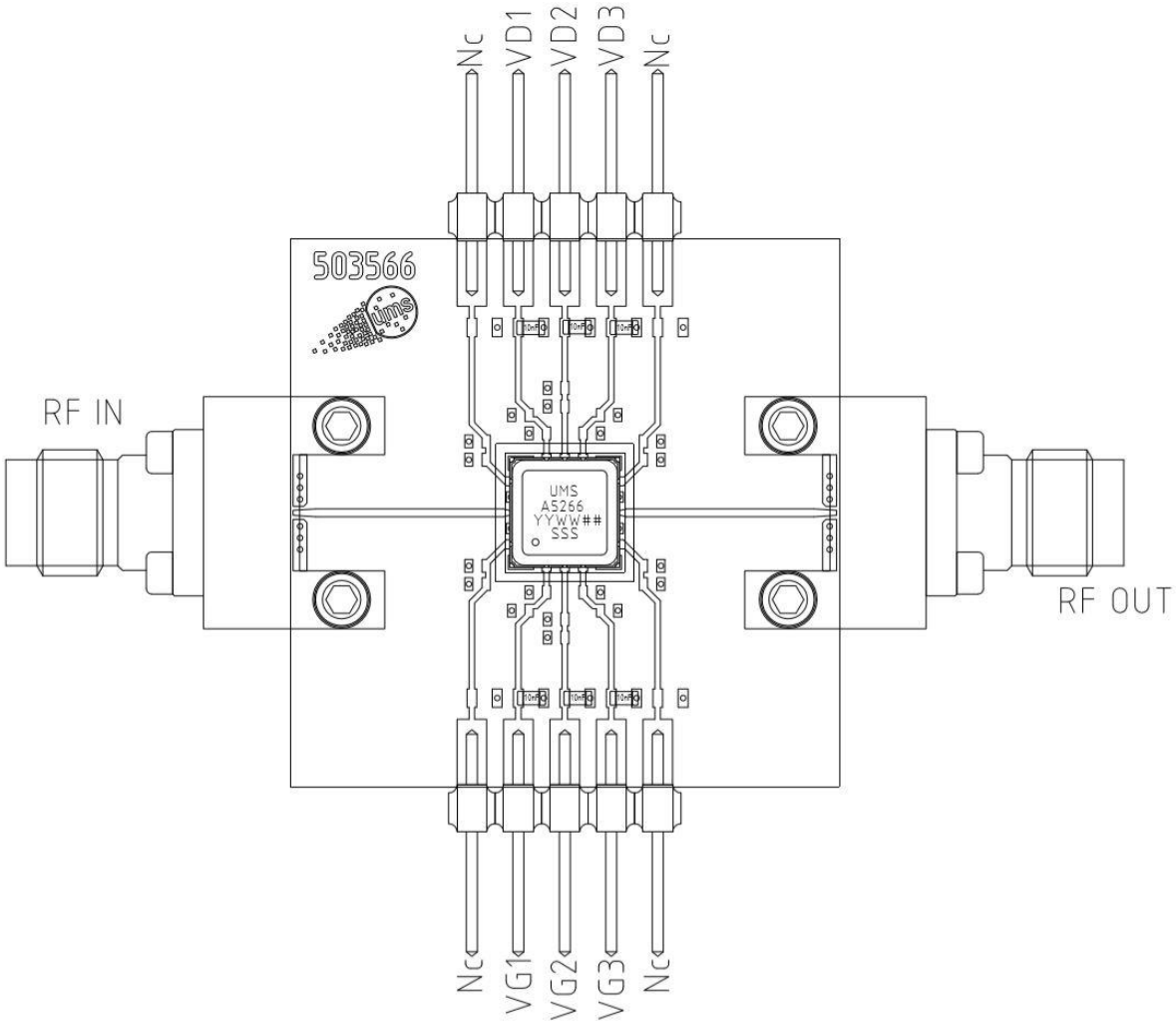
Evaluation board description

■ Compatible with the proposed footprint.
■ Based on typically Ro4003 / 8mils or equivalent.
■ Using a micro-strip to coplanar transition to access the package.
■ Recommended for the implementation of this product on a module board.
■ Decoupling capacitors of 10nF are recommended on each DC access (Vg1 / Vg2 / Vg3 / Vd1 / Vd2 / Vd3)



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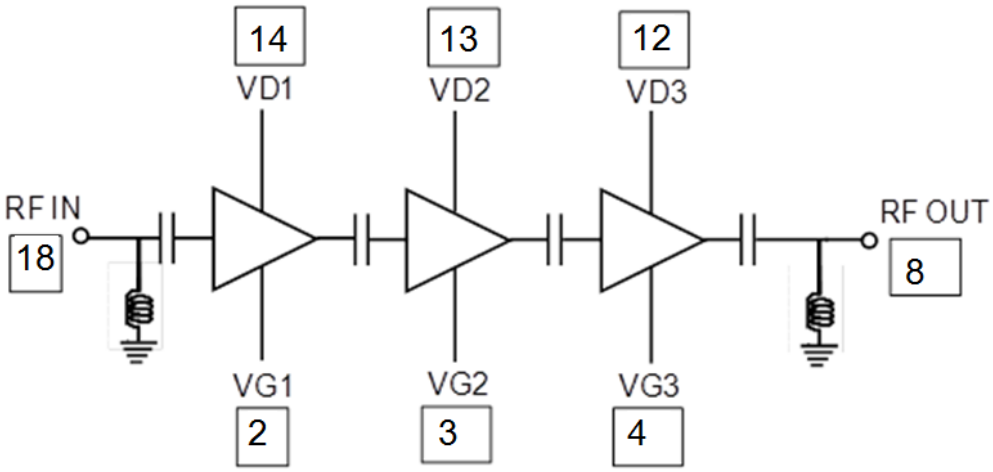
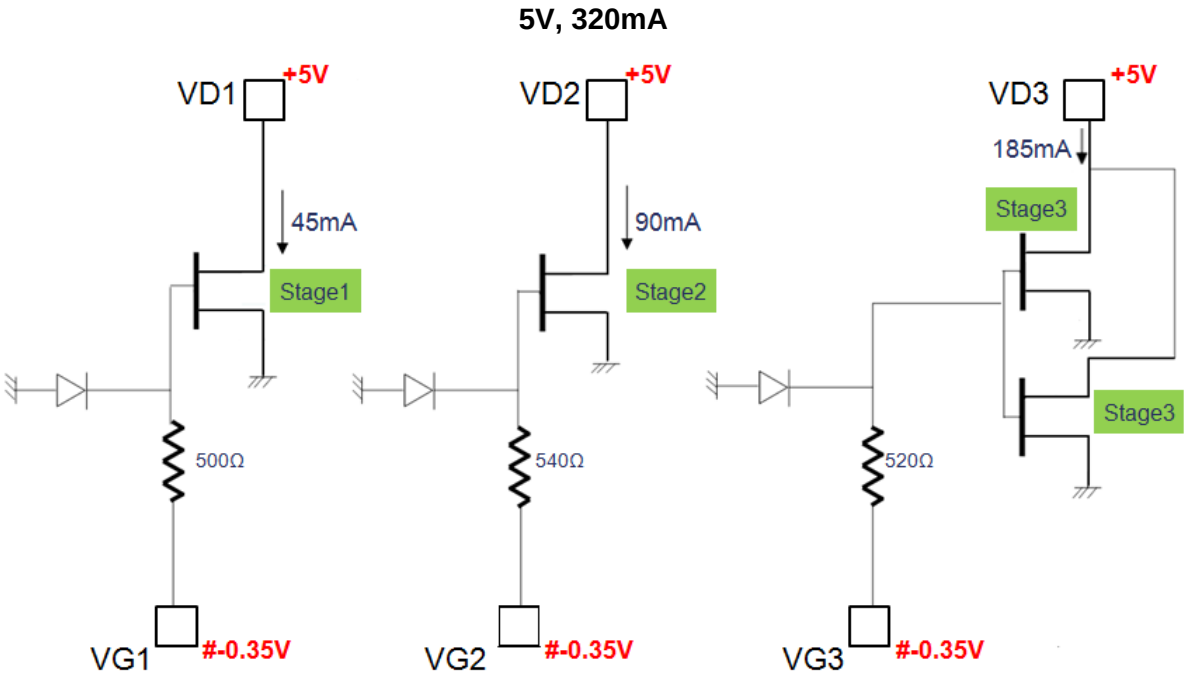
Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



ESD protections are also implemented on gate and control accesses.

DC Schematic



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Notes

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Recommended package footprint for FAB Package

Refer to the application note AN0024 available at https://www.ums-rf.com for package foot print recommendations and exact package dimensions.

SMD mounting procedure for FAB Package

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0024 available at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

FAB package:	CHA5266-FAB/XY Waffle pack: XY = 24

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