CHA5350-99F

17-24GHz Medium Power Amplifier

GaAs Monolithic Microwave IC

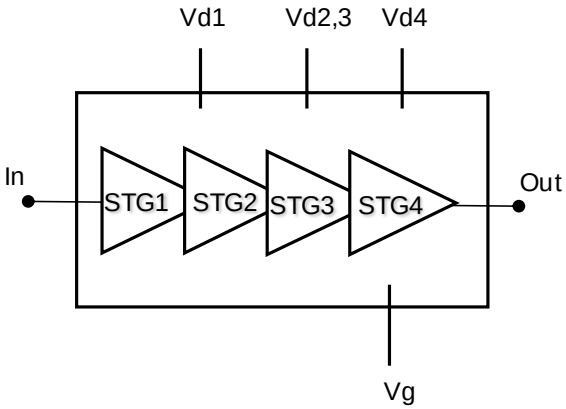
Description

The CHA5350-99F is a four stage monolithic MPA that typically provides an output power of 26.5dBm at 1dB gain compression associated to a high IP3 output of 34dBm.

It is designed for a wide range of applications, from professional to commercial communication systems.

The circuit is manufactured with a pHEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

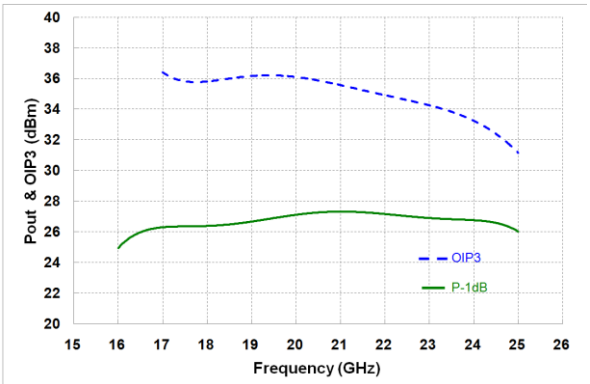
It is available in chip form.



Main Features

- Broadband performances: 17-24GHz
- Linear gain = 26dB
- Pout = 26.5dBm @ 1dB comp.
- High OIP3 = 34dBm
- DC bias: Vd=6Volt @ Id=300mA
- Chip size 2.38x1.46x0.07mm

Pout +IP3



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17		24	GHz
Gain	Linear Gain		26		dB
P_{-1dB}	Output Power @1dB gain compression		26.5		dBm
OIP3	Output third order interception point		34		dBm

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Electrical Characteristics

Tamb.= +25°C, $Vd_{1,2,3,4}$ = +6V, Idq = 300mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17		24	GHz
Gain	Linear Gain		26		dB
Gain_T	Linear gain variation versus temperature		-0.035		dB/°C
RLin	Input Return Loss		-17		dB
RLout	Output Return Loss		-12		dBm
P_{-1dB}	Output Power @1dB gain compression		26.5		dBm
P_{sat}	Saturated output power		27		dBm
PAE_ P_{-1dB}	Power added efficiency @1dB gain comp.		25		%
Id_ P_{-1dB}	Drain current @1dB gain compression		350		mA
Id_ P_{sat}	Drain current @ saturation		400		mA
OIP3	Output third order interception point on the frequency range 17-21 GHz		35.5		dBm
	Output third order interception point on the frequency range 21-24 GHz		34		dBm
$Vd_{1,2,3,4}$	Drain supply voltage		6		V
Id	Drain quiescent current		300		mA
Vg	Gate supply voltage		-0.7		V

These values are representative of measurements in test fixture that are made with bonding wires at the RF ports.
Wire bonding at RF accesses: 0.3nH, typically.

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
$Vd_{1,2,3,4}$	Drain bias voltage	8V	V
Id	Drain bias current (1)	650	mA
Vg	Gate bias voltage	-2 to -0.3	V
Pin	Maximum peak input power overdrive (2)	+15	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
Vg	10	DC gate Voltage	-0.7	V
$Vd_{1,2,3,4}$	3, 5, 7	DC drain Voltage	6	V
Id		DC Drain current controlled with Vg (1)	300	mA

(1) To be adjusted in order to achieve Id: 300mA

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Typical on-wafer Sij parameters

Tamb.= +25°C, $Vd_{1,2,3,4}$ = +6V, Id = 300mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2.0	-0.07	-9.44	-78.88	159.60	-52.68	72.93	-0.85	-75.67
3.0	-0.14	-18.26	-68.51	81.71	-49.70	-125.90	-0.53	-122.60
4.0	-0.18	-27.23	-79.86	53.21	-35.51	96.97	-0.43	-146.70
5.0	-0.19	-36.57	-87.07	-177.80	-41.13	-22.73	-0.34	-167.70
6.0	-0.35	-46.92	-78.25	89.10	-42.71	-47.59	-0.38	176.80
7.0	-0.45	-54.72	-75.64	-123.20	-29.13	-141.00	-0.40	163.80
8.0	-0.41	-65.00	-68.15	-112.30	-23.35	148.90	-0.46	150.80
9.0	-0.48	-75.90	-63.28	155.10	-18.62	93.87	-0.62	137.90
10.0	-0.61	-88.48	-71.90	-167.70	-14.08	44.06	-0.87	124.80
11.0	-0.94	-102.00	-73.31	-84.77	-9.38	-2.71	-1.22	110.90
12.0	-1.62	-118.40	-65.53	-177.50	-4.54	-49.34	-1.66	96.05
13.0	-2.78	-136.00	-66.25	93.70	0.68	-97.29	-2.23	79.67
14.0	-4.73	-155.60	-64.18	-155.30	6.29	-148.20	-3.06	61.16
15.0	-7.82	-178.90	-62.89	81.10	12.39	156.00	-4.09	39.87
16.0	-13.34	155.10	-66.33	99.71	19.16	89.99	-5.68	15.94
17.0	-24.98	93.42	-67.24	107.60	25.25	0.27	-8.59	-4.08
18.0	-22.61	4.93	-74.75	-58.96	26.56	-95.76	-9.80	-12.28
19.0	-15.63	-18.92	-63.85	118.40	25.89	-174.60	-9.73	-27.73
20.0	-12.39	-46.99	-65.04	66.25	25.24	118.50	-12.00	-40.32
21.0	-13.02	-66.87	-64.69	11.09	26.79	48.04	-12.44	-40.82
22.0	-13.46	-69.21	-53.18	102.10	26.76	-27.44	-11.63	-42.73
23.0	-15.49	-67.50	-61.36	-31.78	26.41	-102.50	-10.35	-43.71
24.0	-15.18	-49.01	-60.01	-130.60	25.77	-179.50	-7.83	-46.90
25.0	-15.06	-31.73	-53.04	179.10	24.54	100.50	-5.16	-59.34
26.0	-9.04	-8.19	-61.37	-154.70	23.17	12.93	-3.72	-76.60
27.0	-3.83	-36.15	-60.71	14.69	17.35	-88.24	-3.06	-91.44
28.0	-3.32	-58.66	-68.44	-21.18	8.69	-157.80	-2.63	-102.80
29.0	-3.67	-68.03	-55.10	-93.55	1.28	149.50	-2.39	-112.80
30.0	-3.16	-73.69	-61.90	85.85	-5.59	103.50	-2.25	-122.10
31.0	-3.18	-80.86	-57.37	153.70	-11.50	62.37	-2.05	-130.50
32.0	-2.57	-88.42	-75.25	-17.50	-17.32	23.99	-1.92	-136.50
33.0	-3.30	-90.72	-54.64	161.40	-22.56	-12.22	-1.81	-145.00
34.0	-3.07	-99.44	-48.99	37.95	-27.67	-44.97	-1.63	-152.40
35.0	-3.02	-100.70	-51.88	68.05	-32.94	-82.00	-1.78	-160.30
36.0	-2.93	-104.80	-53.91	41.18	-37.31	-106.10	-1.76	-166.30
37.0	-3.82	-108.60	-49.95	86.53	-40.50	-145.90	-1.72	-177.30
38.0	-3.49	-109.20	-59.92	28.09	-43.89	-157.80	-1.84	172.10
39.0	-4.14	-112.50	-55.74	99.34	-48.24	162.60	-1.86	160.70
40.0	-3.21	-116.50	-58.42	107.20	-60.58	118.40	-3.28	143.60

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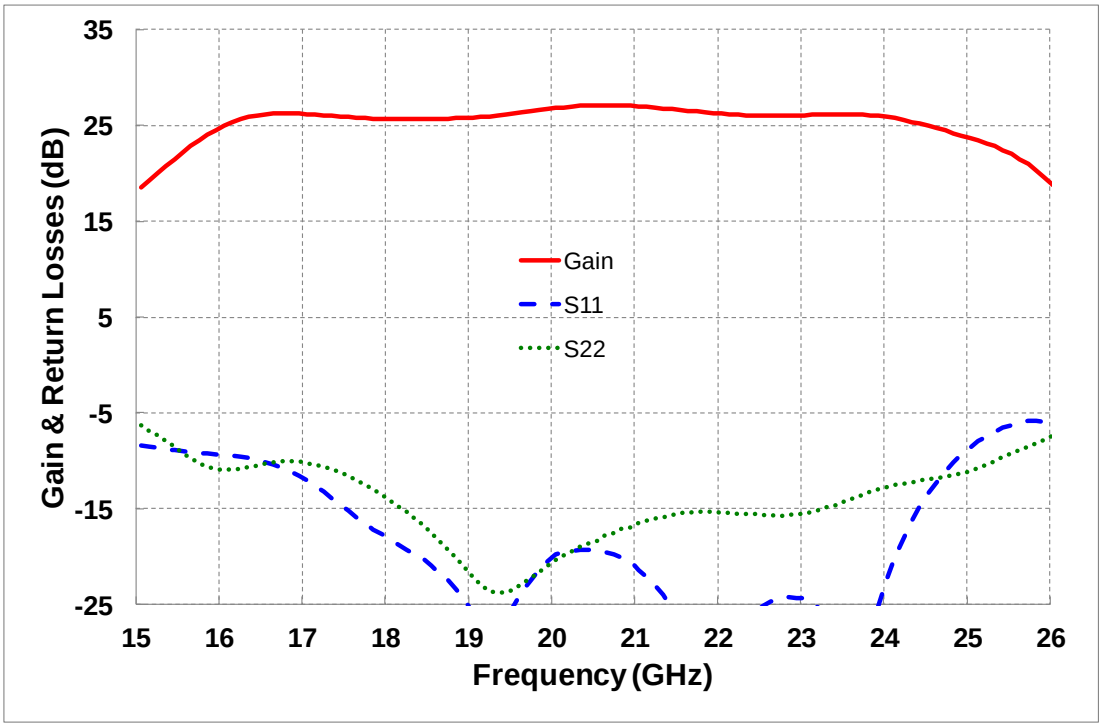
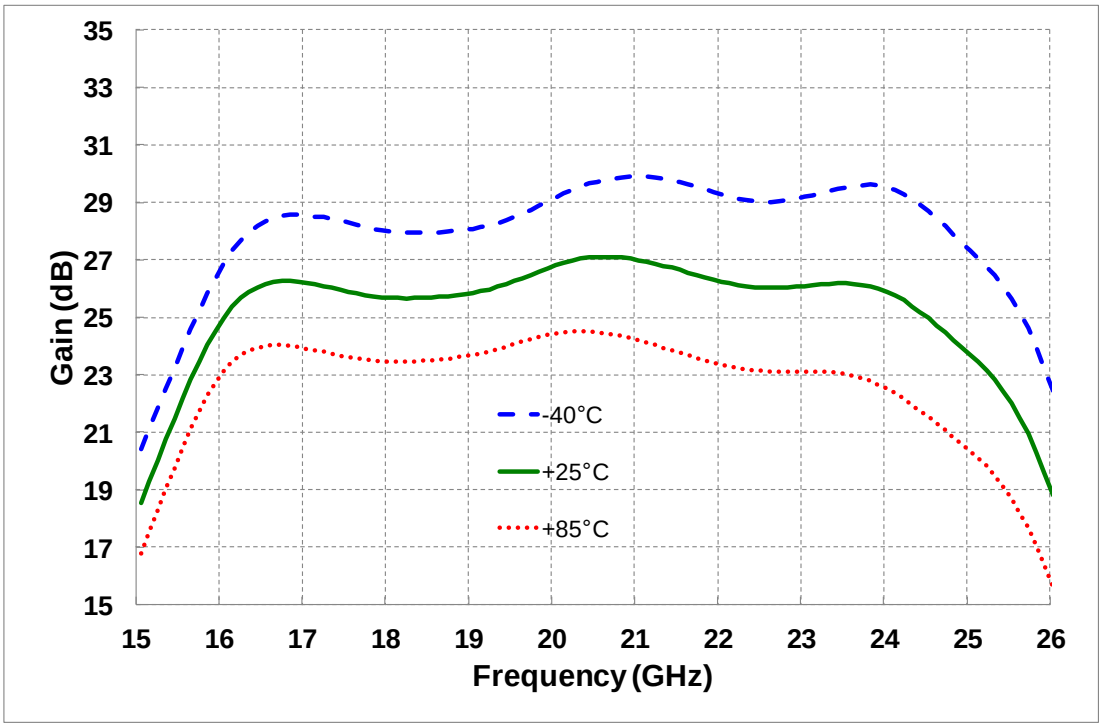
Typical Test Fixture Measurements

$Vd_{1,2,3,4}$ = +6V, Idq = 300mA

Linear Gain & Return Losses versus Frequency



Linear Gain versus Frequency and Temperature



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Typical Test Fixture Measurements

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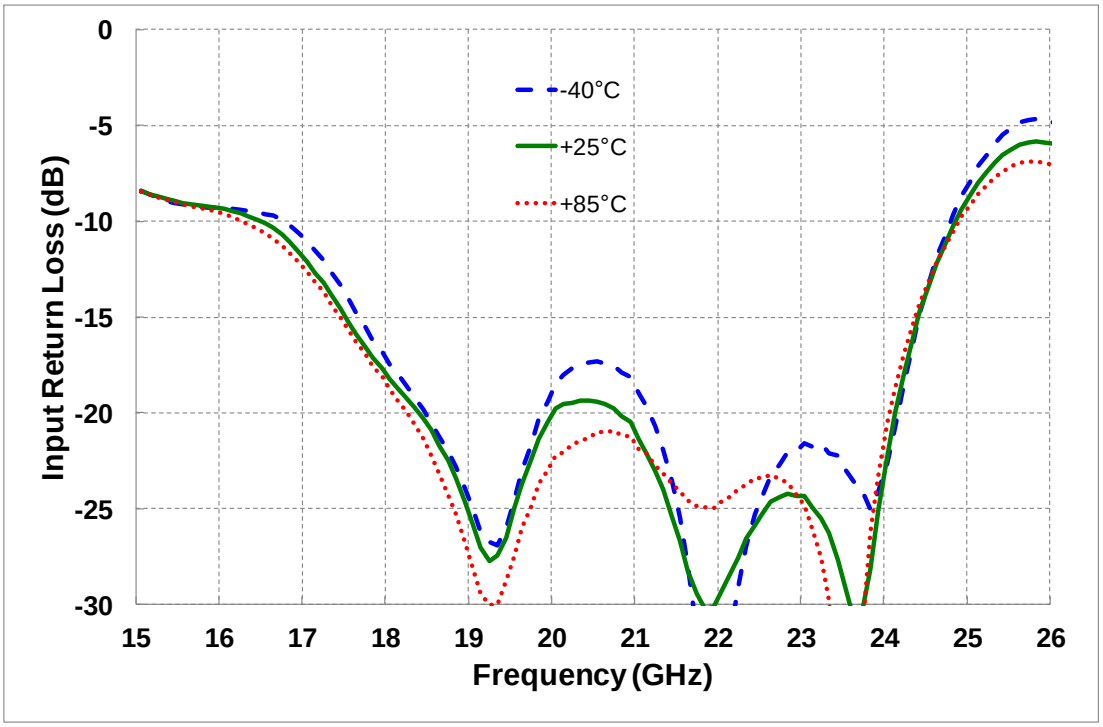
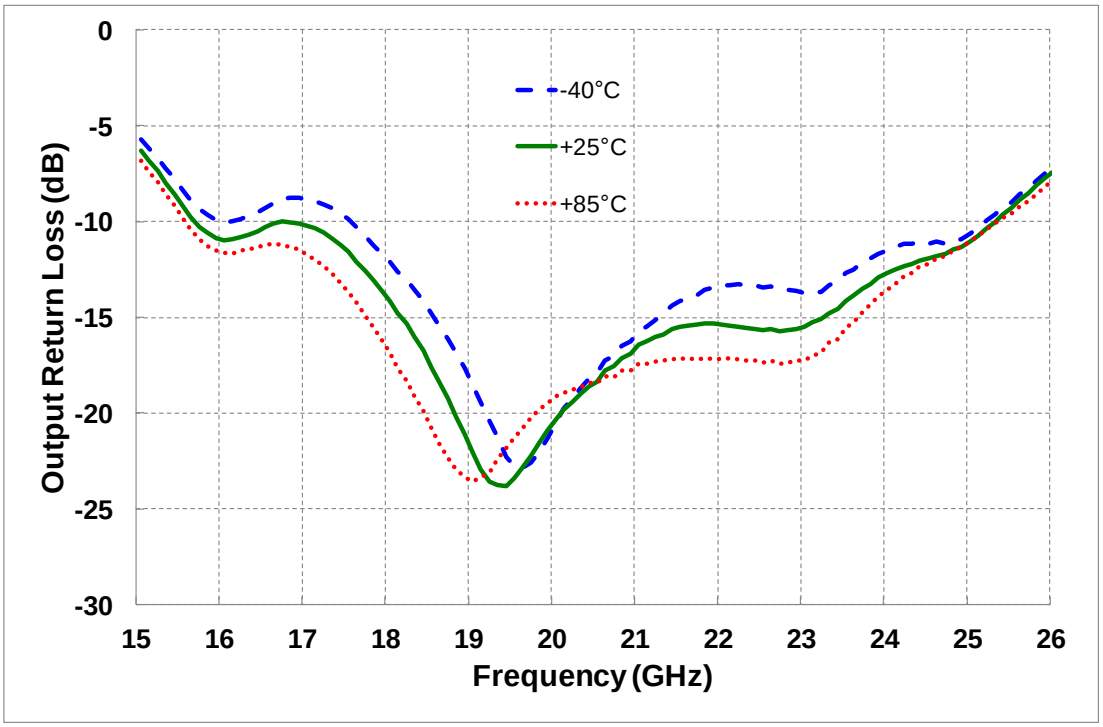
Input Return Loss versus Frequency and Temperature



Output Return Loss versus Frequency and Temperature



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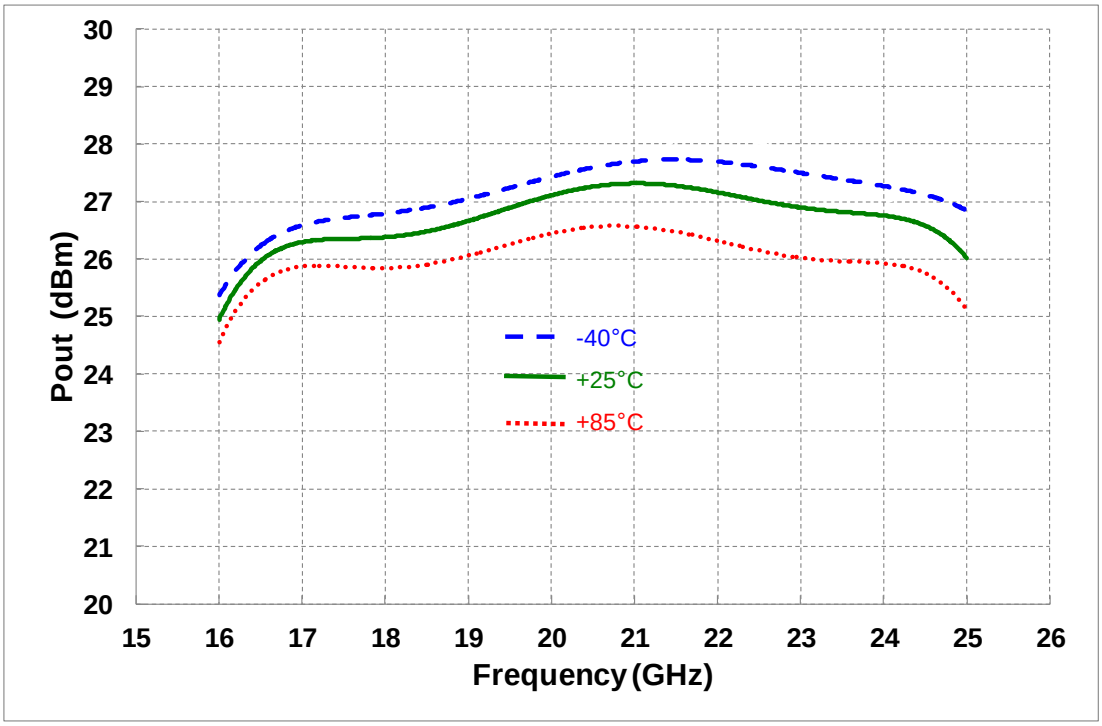
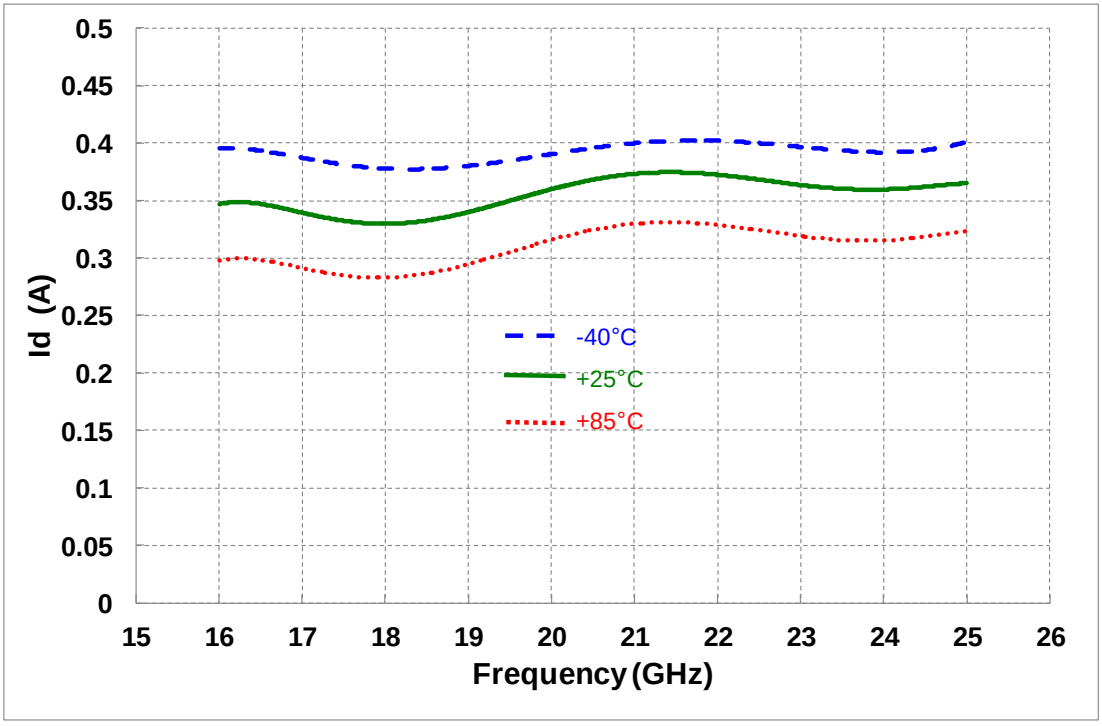
Typical Test Fixture Measurements

$Vd_{1,2,3,4}$ = +6V, Idq = 300mA

Output Power @ 1dB Comp versus Frequency and Temperature



Drain Current @ 1dB Comp versus Frequency and Temperature



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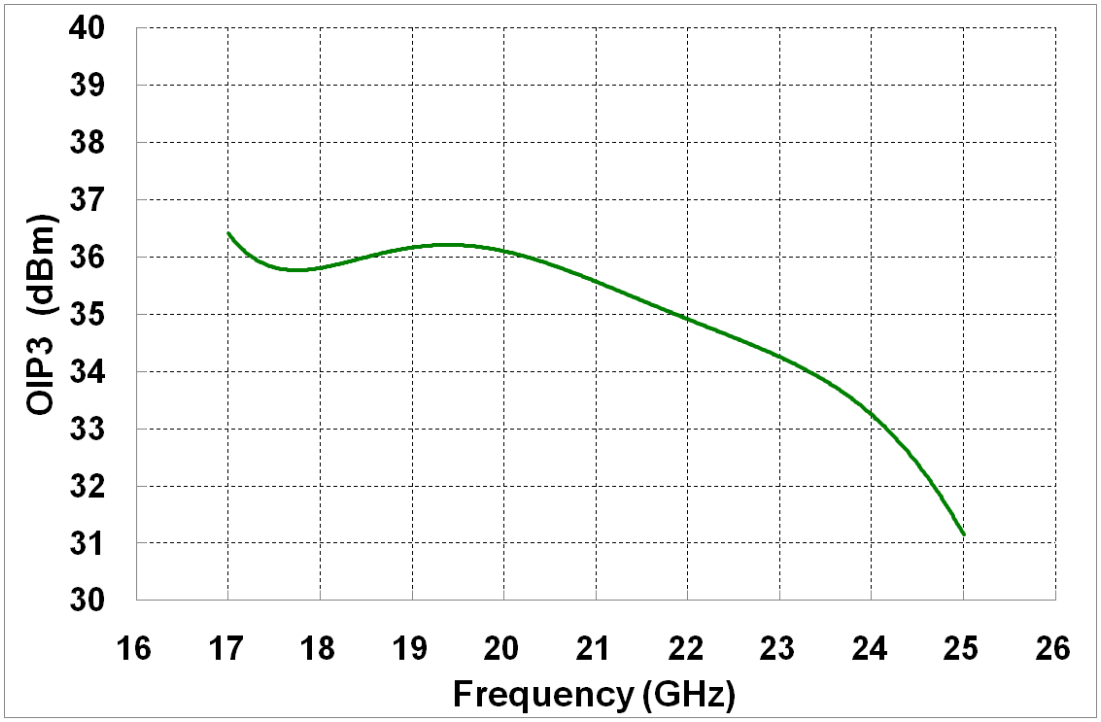
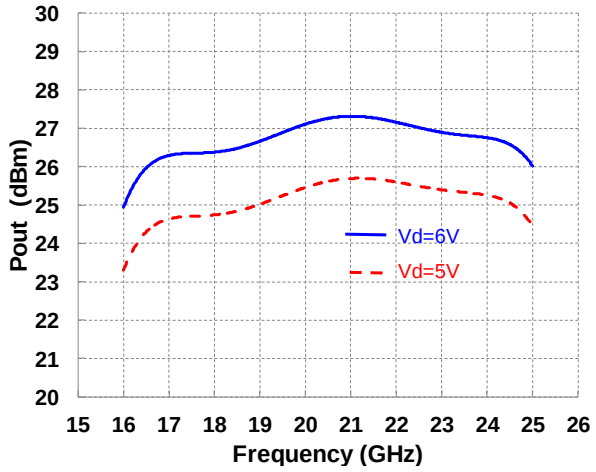
Typical Test Fixture Measurements

$Vd_{1,2,3,4}$ = +6V, Idq = 300mA

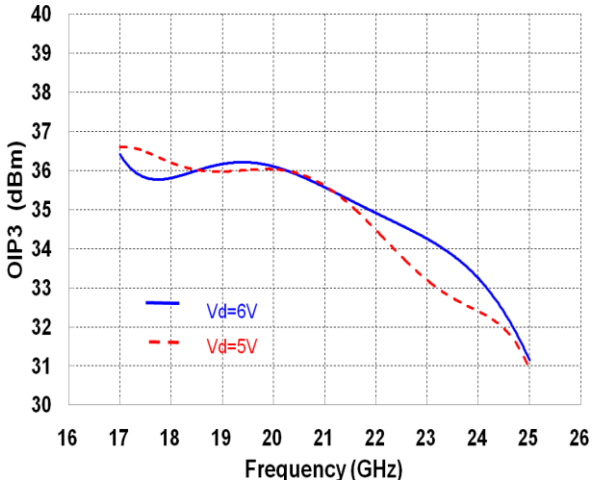
Output IP3 versus Frequency and Temperature



Output Power @ 1dB Comp versus Frequency and Vd



Output IP3 versus Frequency and Vd



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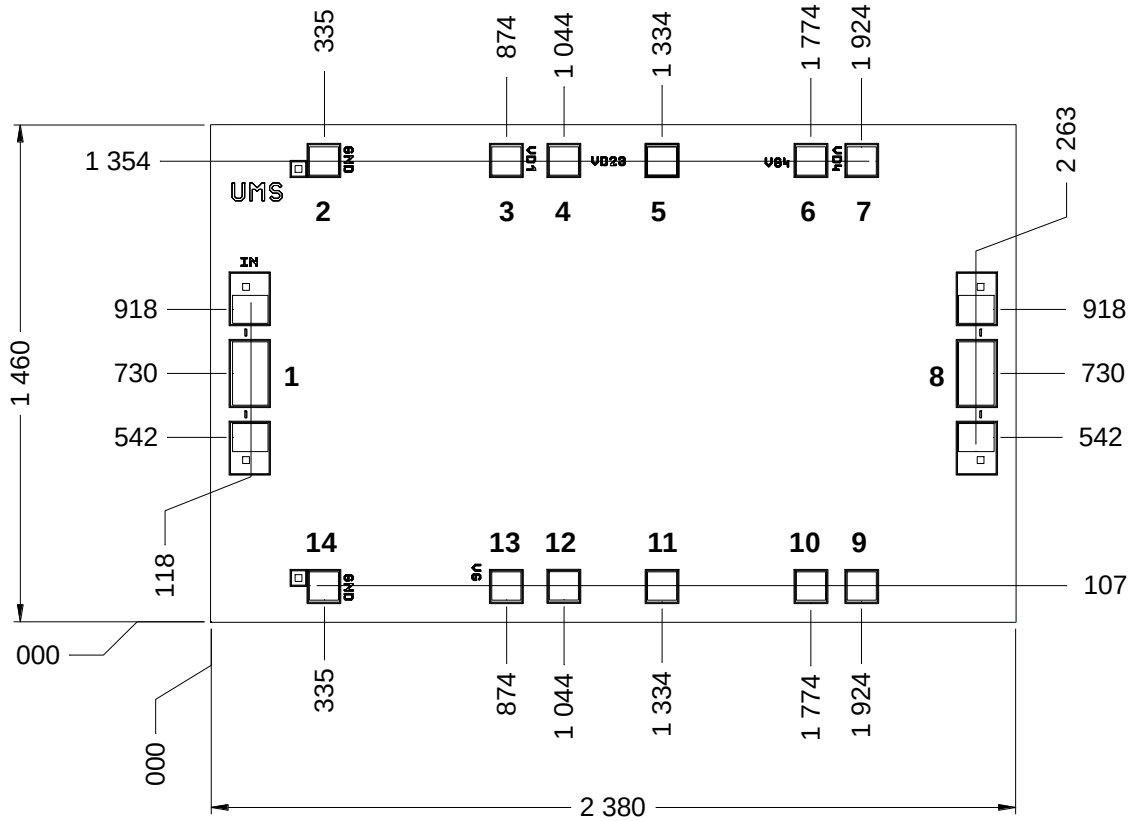
Mechanical data



All dimensions are in micrometers
Chip size = 2380x1460 ±35µm
Chip thickness = 70µm ±10µm
RF pads (1, 8) = 110 x 200µm²
DC pads = 100 x 100µm²
Chip width and length are given with a tolerance of ±35µm

Pin number	Pin name	Description
1	IN	Input RF
2, 14	Gnd	Gnd (NC)
3	Vd1	1st stage drain voltage
5	Vd2, Vd3	2nd and 3rd drain voltage
7	Vd4	4th drain voltage
8	OUT	Output RF
10	Vg	Gate voltage
4, 6, 9, 11, 12, 13	/	NC

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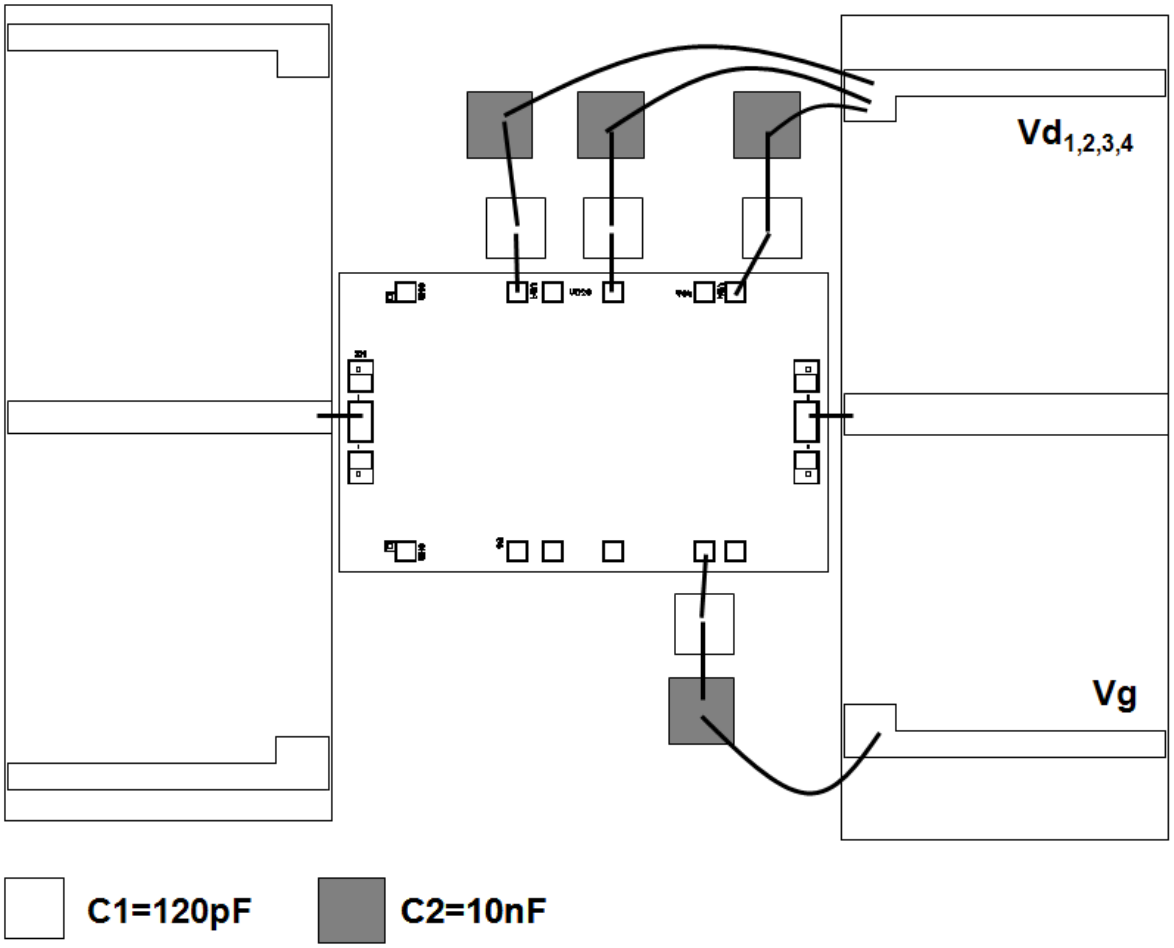
Recommended assembly plan



25µm wedge bonding is preferred

Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Recommended circuit bonding table

Label	Type	Decoupling	Comment
IN, OUT	RF	Not required	Inductance (Lbonding) = 0.3nH 400µm length with a wire diameter of 25 µm
Vd1, Vd2, Vd3 Vd4	Vd	120pF & 10nF	Drain Supply
Vg	Vg	120pF & 10nF	Gate Supply

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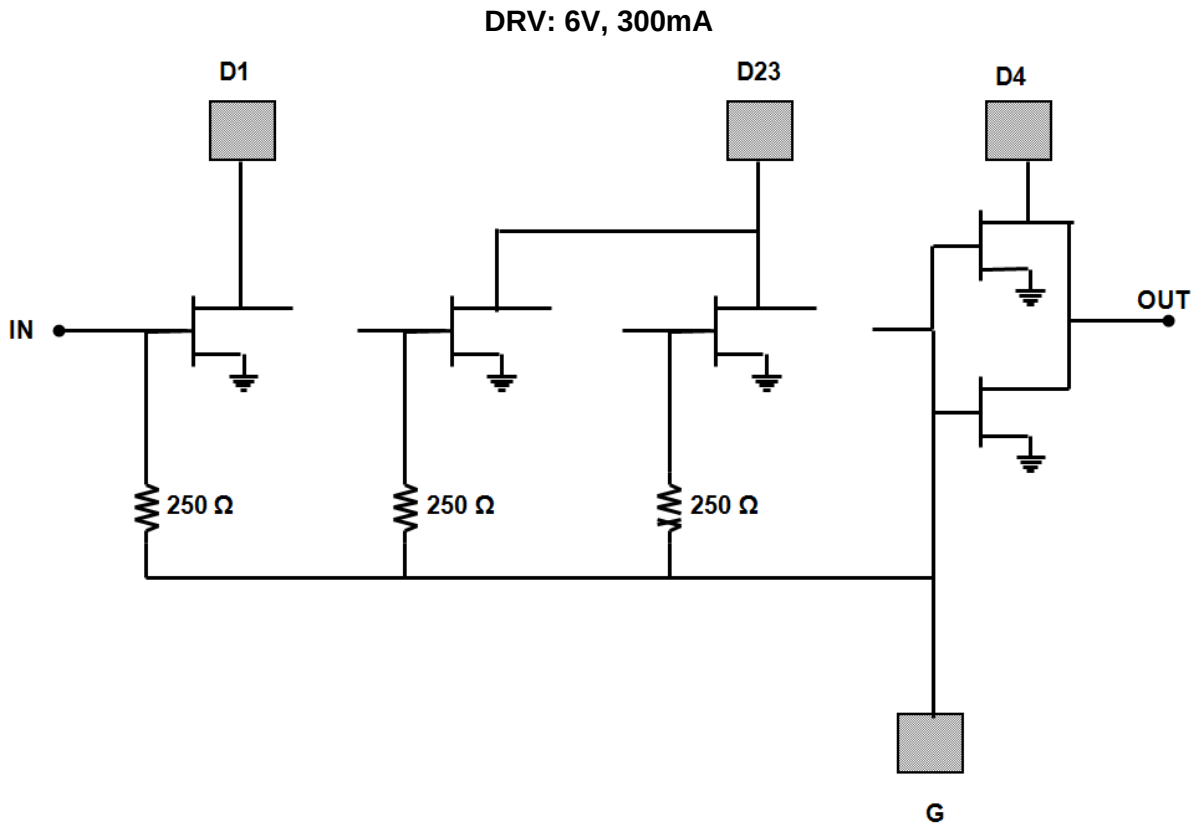
DC Schematic



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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Ordering Information

Chip form:	CHA5350-99F/00

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