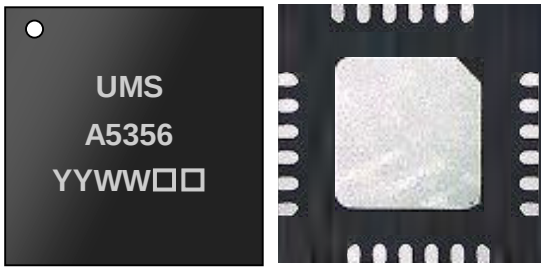
17.7-23.6GHz Packaged HPA

GaAs Monolithic Microwave IC in SMD leadless package

Description

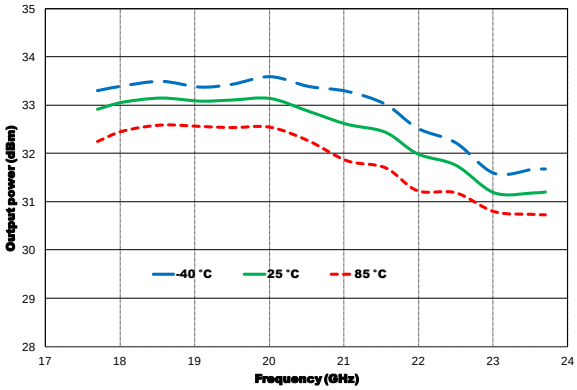
The CHA5356-QGG is a three stage monolithic GaAs high power amplifier, which integrates a power detector.
It is designed for a wide range of applications, from military to commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.15µm gate length.
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 17.7-23.6GHz
- 33dBm Pout in saturation
- 38dBm OIP3
- 19dB Gain
- 30dB power detection dynamic
- DC bias: Vd=6.0Volt@Id=700mA
- QGG-QFN5x5
- MSL3

Saturated power



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.7		23.6	GHz
Gain	Linear Gain		19		dB
Psat	Saturated Output Power		33		dBm
OIP3	Output IP3		38		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +6.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Operating frequency range	17.7		23.6	GHz
G	Small Signal Gain		19		dB
ΔG	Gain variation in temperature		0.045		dB/°C
Psat	Saturated output power in 17.7- 19.7GHz Saturated output power in 21.2- 23.6GHz		33 31.5		dBm
P1dB	Output power @1dB compression		31		dBm
OIP3	Output IP3 in 17.7- 19.7GHz Output IP3 in 21.2- 23.6GHz		38 36		dBm
PAE	PAE at 1dB compression		20		%
Rlin	Input Return Loss		12		dB
Rlout	Output Return Loss		15		dB
NF	Noise Figure		7.5		dB
Dr	Detection dynamic range (1)		30		dB
Vdet_min	Voltage detection Vref-Vdet min		10		mV
Vdet_max	Voltage detection Vref-Vdet up to Psat		2100		mV
Vg	DC Gate voltage		-0.75		V
Idet	Detector current		3.0		mA
Idq	Total drain current		700		mA

(1) Detection dynamic range for output power detection up to Psat.

These values are representative of on-board measurements.

Electrostatic discharge sensitive device observe handling precautions!

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6.5V	V
Id	Drain bias quiescent current	900	mA
Vg	Gate bias voltage	-2 to +0.4	V
Pin	Maximum peak input power overdrive (2)	+20	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vd1	28	DC Drain voltage 1st stage	6.0	V
Vd2	26	DC Drain voltage 2nd stage	6.0	V
Vd3	24, 12	DC Drain voltage 3rd stage	6.0	V
Vg1	9	DC Gate voltage 1st stage	-0.75	V
Vg2	10	DC Gate voltage 2nd stage	-0.75	V
Vg3	25, 11	DC Gate voltage 3rd stage	-0.75	V
VDC	22	DC Detector voltage	6.0	V

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

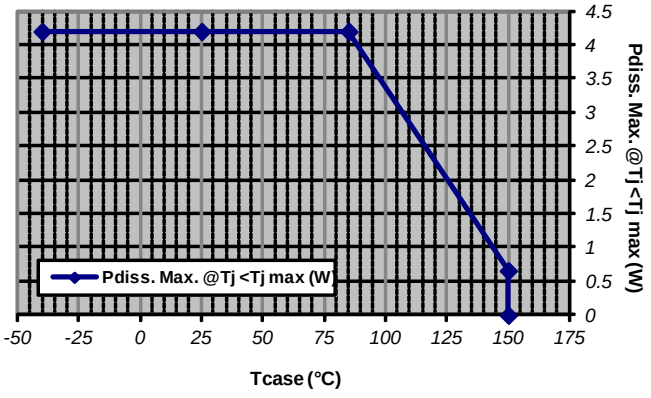
A derating must be applied on the dissipated power if the Tcase temperature cannot be maintained below the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

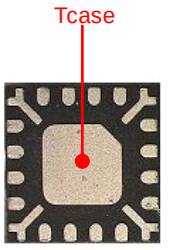
DEVICE THERMAL SPECIFICATION : CHA5356-QGG				
Recommended max. junction temperature (Tj max)			:	162 °C
Junction temperature absolute maximum rating			:	175 °C
Max. continuous dissipated power (Pdiss. Max.)			:	4.2 W
=> Pdiss. Max. derating above Tcase(1)=	85	°C	:	54 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)			:	<18 °C/W
Minimum Tcase operating temperature(3)			:	-40 °C
Maximum Tcase operating temperature(3)			:	85 °C
Minimum storage temperature			:	-55 °C
Maximum storage temperature			:	150 °C

(1) Derating at junction temperature constant = Tj max.

*(2) Rth J-C is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temeprature reference point (Tcase) on package's bottom side

6.4

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Typical Package Sij parameters

Tamb.= +25°C, Vd = +6.0V, Id = 700mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S21 (dB)	PhS21 (°)	S12 (dB)	PhS12 (°)	S22 (dB)	PhS22 (°)
2.0	-0.658	119.1	-71.121	-3.0	-89.555	5.7	-1.054	97.2
3.0	-0.766	88.6	-77.421	178.3	-97.160	24.1	-2.194	8.7
4.0	-0.872	57.3	-66.866	76.5	-68.385	58.4	-1.421	-139.2
5.0	-0.936	26.7	-65.608	-8.0	-67.363	-12.6	-0.566	140.4
6.0	-1.005	-4.4	-66.751	-78.1	-69.688	-67.9	-0.480	95.1
7.0	-1.010	-34.2	-71.814	-134.0	-77.627	-148.2	-0.565	57.8
8.0	-1.079	-65.9	-63.086	-176.0	-66.783	96.4	-0.712	25.0
9.0	-1.137	-94.6	-56.663	168.3	-61.013	21.5	-0.947	-11.1
10.0	-1.129	-121.9	-45.980	134.8	-57.513	-73.7	-1.353	-48.4
11.0	-1.220	-149.2	-35.808	89.6	-52.366	-150.5	-2.051	-88.3
12.0	-1.366	-175.2	-25.629	32.3	-48.539	152.4	-3.232	-132.0
13.0	-1.646	158.5	-15.348	-32.0	-46.329	83.9	-5.670	178.8
14.0	-2.129	131.6	-4.221	-109.8	-45.659	33.4	-11.889	123.3
15.0	-3.048	104.7	6.750	146.8	-48.249	14.9	-17.191	-141.1
16.0	-4.660	79.9	13.300	22.4	-48.719	-0.8	-9.941	146.4
17.0	-6.032	59.7	16.509	-94.1	-48.890	-61.1	-10.430	105.2
18.0	-8.546	32.8	18.409	154.3	-53.686	-40.1	-11.019	68.4
19.0	-15.338	25.3	19.208	45.5	-53.356	-69.7	-11.654	30.0
20.0	-13.485	60.1	19.418	-61.4	-59.005	-63.5	-15.133	-10.6
21.0	-12.328	43.3	19.028	-165.9	-55.397	-39.1	-20.120	-25.3
22.0	-13.176	34.7	18.629	89.3	-55.521	-37.2	-24.779	-23.5
23.0	-13.351	41.8	18.650	-23.8	-49.120	6.9	-25.348	48.9
24.0	-10.309	38.7	17.446	-155.1	-44.079	-32.1	-13.267	25.6
25.0	-7.458	37.8	12.014	57.1	-44.905	-82.5	-10.199	-27.1
26.0	-3.458	3.1	1.312	-75.1	-45.687	-77.4	-10.236	-53.6
27.0	-2.636	-28.2	-9.903	174.0	-45.232	-64.2	-8.667	-74.4
28.0	-2.066	-57.5	-20.389	45.6	-40.934	-69.0	-6.255	-100.0
29.0	-1.504	-87.4	-30.641	-123.0	-36.560	-96.5	-4.367	-124.3
30.0	-1.308	-116.1	-33.013	-137.4	-32.233	-132.5	-2.204	-158.6
31.0	-1.343	-143.7	-33.298	-176.0	-32.727	-175.5	-1.336	169.7
32.0	-1.221	-168.3	-35.120	146.9	-34.656	147.3	-1.027	141.5
33.0	-1.115	169.5	-36.788	126.3	-36.717	124.4	-0.916	116.8
34.0	-0.856	148.3	-39.133	109.2	-39.509	111.6	-0.992	95.7
35.0	-0.691	128.4	-43.295	85.8	-43.214	87.5	-1.044	75.9
36.0	-0.482	110.1	-44.170	78.5	-43.981	72.8	-0.966	59.1
37.0	-0.125	92.0	-45.894	41.4	-43.926	41.1	-0.992	43.6
38.0	0.092	73.3	-56.527	-55.4	-53.921	-58.8	-0.778	29.3
39.0	0.063	56.0	-46.182	167.1	-47.345	164.2	-0.742	14.3
40.0	0.201	39.0	-45.776	132.8	-45.074	140.4	-0.724	0.3

Refer to the “definition of the Sij reference planes” section below

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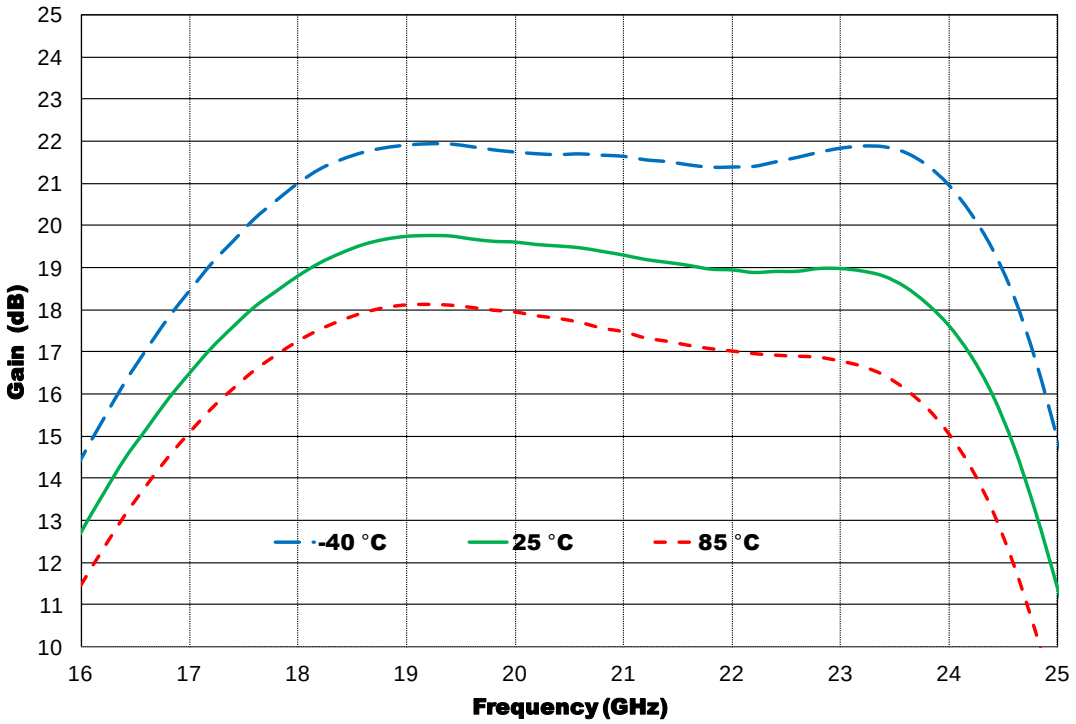
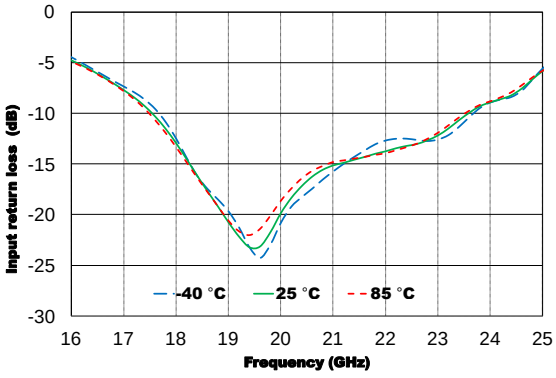
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 700mA
Measurement in the plan of the QFN, using the proposed land pattern & board, as defined in paragraph “Evaluation mother board”

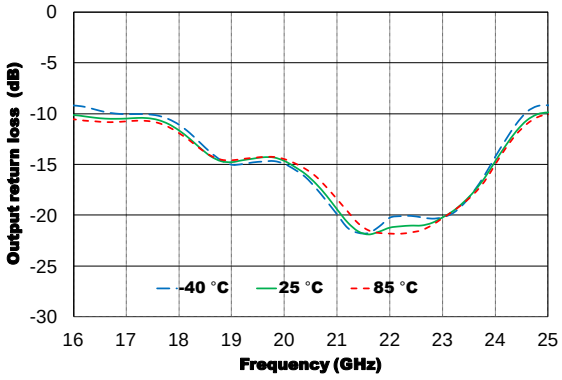
Linear Gain versus Temperature



Input return loss versus Temperature



Output return loss versus Temperature



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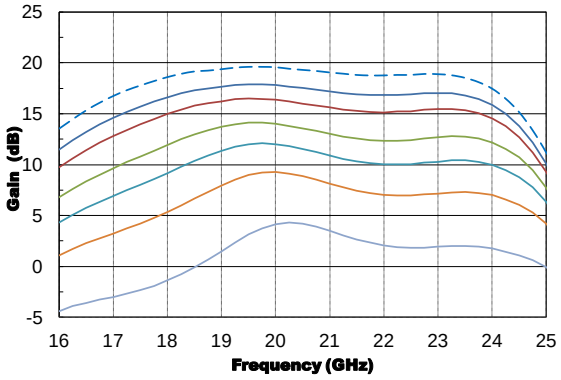
Typical Board Measurements

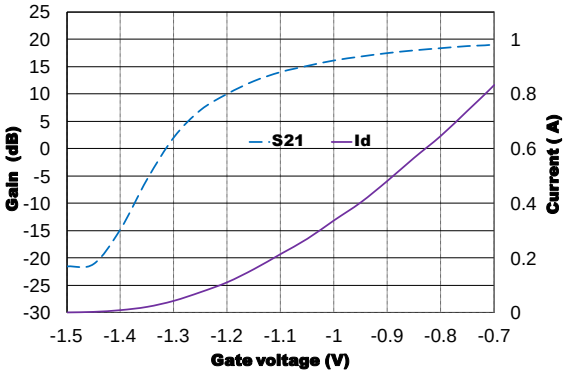
Tamb.= +25°C, Vd = +6.0V, Id = 700mA

Gain control

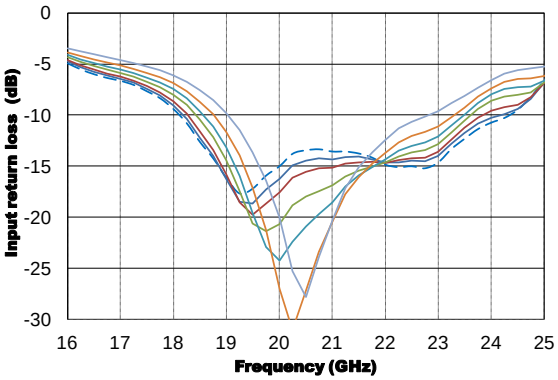


Gain & current versus Gate Voltage

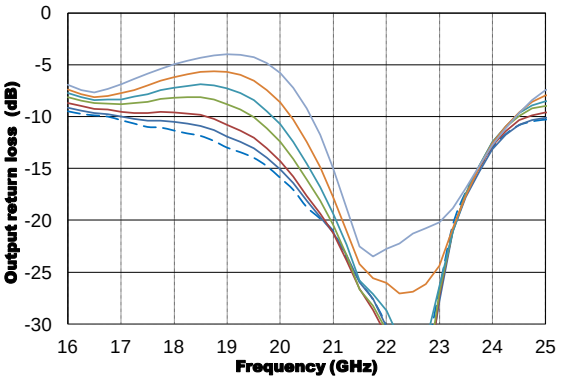
at 22GHz



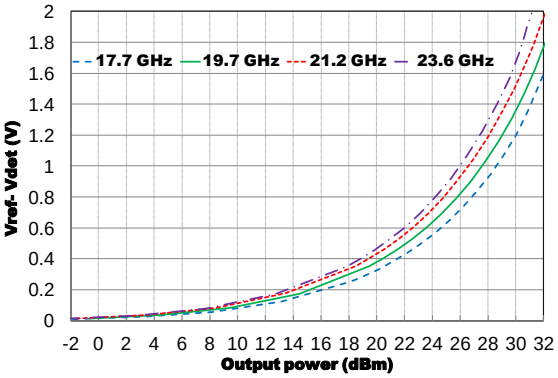
Input return loss versus Gain control



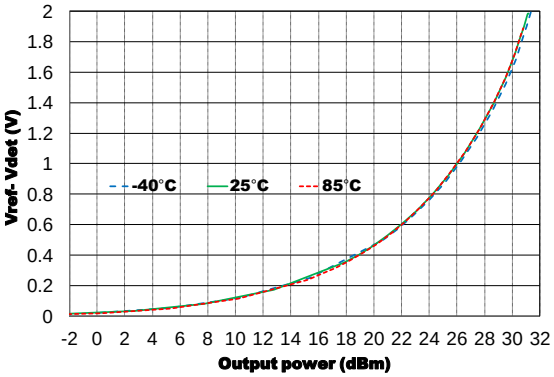
Output return loss versus Gain control



Detector voltage versus Frequency



Detector voltage versus Temperature



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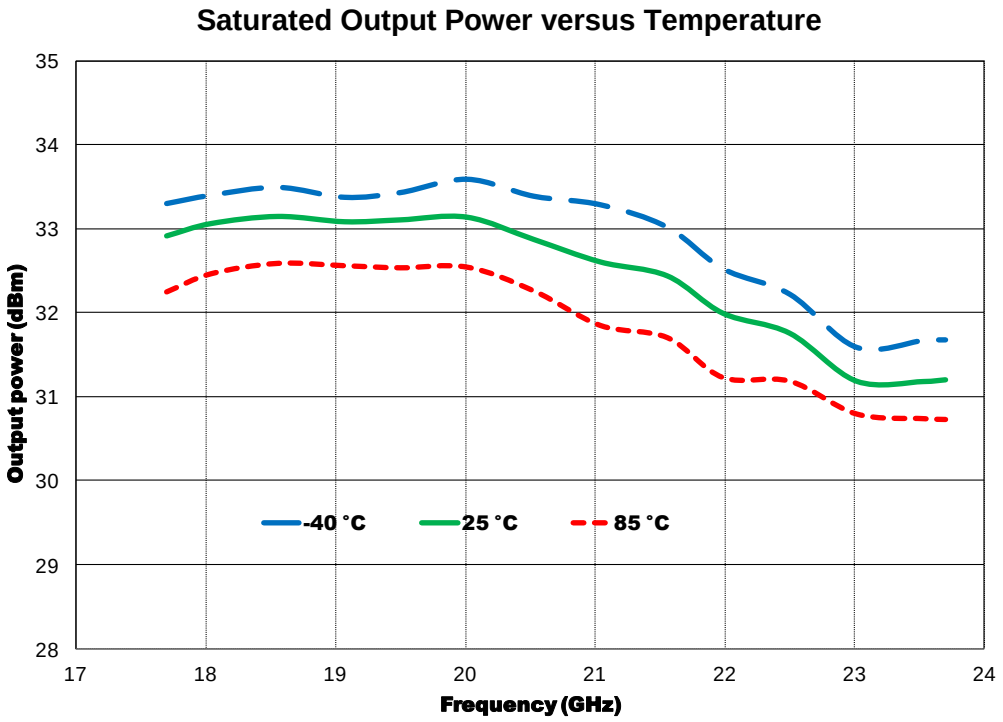
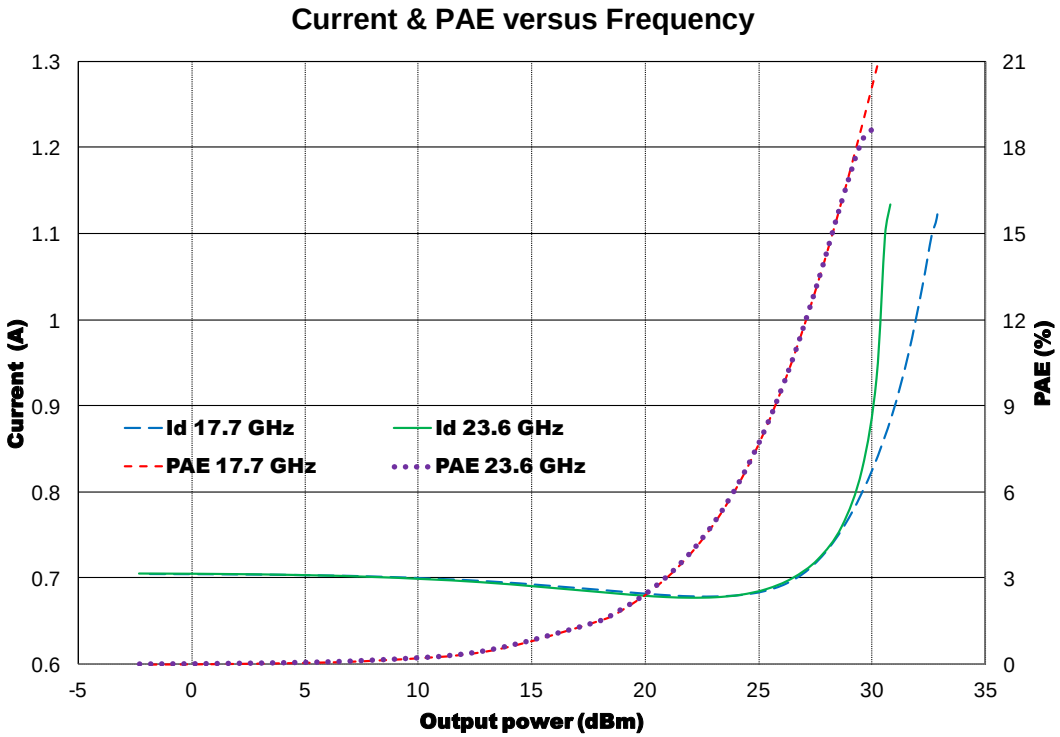
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 700mA





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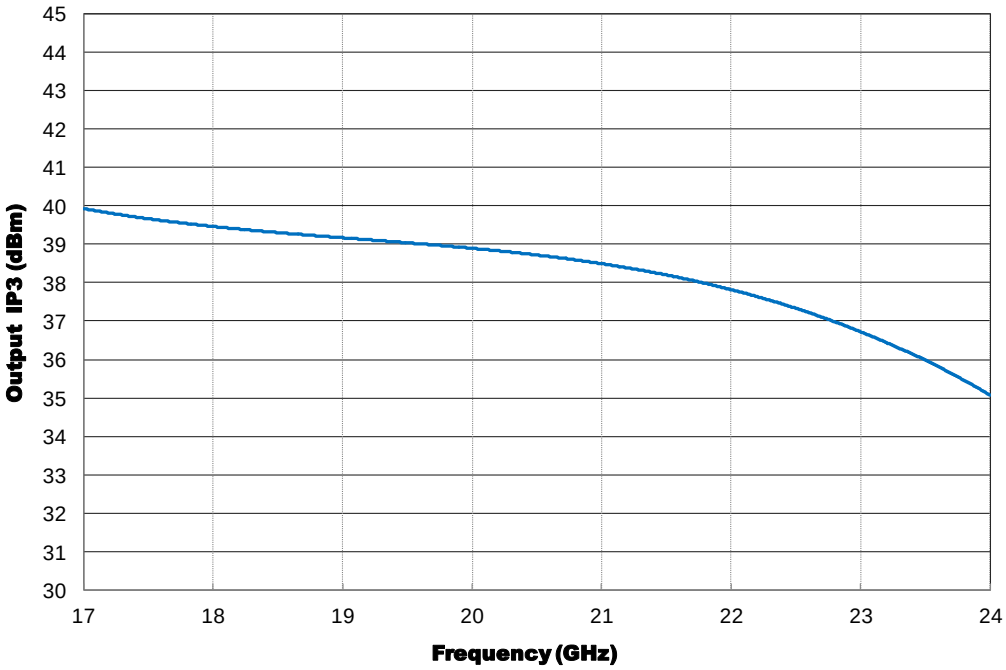
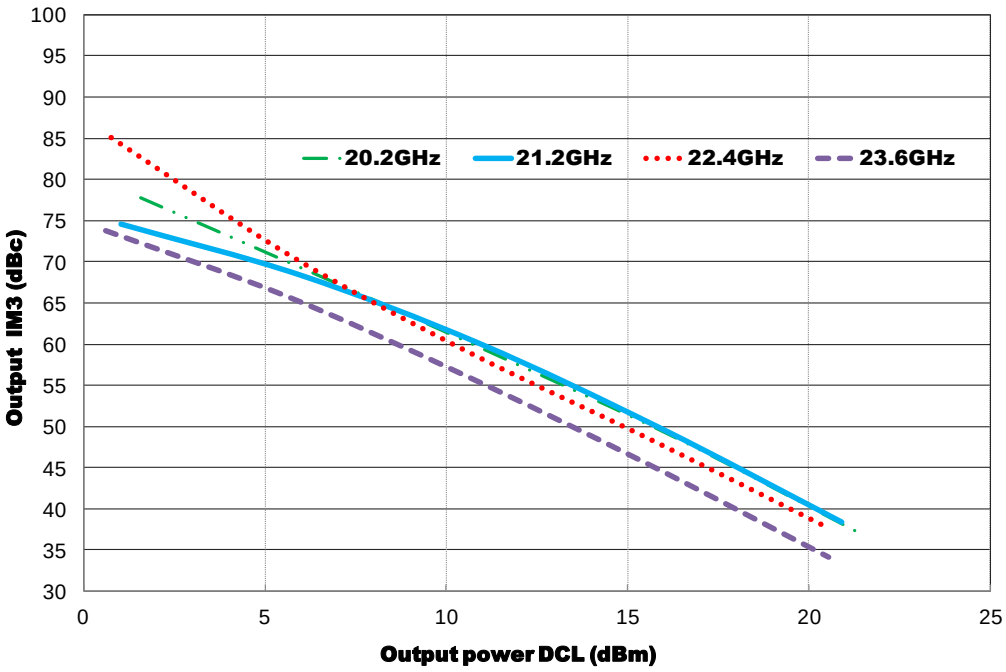
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 700mA

OIP3 versus Frequency
at Pout DCL= 12dBm



IM3 versus Frequency



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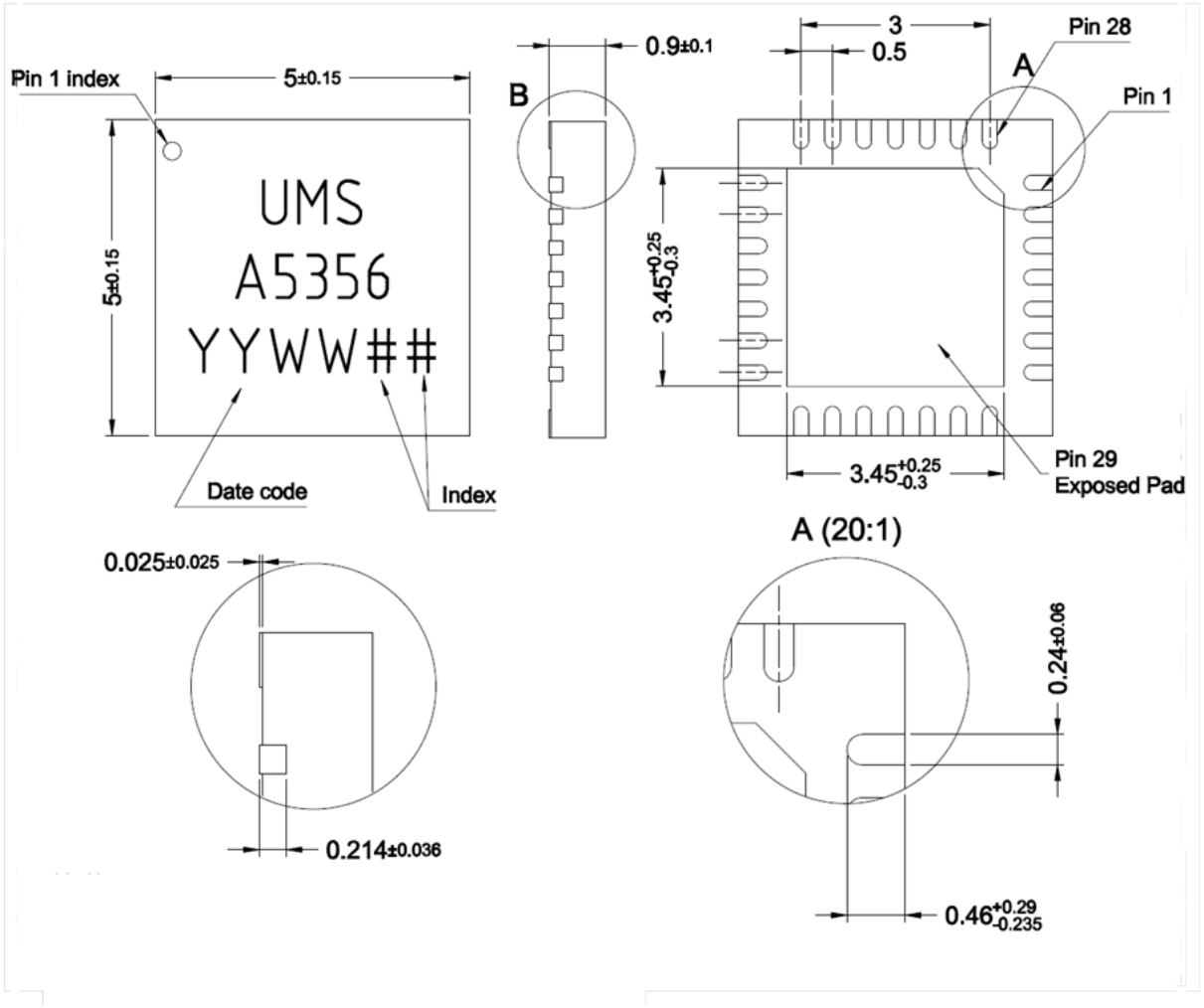
Package outline (1)



Matte tin, Lead Free (Green)		1- Gnd(2)	11- Vg3	21- Gnd(2)
Units :	mm	2- Gnd(2)	12- Vd3	22- VDC
From the standard :	JEDEC MO-220 (VGGD)	3- Gnd(2)	13- Nc	23- VDET
		4- Gnd(2)	14- Gnd(2)	24- Vd3
29-	GND	5- RF in	15- Gnd(2)	25- Vg3
		6- Gnd(2)	16- Gnd(2)	26- Vd2
		7- Gnd(2)	17- RF out	27- Nc
		8- Gnd(2)	18- Gnd(2)	28- Vd1
		9- Vg1	19- Gnd(2)	
		10- Vg2	20- VREF	

(1) The package outline drawing included in this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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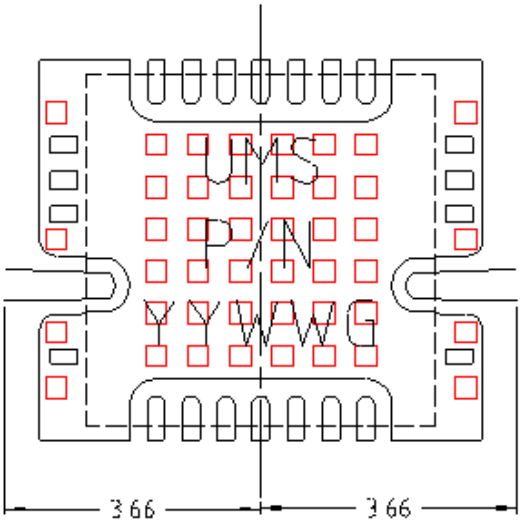
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.66mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL3

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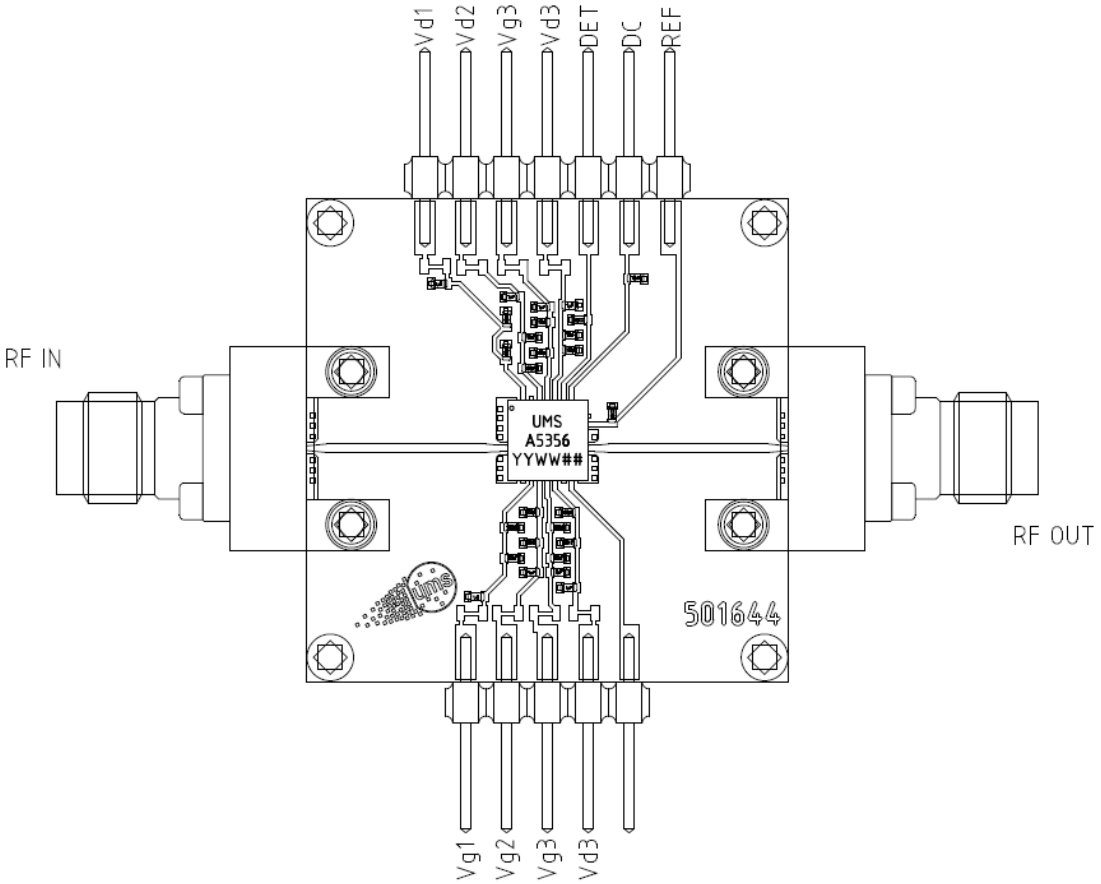
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4350 / 10mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF ±5%, 10nF ±10% and 1µF ±10% are recommended for all DC accesses.
- A 10KΩ resistor is recommended on VREF & VDET accesses for the detector
- See application note AN0017 for details.



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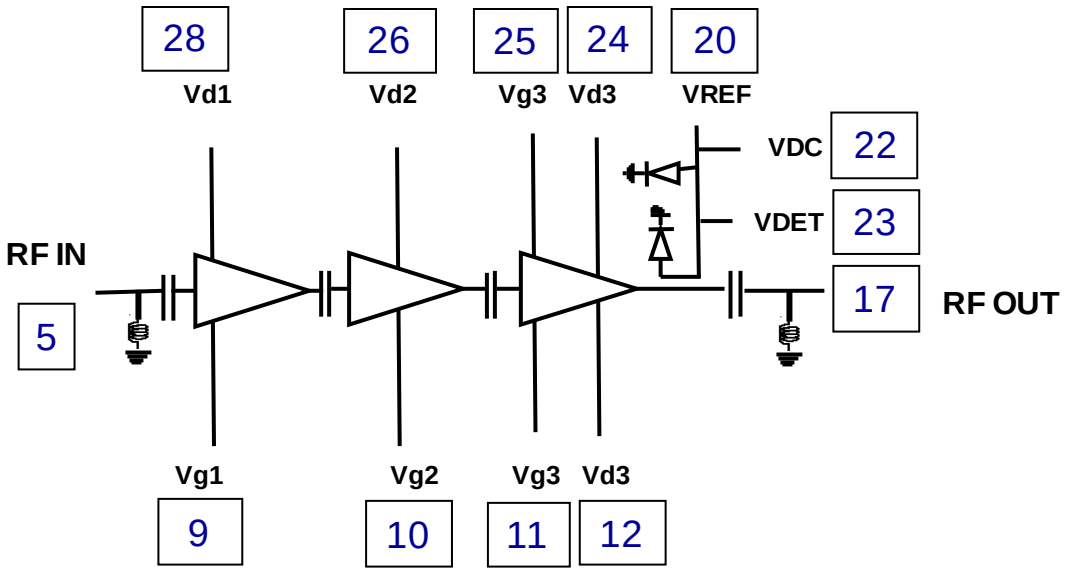
Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF, 10nF, 1µF) on the PC board, as close as possible to the package.

A 10KΩ resistor is recommended in parallel to VDET, and VREF accesses.

The circuit includes ESD protections on all RF and DC accesses.

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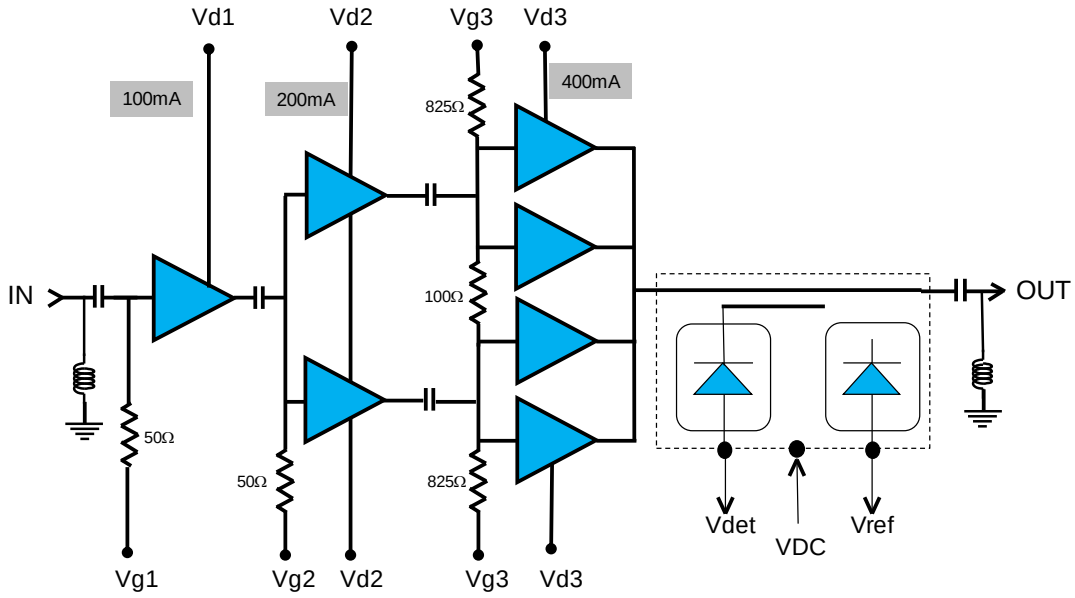
DC Schematic

Biasing: 6V, 700mA



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Notes

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 5x5 package:	CHA5356-QGG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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