

21.2 - 23.6GHz Power Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

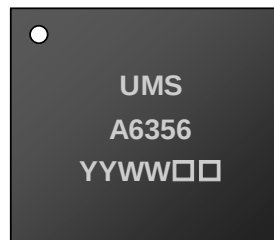
Description

The CHA6356-QXG is a three stage monolithic GaAs high power circuit producing 2 Watt output power. It integrates a power detector and allows gain control. ESD protections are included.

It is designed for Point To Point Radio or K-band Sat-Com application.

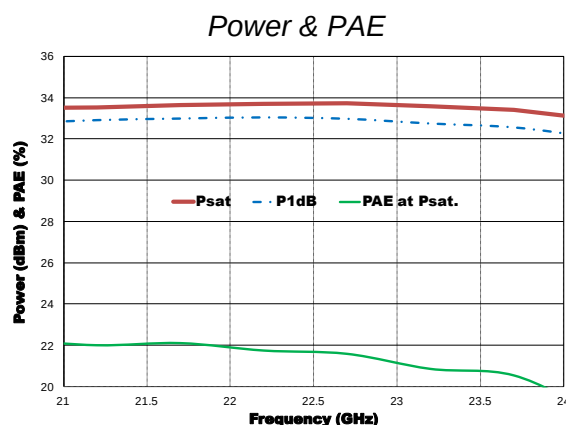
The circuit is manufactured with a pHEMT process, 0.15µm gate length.

It is supplied in RoHS compliant SMD package.



Main Features

- Frequency range: 21.2- 23.6GHz
- 33.5dBm saturated power
- 42dBm OIP3
- 20dB gain
- DC bias: Vd = 6.0Volt @ Id = 1.3A
- QFN5x6
- MSL3



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	21.2		23.6	GHz
Gain	Linear Gain		20		dB
Psat	Saturated output power		33.5		dBm
OIP3	Output IP3		42		dBm

Electrical Characteristics

Tamb.= +25°C, Vd = +6V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	21.2		23.6	GHz
Gain	Small Signal Gain		20		dB
Psat	Saturated Output Power		33.5		dBm
ΔG	Gain variation in temperature		+/- 0.03		dB/°C
OIP3	Output IP3		42		dBm
PAE	PAE at saturation		22		%
CG	Gain regulation range		15		dB
NF	Noise Figure @ nominal gain		4.5		dB
Rlin	Input Return Loss		18		dB
Rlout	Output Return Loss		14		dB
Dr	Detection dynamic range(for output power detection up to Psat)		30		dB
Vdetect	Voltage detection V_{REF} - V_{DET} up to Psat		10 to 2800		mV
Vg	DC gate Voltage		-0.85		V
Idet	Detector current		850		μA
Idq	Total drain current		1.3		A

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6.5V	V
Id	Drain bias quiescent current	1700	mA
Vg	Gate bias voltage	-2 to 0	V
Pin	Maximum peak input power overdrive ⁽²⁾	+20	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

⁽²⁾ Thermal Resistance channel to ground paddle =9.3°C/W for Tamb. = +85°C with 6.0V & 1.3A.

Typical Bias Conditions

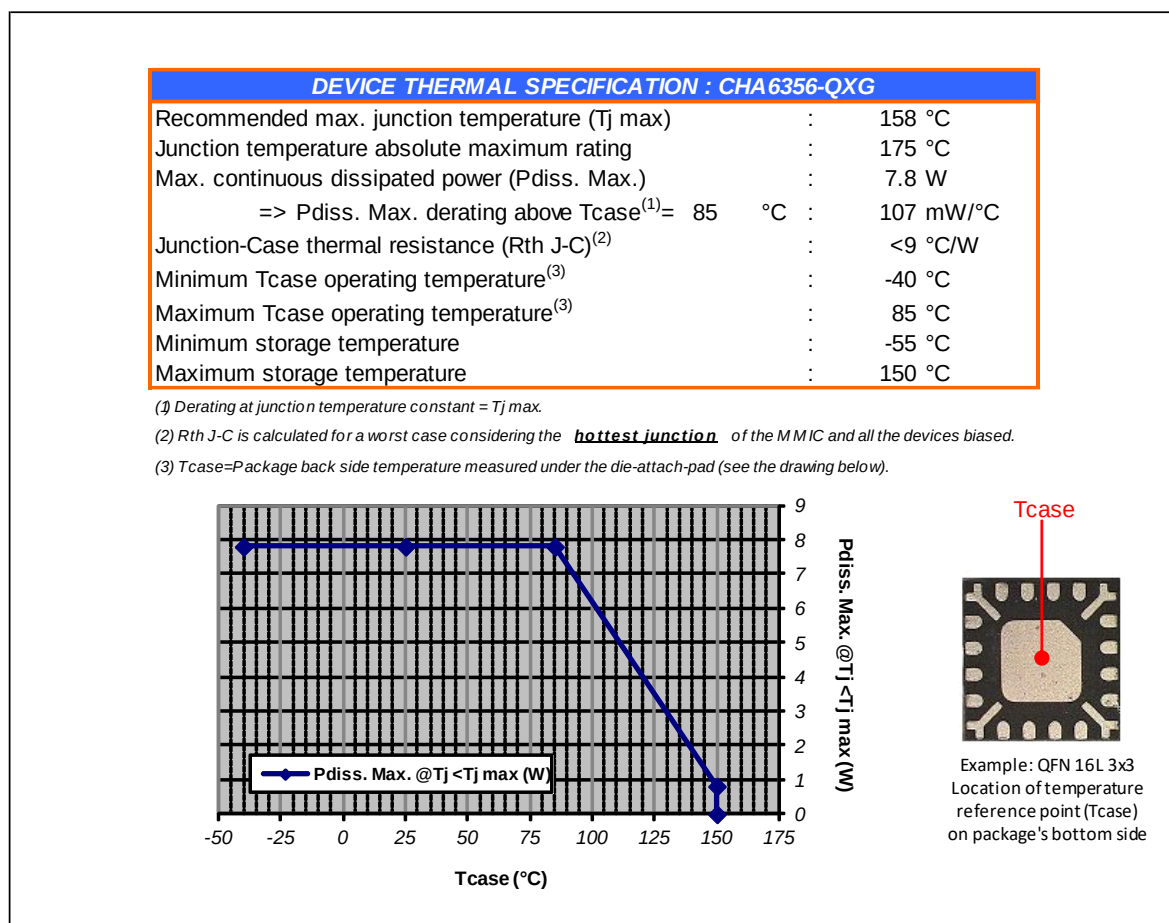
Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
VD1	7, 20	DC Drain voltage 1 st stage	6.0	V
VD2	5, 22	DC Drain voltage 2 nd stage	6.0	V
VD3	3, 24	DC Drain voltage 3 rd stage	6.0	V
VG1	8, 19	DC Gate voltage 1 st stage	-0.85	V
VG2	6, 21	DC Gate voltage 2 nd stage	-0.85	V
VG3	4, 23	DC Gate voltage 3 rd stage	-0.85	V
DC	1	DC Detector voltage	6.0	V

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below. The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).



Typical Package Sij parameters

Tamb.= +25°C, Vd = +6V, Id = 1300mA

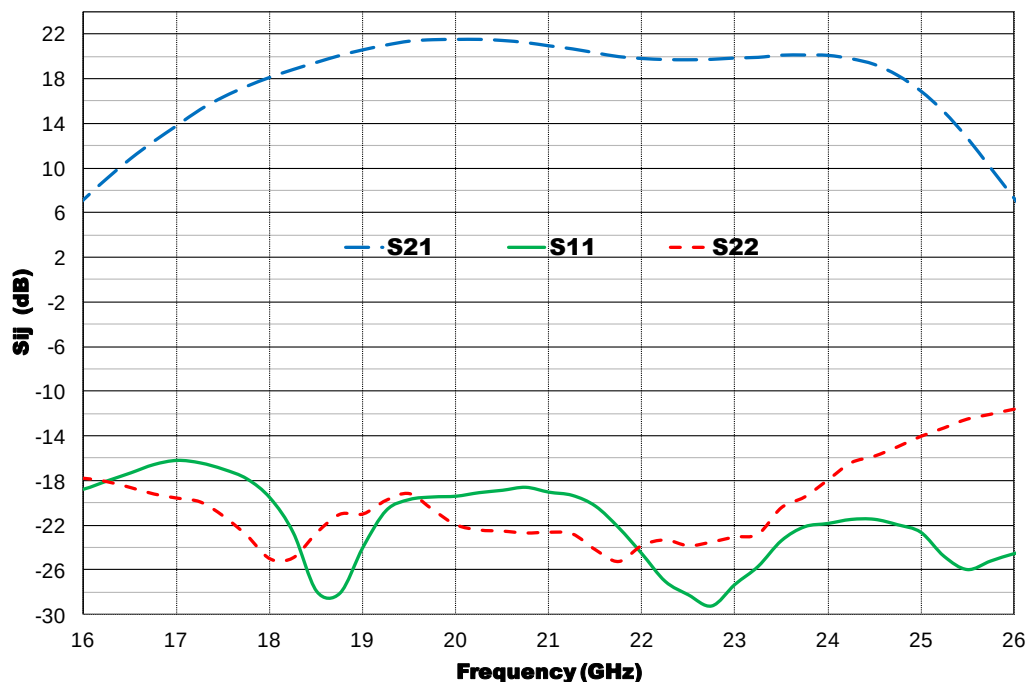
Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
1	-0.414	156.2	-73.770	99.8	-73.330	4.3	-0.299	155.8
2	-0.541	131.5	-73.384	53.7	-78.135	7.0	-0.495	131.1
3	-0.667	104.1	-71.320	58.3	-75.463	-3.6	-0.687	103.9
4	-2.088	66.2	-64.404	28.7	-67.133	21.3	-3.741	74.9
5	-6.237	68.8	-68.624	-151.7	-71.395	175.1	-3.342	73.8
6	-5.020	50.4	-68.331	30.4	-69.456	29.5	-3.044	50.1
7	-5.217	27.8	-65.479	-2.2	-64.668	-38.6	-3.307	25.2
8	-5.726	4.1	-69.860	-59.0	-67.388	-39.7	-3.719	-1.4
9	-6.073	-21.4	-67.716	-14.8	-74.019	-21.6	-4.505	-32.5
10	-6.597	-48.2	-61.953	-80.2	-65.246	-29.0	-5.659	-66.7
11	-7.429	-76.9	-57.920	-143.6	-60.041	-29.9	-7.255	-104.0
12	-8.541	-108.0	-55.590	149.5	-42.647	-70.9	-9.759	-143.5
13	-10.487	-144.4	-54.870	100.3	-28.090	-142.3	-13.681	176.4
14	-13.929	168.4	-54.928	75.1	-14.422	127.2	-23.328	130.9
15	-19.097	94.0	-53.426	59.2	-2.267	15.7	-24.497	-69.6
16	-18.791	-3.6	-51.127	45.6	7.156	-109.9	-17.083	-109.7
17	-15.960	-75.4	-54.760	9.6	13.717	120.1	-16.829	-130.3
18	-19.082	-133.7	-49.119	18.4	17.995	-10.6	-18.821	-138.4
19	-24.182	-93.4	-47.738	-14.5	20.484	-136.3	-16.444	-123.7
20	-19.596	-132.7	-47.859	-49.9	21.358	98.8	-16.288	-136.5
21	-18.555	177.2	-54.511	-58.8	20.688	-20.2	-16.633	-134.0
22	-22.444	106.8	-51.969	-21.2	19.562	-128.9	-17.220	-128.2
23	-27.941	-3.9	-48.925	-21.3	19.619	122.7	-16.107	-122.3
24	-25.000	-90.3	-47.679	-40.4	19.880	-1.7	-13.638	-119.7
25	-24.519	-155.6	-42.340	-31.6	16.701	-147.9	-11.594	-136.8
26	-27.392	-127.3	-40.176	-67.8	7.237	77.9	-11.681	-165.7
27	-23.100	-120.2	-38.911	-85.1	-3.420	-26.6	-13.771	160.1
28	-16.543	-137.6	-36.840	-114.7	-13.054	-115.1	-17.184	112.1
29	-12.498	-168.2	-36.523	-137.7	-22.251	174.1	-19.473	38.3
30	-9.962	157.7	-36.450	-160.7	-31.980	126.6	-17.184	-33.2
31	-8.771	123.9	-36.602	178.1	-40.595	137.4	-15.351	-92.2
32	-8.649	87.3	-36.094	150.6	-38.033	148.5	-13.335	-155.4
33	-9.533	42.1	-40.457	121.9	-41.617	127.6	-9.801	147.8
34	-10.924	-29.5	-43.517	115.6	-46.351	113.5	-6.945	104.4
35	-8.097	-116.9	-46.137	109.2	-48.926	131.7	-4.999	71.0
36	-4.314	-178.1	-49.039	104.7	-45.760	151.7	-4.439	43.3
37	-2.218	140.5	-46.798	159.6	-43.979	156.8	-6.552	17.3
38	-1.185	108.2	-38.359	140.5	-39.640	137.2	-9.898	61.2
39	-0.966	82.9	-37.092	114.8	-36.878	99.1	-3.015	48.5
40	-0.729	60.9	-37.276	81.6	-35.367	75.5	-1.652	26.8

Typical board Measurements

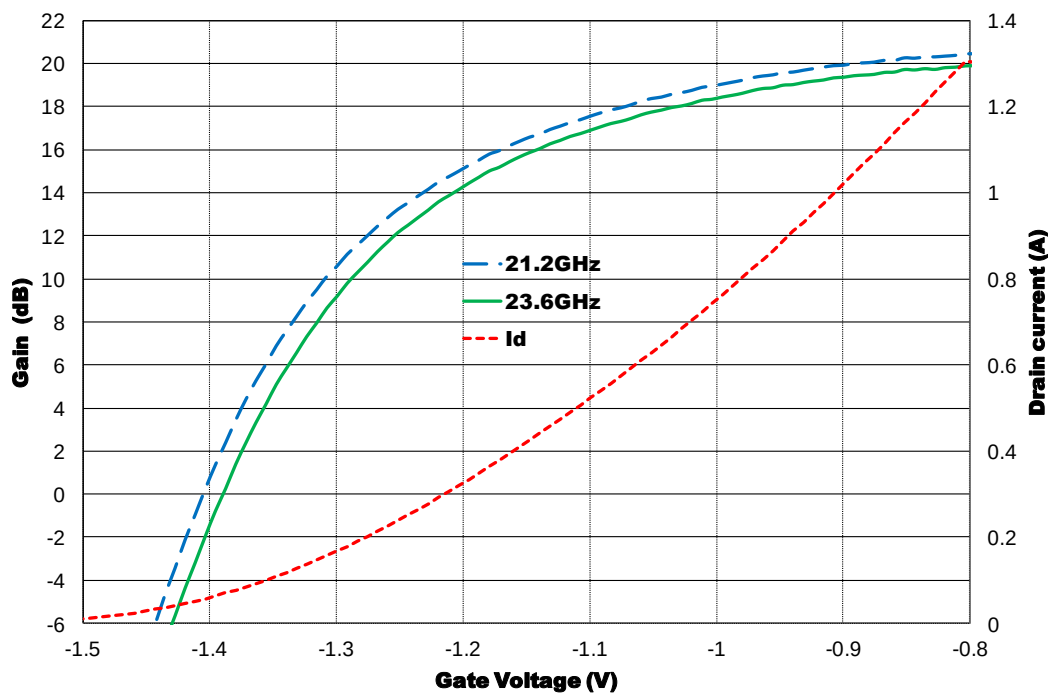
Tamb = +25°C, Vd = +6V, Id = 1300mA

Measurement in the plan of the QFN, using the proposed land pattern & board, as defined in paragraph "Evaluation mother board"

S parameters versus Frequency



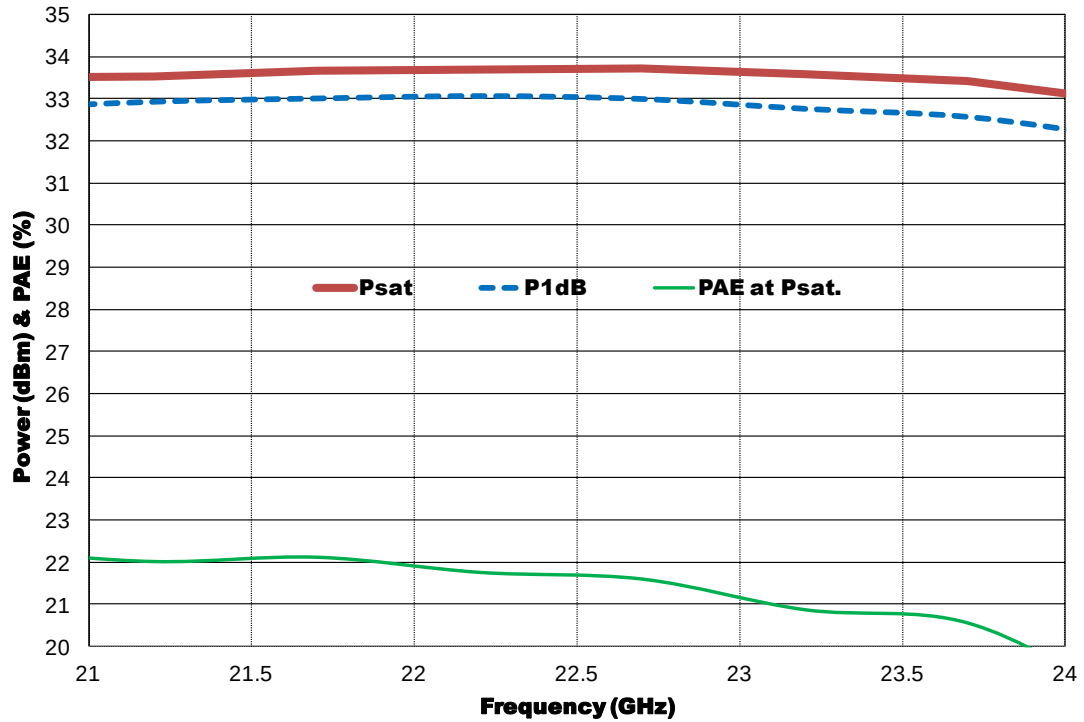
Linear Gain & current versus Gate Voltage



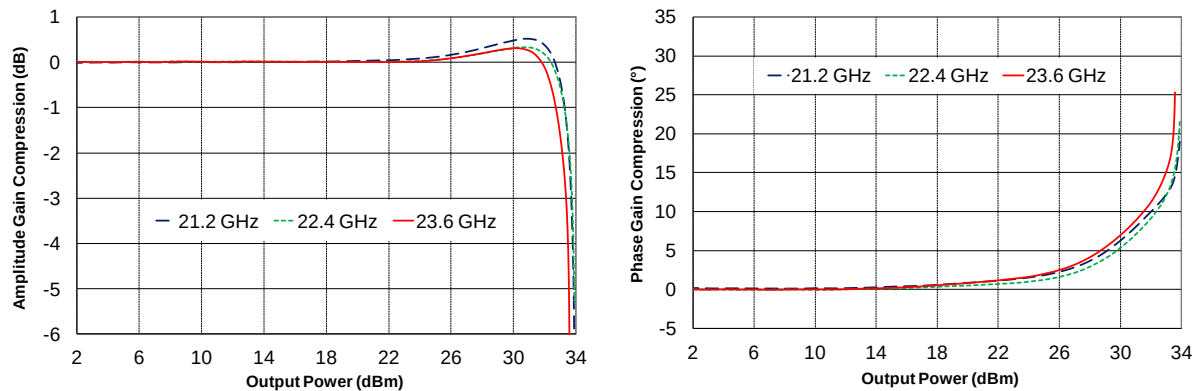
Typical Board Measurements

Tamb.= +25°C, Vd = +6V, Id = 1300mA

Output power & PAE versus Frequency



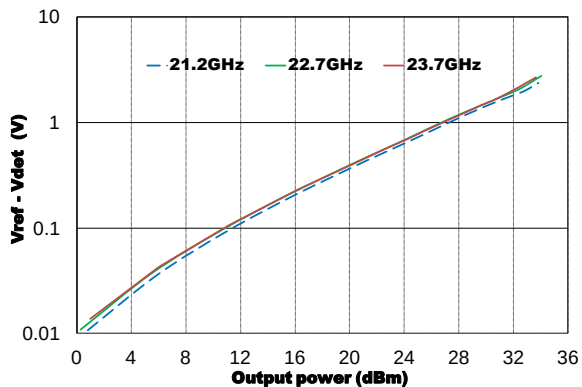
Amplitude & Phase variation versus Output Power



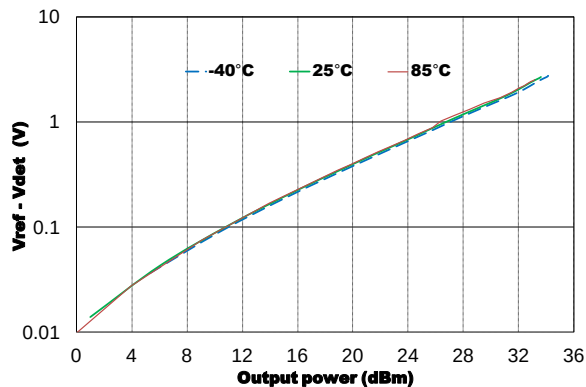
Typical board Measurements

Tamb.= +25°C, Vd = +6V, Id = 1300mA

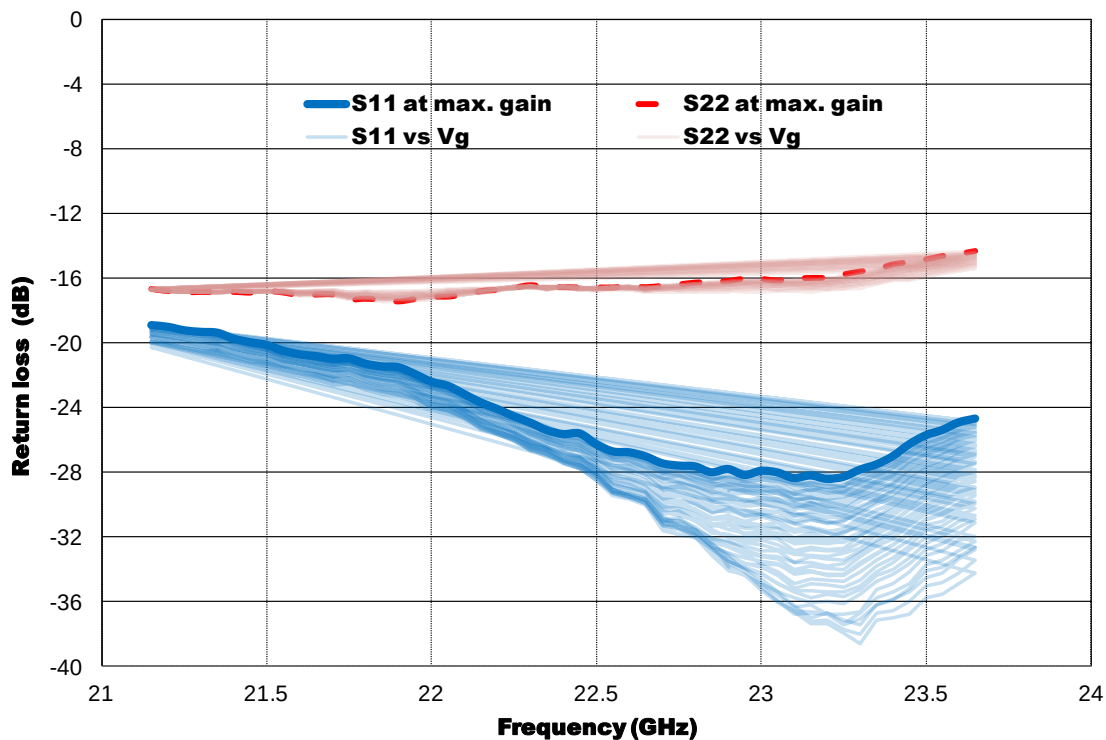
Power Detector versus Pout & Frequency



Power Detector versus Pout & Temperature

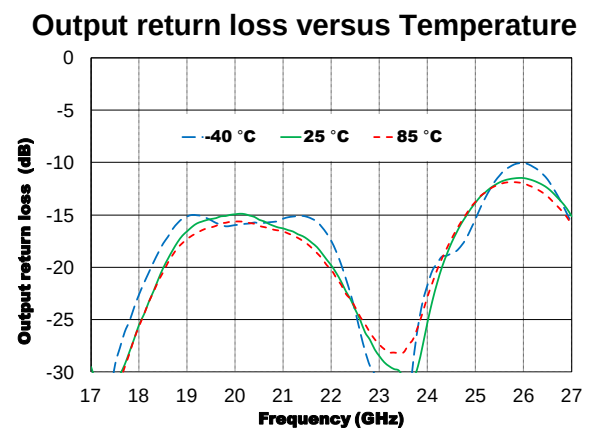
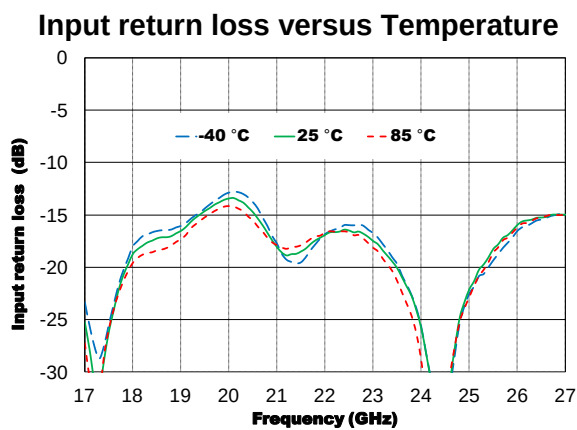
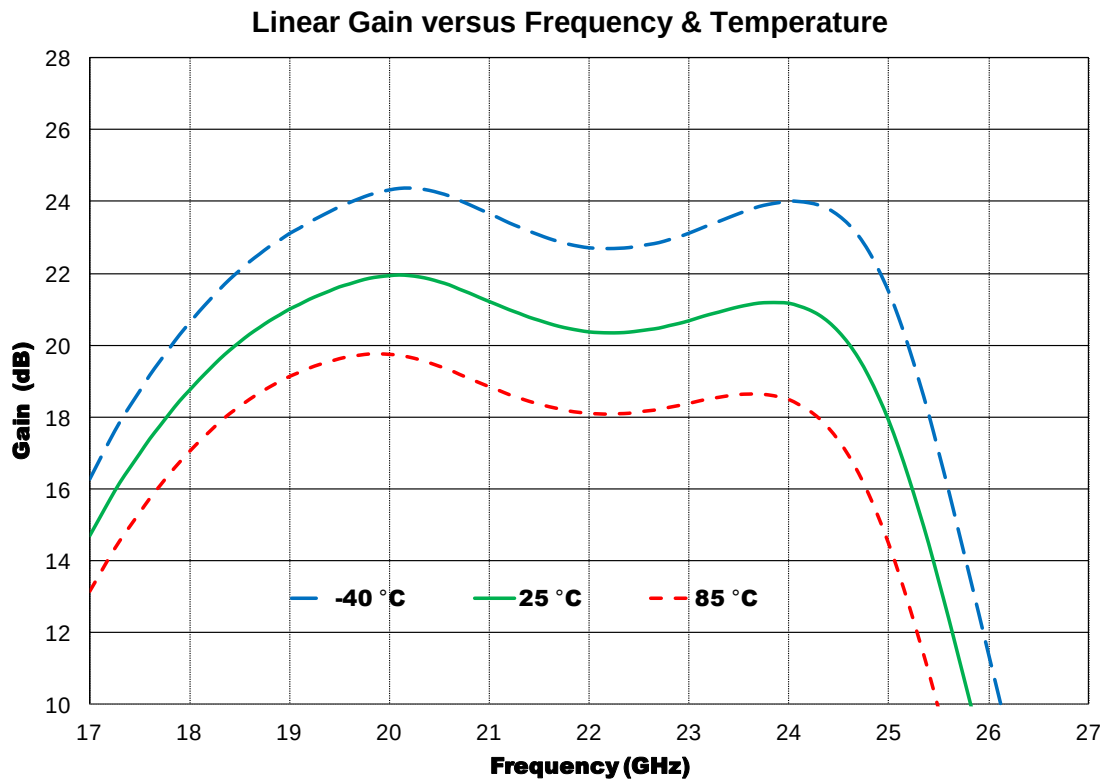


Return Losses versus Gain Control



Typical bord Measurements

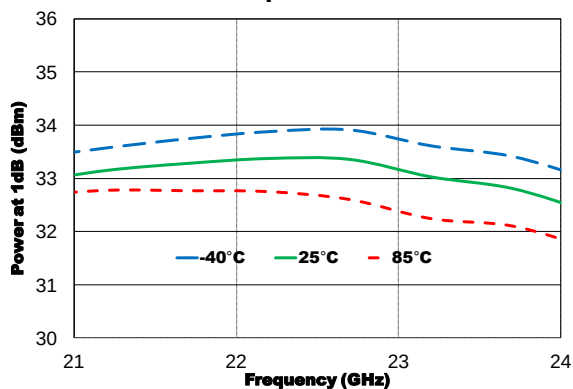
Tamb.= +25°C, Vd = +6V, Id = 1300mA



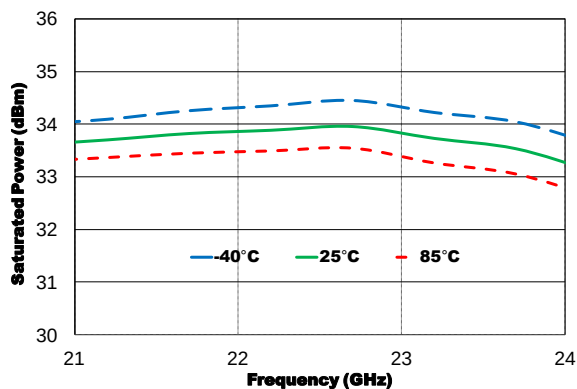
Typical Board Measurements

Tamb.= +25°C, Vd = +6V, Id = 1300mA

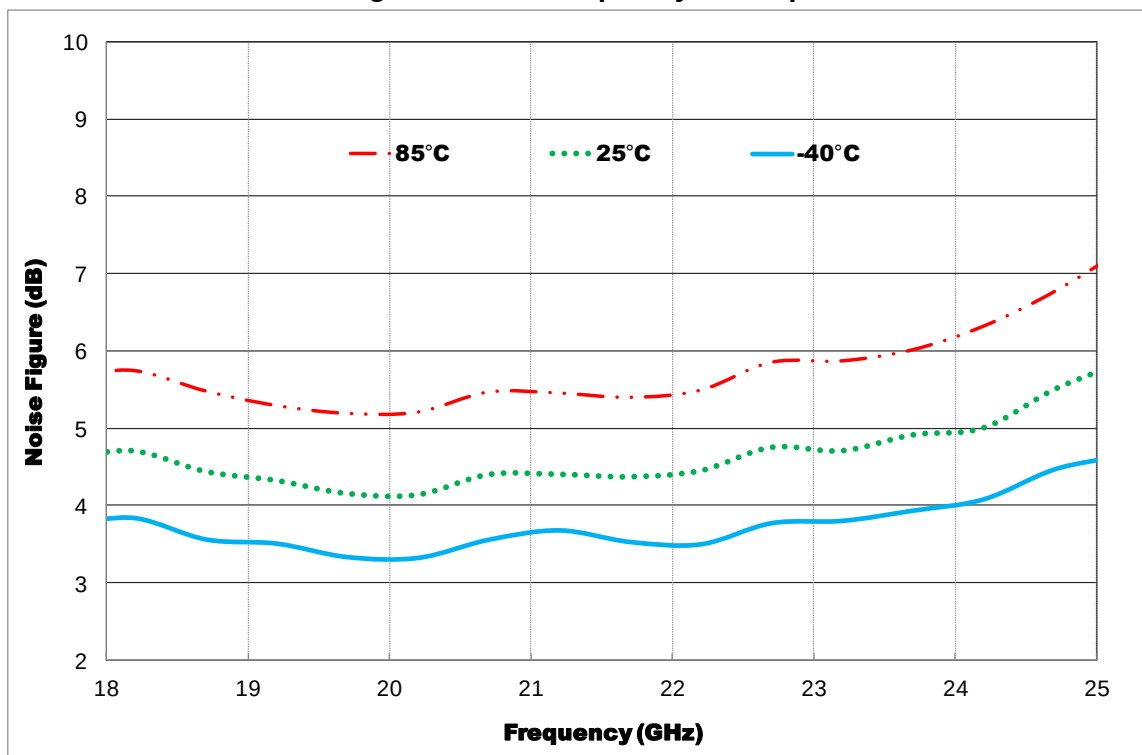
Power at 1dB compression versus Temperature



Saturated Power versus Temperature



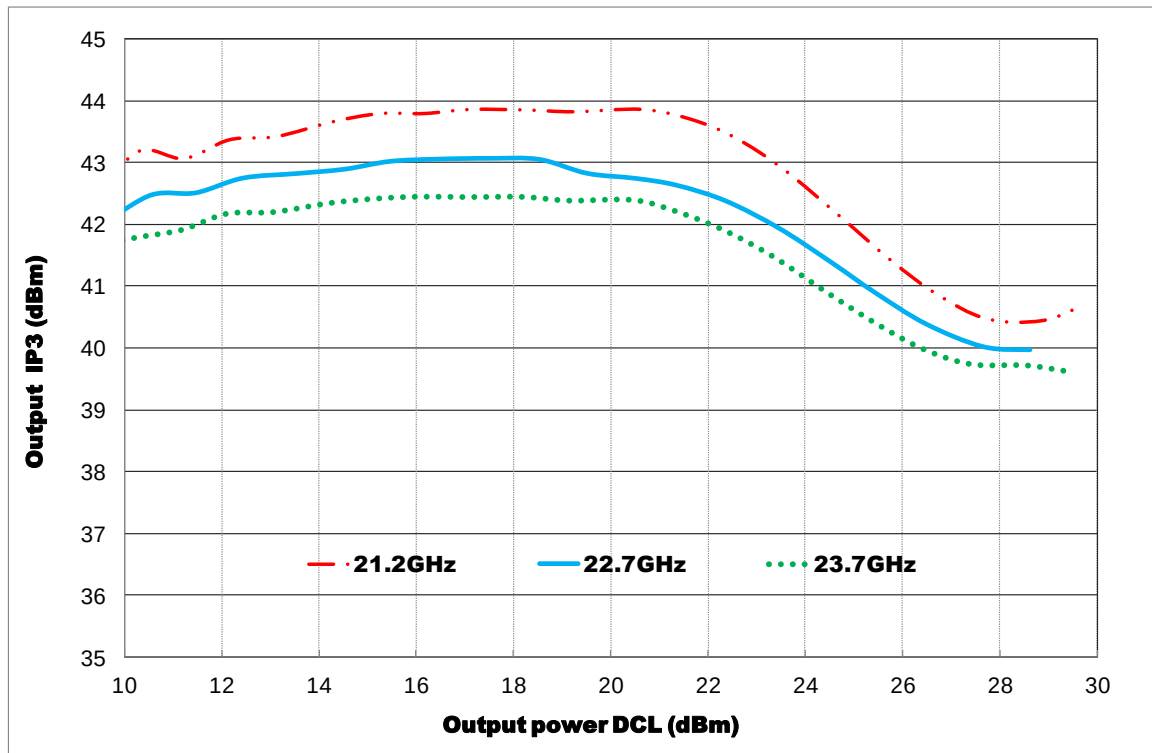
Noise Figure versus Frequency & Temperature



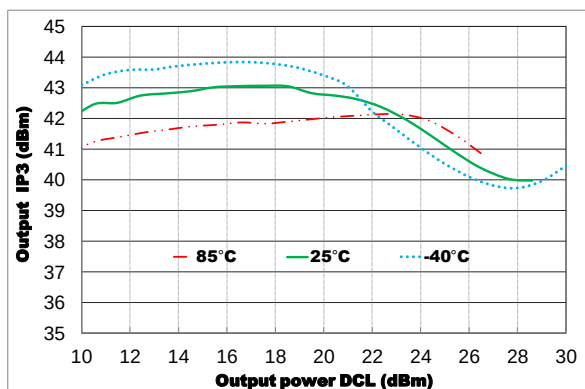
Typical Board Measurements

Tamb.= +25°C, Vd = +6V, Id = 1300mA

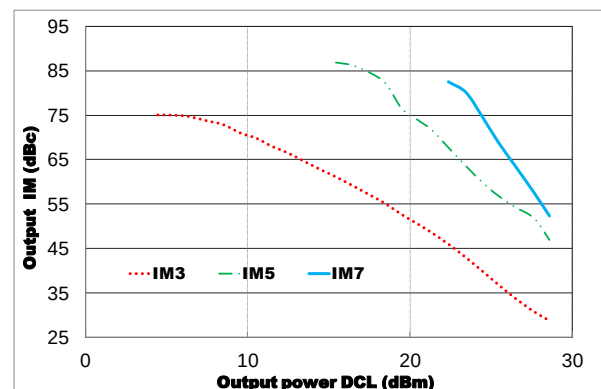
Output IP3 versus Output Power



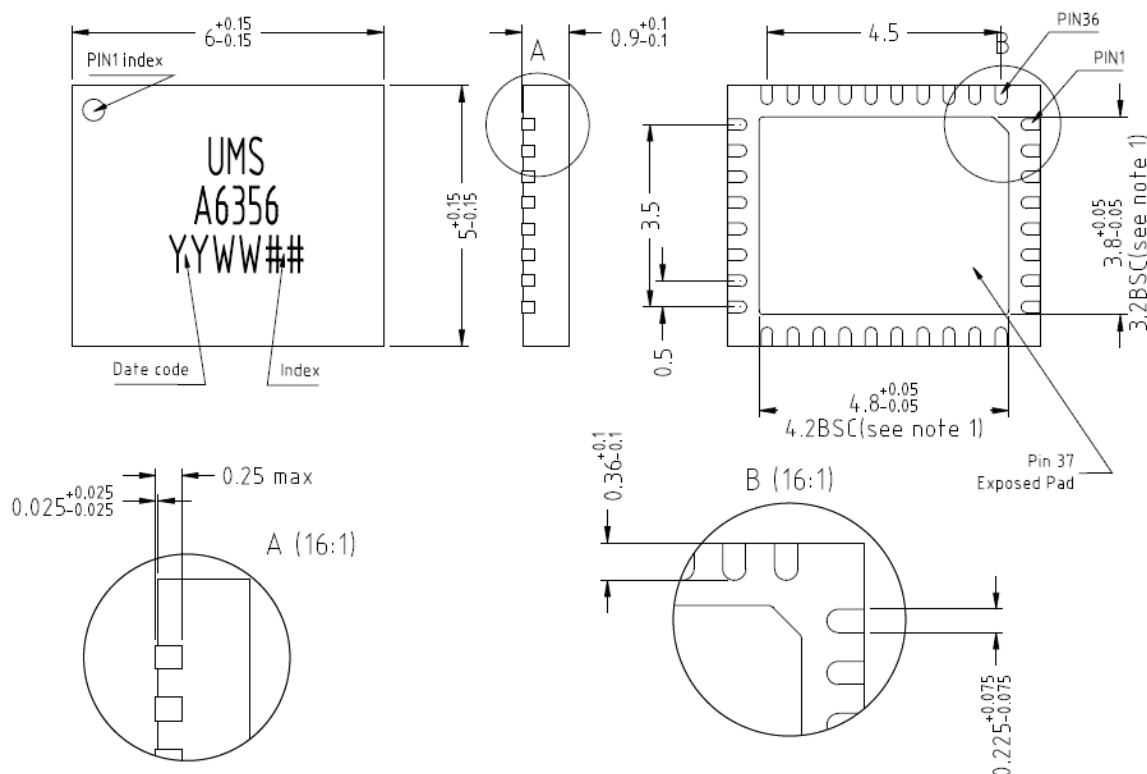
OIP3 versus temperature
at 22.7GHz



IMD3 versus Output Power



Package outline ⁽¹⁾



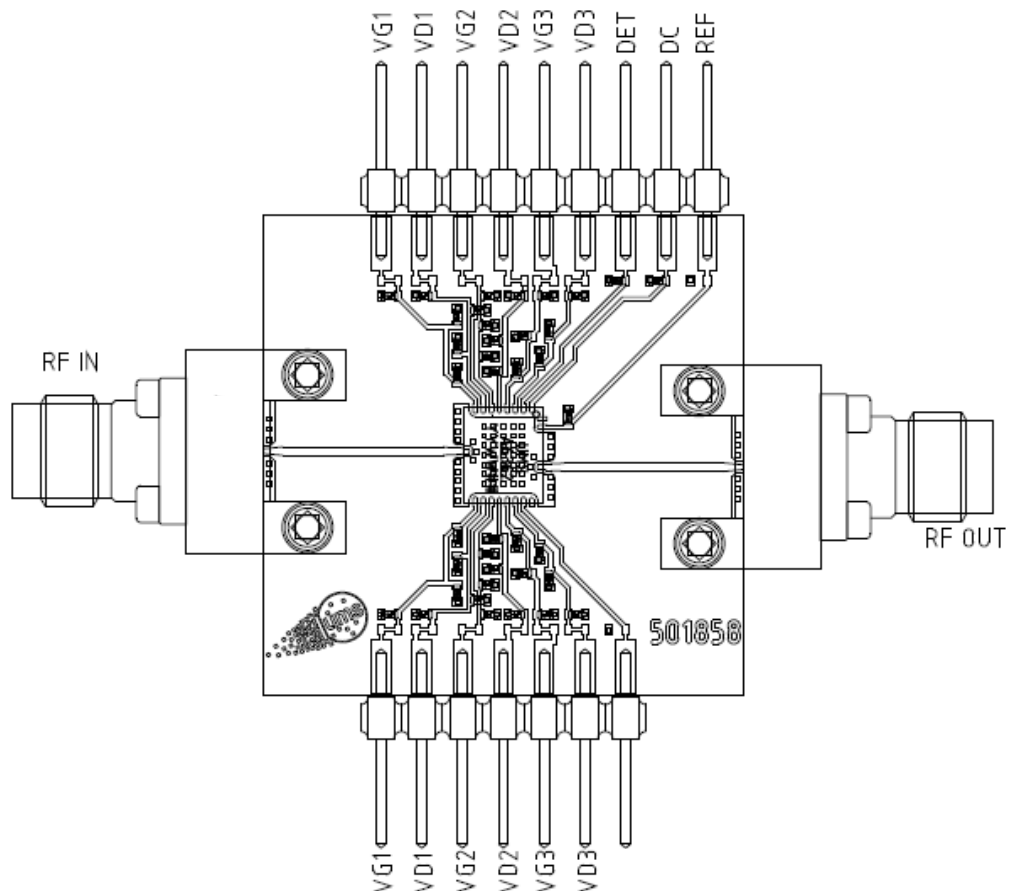
Matte tin, Lead Free (Green)	1- DC	13- RF in	25- Gnd ⁽²⁾
Units : mm	2- DET	14- Gnd ⁽²⁾	26- Nc
From the standard : JEDEC MO-220	3- VD3	15- Nc	27- Gnd ⁽²⁾
(VGGD)	4- VG3	16- Nc	28- Nc
37- GND	5- VD2	17- Nc	29- Gnd ⁽²⁾
	6- VG2	18- Nc	30- RF out
	7- VD1	19- VG1	31- Nc
	8- VG1	20- VD1	32- Nc
	9- Nc	21- VG2	33- Nc
	10- Nc	22- VD2	34- Nc
	11- Nc	23- VG3	35- REF
	12- Nc	24- VD3	36- Nc

⁽¹⁾ The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<https://www.ums-rf.com>) for exact package dimensions.

⁽²⁾ It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

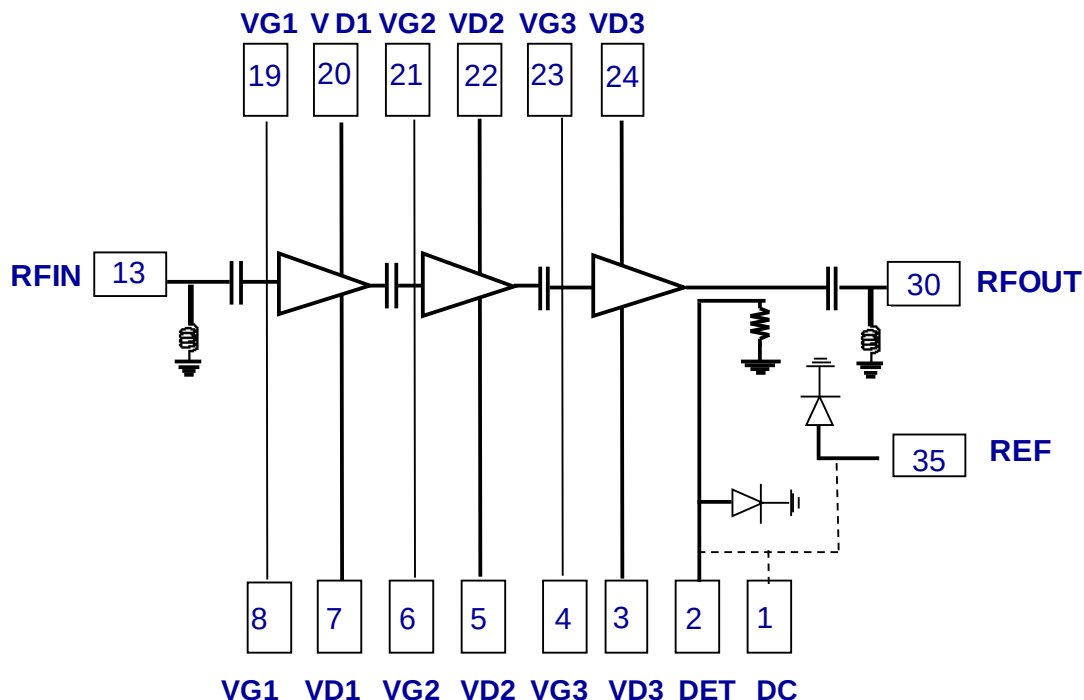
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4350 / 10mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF $\pm 5\%$, 10nF $\pm 10\%$ and 1 μ F $\pm 10\%$ are recommended for all DC accesses.
- A 10K Ω resistor is recommended on VREF & VDET accesses for the detector
- See application note AN0017 for details.



Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



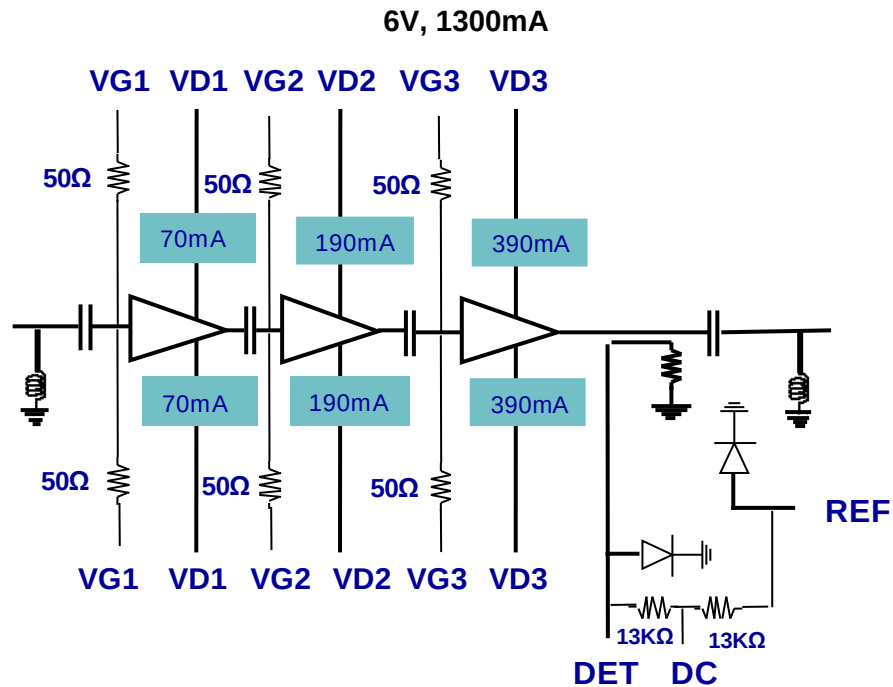
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF, 10nF, 1μF) on the PC board, as close as possible to the package.

A 10KΩ resistor is recommended in parallel to VDET, and VREF accesses.

The circuit includes ESD protections on all RF and DC leads

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	3

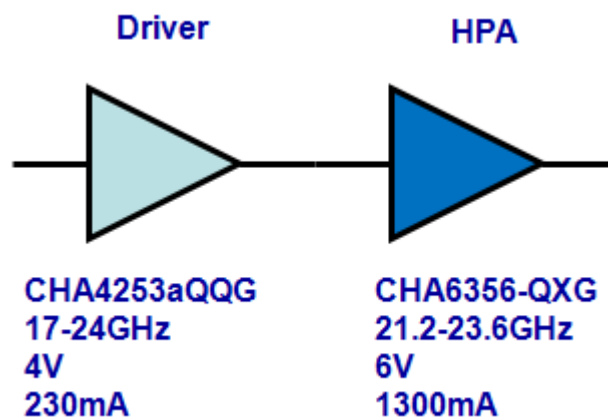
DC Schematic**Recommended UMS Power chain**

The CHA6356-QXG could be associated with the CHA4253aQQG as driver.

Total Gain: 44dB

Gain control: 30dB with the both amplifiers.

For more information, please see the CHA4253aQQG datasheet.



Recommended package footprint

Refer to the application note AN0017 available at <https://www.ums-rf.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 5x6 package:

CHA6356-QXG/XY

Stick: XY = 20

Tape & reel: XY = 21

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