12-16GHz 1W High Power Amplifier

Preliminary

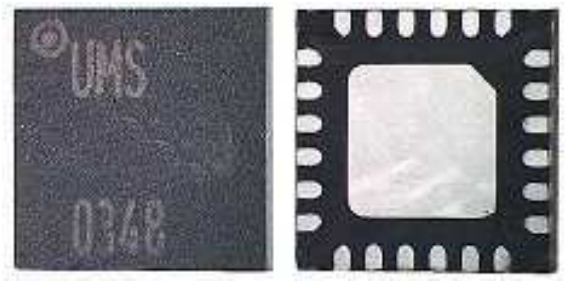
GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHA6664-QDG is a three-stages Ku-band high power amplifier.

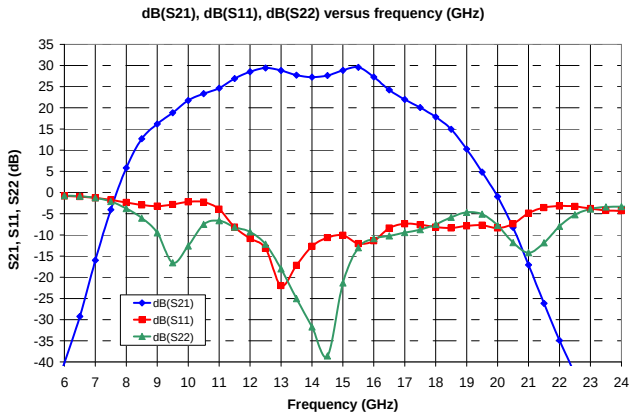
The circuit is manufactured with a standard Power P-HEMT process: 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in RoHS compliant SMD package.



Main Features

- 0.25 µm Power pHEMT Technology
- 12-16 GHz Frequency Range
- 31.5 dBm Saturated Output Power
- High gain: 28dB
- Quiescent Bias Point: 8V, 600mA
- 24L-QFN4x4 SMD package



Typical on board measurements

Main Characteristics

Tamb = +25°C, Vd1=Vd2=Vd3=+8V, Id (Quiescent)=600mA , CW biasing mode

Symbol	Parameter	Min	Typ	Max	Unit
F_op	Operating Frequency Range	12		16	GHz
P_Sat	Saturated output power		31.5		dBm
G_lin	Linear Gain		28		dB

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics

Tamb = +25℃, Vd1=Vd2=Vd3=+8V, Id (Quiescent)=600mA , CW biasing mode
These values are representative of onboard measurements as defined on the drawing 96372

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	12		16	GHz
G_lin	Linear Gain		28		dB
ΔG	Gain flatness (12 – 16GHz)		±2		dB
G_lin_T	Linear gain variation versus temperature		±0.06		dB/℃
IS11I	Input return loss (12 – 16GHz)		2.0:1		
IS22I	Output return loss		2.0:1		
P1dB	Output power at 1dB gain compression		30		dBm
P_Sat	Saturated Output power		31.5		dBm
PAE_Sat	Power Added Effciency in saturation		25		%
Id	Power supply quiescent current (1)		600		mA
Id_1dBc	Power supply @1dB gain compression		750		mA
Id_sat	Power supply in saturation		800		mA
Vd 1,2,3	Positive drain bias voltage		8		V
Vg 1,2,3	Negative gate bias voltage		-0.8		V

(1) This parameter is fixed by gate voltage Vg
(2) The reference is the backside of the package

Absolute Maximum Ratings (1)

Tamb = +25℃

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	9	V
Pin	RF input power	14	dBm
Tj	Junction temperature (2)	175	℃
Top	Operating temperature range	-40 to +85	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

(2) Equivalent thermal resistance channel to ground paddle =15.7℃/W for Tground paddle. = +85℃ with 8V, 600mA

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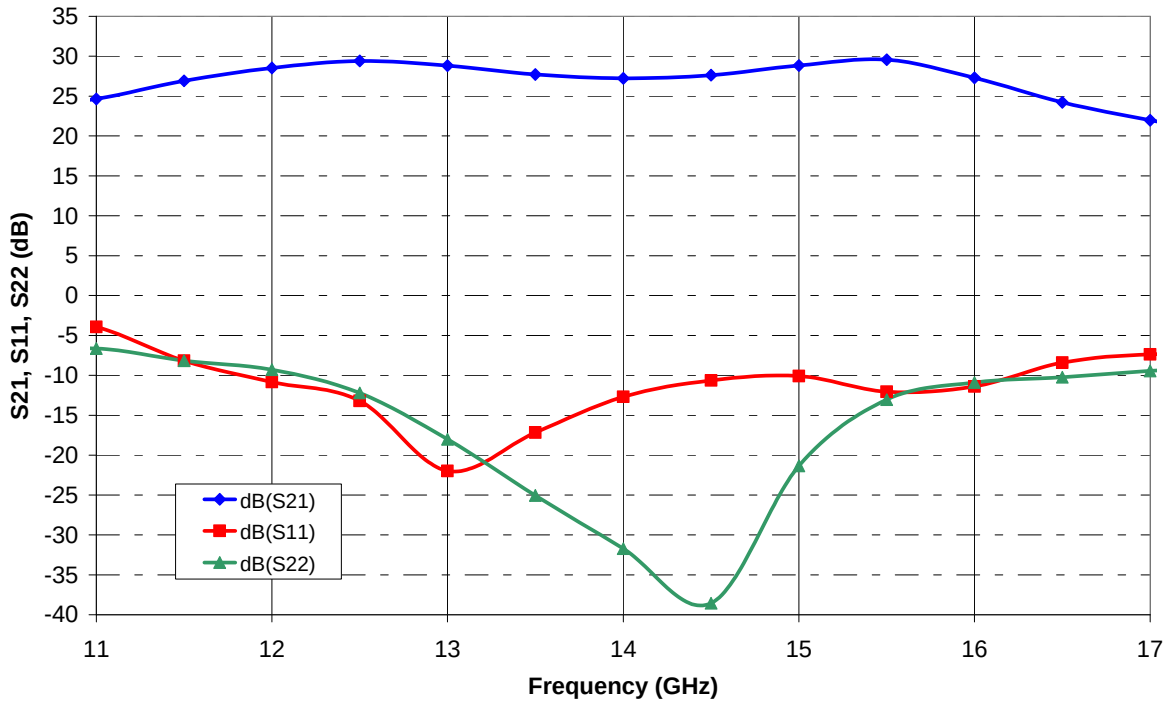
Typical Measured Performance

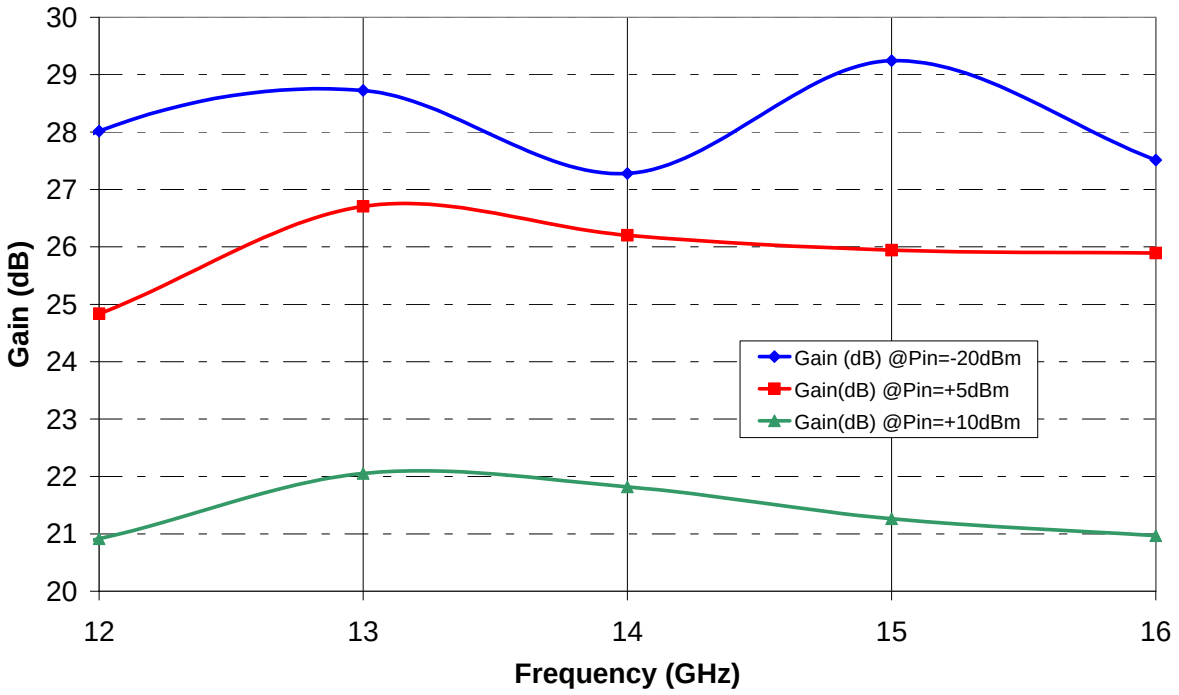
Tamb = +25°C, Vd1=Vd2=Vd3=+8V, Id (Quiescent)=600mA , CW biasing mode

Measurements in the board access planes (without any correction), using the proposed land pattern & board 96372.

Gain and Input/Output Return Losses (dB)



Gain (dB) versus Frequency @Pin=[-20; +5; +10dBm]



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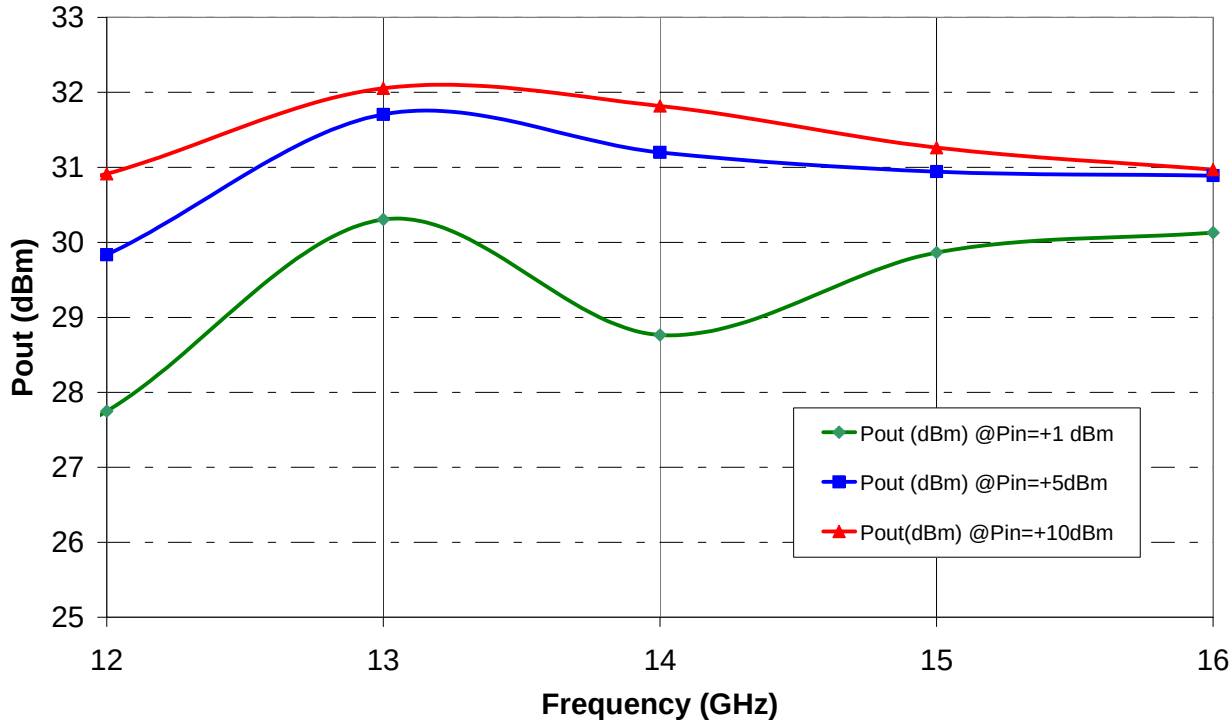
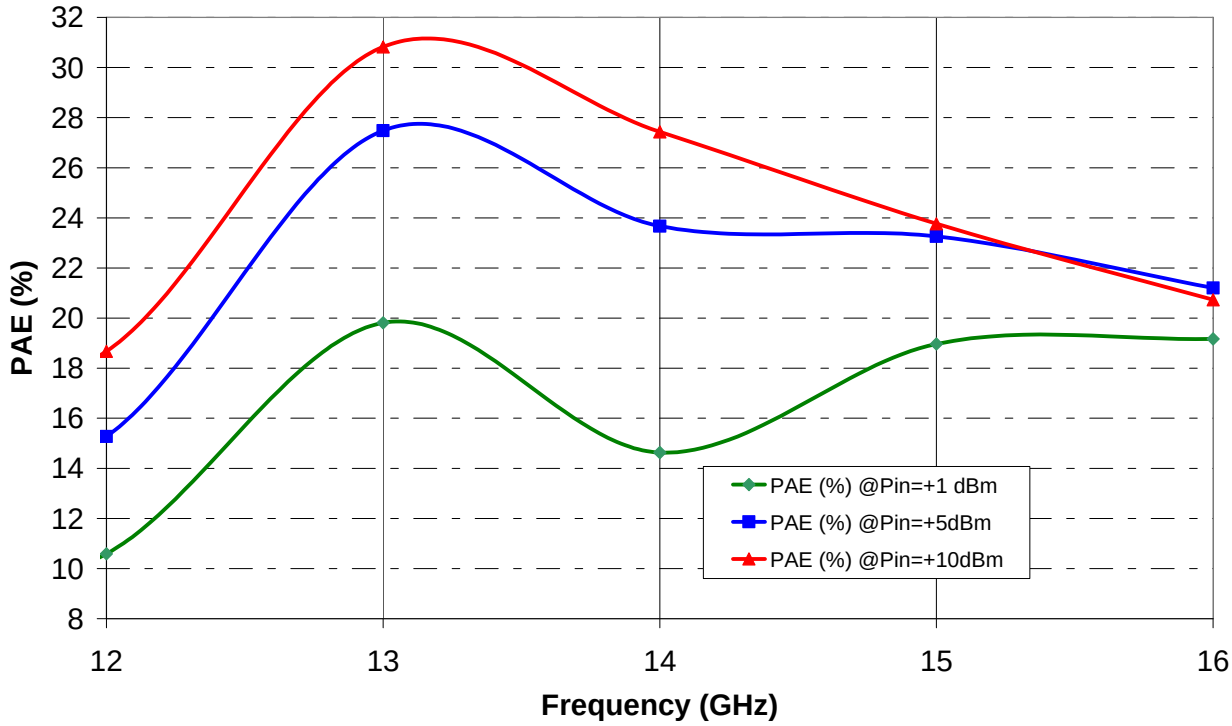
Output power (dBm) versus Frequency @Pin=[+1; +5; +10dBm]



Power Added Efficiency (%) versus Frequency @Pin=[+1; +5; +10dBm]



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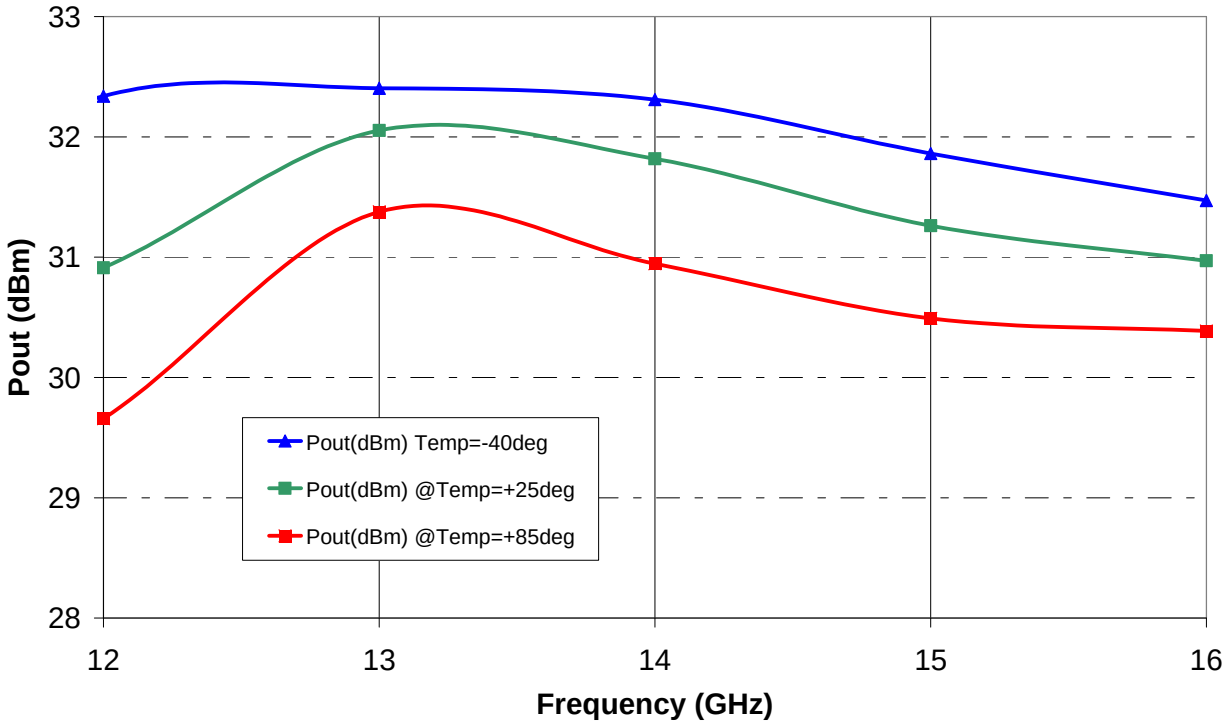
Output power (dBm) versus Frequency @Pin=+10dBm
Temp=[-40 / +25 / +85 deg]



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Package outline:

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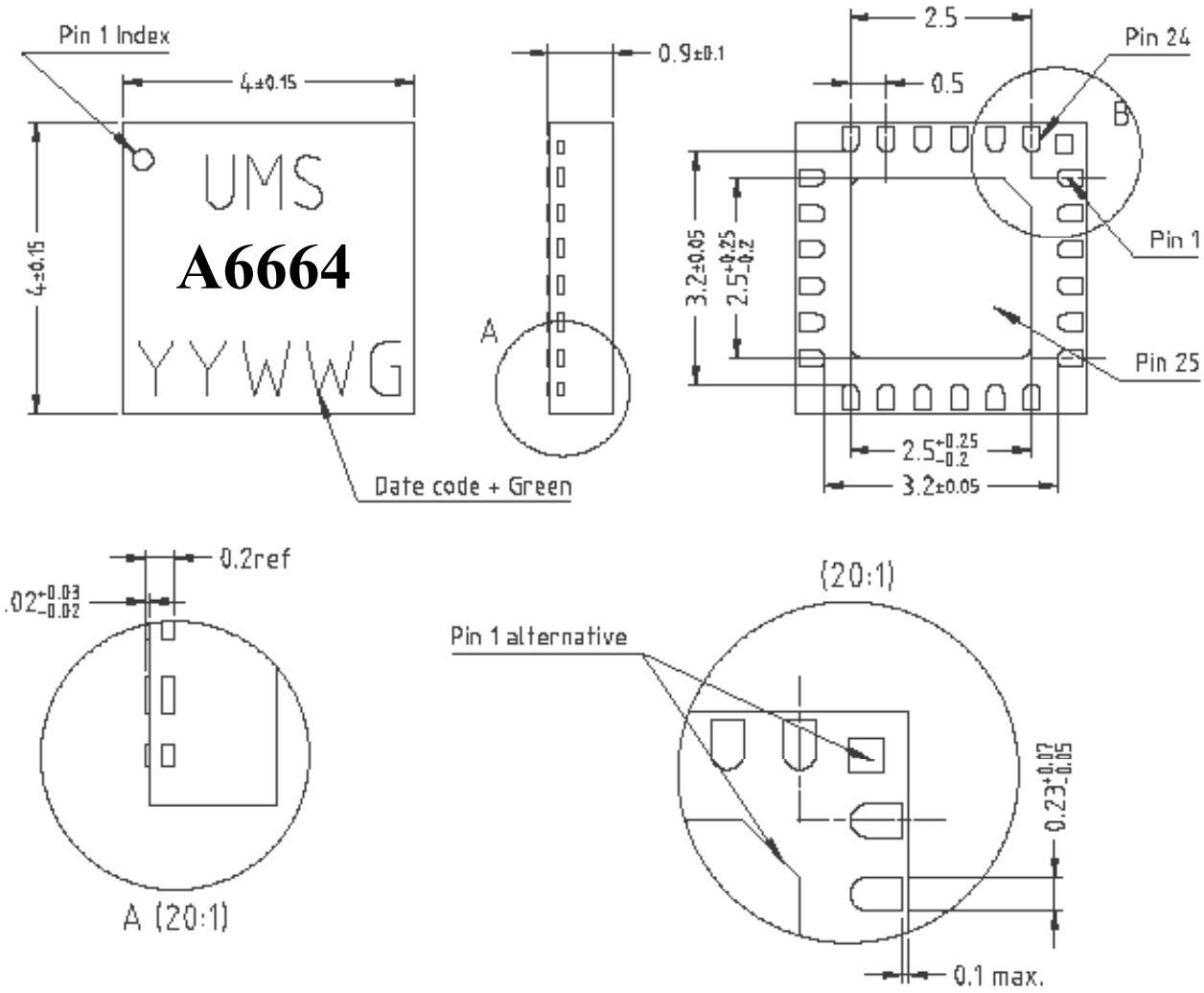

Matt tin, Lead Free	(Green)	1-		Nc	13-		Gnd
Units	mm	2-		Gnd	14-		Gnd
From the standard	JEDEC MO-220	3-		Gnd	15-		RF IN
Pin 25 (paddle)	GND	4-		RF OUT	16-		Gnd
		5-		Gnd	17-		Gnd
		6-		Gnd	18-		Nc
		7-		Vd3	19-		Nc
		8-		Vd2	20-		Vg1
		9-		Nc	21-		Vg2
		10-		Vd1	22-		Vg3
		11-		Nc	23-		Nc
		12-		Nc	24-		Nc

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Application note

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The design of the motherboard has a strong impact on the over all performance since the transition from the motherboard to the package is comparably large. In case of the SMD type packages of United Monolithic Semiconductors the motherboard should be designed according to the information given in the following to achieve good performance. Other configurations are also possible but can lead to different results. If you need advise please contact United Monolithic Semiconductors for further information.

SMD type packages of UMS should allow design and fabrication of micro- and mm-wave modules at low cost. Therefore, a suitable motherboard environment has been chosen. All tests and verifications have been performed on Rogers RO4003. This material exhibits a permittivity of 3.38 and has been used with a thickness of 200µm [8 mils] and a 1/2oz or less copper cladding. The corresponding 50Ohm transmission line has a strip width of about 460µm [approx. 18 mils].

The contact areas on the motherboard for the package connections should be designed according to the footprint given above. The proper via structure under the ground pad is very important in order to achieve a good RF and lifetime performance. All tests have been done by using a grid of plenty plated through vias with a diameter of less than 300µm [12 mils] and a spacing of less than 700µm [28 mils] from the centres of two adjacent vias. The via grid should cover the whole space under the ground pad and the vias closest to the RF ports should be located near the edge of the pad to allow a good RF ground connection. Since the vias are important for heat transfer, a proper via filling should be guaranteed during the mounting procedure to get a low thermal resistance between package and heat sink. For power devices the use of heat slugs in the motherboard instead of a grid of via's is recommended.

For the mounting process the SMD type package can be handled as a standard surface mount component. The use of either solder or conductive epoxy is possible. The solder thickness after reflow should be typical 50µm [2 mils] and the lateral alignment between the package and the motherboard should be within 50µm [2 mils]. Caution should be taken to obtain a good and reliable contact over the whole pad areas. Voids or other improper connections, in particular, between the ground pads of motherboard and package will lead to a deterioration of the RF performance and the heat dissipation. The latter effect can reduce drastically reliability and lifetime of the product.

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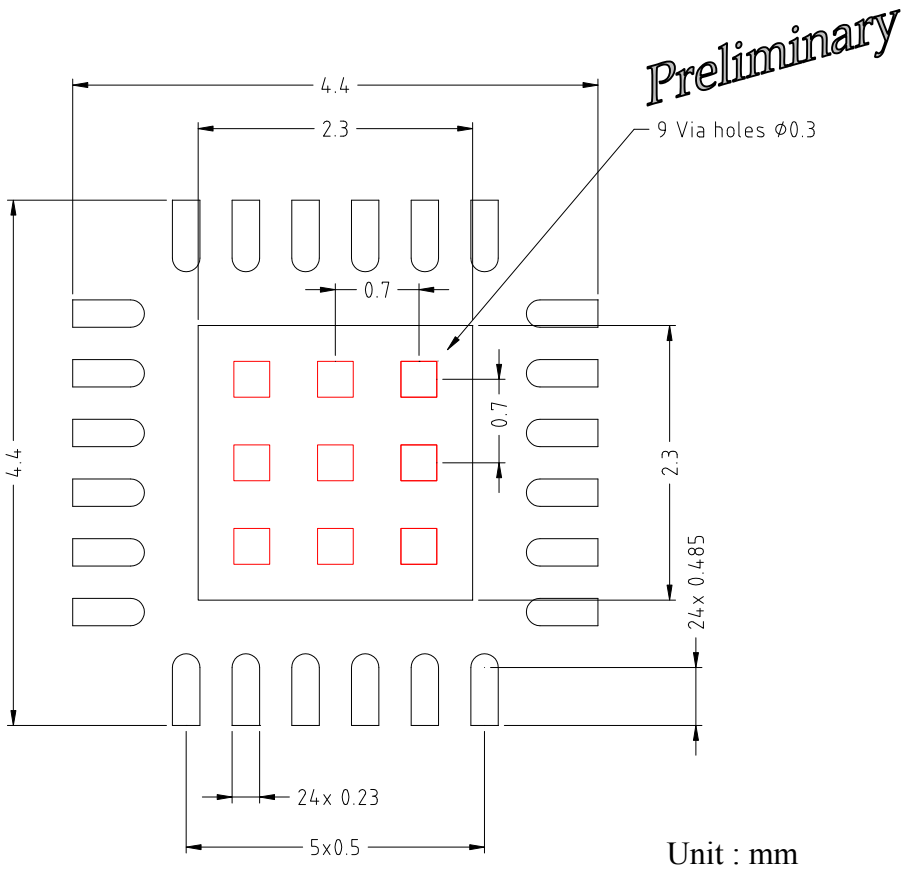

(For production, design must be adapted with regard to PCB tolerances and assembly process)

Basic footprint for a 24L-QFN4x4
(Please, refer to the UMS proposed footprint for optimum operation in the following “Proposed Assembly board” section)

The RF ports are DC blocked on chip. The DC connection (Vd) does not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

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Proposed Assembly board “96372” for the 24L-QFN4x4 products characterization.

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- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
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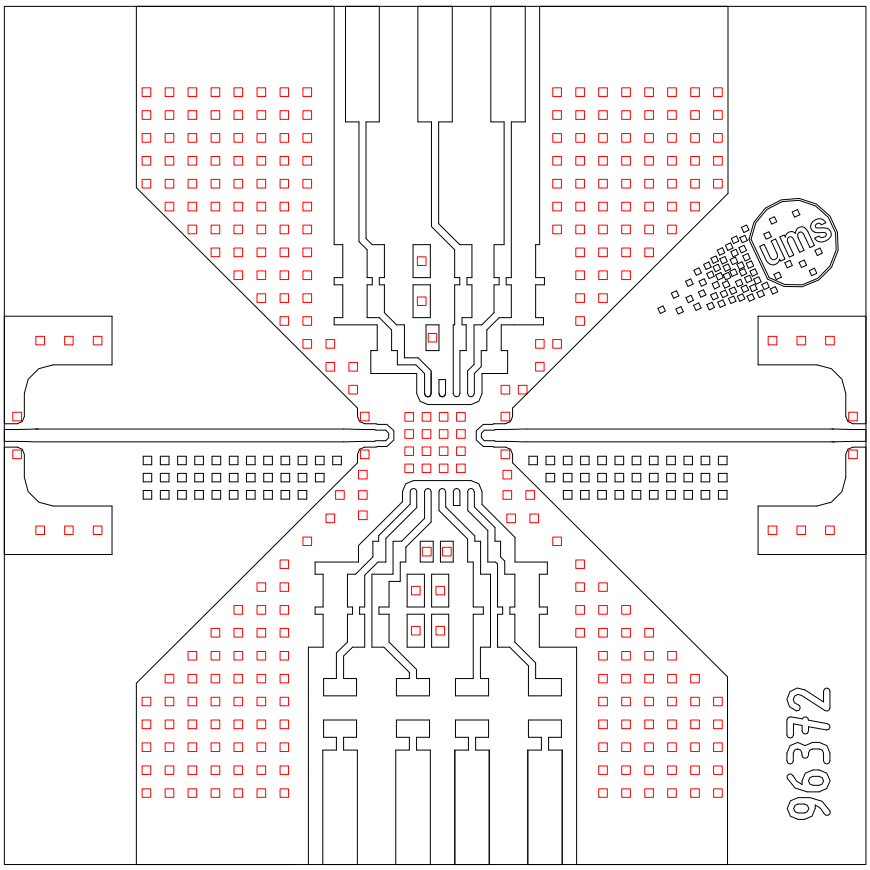

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Ordering Information

QFN 4x4 RoHS compliant package: CHA6664-QDG/XY
Stick: XY = 20 Tape & reel: XY = 21

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