United Monolithic Semiconductors

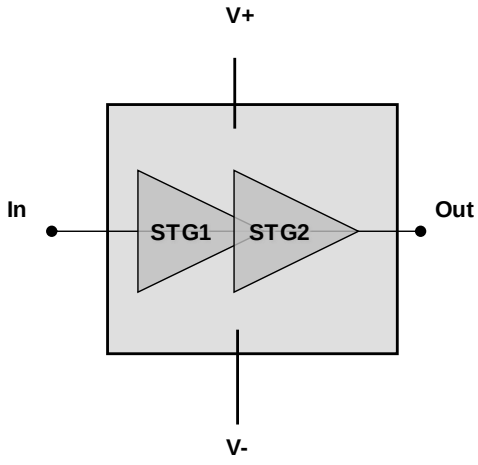
CHA6710-99F

5W X Band Medium Power Amplifier

GaN Monolithic Microwave IC

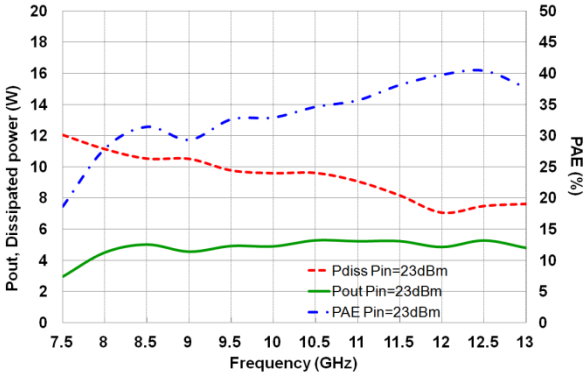
Description

The CHA6710-99F is a two stage Medium Power Amplifier operating between 8 and 12.75GHz. It typically provides 5W of saturated output power and 36% of power added efficiency.
It is designed for a wide range of applications, from military to commercial communication systems.
The circuit is manufactured with a GaN pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Main Features

- Frequency range: 8-12.75GHz
- High output power: 5.5W
- High PAE: 36%
- Linear Gain: 23.5dB
- DC bias: Vd=25Volt @ Idq=0.2A
- Chip size 2.7x2.15x0.1mm
- Available in bare die



Main Electrical Characteristics

Tamb.= +25°C, Vd = +25V, Idq = 200mA, Pulse width=25µs, Duty cycle =10%

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	8		12.75	GHz
Gain	Linear Gain		23.5		dB
Pout	Output Power		5.5		W
PAE	Associated Power Added Efficiency		36		%

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Electrical Characteristics (Pulsed mode)

Tamb.= +25°C, Vd = +25V, Idq = 200mA, Pulse width=25µs, Duty cycle =10%

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	8		12.75	GHz
Gain	Linear Gain		23.5		dB
Pout	Output Power (Pin=23dBm)		5.5		W
PAE	Associated Power Added Efficiency (Pin=23dBm)		36		%
Id	Associated current (Pin=23dBm)		0.58		A
IRL	Input Return Loss		12		dB
ORL	Output Return Loss		12		dB
Idq	Quiescent Current		0.2		A
Vd	Drain Voltage		25		V
Vg	Gate Voltage		-3.2		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

Electrical Characteristics (CW mode)

Tamb.= +25°C, Vd = +25V, Idq = 200mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	8		12.75	GHz
Gain	Linear Gain		23		dB
Pout	Output Power (Pin=23dBm)		5		W
PAE	Associated Power Added Efficiency (Pin=23dBm)		34		%
Id	Associated current (Pin=23dBm)		0.55		A
IRL	Input Return Loss		12		dB
ORL	Output Return Loss		12		dB
Idq	Quiescent Current		0.2		A
Vd	Drain Voltage		25		V
Vg	Gate Voltage		-3.25		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

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Electrical Characteristics (Pulsed mode)

Tamb.= +25°C, Vd = +30V, Idq = 200mA, Pulse width=25µs, Duty cycle =10%

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	8		12.75	GHz
Gain	Linear Gain		24		dB
Pout	Output Power (Pin=24dBm)		6		W
PAE	Associated Power Added Efficiency (Pin=24dBm)		33		%
Id	Associated current (Pin=24dBm)		0.62		A
IRL	Input Return Loss		12		dB
ORL	Output Return Loss		10		dB
Idq	Quiescent Current		0.2		A
Vd	Drain Voltage		30		V
Vg	Gate Voltage		-3.2		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

Electrical Characteristics (CW mode)

Tamb.= +25°C, Vd = +30V, Idq = 200mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	8		12.75	GHz
Gain	Linear Gain		23.5		dB
Pout	Output Power (Pin=24dBm)		5.5		W
PAE	Associated Power Added Efficiency (Pin=24dBm)		32		%
Id	Associated current (Pin=28dBm)		0.6		A
IRL	Input Return Loss		12		dB
ORL	Output Return Loss		10		dB
Idq	Quiescent Current		0.2		A
Vd	Drain Voltage		30		V
Vg	Gate Voltage		-3.25		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	55V	V
Pin	Maximum peak input power overdrive	30	dBm
Pdiss	Maximum dissipated power	22	W
Tj	Junction temperature	230	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
Vd	Vd1, Vd2	Drain voltage	25	V
Vg	Vg1, Vg2	Gate voltage HPA on (pulsed mode) HPA on (CW mode) HPA off	 -3.2 -3.25 -8 to -5	 V V V

Biasing up Procedure

1. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5V)
2. Apply Vds bias voltage (Typically: Vd = 25V)
3. Increase slowly Vgs up to quiescent bias drain current Idq (pulsed applied on the gate)
4. Apply RF signal

Biasing down Procedure

1. Turn off RF signal
2. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5V)
3. Turn Vds bias voltage to 0V
4. Turn Vgs bias voltage to 0V

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Typical on-wafer Sij parameters (Pulsed mode)

Tamb.= +25°C, Vd = +25V, Idq = 200mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
0.50	-0.07	-20.18	-24.05	42.54	-75.62	-42.93	-0.35	-28.90
1.00	-0.17	-40.74	-42.38	-108.95	-79.83	-43.28	-0.43	-51.56
1.50	-0.42	-63.11	-51.86	1.49	-79.48	40.14	-0.43	-77.43
2.00	-1.06	-88.11	-60.49	-5.98	-77.66	-61.48	-0.63	-102.01
2.50	-2.54	-115.60	-37.62	-78.15	-72.69	-94.52	-1.04	-126.55
3.00	-5.19	-143.17	-15.69	-146.37	-67.68	-136.01	-1.65	-150.38
3.50	-9.27	-170.37	-11.26	125.13	-65.65	-147.13	-2.49	-174.75
4.00	-15.83	162.91	-10.33	84.91	-67.66	152.10	-3.88	163.16
4.50	-30.59	114.16	-9.47	59.94	-67.05	130.45	-5.45	139.80
5.00	-23.68	-35.15	-8.04	57.69	-64.77	97.89	-7.39	117.28
5.50	-19.92	-56.92	-3.08	57.77	-65.70	56.75	-9.12	96.86
6.00	-21.31	-46.24	4.38	41.76	-64.47	17.40	-9.52	74.35
6.50	-14.07	-20.92	11.49	4.43	-68.40	-100.84	-8.44	42.08
7.00	-9.30	-47.57	16.85	-44.48	-62.62	-172.69	-7.04	1.50
7.50	-8.34	-71.65	20.58	-100.22	-57.19	125.91	-6.88	-42.26
8.00	-8.48	-85.30	21.99	-158.99	-53.81	75.61	-8.84	-73.81
8.50	-8.08	-94.62	21.62	151.94	-52.01	36.61	-10.47	-82.94
9.00	-7.69	-107.00	21.16	112.77	-51.98	2.71	-9.90	-89.50
9.50	-7.79	-121.98	21.37	77.52	-50.47	-24.94	-9.21	-102.33
10.00	-8.79	-139.83	22.28	41.59	-48.95	-54.01	-9.09	-119.74
10.50	-12.21	-164.07	23.58	-0.21	-46.86	-87.13	-10.18	-143.65
11.00	-31.67	167.65	24.42	-50.09	-45.41	-126.51	-14.53	-172.40
11.50	-13.47	-46.90	24.01	-103.19	-45.30	-170.72	-31.01	166.21
12.00	-8.95	-68.98	22.98	-154.65	-45.92	150.68	-23.95	-36.10
12.50	-7.13	-79.25	21.88	149.29	-47.02	107.29	-17.18	-6.99
13.00	-4.59	-88.01	18.86	81.93	-50.83	51.77	-7.97	-19.09
13.50	-3.23	-104.79	12.25	21.89	-59.99	1.89	-4.62	-47.52
14.00	-2.78	-117.88	5.01	-19.29	-71.32	-152.28	-3.41	-66.64
14.50	-2.59	-127.81	-1.93	-50.56	-61.57	124.70	-2.76	-79.78
15.00	-2.40	-136.81	-8.43	-76.69	-59.43	100.22	-2.34	-89.67
15.50	-2.30	-144.52	-14.68	-98.36	-60.59	66.24	-1.80	-98.20
16.00	-2.15	-151.53	-20.90	-118.05	-61.75	57.28	-1.49	-106.05
16.50	-2.03	-158.60	-27.19	-134.89	-61.87	66.30	-1.21	-112.93
17.00	-1.94	-165.06	-33.65	-149.14	-58.44	47.64	-1.00	-119.28
17.50	-1.89	-171.72	-41.24	-156.98	-54.80	17.19	-0.87	-125.07
18.00	-1.86	-177.75	-50.21	-143.90	-53.71	-20.40	-0.73	-130.53
18.50	-1.75	176.07	-52.58	-124.31	-55.60	-56.95	-0.65	-135.46
19.00	-1.73	170.11	-56.25	-97.80	-58.08	-80.40	-0.57	-140.16
19.50	-1.69	164.07	-53.47	-92.48	-56.53	-85.44	-0.52	-144.38
20.00	-1.68	158.21	-51.26	-101.05	-59.00	-90.74	-0.47	-148.79

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Device thermal information

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA6710-99F is manufactured (GaN Power PHEMT 0.25µm).
The temperature Tb_{chip} is defined as the chip back side temperature and $Tb_{carrier}$ is defined as the carrier back side temperature. The thermal resistance (Rth_eq) is given for the full circuit, and assumes CW and pulsed operation mode are given in the table.

Thermal Resistance(1)	Rth_eq	Tb_{chip} =85°C, Vd=25V, Id_drive=0.58A Pin=25dBm Pout=37dBm Pdiss=10W **CW**	5.5	°C/W
Junction Temperature	Tj		140	°C
Median Life	T50		$1x10^8$	Hrs

Thermal Resistance(1)	Rth_eq	Tb_{chip} =85°C, Vd=30V, Id_drive=0.62A Pin=25dBm Pout=37.8dBm Pdiss=13W **CW**	7.5	°C/W
Junction Temperature	Tj		160	°C
Median Life	T50		$3x10^7$	Hrs

Thermal Resistance(2)	Rth_eq	$Tb_{carrier}$ =85°C, Vd=25V, Id_drive=0.58A Pin=25dBm Pout=37dBm Pdiss=10W **CW**	8.2	°C/W
Junction Temperature	Tj		167	°C
Median Life	T50		$2x10^7$	Hrs

Thermal Resistance(2)	Rth_eq	$Tb_{carrier}$ =85°C, Vd=30V, Id_drive=0.62A Pin=25dBm Pout=37.8dBm Pdiss=13W **CW**	8.6	°C/W
Junction Temperature	Tj		195	°C
Median Life	T50		$4x10^6$	Hrs

(1) Thermal resistance measured to back of the chip.
(2) Thermal resistance measured to back of carrier plate (20µm Au/Sn soldering + 1.4mm Cu/Mo/Cu). Thermal analysis is highly recommended, more details are available on request.

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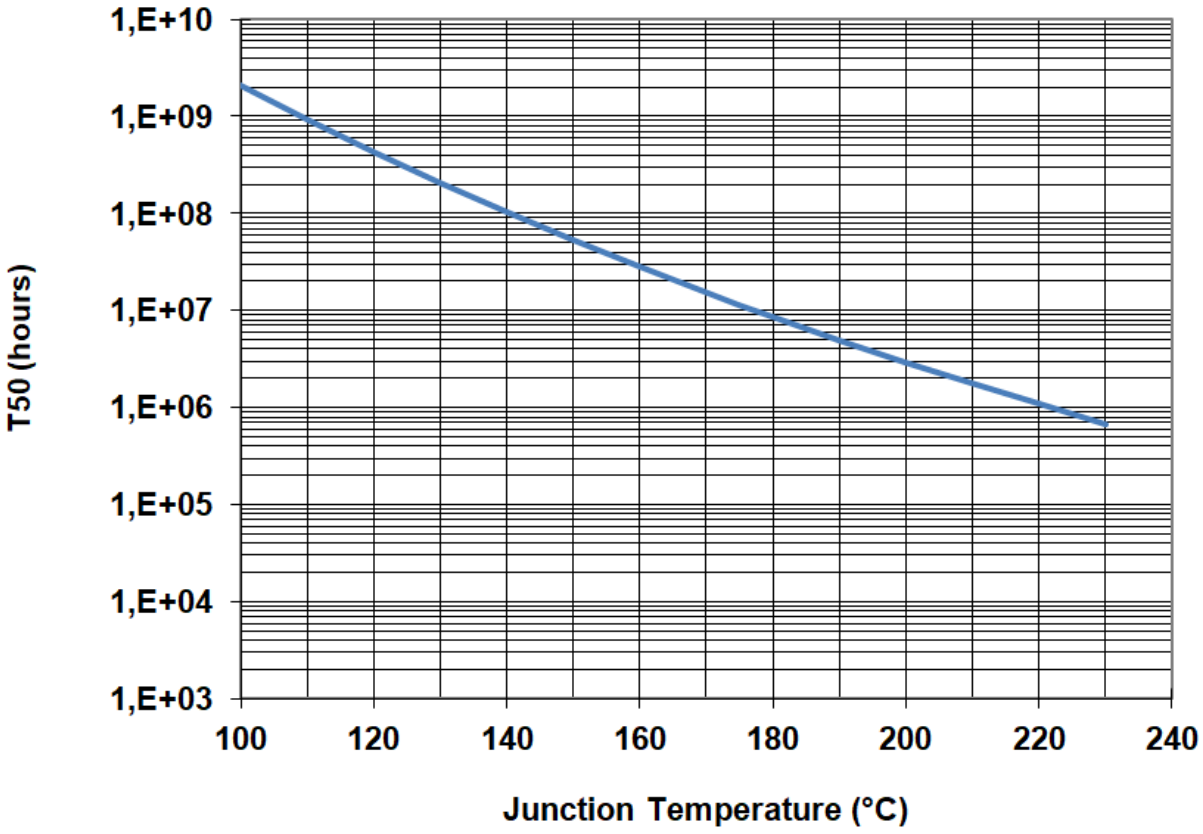
Median Life Time versus Junction Temperature



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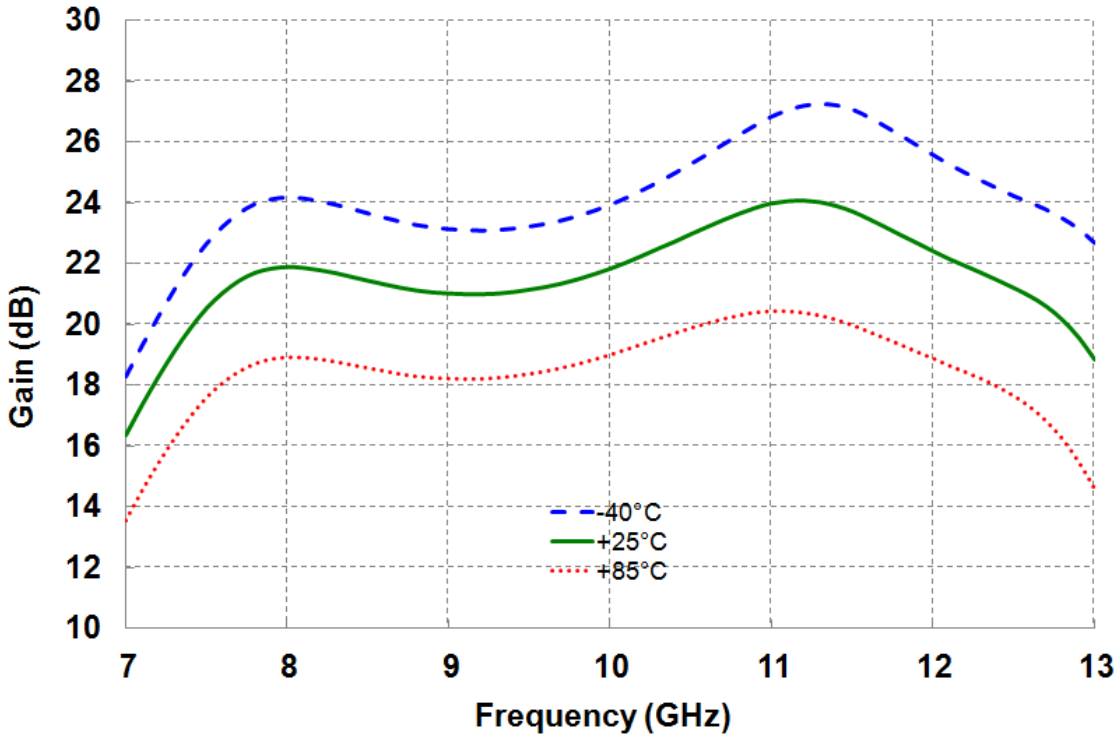
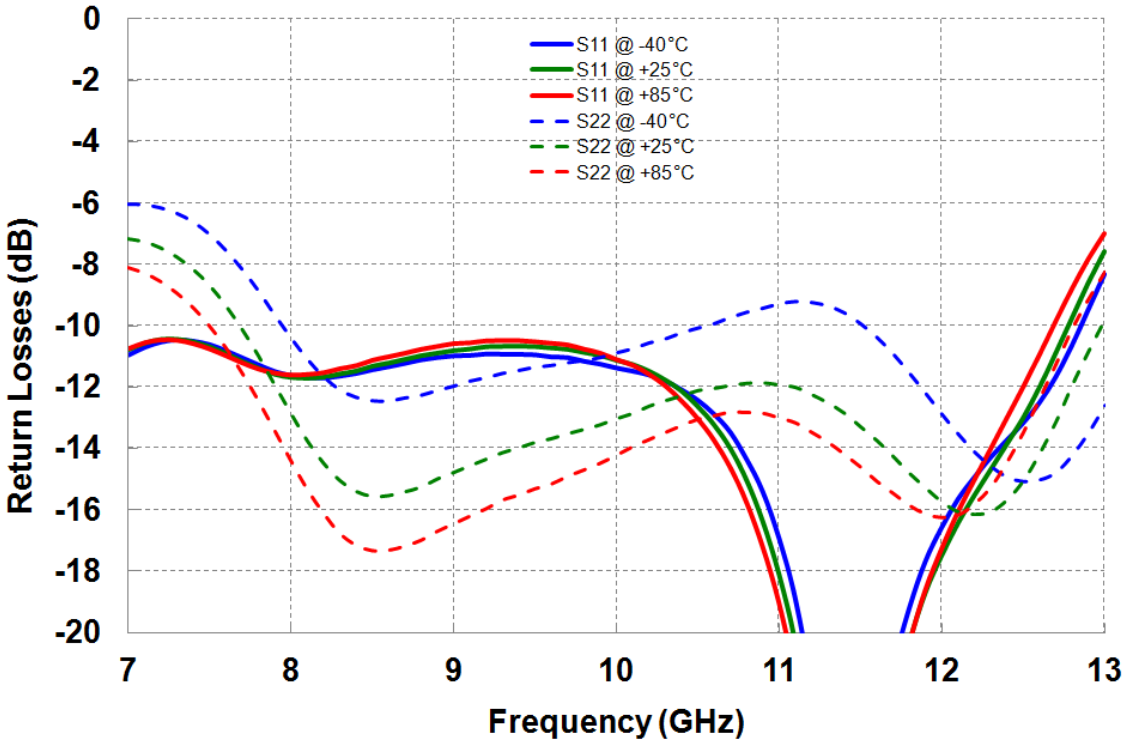
Typical Board Measurements (Pulsed mode)

Tamb.= +25°C, Vd = +25V, Idq = 200mA, Pulse width=25µs, Duty cycle =10%

Linear Gain versus Frequency (Temp.=-40 & +25 & +85 °C)



Return Losses versus Frequency (Temp.=-40 & +25 & +85 °C)



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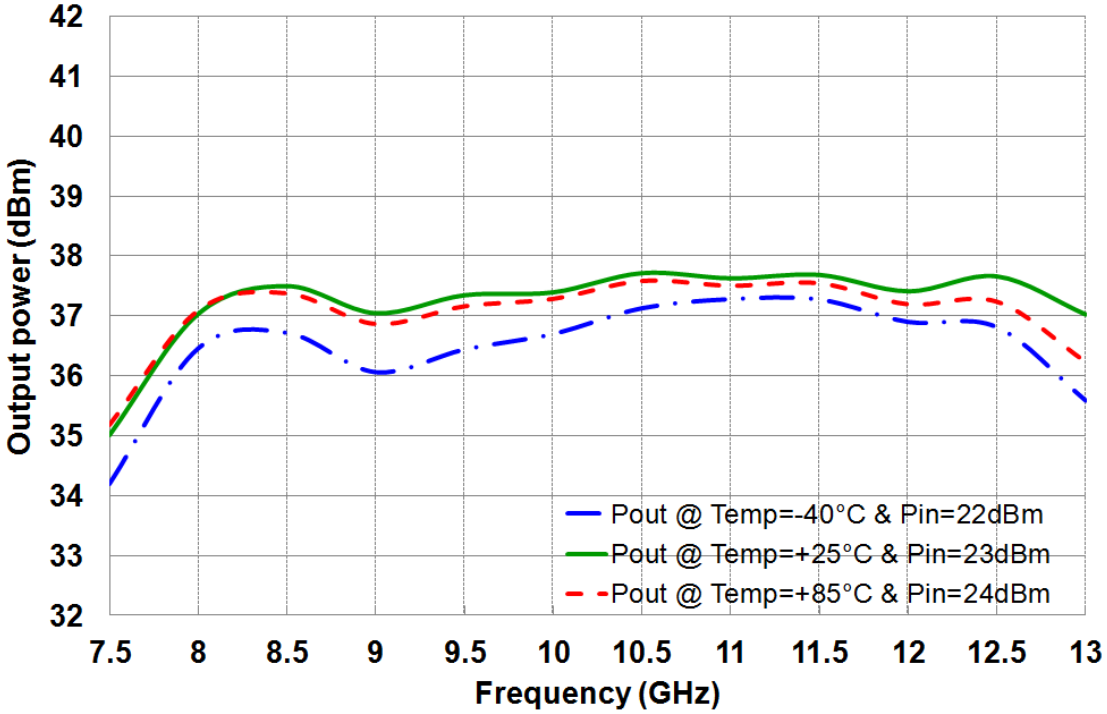
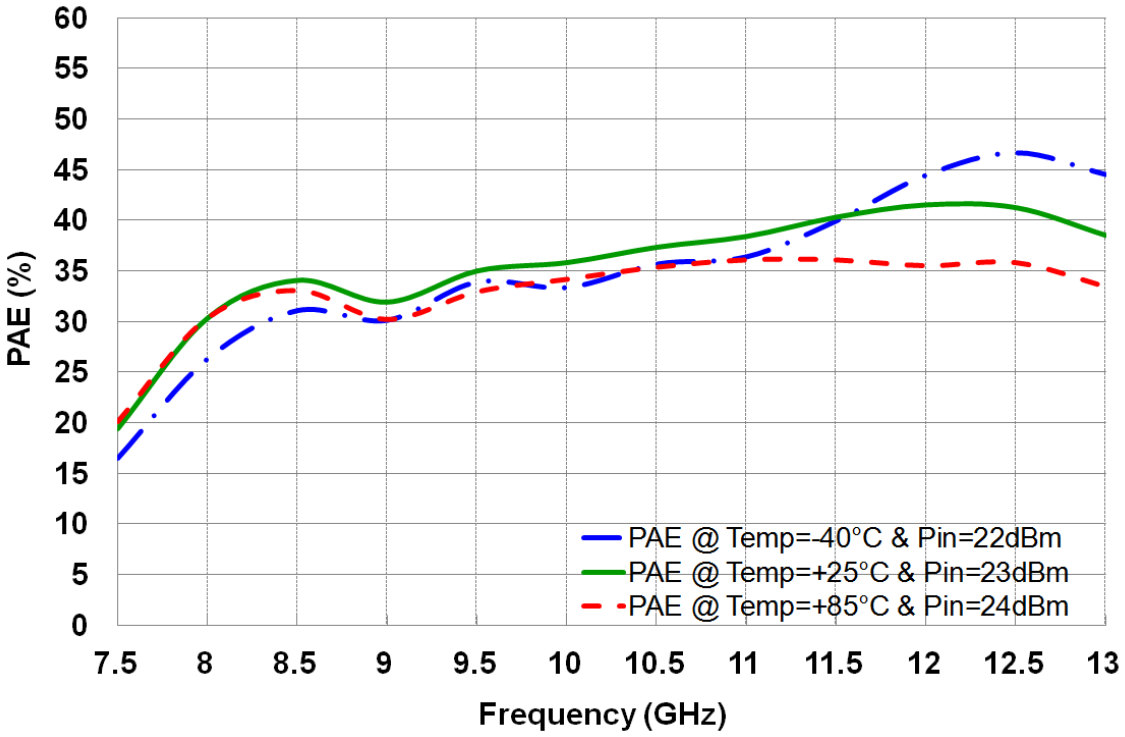
Typical Board Measurements (Pulsed mode)

Tamb.= +25°C, Vd = +25V, Idq = 200mA, Pulse width=25µs, Duty cycle =10%

Output Power versus Frequency (Temp.=-40 & +25 & +85 °C)



Power Added Efficiency versus Frequency (Temp.=-40 & +25 & +85 °C)



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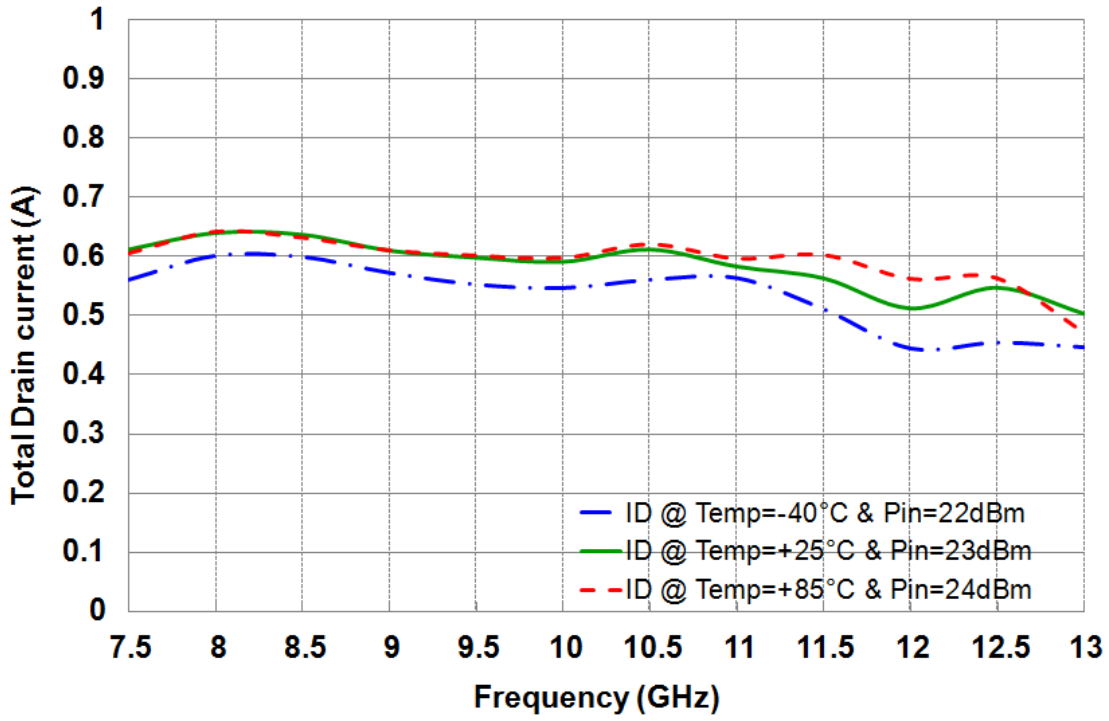
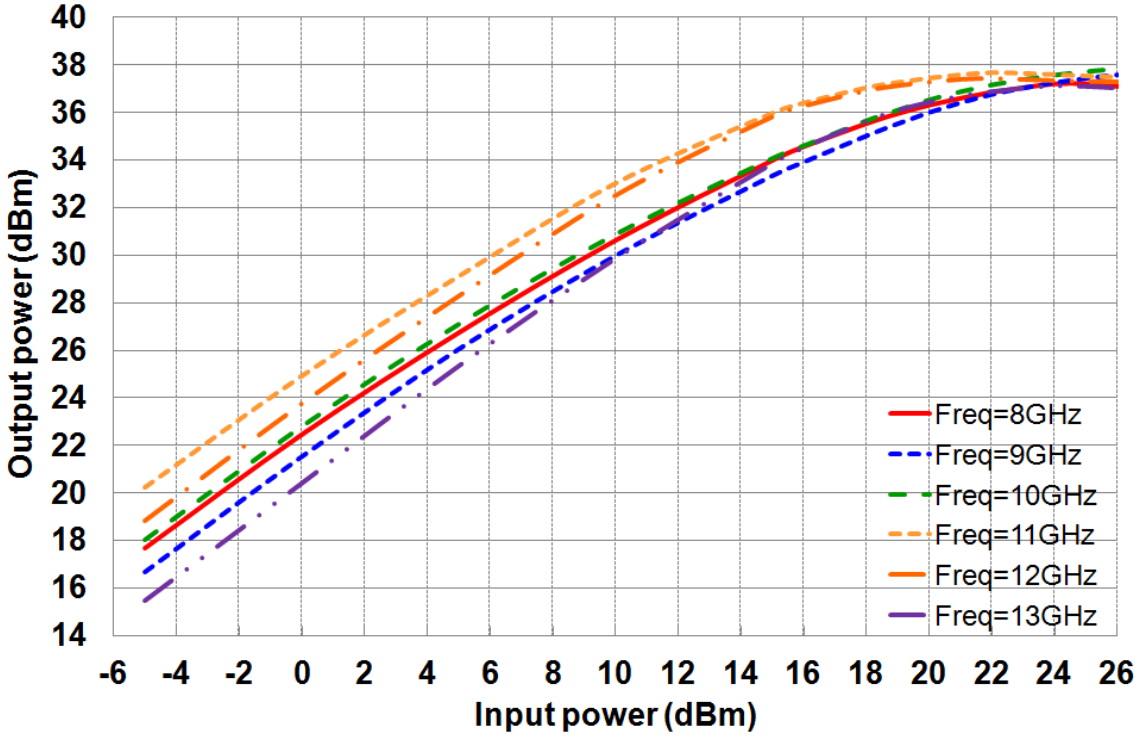
Typical Board Measurements (Pulsed mode)

Tamb.= +25°C, Vd = +25V, Idq = 200mA, Pulse width=25µs, Duty cycle =10%

Drain Current versus Frequency (Temp.=-40 & +25 & +85 °C)



Output Power versus Input Power (Temp=+25°C)



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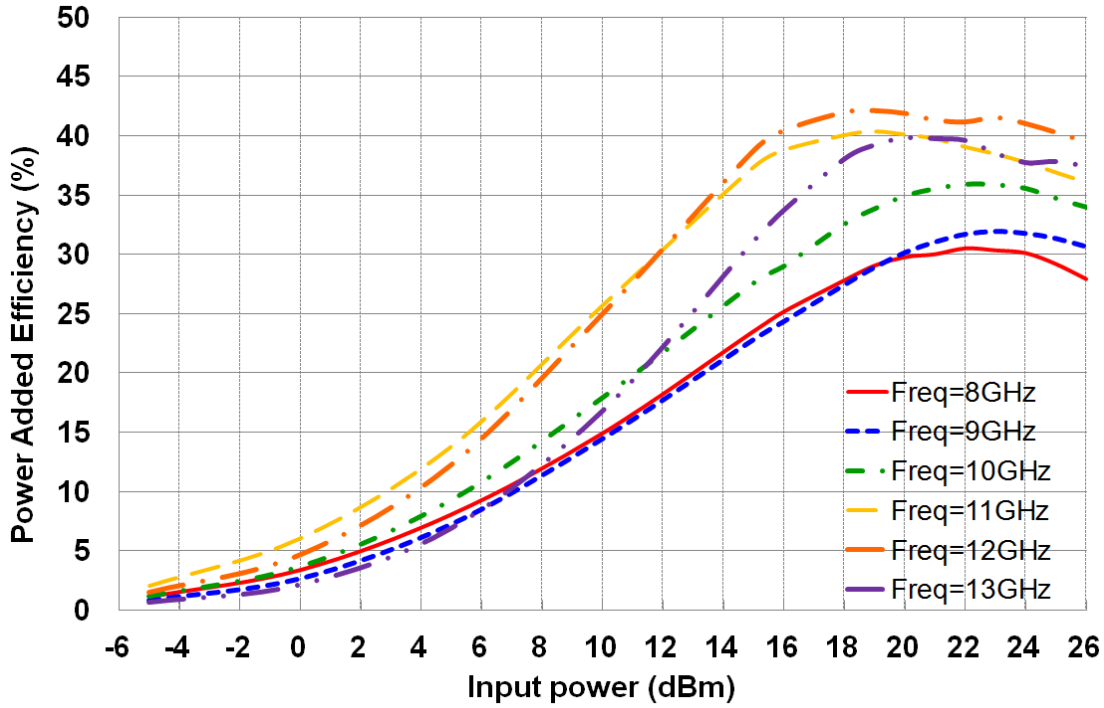
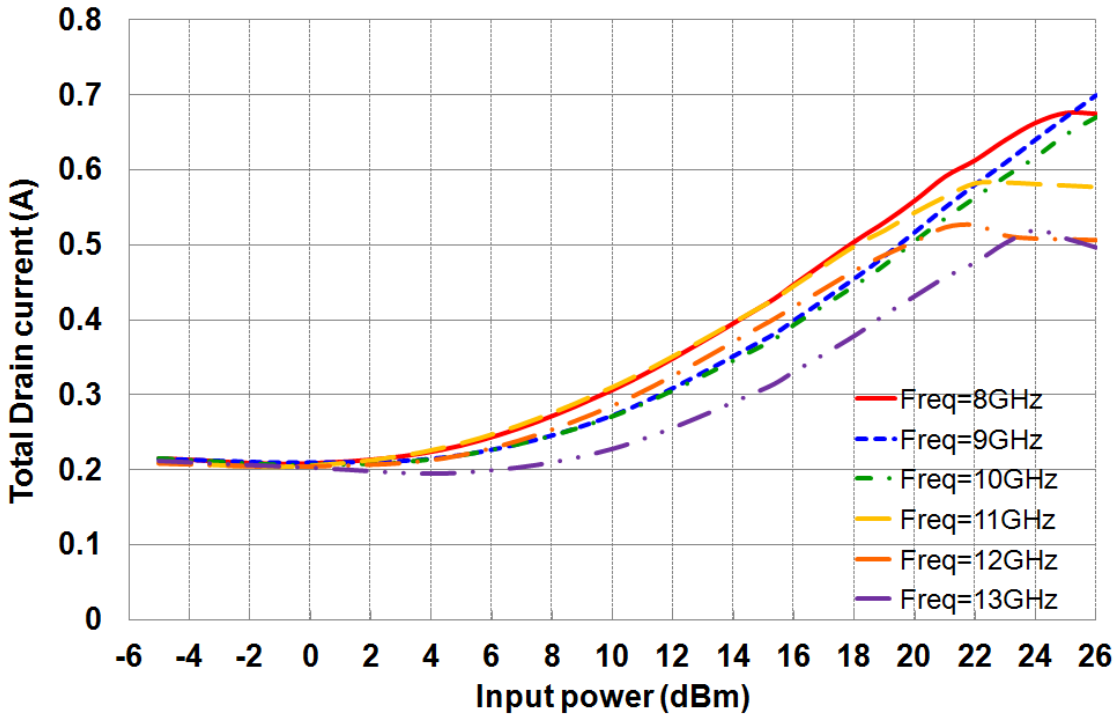
Typical Board Measurements (Pulsed mode)

Tamb.= +25°C, Vd = +25V, Idq = 200mA, Pulse width=25µs, Duty cycle =10%

Power Added Efficiency versus Input Power (Temp=+25°C)



Drain Current versus Input Power (Temp=+25°C)



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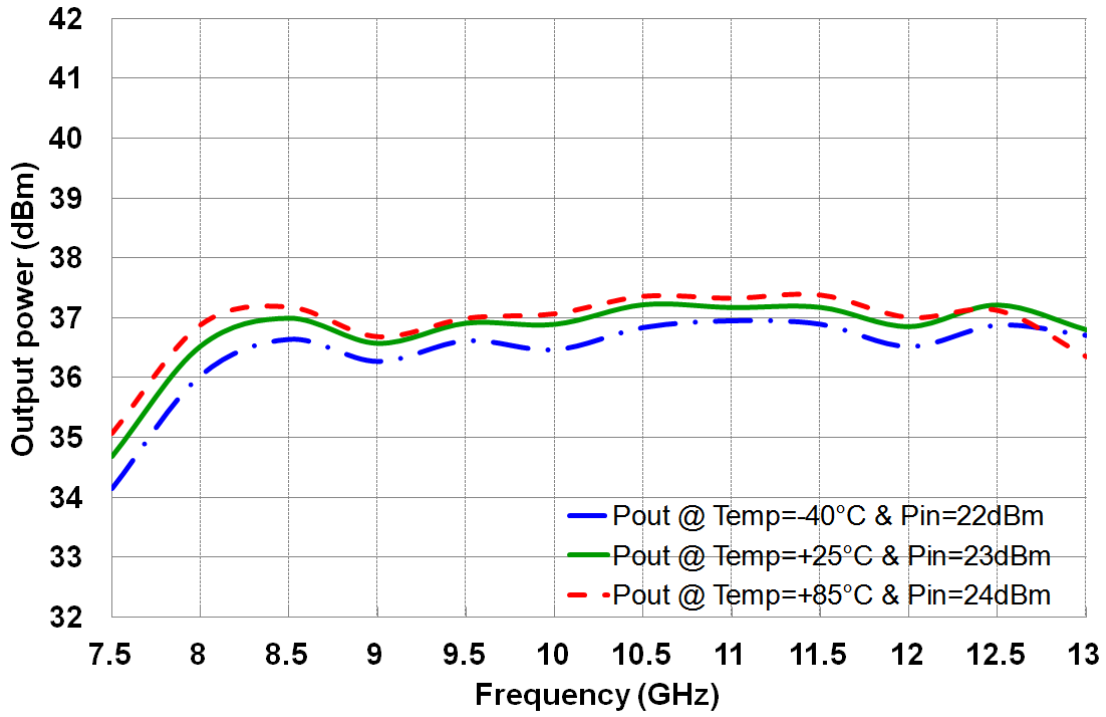
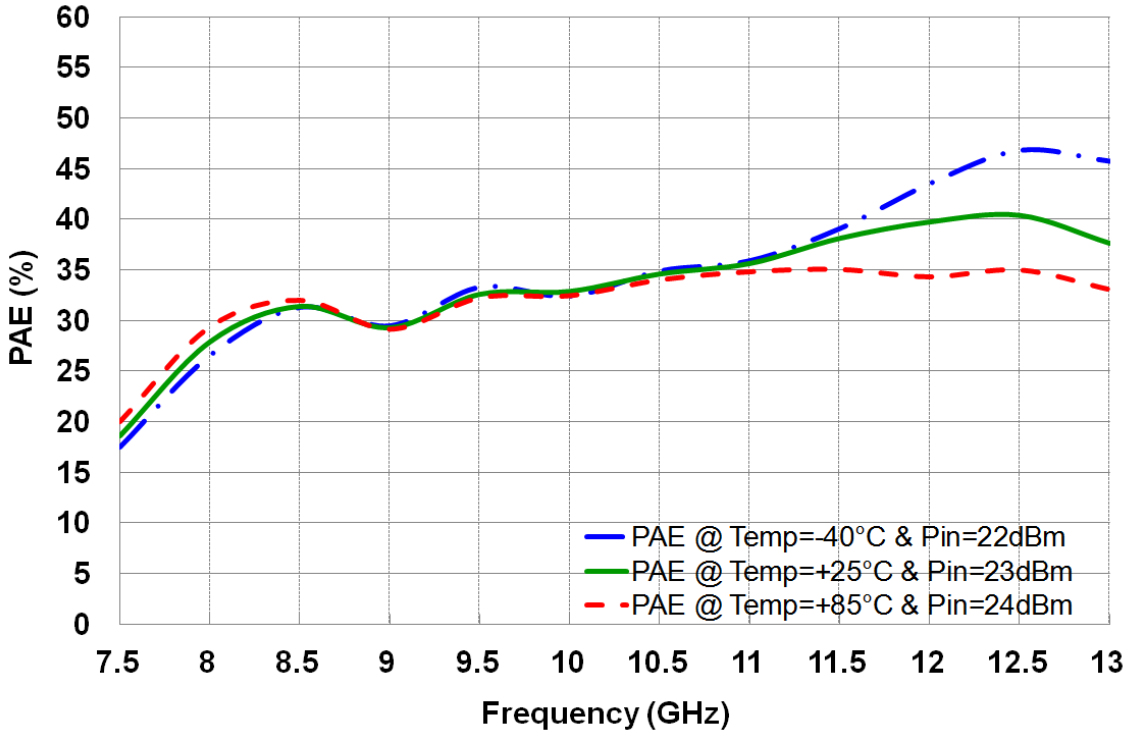
Typical Board Measurements (CW mode)

Tamb.= +25°C, Vd = +25V, Idq = 200mA

Output Power versus Frequency (Temp.=-40 & +25 & +85 °C)



Power Added Efficiency versus Frequency (Temp.=-40 & +25 & +85 °C)



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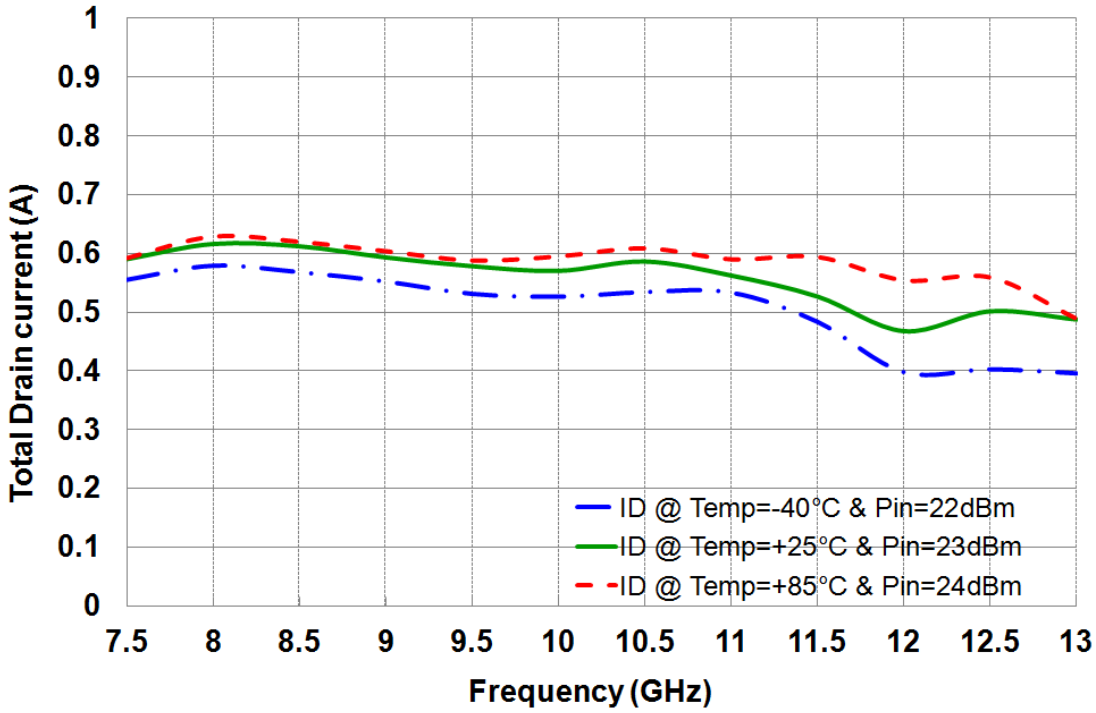
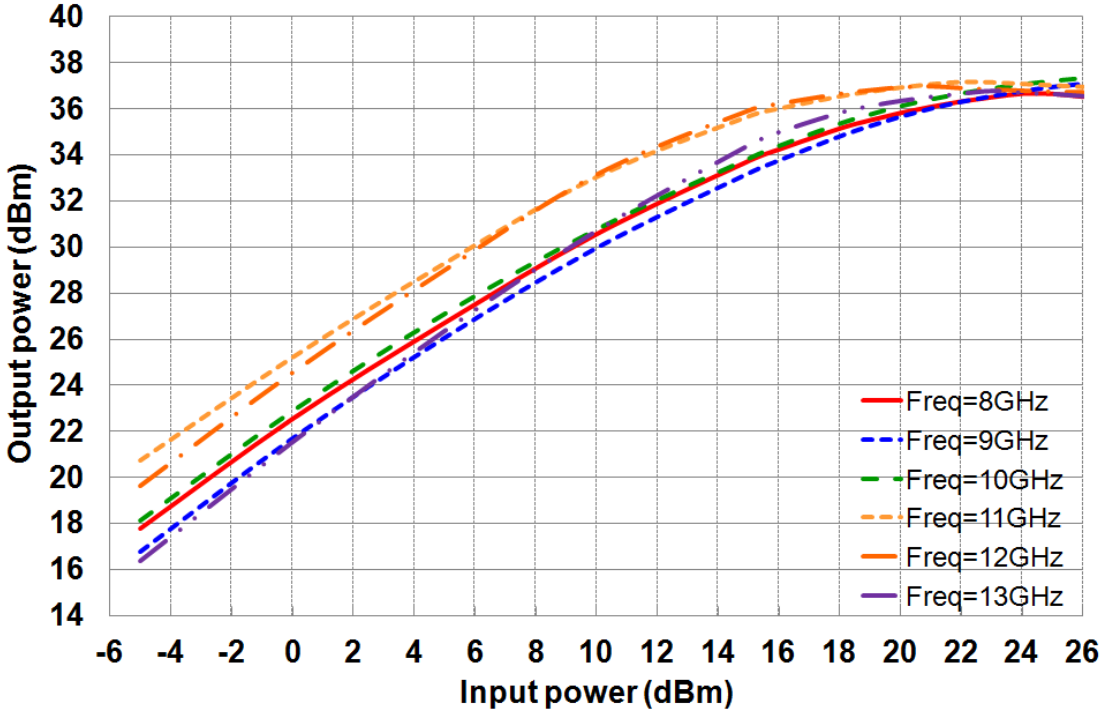
Typical Board Measurements (CW mode)

Tamb.= +25°C, Vd = +25V, Idq = 200mA

Drain Current versus Frequency (Temp.=-40 & +25 & +85 °C)



Output Power versus Input Power (Temp=+25°C)



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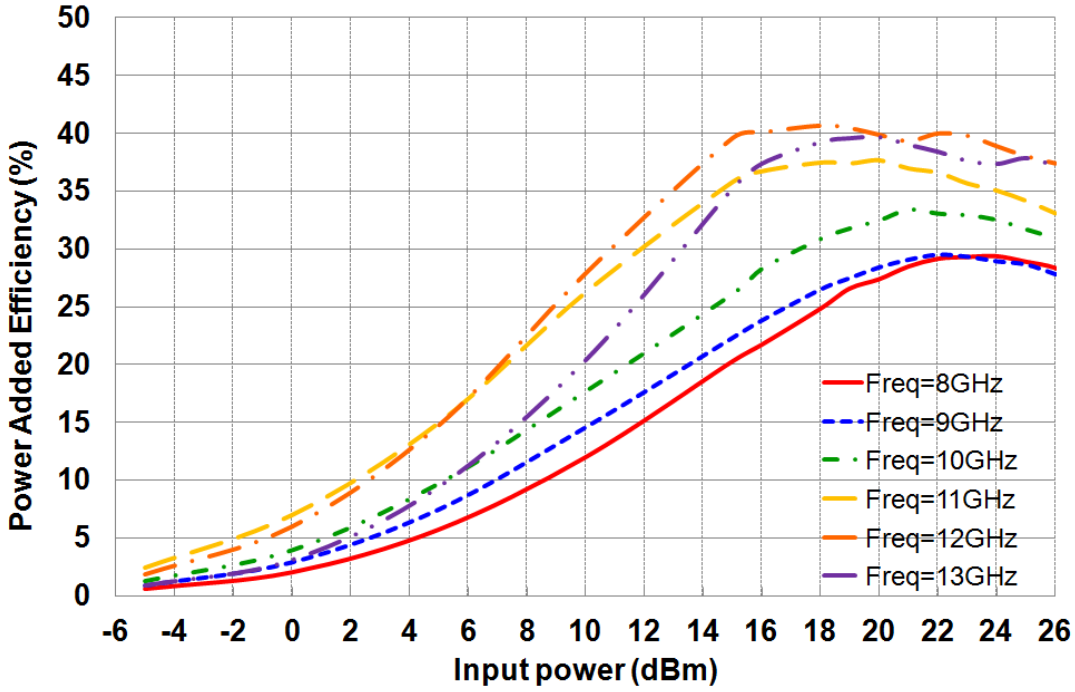
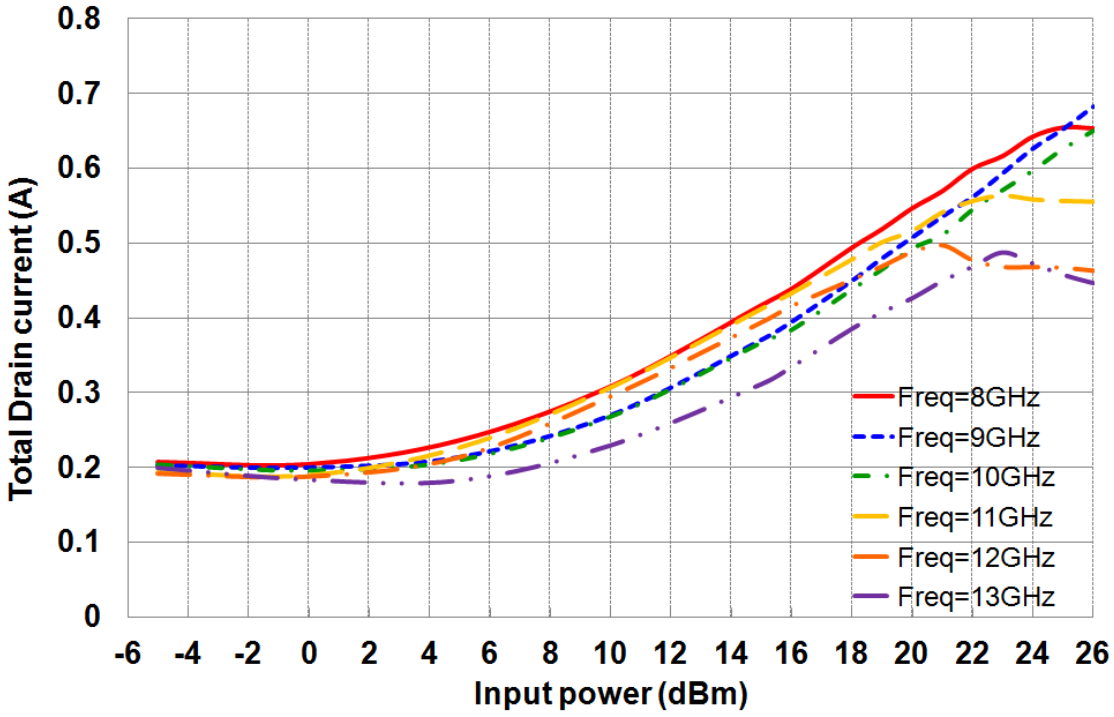
Typical Board Measurements (CW mode)

Tamb.= +25°C, Vd = +25V, Idq = 200mA

Power Added Efficiency versus Input Power (Temp=+25°C)



Drain Current versus Input Power (Temp=+25°C)



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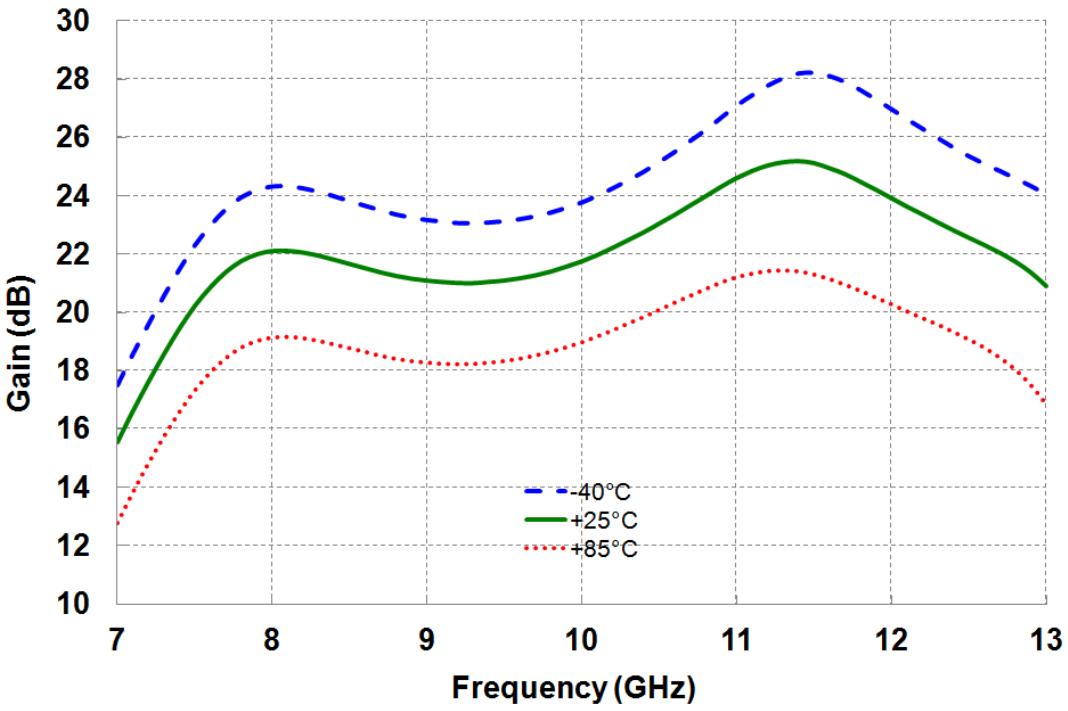
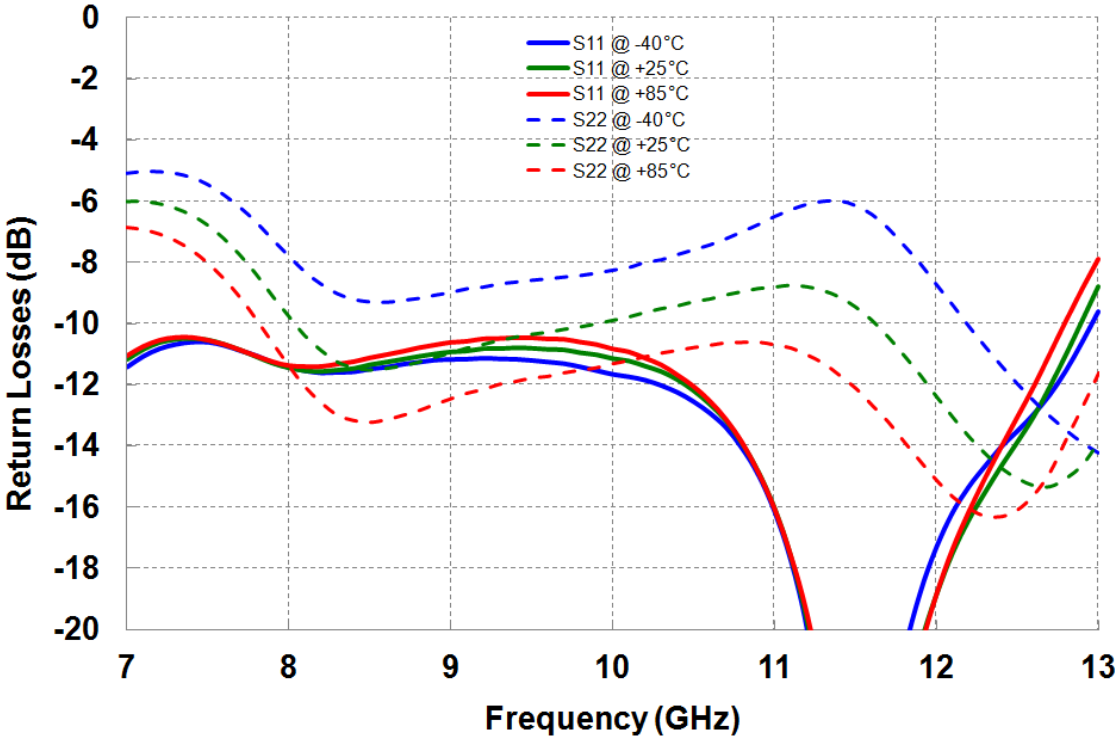
Typical Board Measurements (Pulsed mode)

Tamb.= +25°C, Vd = +30V, Idq = 200mA, Pulse width=25µs, Duty cycle =10%

Linear Gain versus Frequency (Temp.=-40 & +25 & +85 °C)



Return Losses versus Frequency



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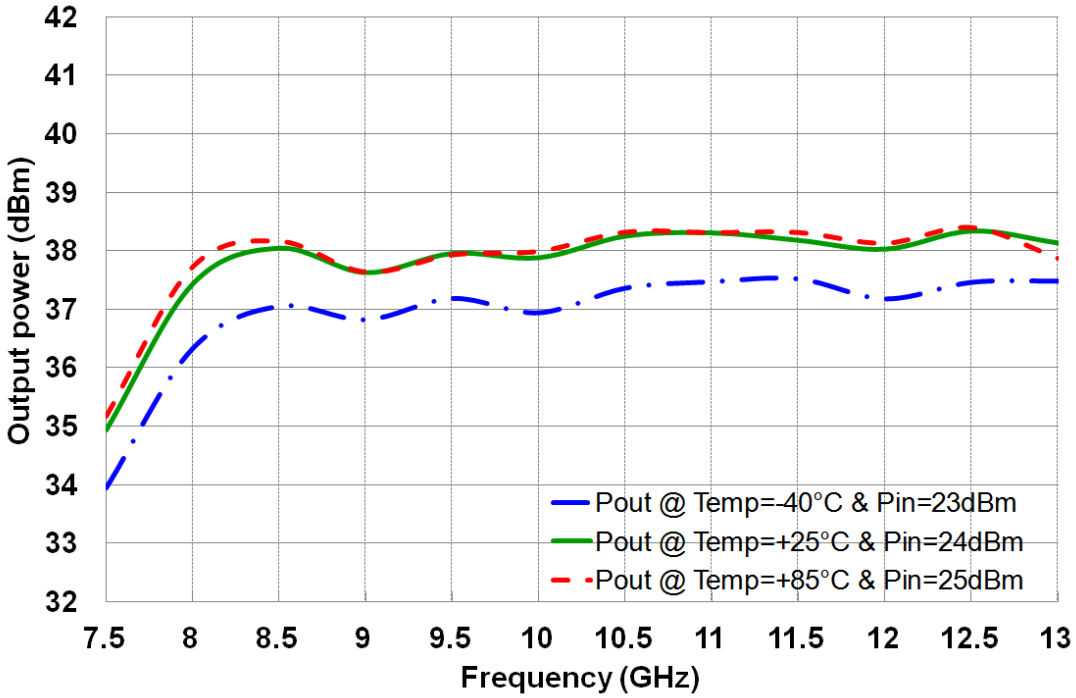
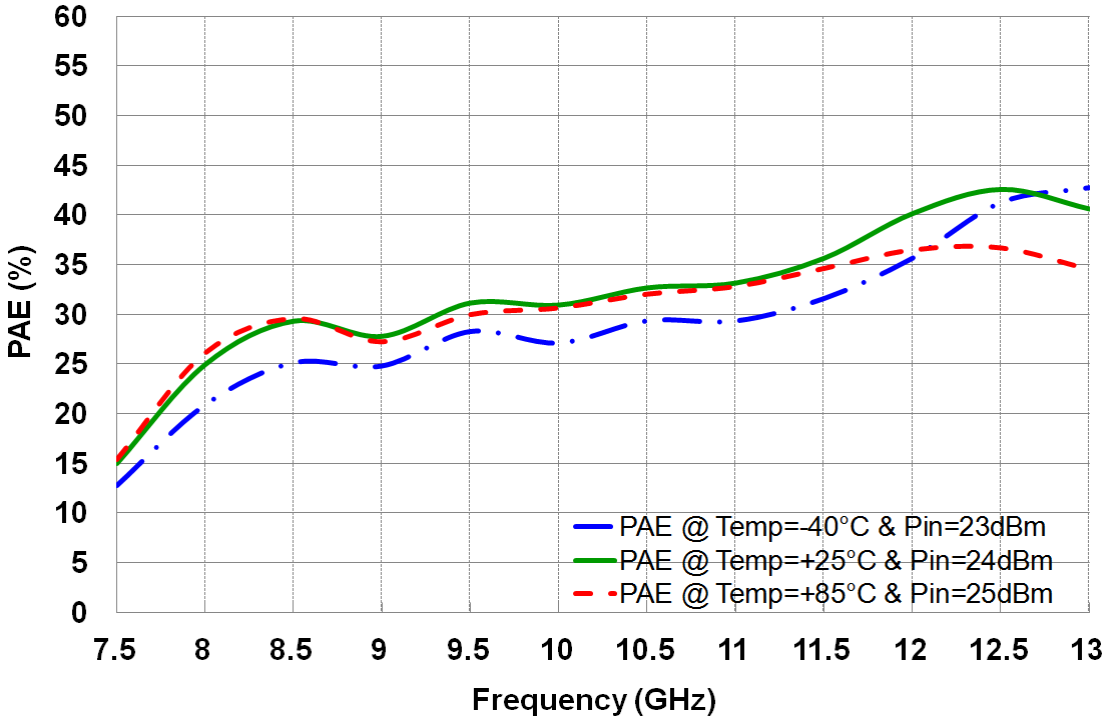
Typical Board Measurements (Pulsed mode)

Tamb.= +25°C, Vd = +30V, Idq = 200mA, Pulse width=25µs, Duty cycle =10%

Output Power versus Frequency (Temp.=-40 & +25 & +85 °C)



Power Added Efficiency versus Frequency (Temp.=-40 & +25 & +85 °C)



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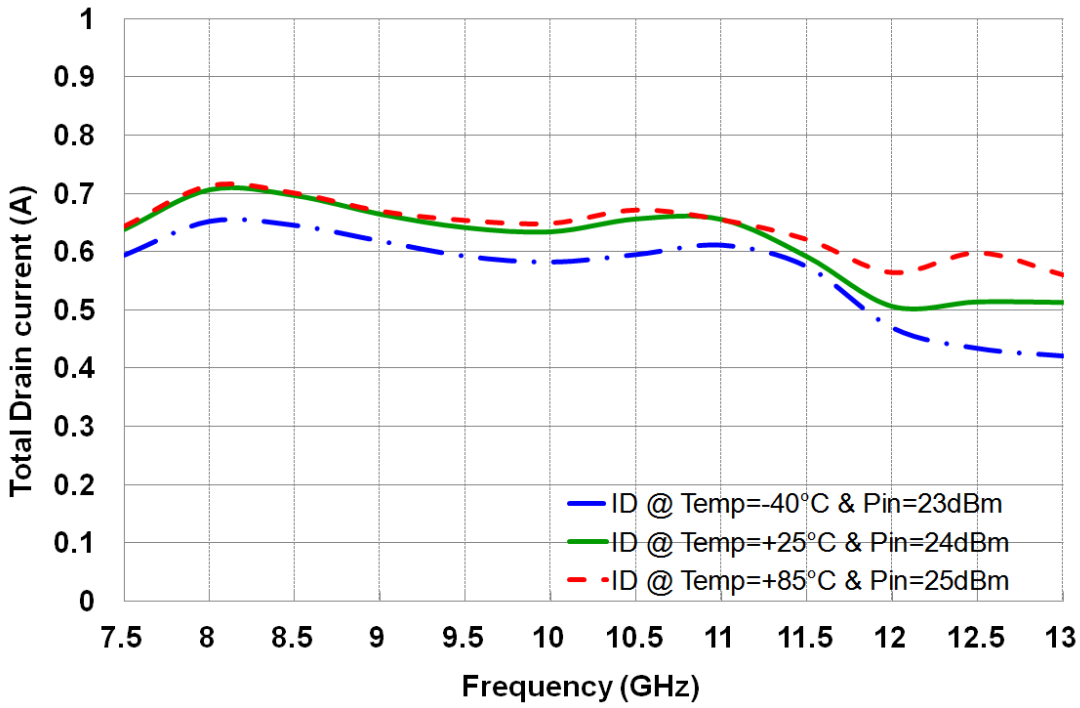
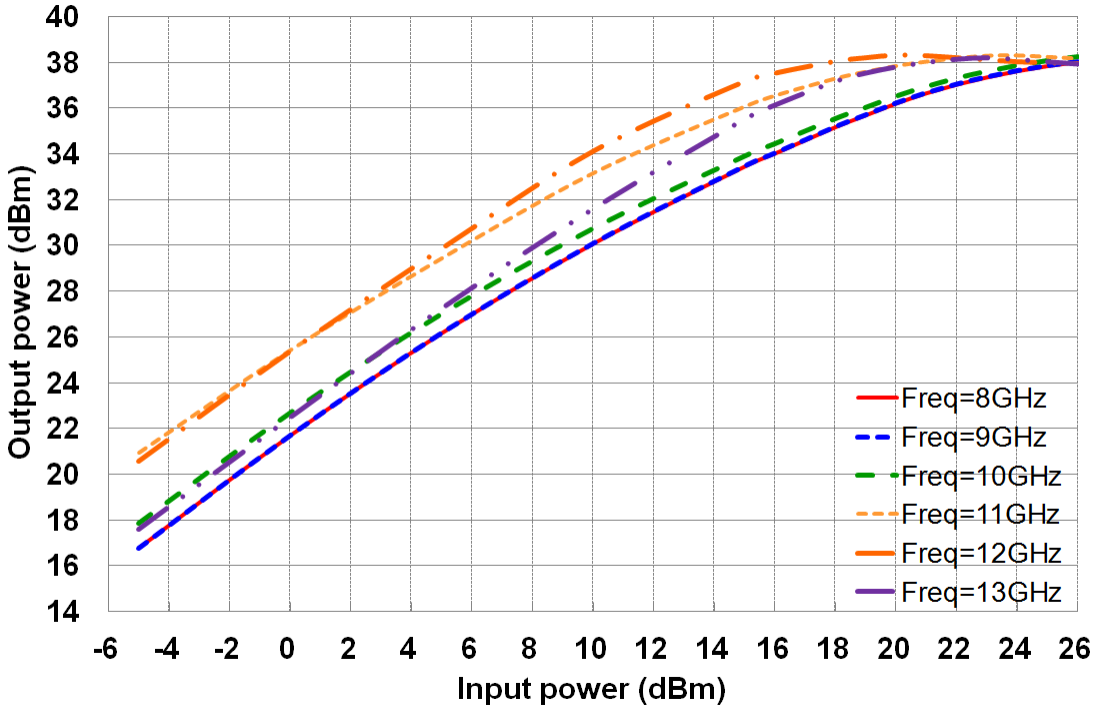
Typical Board Measurements (Pulsed mode)

Tamb.= +25°C, Vd = +30V, Idq = 200mA, Pulse width=25µs, Duty cycle =10%

Drain Current versus Frequency (Temp.=-40 & +25 & +85 °C)



Output Power versus Input Power (Temp=+25°C)



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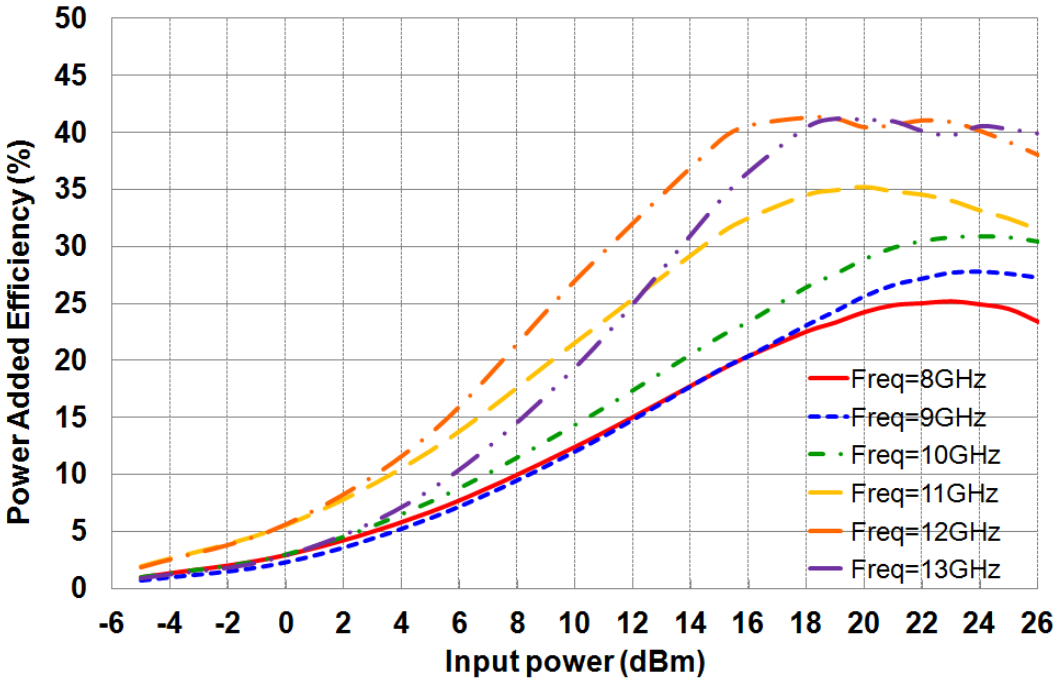
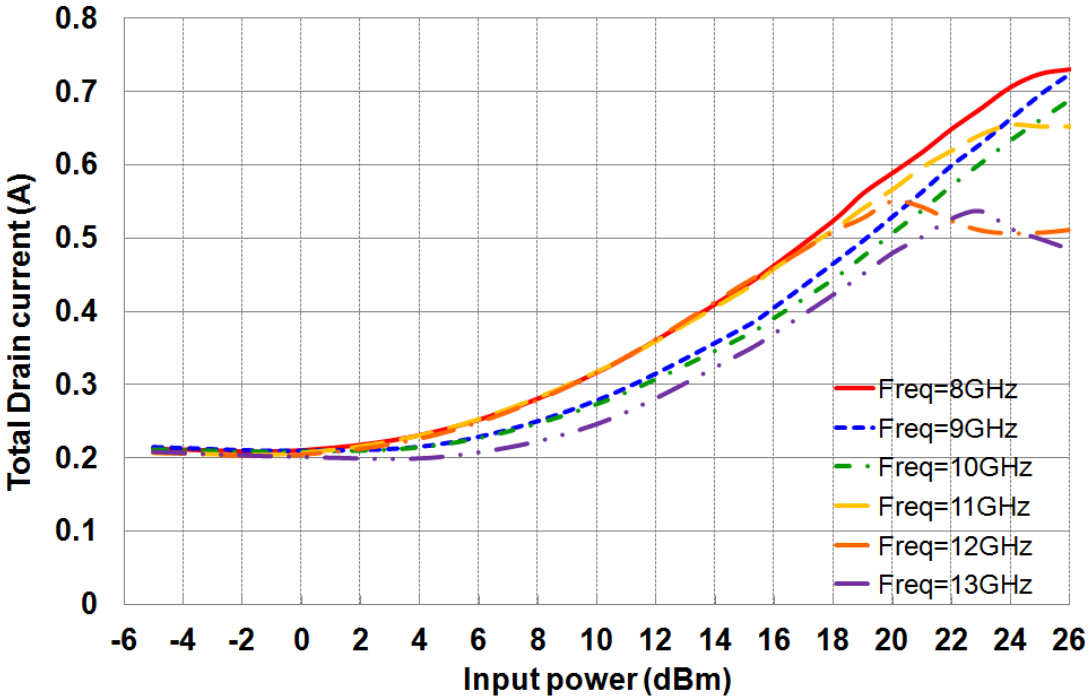
Typical Board Measurements (Pulsed mode)

Tamb.= +25°C, Vd = +30V, Idq = 200mA, Pulse width=25µs, Duty cycle =10%

Power Added Efficiency versus Input Power (Temp=+25°C)



Drain Current versus Input Power (Temp=+25°C)



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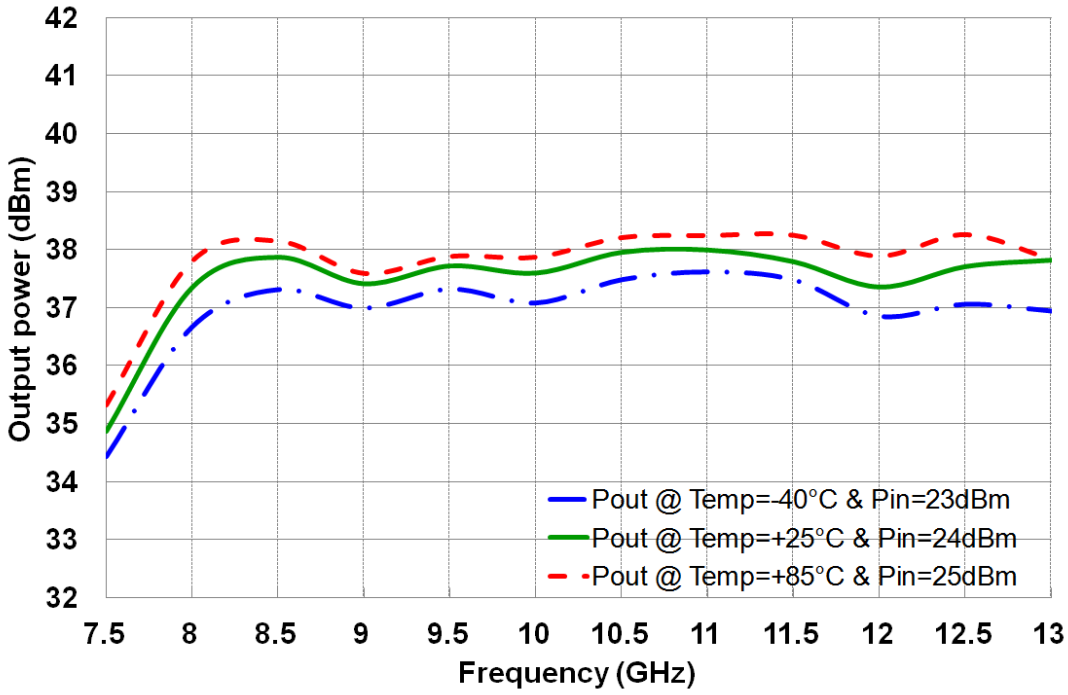
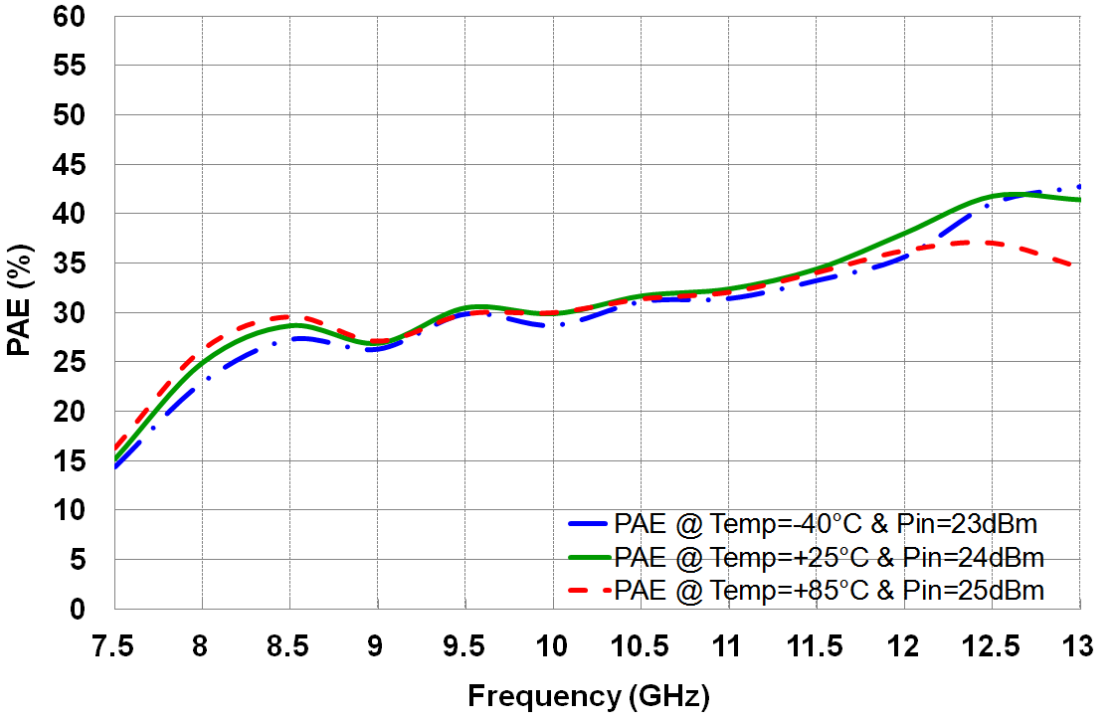
Typical Board Measurements (CW mode)

Tamb.= +25°C, Vd = +30V, Idq = 200mA

Output Power versus Frequency (Temp.=-40 & +25 & +85 °C)



Power Added Efficiency versus Frequency (Temp.=-40 & +25 & +85 °C)



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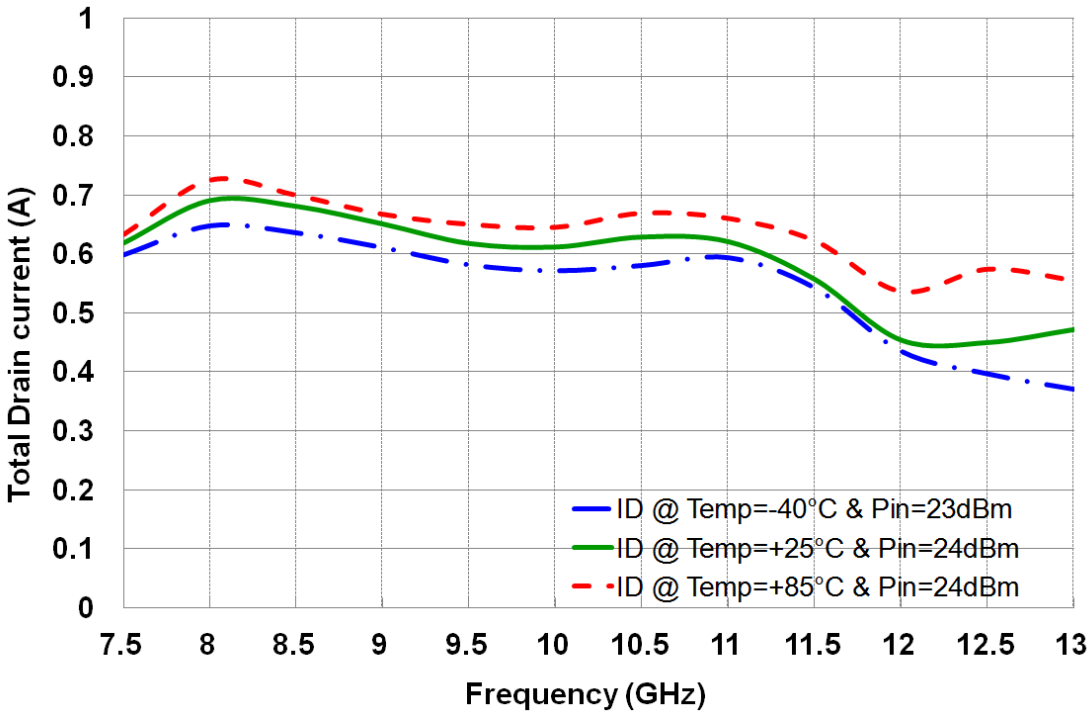
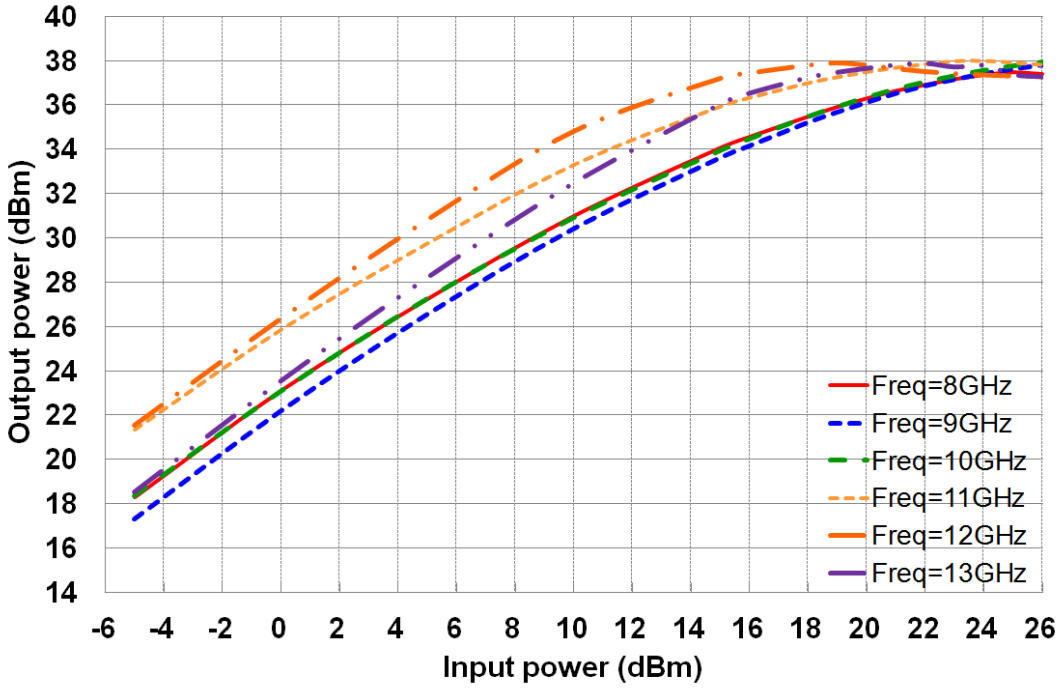
Typical Board Measurements (CW mode)

Tamb.= +25°C, Vd = +30V, Idq = 200mA

Drain Current versus Frequency (Temp.=-40 & +25 & +85 °C)



Output Power versus Input Power (Temp=+25°C)



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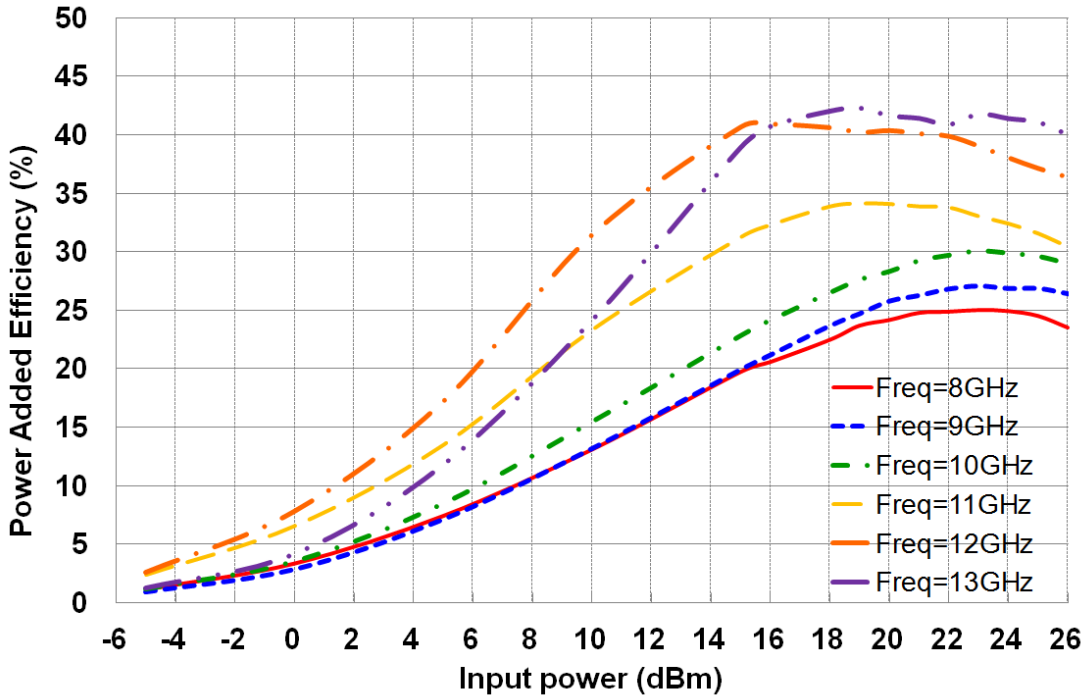
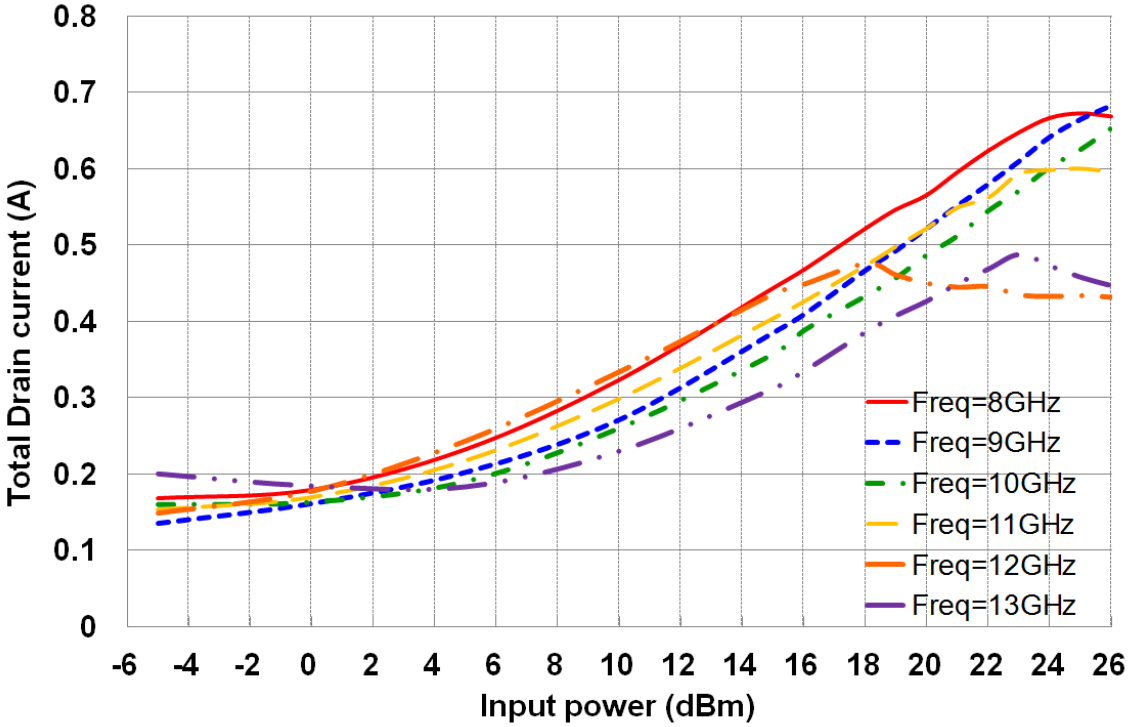
Typical Board Measurements (CW mode)

Tamb.= +25°C, Vd = +30V, Idq = 200mA

Power Added Efficiency versus Input Power (Temp=+25°C)



Drain Current versus Input Power (Temp=+25°C)



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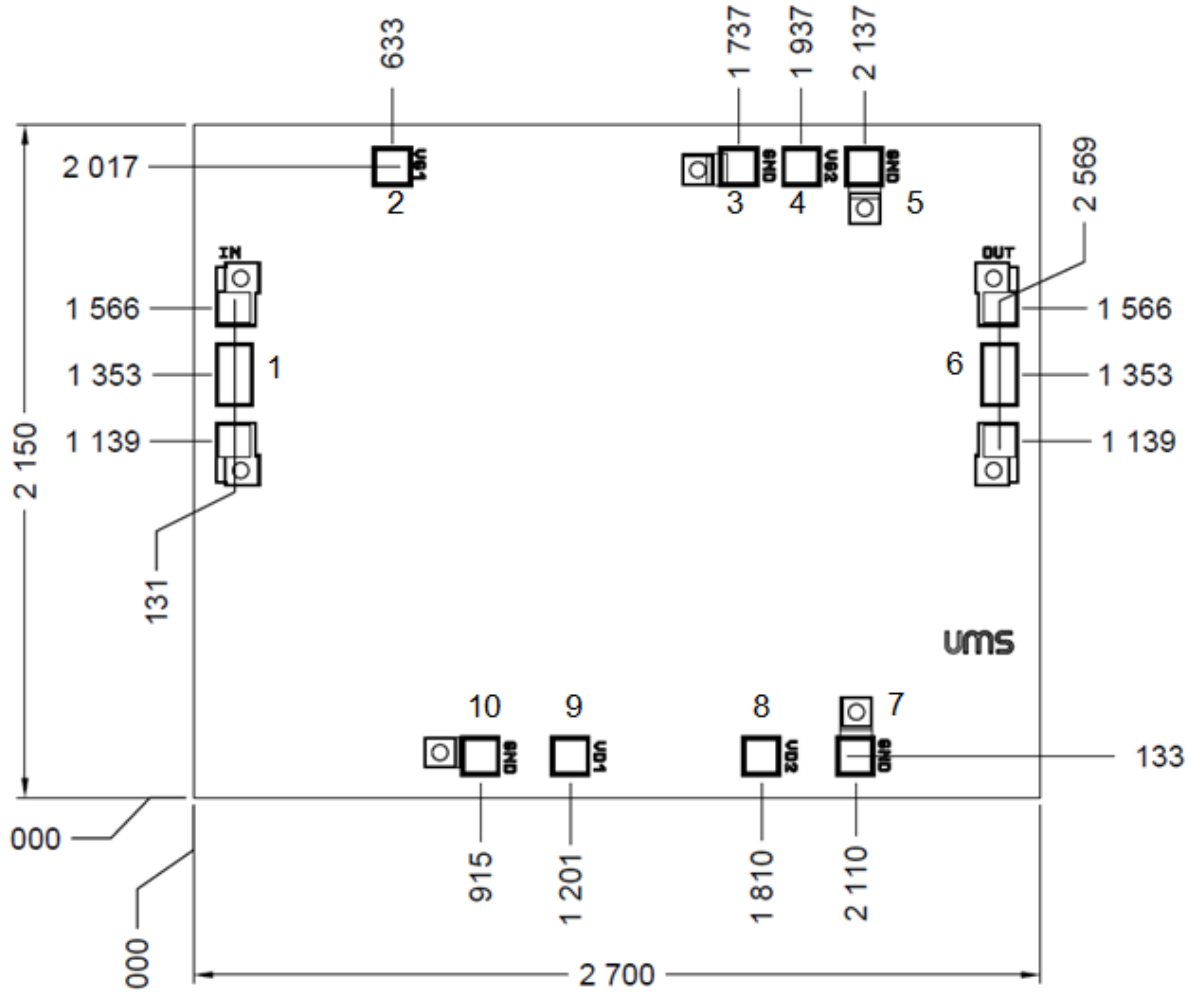
Mechanical data



Chip thickness: 100µm (±50µm).
All dimensions are in micrometers

PAD Number	Name	Description
1	IN	Input RF port
2	VG1	Negative supply voltage (gate of stage 1)
4	VG2	Negative supply voltage (gate of stage 2)
9	VD1	Positive supply voltage (drain of stage 1)
8	VD2	Positive supply voltage (drain of stage 2)
3, 5, 7, 10	GND	Ground (NC)
6	OUT	Output RF port

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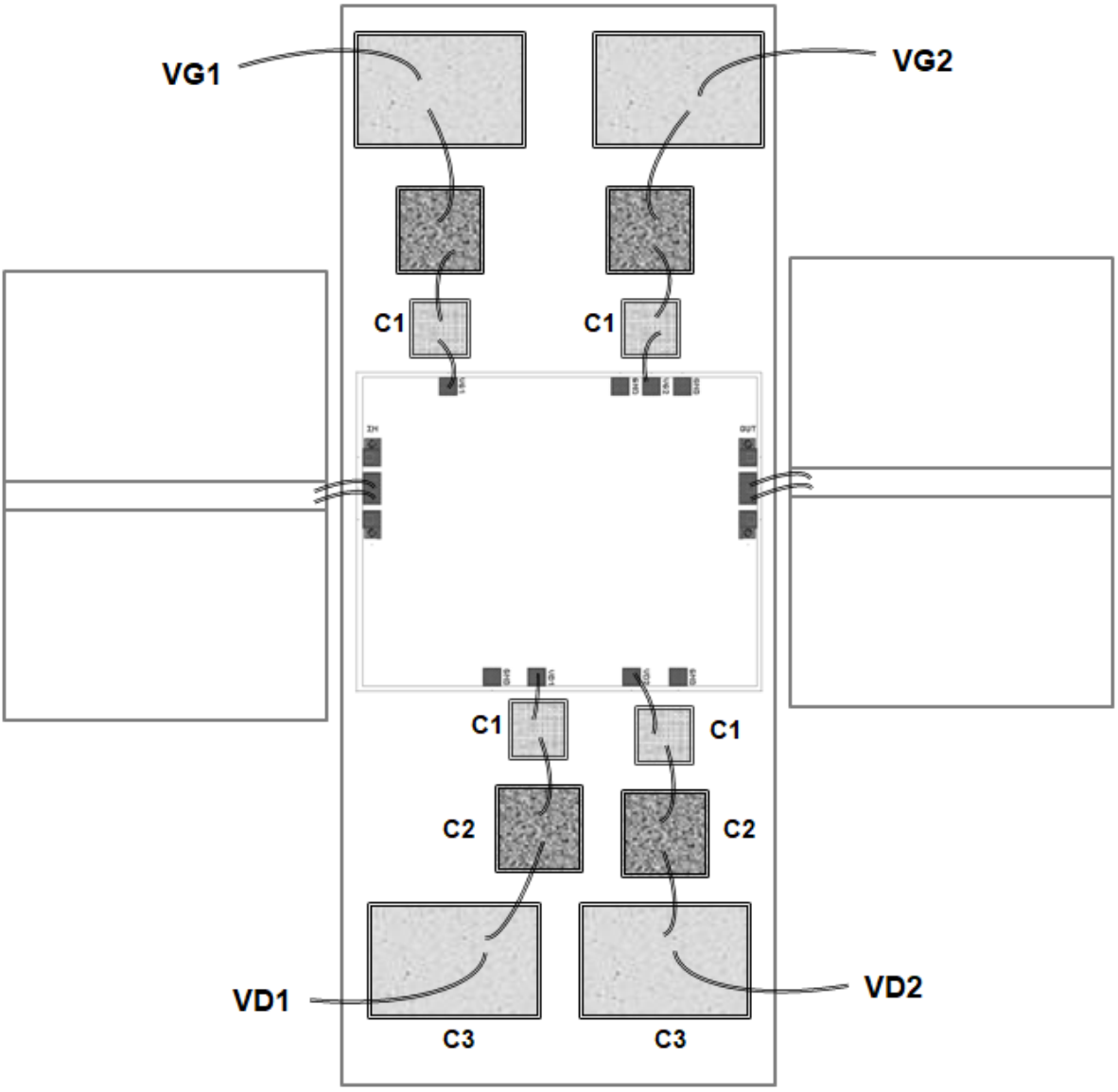
Recommended assembly drawing in CW mode



Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Bill of Materials

Label	Value	Description
C1	RF	Capa 120pF +-10% 50V
C2	RF	Capa 10nF +-20% 50V
C3	RF	Capa 68nF +-20% 50V

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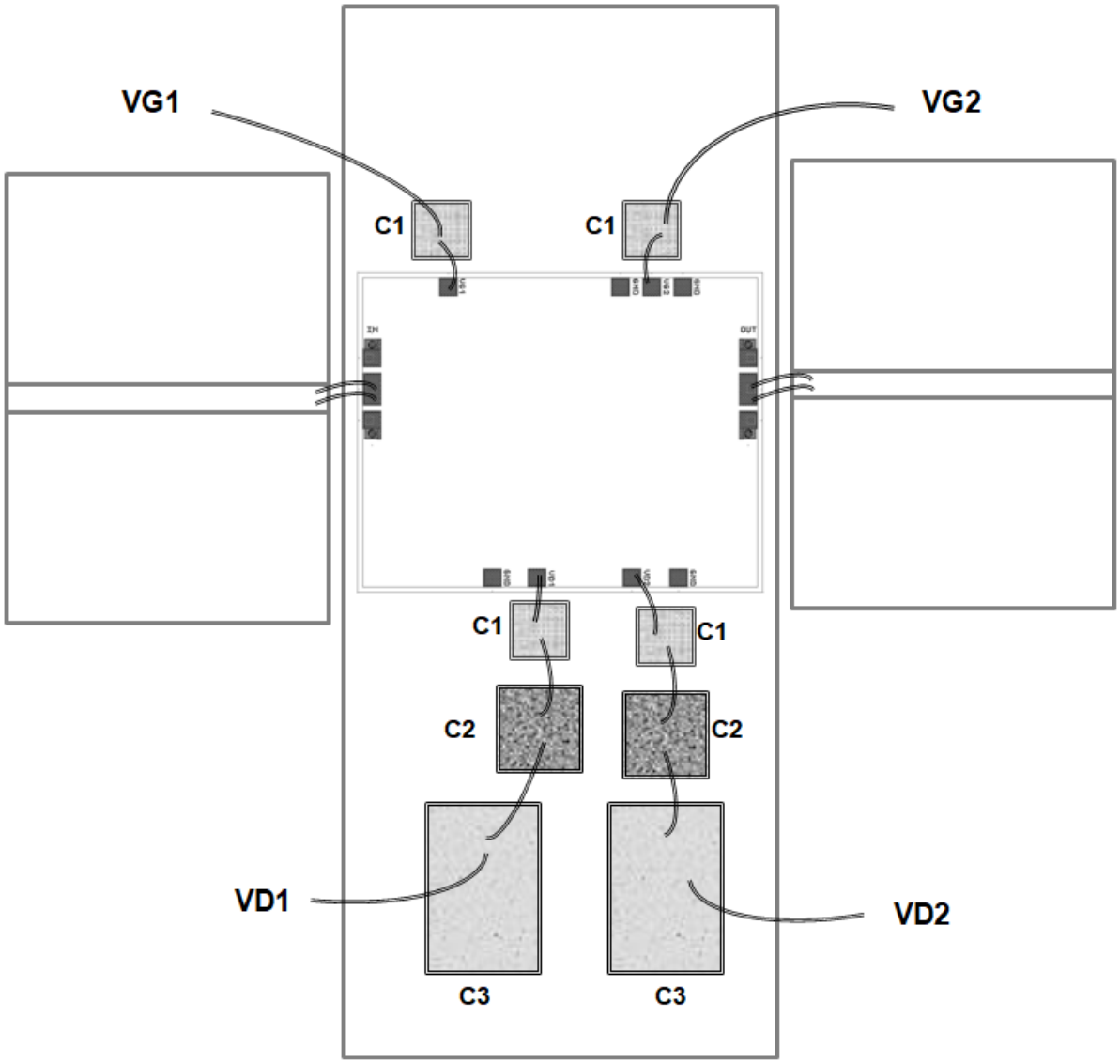
Recommended assembly drawing in gate pulsed mode



Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Bill of Materials

Label	Value	Description
C1	RF	Capa 120pF +-10% 50V
C2	RF	Capa 10nF +-20% 50V
C3	RF	Capa 68nF +-20% 50V

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Recommended circuit bonding table

Label	Type	Decoupling	Comment
RFIN	RF	Not required	Inductance (Lbonding) = 0.3nH 2 gold wires with diameter of 25 µm (500µm)
RFOUT	RF	Not required	Inductance (Lbonding) = 0.3nH 2 gold wires with diameter of 25 µm (500µm)
Vd	DC	120pF & 10nF	Inductance ≤ 1nH (mainly for first decoupling level) ⇒1.2mm length wires with a diameter of 25 µm
Vg	DC	120pF	Inductance ≤ 1nH (mainly for first decoupling level) ⇒1.2mm length wires with a diameter of 25 µm

- The overall biasing network proposed is compliant with a DC pulse applied on the gate; it can be integrated differently depending on module technology and on modulation characteristics (gate or drain pulse, pulse length and Duty Cycle). However, the first decoupling level should always be kept, the second one should be adapted to modulator characteristics and the third one should be kept and optimized on the non-modulated ports.

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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Ordering Information

Chip form:	CHA6710-99F/00

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