CHA7060-QAB

5.6-8.5GHz Power Amplifier

GaN Monolithic Microwave IC in SMD leadless package

Description

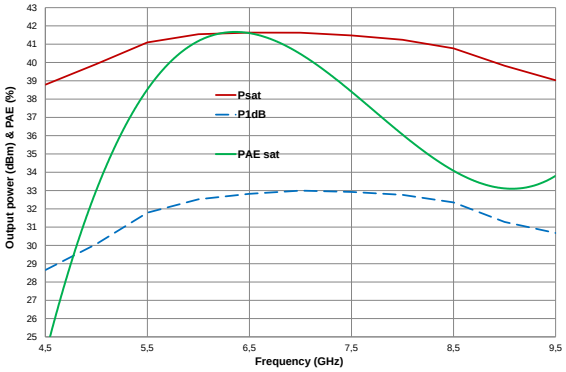
The CHA7060-QAB is a two stages monolithic GaN High Power Amplifier, reaching 12 Watt output power over 6-9GHz bandwidth.
It offers high linearity performance with 30dB of Gain and an EVM of 33dB @34dBm average Pout (56MHz modulation bandwidth, 4QAM).
The circuit is based on GaN technology; 150nm Gallium Nitride on Silicon Carbide (AlGaN/GaN on SiC).
It is a low cost plastic packaged designed for Point To Point Radio applications.
It is supplied in RoHS compliant SMD package.

Main Features

- RF bandwidth: 5.6-8.5GHz
- Gain: 30dB
- Psat: 41dBm (@5dB gain comp)
- EVM: -33dB@34dBm average Pout (1)
- PAE : 40% @41dBm average Pout
- Low AM/AM & AM/PM
- DC bias: Vd = 20.0Volt @ Idq = 420mA
- 38 leads QFN 6x6mm // MSL3

(1) *56MHz modulation bandwidth, 4QAM*

Output power & PAE vs frequency



Main Electrical Characteristics

Tamb.= +25°C, Vd = +20.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.6		8.5	GHz
Gain	Linear Gain		30		dB
P_{5dB}	Output power at 5dB gain compression		41		dBm
Idq	Total drain current		420		mA

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Electrical Characteristics

Tamb.= +25°C, Vd = +20.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.6		8.5	GHz
Gain	Linear Gain		30		dB
RL_{in}	Input return loss		20		dB
RL_{out}	Output return loss		10		dB
PAE	5dB gain comp. / Pout ≈41dBm		40		%
P_{5dB}	Output power at 5dB gain compression		41		dBm
Vg	DC gate Voltage		-2.9		V
Idq	Total drain current		420		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Electrostatic discharge sensitive device observe handling precautions

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Typical Bias Conditions

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain voltage	20	V
Vg	Gate voltage	-3	V
Id	DC Drain current Max. HPA drain current vs. Pin max.	420 2000	mA
Ig	DC HPA gate current Max. HPA gate current vs. Pin max.	0.03 1	mA

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Vg	Gate bias voltage	-10 , -2	V
Id	Drain current at max. input power	2000	mA
Pin	Maximum input power	+22	dBm
Ta	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range (2) (3)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	20	V
Vg	Gate bias voltage	-2.9	V
Id	Drain current	420 to 720	mA
Pin	Maximum Input power	+20	dBm

(2) Electrical performances are defined for specified test conditions

(3) Electrical performances are not guaranteed over all recommended operation conditions

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Biasing procedure

Device Power Up instructions:

1. Ground the device: I_D=0A
2. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg -5V)
3. Set Vd bias voltage to 0V *(pinch off test)* : I_D=0A
4. Apply Vd bias voltage (Typically: Vd = 20V*)*
5. Increase slowly Vg up to quiescent bias drain current Id=420mA
6. Put the RF input Power

Device Power Down instructions:

1. Remove RF input power
2. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5V)
3. Decrease Vd bias voltage down to 0V
4. Turn Vg bias voltage to 0V

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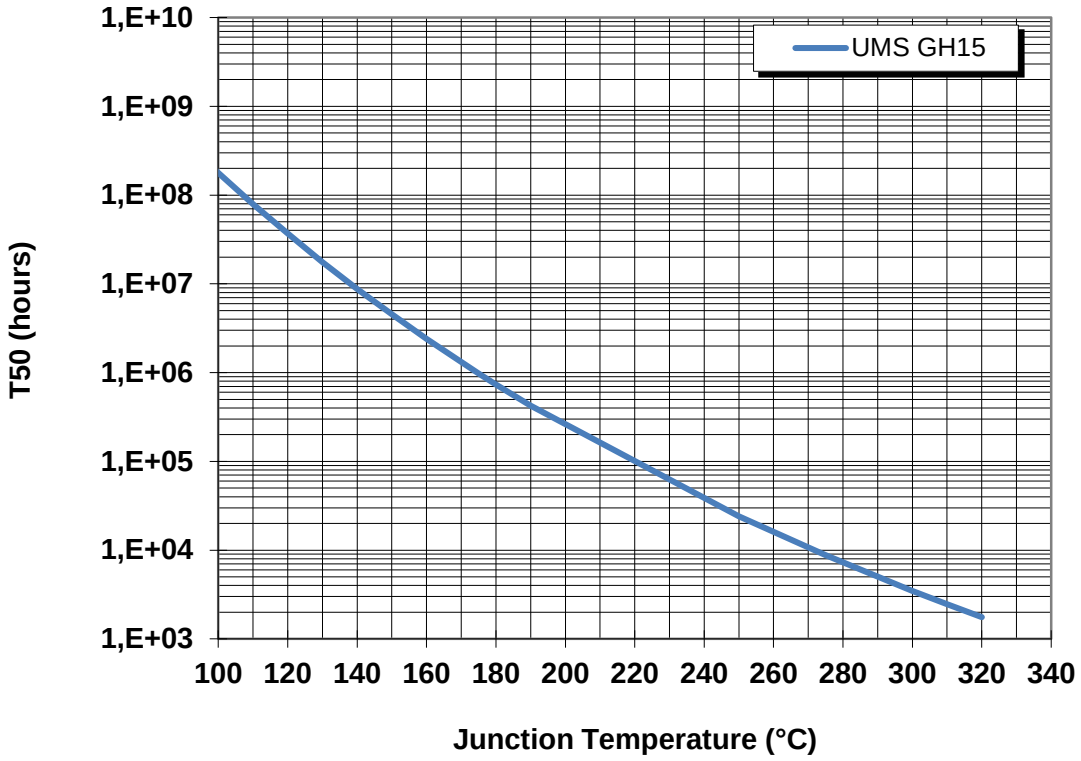
Device thermal performances

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA7060-QAB is manufactured

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} [1] Thermal Resistance (Junction to Case)	Vd= 20V Id= 420mA Pout = 32dBm Pdiss= 12W CW	155	5.8	4.5E+6

[1] Assuming 85°C Tcase



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Typical Package Sij parameters

Tamb.= +25°C, Vd = +20.0V, Id = 420mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
3	-3.7	42.7	-83.7	34.5	-24.9	-75.0	-1.4	-48.2
3.5	-6.7	7.8	-80.8	59.1	-1.4	-94.6	-1.7	-88.4
4	-12.4	-26.6	-75.8	-82.6	17.1	152.3	-3.8	-143.7
4.5	-22.1	-36.6	-61.7	151.3	26.3	20.6	-12.3	107.7
5	-24.8	-23.3	-59.0	67.6	28.6	-97.6	-9.7	-72.2
5.5	-31.6	-93.7	-60.5	3.8	28.9	169.9	-9.3	-141.3
6	-26.9	149.3	-64.6	-55.7	29.0	89.7	-11.8	168.6
6.5	-22.2	97.5	-66.4	-160.5	29.1	15.0	-12.6	115.7
7	-22.9	48.1	-60.5	100.3	29.2	-58.8	-11.2	51.5
7.5	-28.6	-15.0	-56.6	30.8	29.1	-133.7	-9.4	-10.3
8	-31.1	-132.1	-54.4	-31.2	28.3	150.3	-10.1	-65.7
8.5	-29.8	171.9	-53.9	-95.4	26.9	73.7	-16.0	-111.5
9	-31.1	-100.7	-54.8	-163.3	24.9	-4.0	-22.5	-5.4
9.5	-16.1	-119.6	-58.4	118.6	21.9	-85.8	-11.1	-25.1
10	-9.5	-154.6	-64.5	-9.1	16.8	-168.2	-6.6	-50.1
10.5	-5.9	170.6	-59.4	-128.2	9.6	120.7	-3.7	-78.1
11	-4.2	140.4	-54.7	-177.7	2.2	65.3	-2.3	-105.0
11.5	-3.4	116.1	-54.6	135.0	-4.3	18.9	-1.6	-128.2
12	-3.1	97.9	-55.7	116.5	-9.8	-26.8	-1.3	-148.7
12.5	-2.4	84.1	-54.1	90.7	-15.6	-77.6	-1.1	-167.2
13	-1.5	68.4	-55.2	73.5	-22.2	-124.2	-0.9	175.7
13.5	-0.9	51.7	-56.6	66.9	-29.2	-171.5	-0.8	159.6
14	-0.7	36.1	-55.1	56.8	-36.2	148.7	-0.7	144.1
14.5	-0.6	22.0	-55.6	52.0	-41.3	109.2	-0.7	129.5
15	-0.5	9.1	-54.6	38.1	-45.3	64.9	-0.7	115.0
15.5	-0.5	-2.7	-53.1	33.1	-48.1	33.8	-0.7	101.1
16	-0.4	-14.3	-52.1	14.8	-50.0	9.5	-0.7	87.4
16.5	-0.4	-25.5	-51.6	-18.4	-50.9	-20.4	-0.7	73.7
17	-0.4	-36.2	-59.3	-70.5	-58.0	-70.1	-0.7	60.3
17.5	-0.4	-46.2	-63.6	74.4	-62.8	77.4	-0.7	47.2
18	-0.4	-56.2	-59.9	41.0	-59.7	38.3	-0.7	34.2
18.5	-0.3	-66.4	-54.8	37.9	-55.3	39.6	-0.8	21.3
19	-0.4	-76.9	-55.8	36.1	-55.7	33.9	-0.8	8.1

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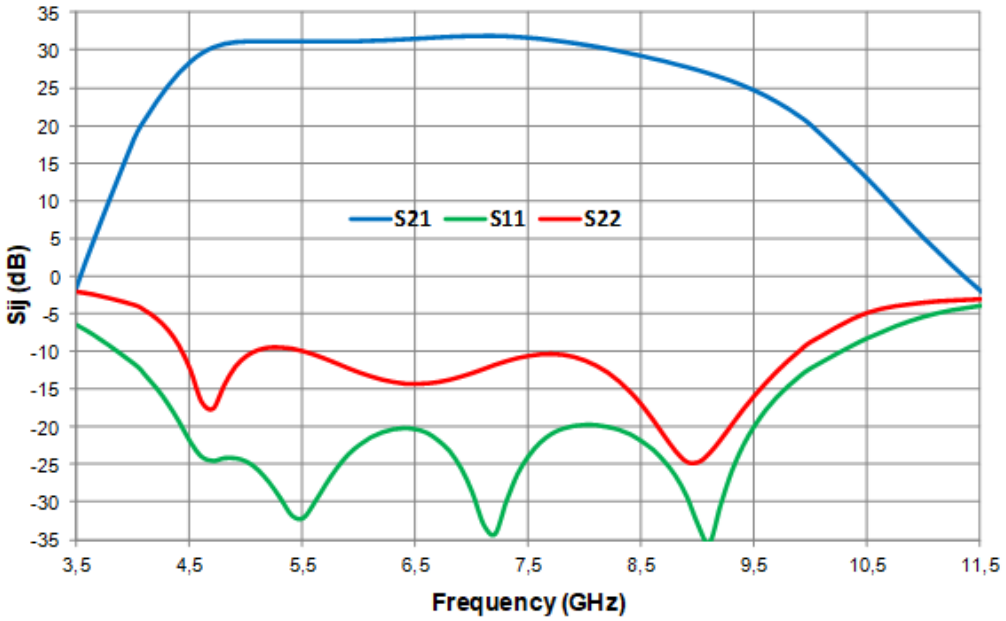
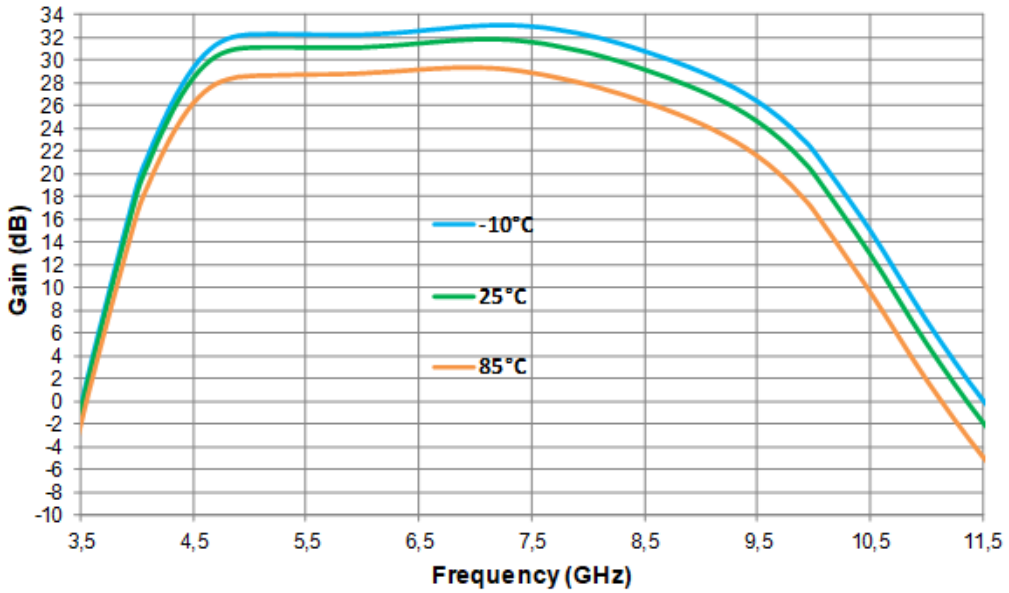
Typical Board Measurements

Tamb.= +25°C, Vd = 20V, Vg set in order to get Id = 420mA
Losses due to board are de-embedded. Measurements are given in the QFN's access planes.

Gain & Return Losses versus Frequency



Gain versus Frequency in Temperature
(Vg fixed for all the temperature)



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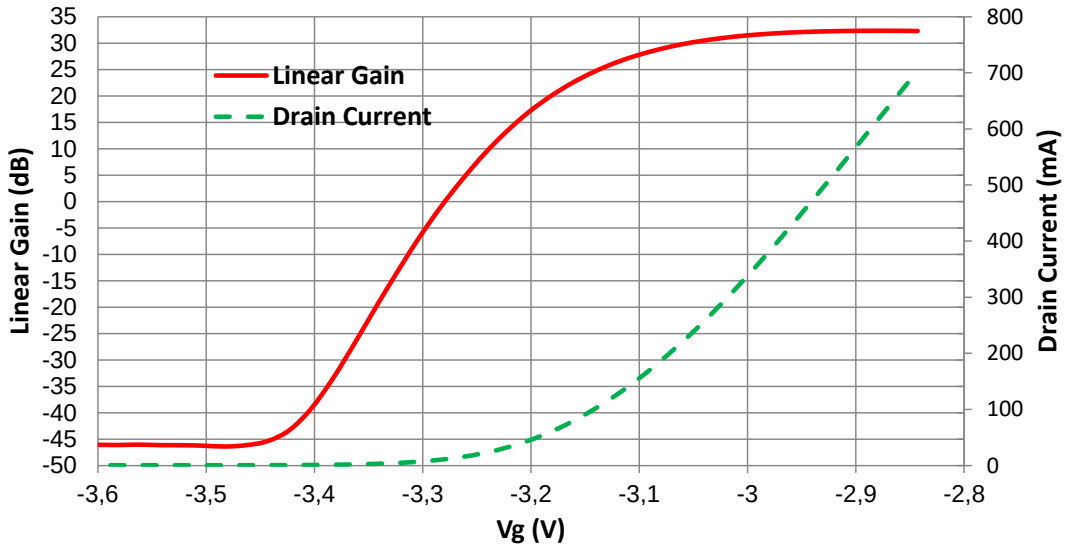
Typical Board Measurements

Tamb.= +25°C, Vd = 20V, Vg set in order to get Id = 420mA
Losses due to board are de-embedded. Measurements are given in the QFN's access planes.

Linear Gain & Drain Current vs. Gate Voltage at 7GHz



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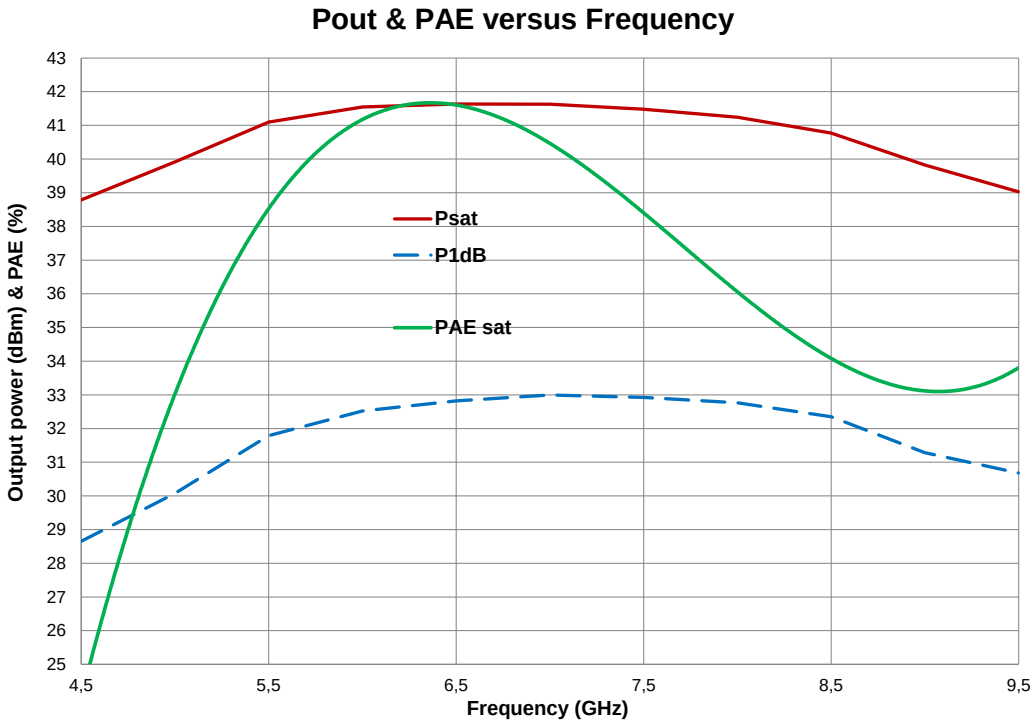
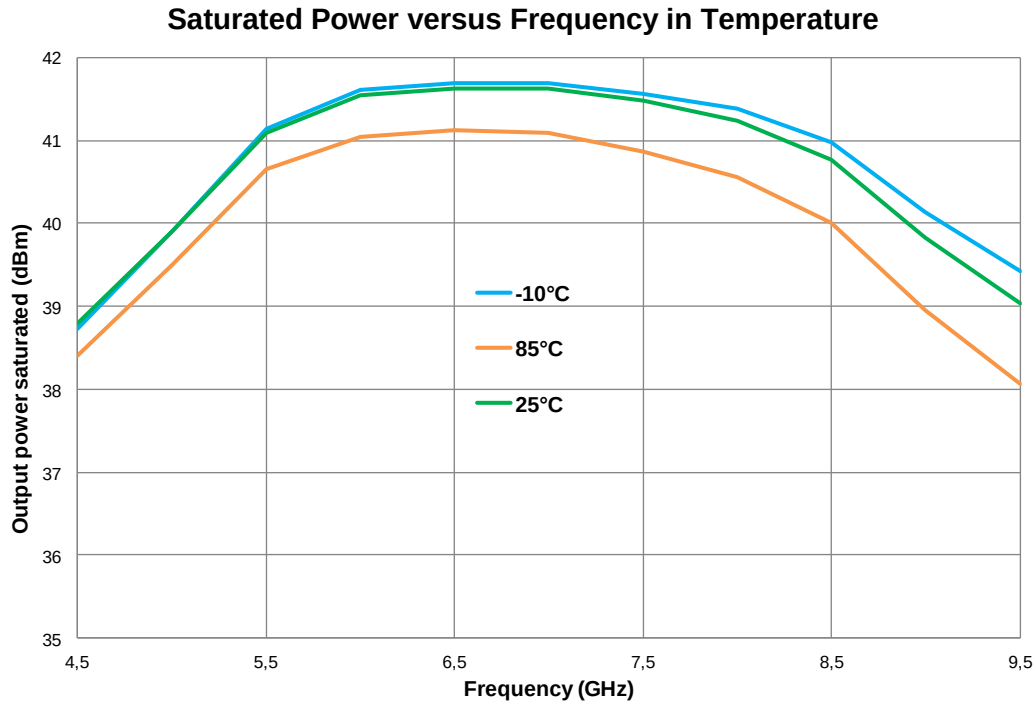
Typical Board Measurements

Tamb.= +25°C, Vd = 20V, Vg set in order to get Id = 420mA
Losses due to board are de-embedded. Measurements are given in the QFN's access planes.





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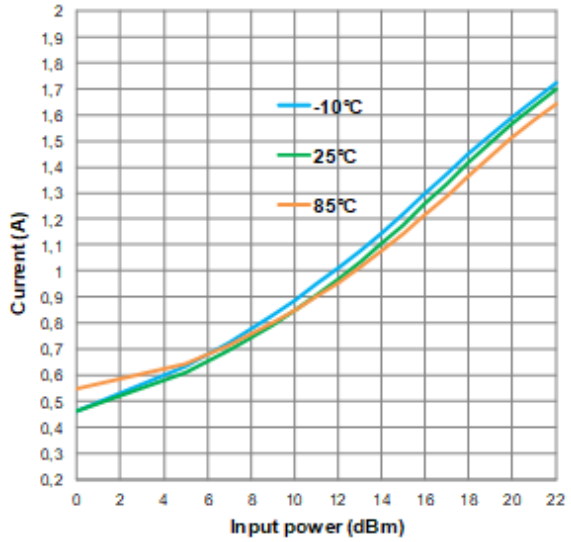
Typical Board Measurements

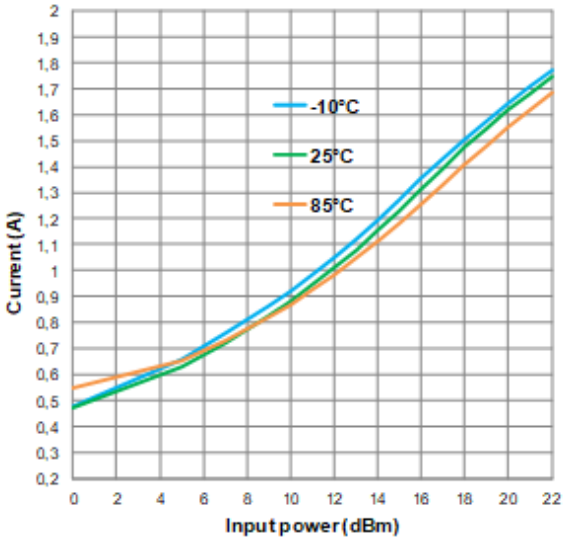
Tamb.= +25°C, Vd = 20V, Vg set in order to get Id = 420mA
Losses due to board are de-embedded. Measurements are given in the QFN's access planes.

Vg fixed for all the temperature

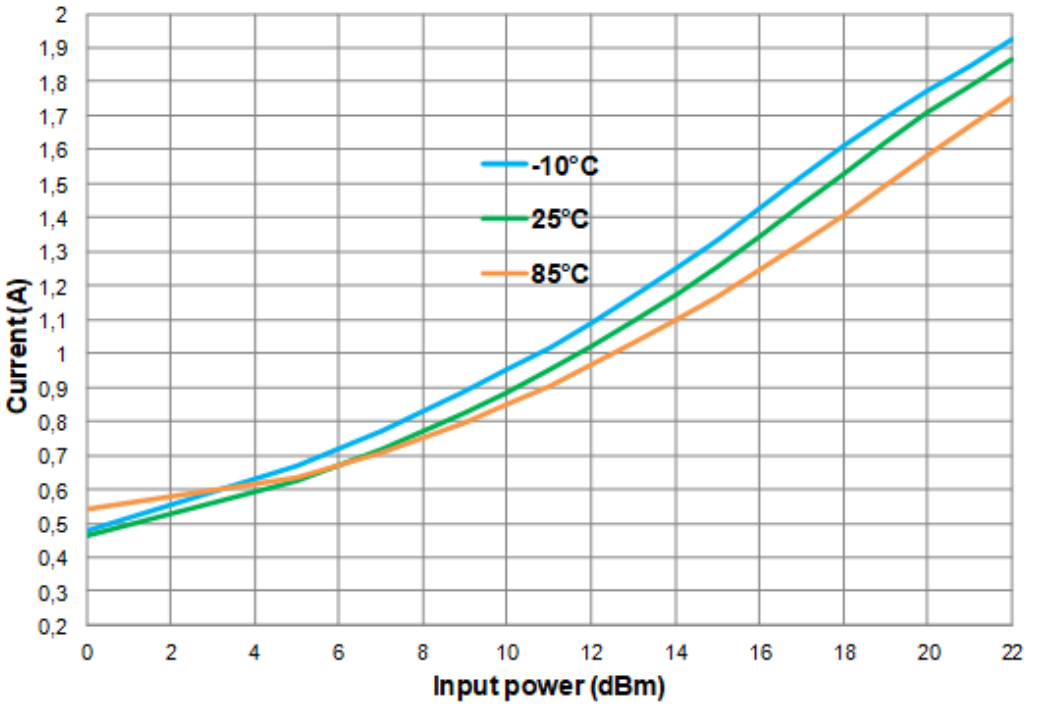
Total Drain Current versus Output Power at 6GHz



Total Drain Current versus Output Power at 7.5GHz



Total Drain Current versus Output Power at 8.5GHz



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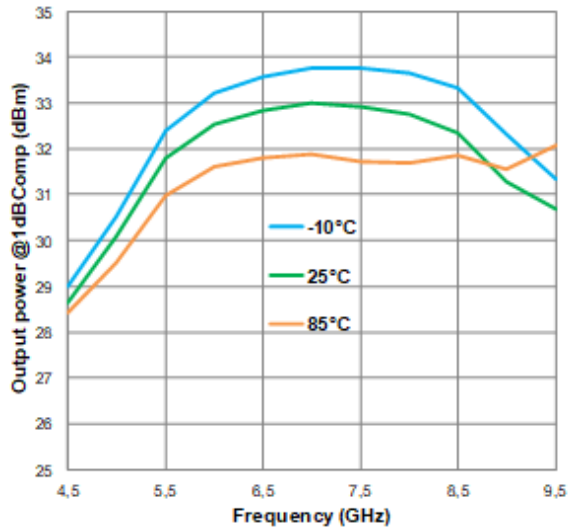
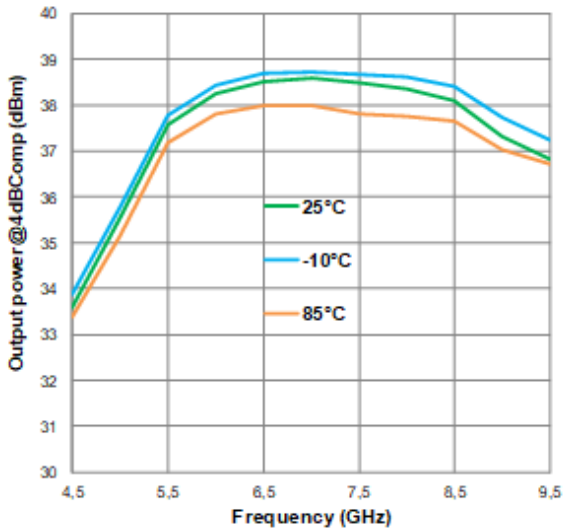
Typical Board Measurements

Tamb.= +25°C, Vd = 20V, Vg set in order to get Id = 420mA
Losses due to board are de-embedded. Measurements are given in the QFN's access planes.

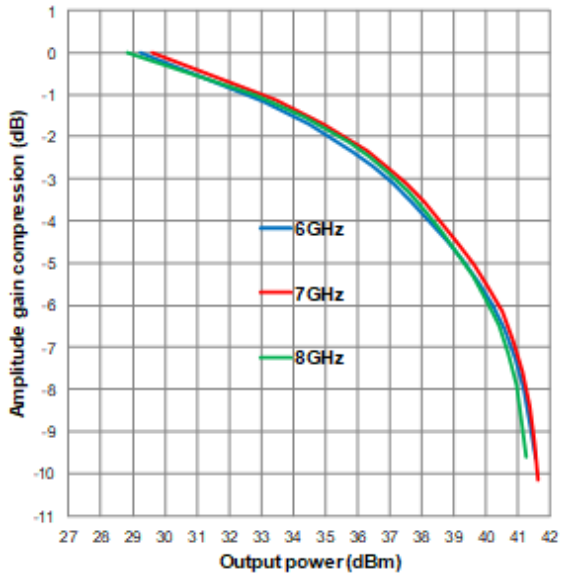
Output Power at P1dB versus Frequency in Temperature
(Vg fixed for all the temperature)

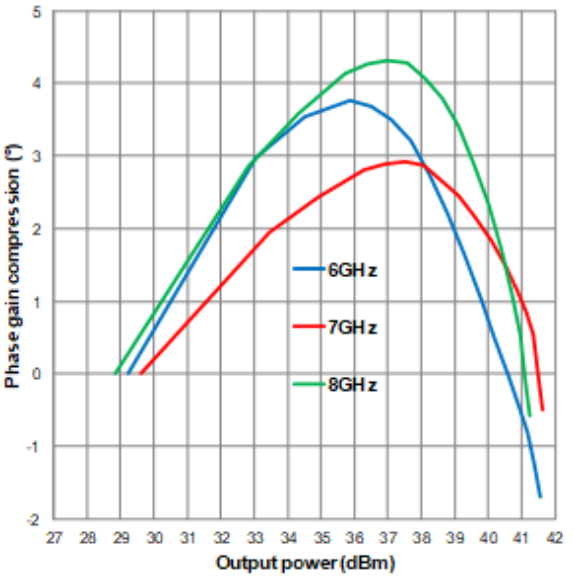


Output Power at P4dB versus Frequency in Temperature
(Vg fixed for all the temperature)



Gain Amplitude & Gain Phase variation versus Output Power





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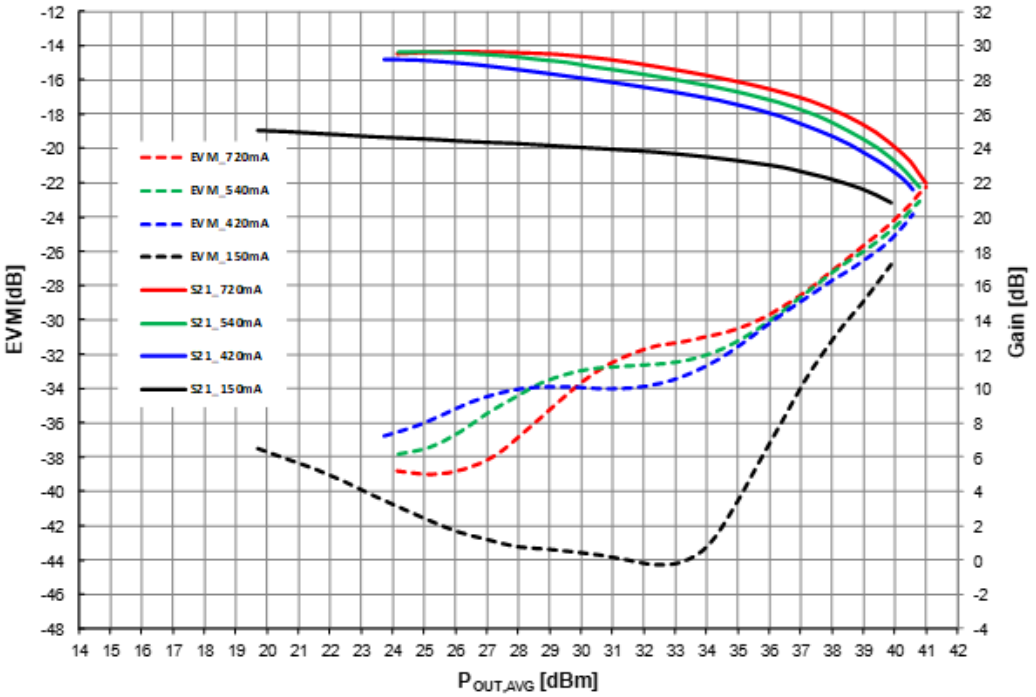
Typical Board Measurements

Tamb.= +25°C, Vd = 20V, Vg set in order to get Id = 420mA

Error Vector Magnitude & Gain versus Output Power

Freq = 7.5GHz ; 150 / 420 / 540 / 720mA

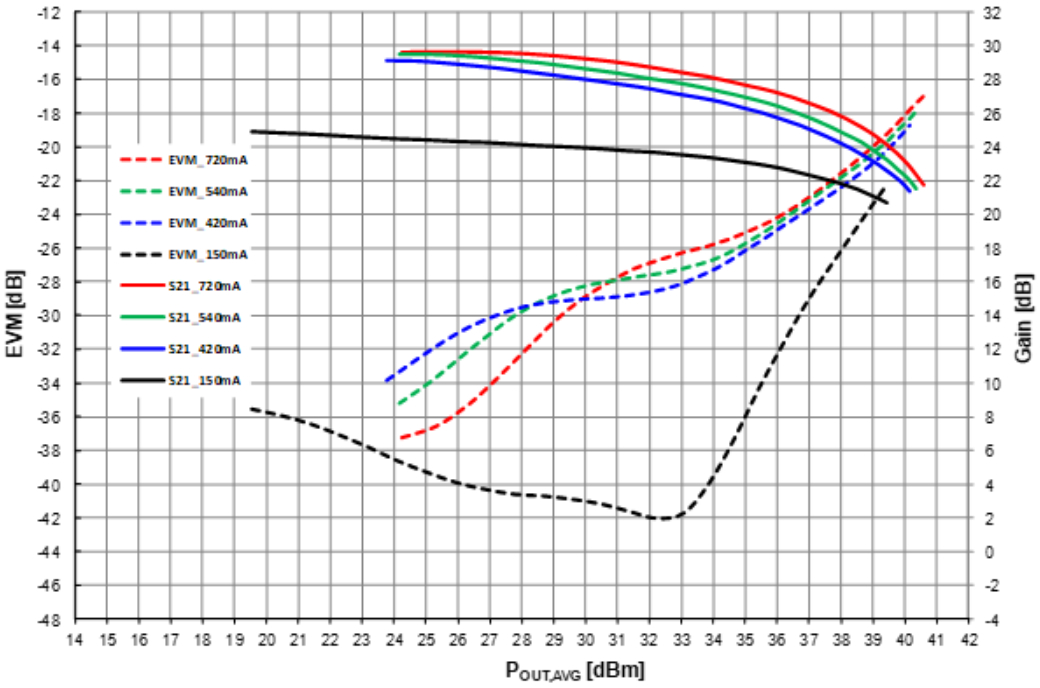
Channel Spacing =56MHz, Modulation = QAM4



Error Vector Magnitude & Gain versus Output Power

Freq = 7.5GHz ; 150 / 420 / 540 / 720mA

Channel Spacing =56MHz, Modulation = QAM2048



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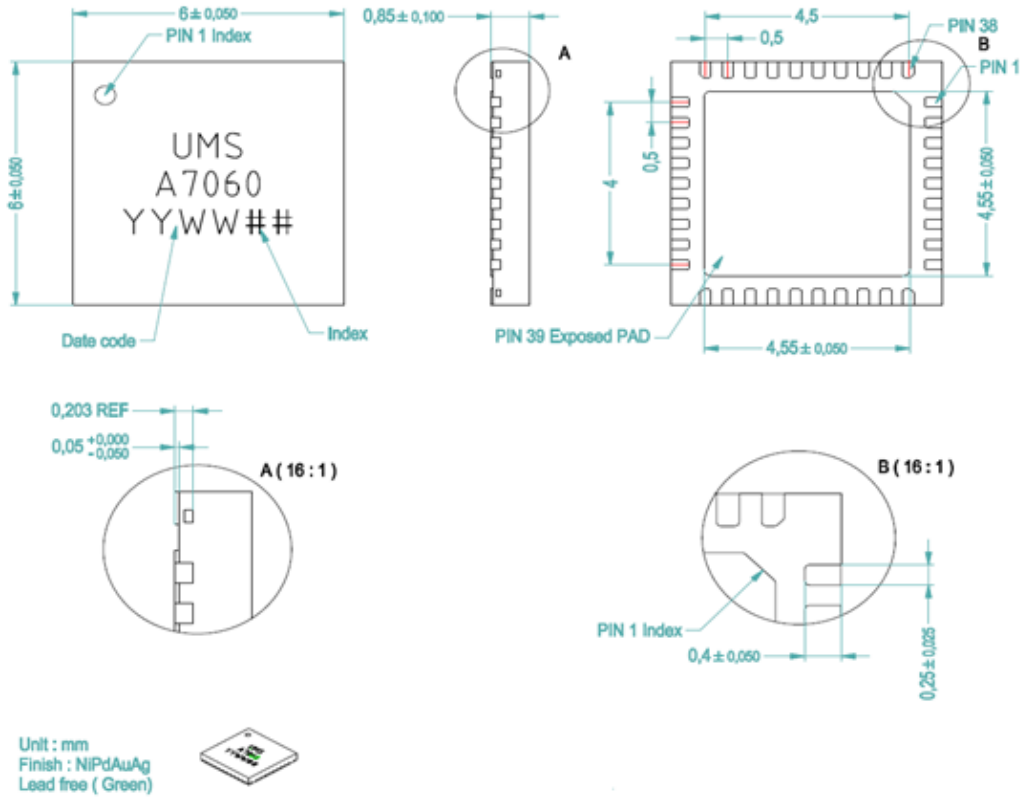
Package outline (1)



Matte tin, Lead Free (Green)	1- NC	14- NC	27- NC
Units : mm	2- NC	15- VG2	28- NC
From the standard : JEDEC MO-220 (VGGD)	3- NC	16- SH	29- NC
	4- Gnd(2)	17- VD2	30- NC
39- GND	5- RF IN	18- NC	31- VD2
	6- Gnd(2)	19- NC	32- G_REF
	7- NC	20- NC	33- VG2
	8- NC	21- NC	34- NC
	9- NC	22- NC	35- VD1
	10- NC	23- Gnd(2)	36- VG1
	11- NC	24- RF OUT	37- NC
	12- VG1	25- Gnd(2)	38- NC
	13- VD1	26- NC	

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-rf.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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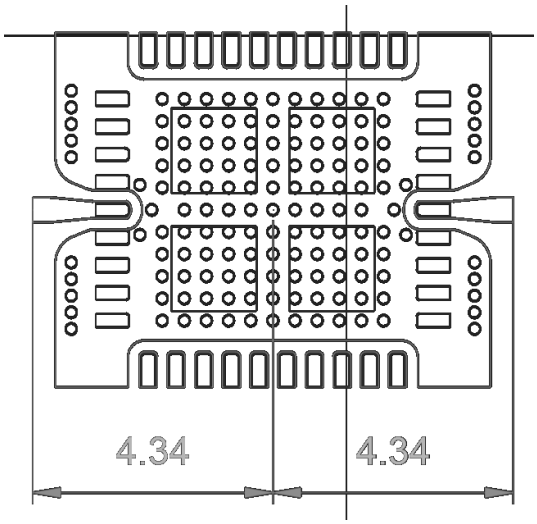
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 4.34mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board" (units in mm).



ESD sensitivity

Standard	Value
MIL-STD-1686C	HBM Class 1 (<2000V)

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL3

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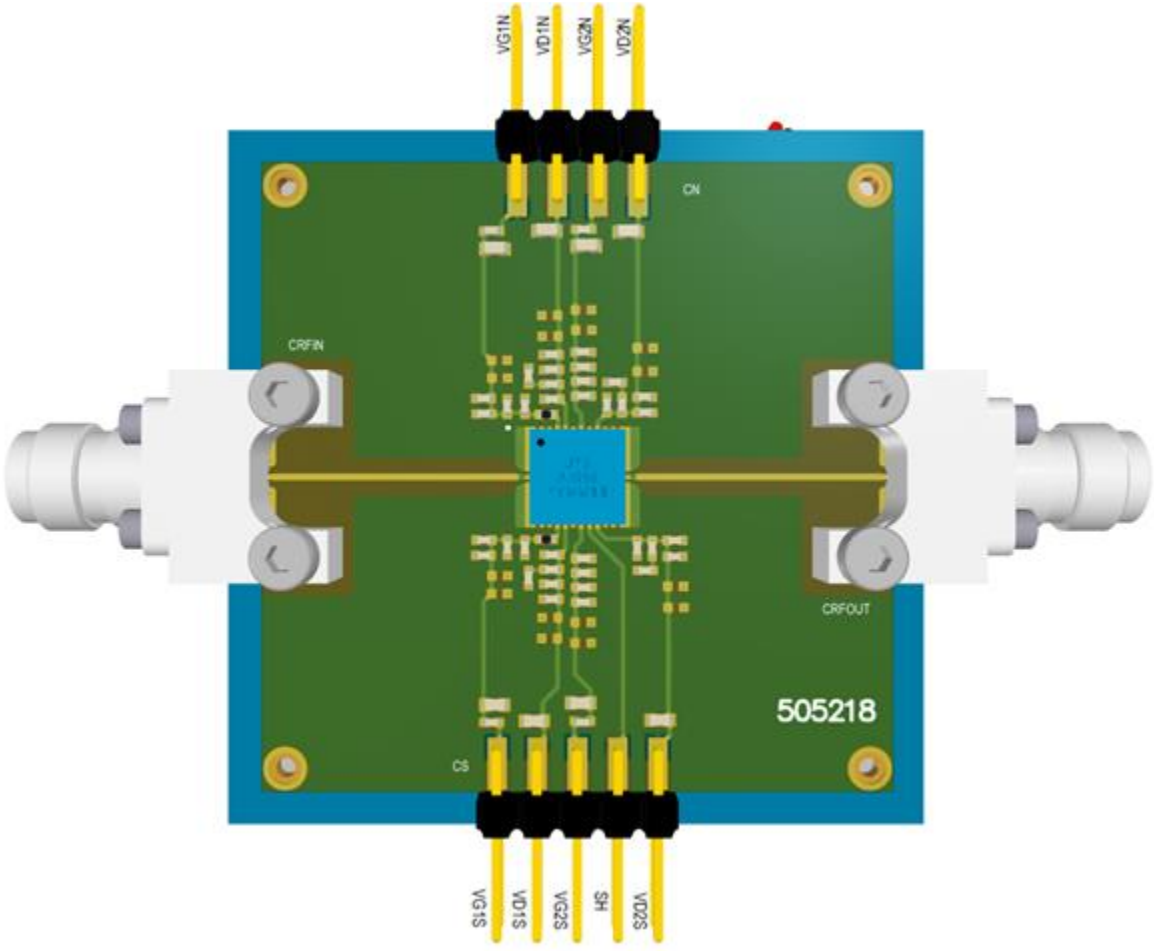
Evaluation mother board

Compatible with the proposed footprint.
■ Based on typically Ro4003 / 8mils or equivalent.
■ Using a micro-strip to coplanar transition to access the package.
■ Recommended for the implementation of this product on a module board.
■ Decoupling capacitors: 100pF ±5%, 1nF ±5%, 10nF ±10%, 100nF ±10%, 1µF ±10% are recommended for all DC accesses.
■ Serial resistors: 100Ohm on the first stage of the gate (North and South).
■ See application note AN0017 for details.



Note: All board measurements are performed using shielded cables, even for DC bias,to ensure safe operation.

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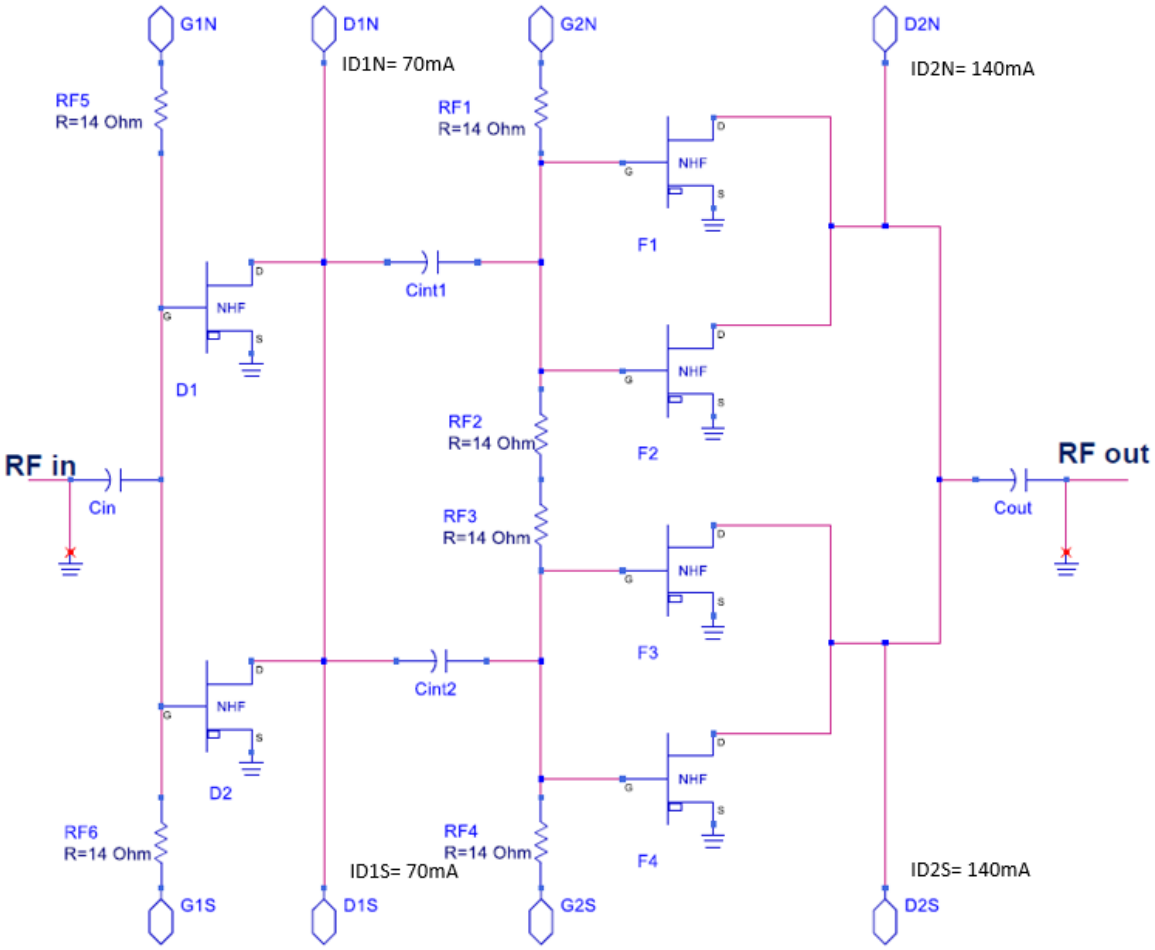
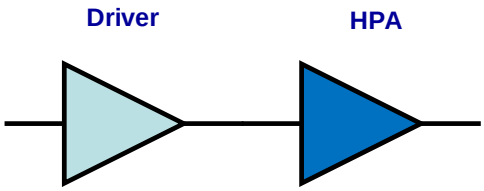
DC Schematic



Recommended UMS Power chain

The CHA7060-QAB is recommended with the CHA4350-QDG as driver.
Total Gain: 56dB
Gain control: 40dB with the both amplifiers.
For more information about the CHA4350-QDG, see our web site www.ums-rf.com



CHA4350-QDG
5.5- 11.7GHz
4V
125mA

CHA7060-QAB
5.6- 8.5GHz
20V
420mA

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Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 6x6 package:	CHA7060-QAB/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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