United Monolithic Semiconductors

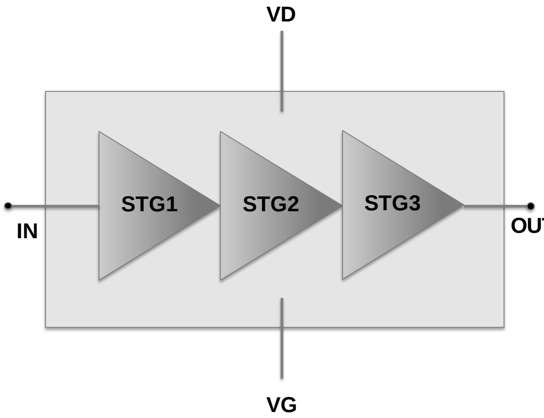
CHA7618-99F

10W Wide-Band High Power Amplifier

GaN Monolithic Microwave IC

Description

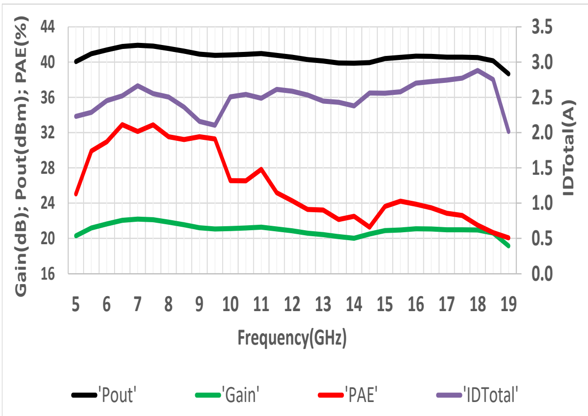
The CHA7618-99F is a three-stage GaN High Power Amplifier in the frequency band 5.5-18GHz. This HPA typically provides 10W of Output Power associated to 20% of Power Added Efficiency. The circuit exhibits a small signal gain of more than 30dB. The overall power supply is of 18V/0.530A (quiescent current).
This circuit is a very versatile amplifier for high performance systems.
The circuit is dedicated to defence applications and well suited for a wide range of microwave applications and systems.
The part is developed on a robust 0.15µm gate length GaN HEMT process and is available as a bare die.



Main Features

- ■ 5.5-18GHz frequency range
- ■ Linear Gain > 30dB
- ■ 40dBm Pout for +20dBm Input Power
- ■ PAE > 20% for +20dBm Input Power
- ■ ID associated current < 3A
- ■ Quiescent Bias : Vd=18V @Idq=0.530A
- ■ Chip size 5.80x3.48x0.07mm

CW measurements: Tb.= 25°C, Vd = +18V/ Idq=530mA Pout versus frequency, Pin=20dBm:



Main Electrical Characteristics

Tb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.5		18	GHz
Gain	Linear Gain		30		dB
Pout	Output Power (Pin=20 dBm)		40		dBm
PAE	Power Added Efficiency (Pin=20 dBm)		20		%

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Specifications (CW mode)

Tb.= +25°C, Vd = +18V, Idq = 530mA,

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.5		18	GHz
Gain	Linear Gain		30		dB
Pout	Output Power (Pin = 20dBm)		40		dBm
PAE	Associated Power Added Efficiency (Pin = 20dBm)		20		%
Id	Associated current (Pin = 20dBm)		2.3		A
S11	Input Return Loss		10		dB
S22	Output Return Loss		7		dB
Idq	Quiescent Current		0.530		A
Vd	Drain Voltage		18	20	V
Vg	Gate Voltage		-2.8		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

Recommended Operating Ratings

Tb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	18 / 20	V
Idq_stg12	1st stage drain current (North and South)	0.075	A
Idq_stg3	2nd stage drain current (North and South)	0.15	A
Idq_stg3	3nd stage drain current (North and South)	0.3	A
Pin	Maximum peak input power overdrive	25	dBm
Tj	Maximum Junction temperature (1)	200	°C

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

Absolute Maximum Ratings (1) (2)

Tb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Pin	Maximum peak input power overdrive	30	dBm
Pdiss.	Dissipated Power (2)	48	W

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) See Thermal Information Page 4/22

Temperature Range

Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

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Typical Bias Conditions

Tb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
VG1,VG2, VG3	2;6;10;18;22;	Gate voltage tuned for Idq ~ 0.530A	-2.8	V
VD1,VD2,VD3	4;8;12;16;20	Drain Voltage	18	V

"Power ON" sequence

1. Bias HPA gate voltage at Vg close to Vpinch-off (example: Vg ≈ -5V).
2. Apply Vd bias voltage (Example: Vd = 18V).
3. Increase Vgs up to quiescent bias drain current Ids0 (applied on the gate: 500mA).
4. Apply RF signal

"Power OFF" sequence

1. Turn off RF signal
2. Bias HPA gate voltage at Vg close to Vpinch-off (example: Vg ≈ -5V)
3. Set Vd to 0V.
4. Turn off Vd supply.
5. Turn off Vg supply.

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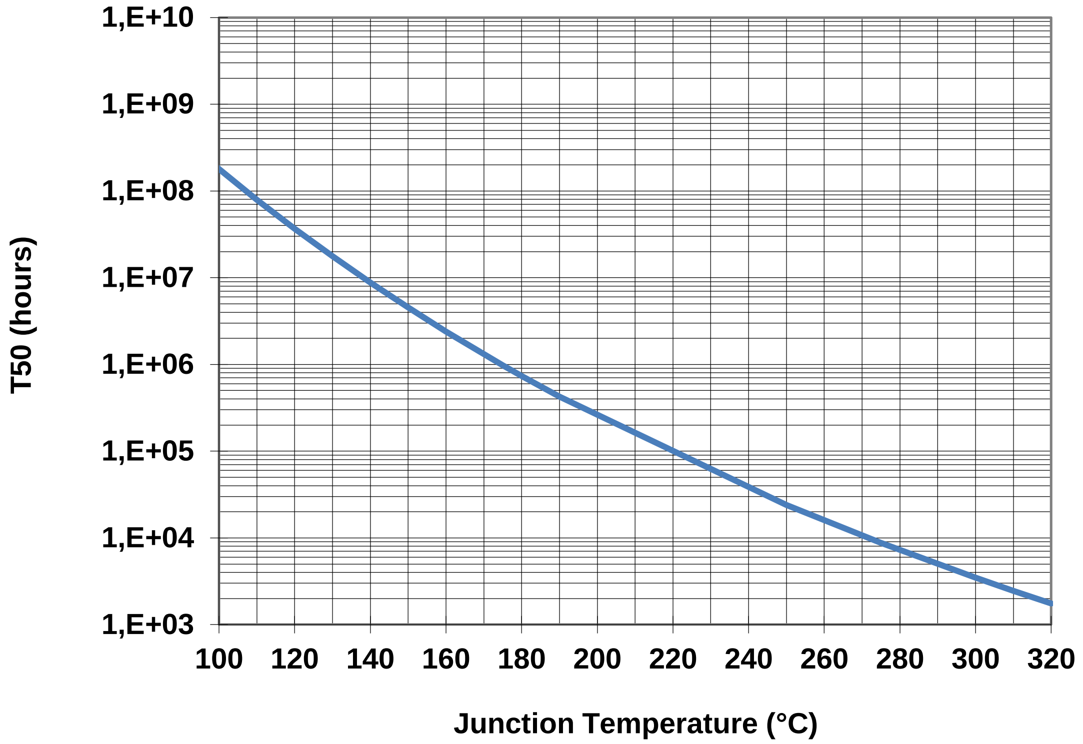
Device thermal information :

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA7618-99F is manufactured (GaN HEMT 0.15µm).
The temperature Tb_{chip} is defined as the chip backside temperature. The thermal resistance (Rth_eq) is given for the full circuit, and assumes CW mode is given in the table.

Thermal Resistance(1)	Rth_eq	Tb_{chip} = 85°C, Vd = 18V, Total ID = 2.8A Pin = 22dBm, Pout = 40dBm 18GHz Pdiss = 40.55W CW	3.0	°C/W
Junction Temperature	Tj		200	°C
Median Life	T50		2.5E6	Hrs

(1) Thermal resistance measured at the back of the chip Worst Case

Median Life Time versus Junction Temperature



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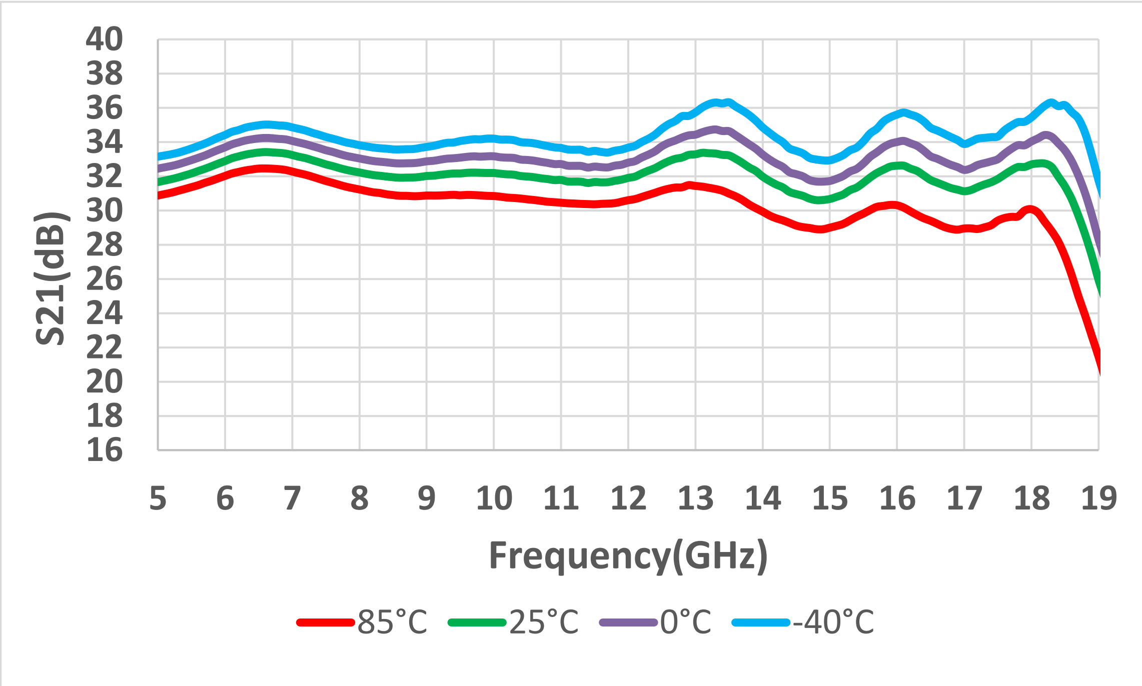
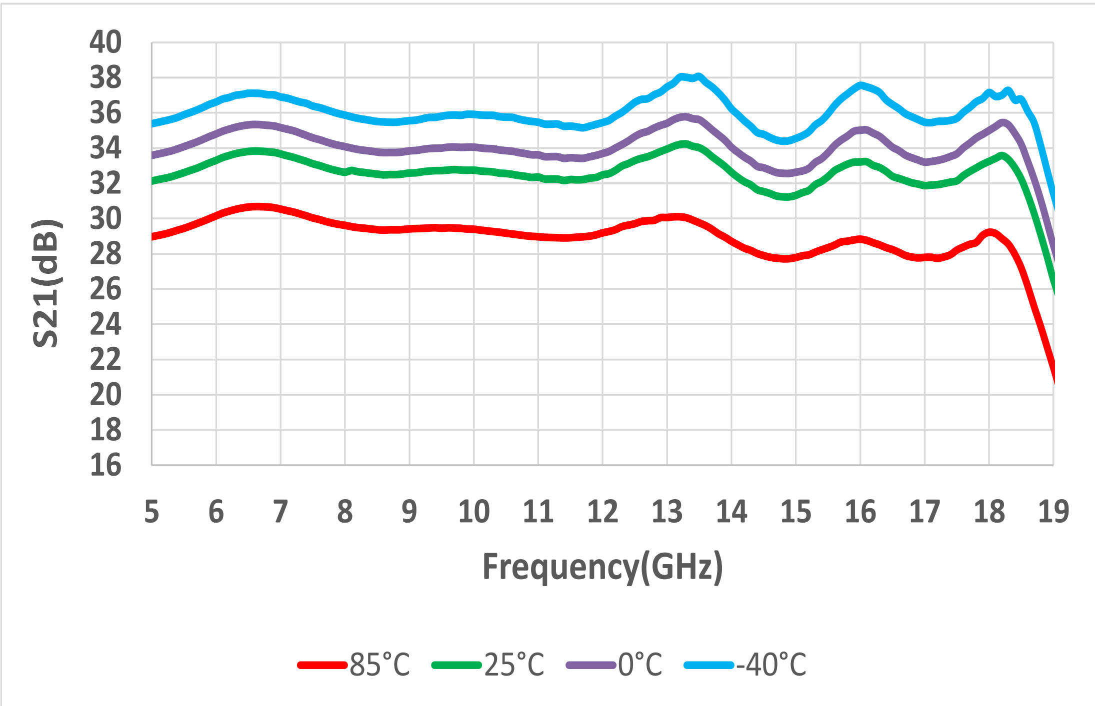
Typical Test Fixture Measurements: Small Signal Performances

CW measurements: Tb.= 25°C/0°C/-40°C/+85°C, Vd = +18V

Linear Gain versus Frequency
(Idq=530mA @25°C)



Linear Gain versus Frequency
Idq=530mA (kept constant versus temperature)



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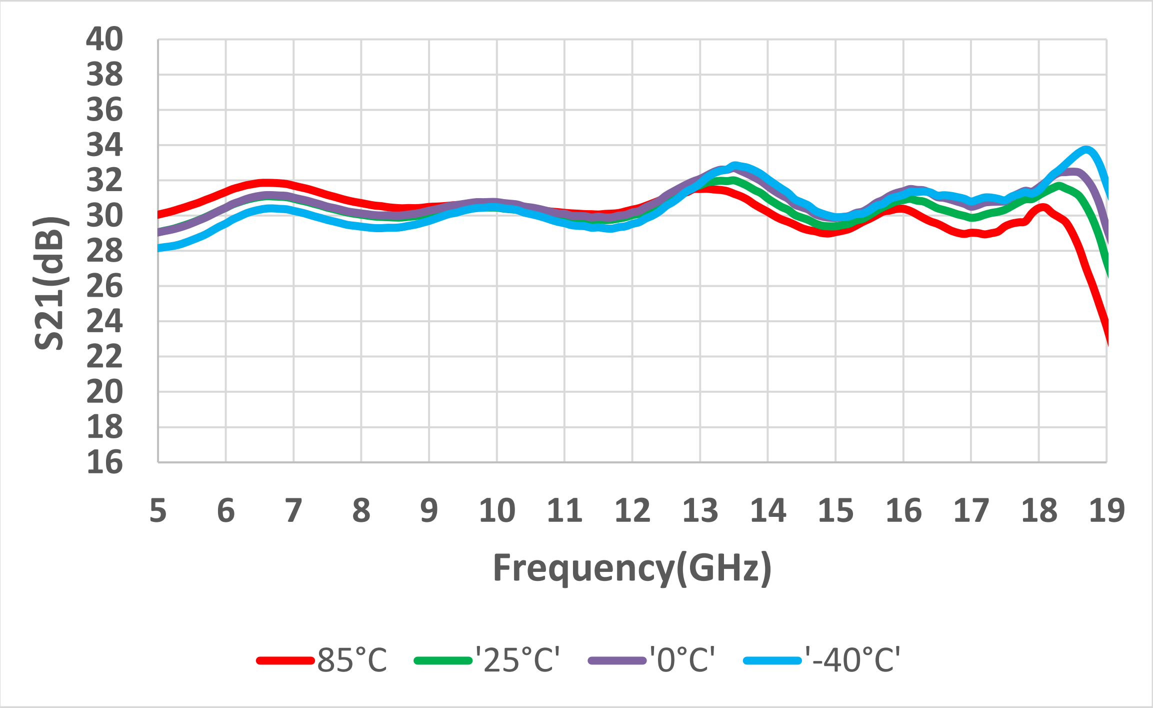
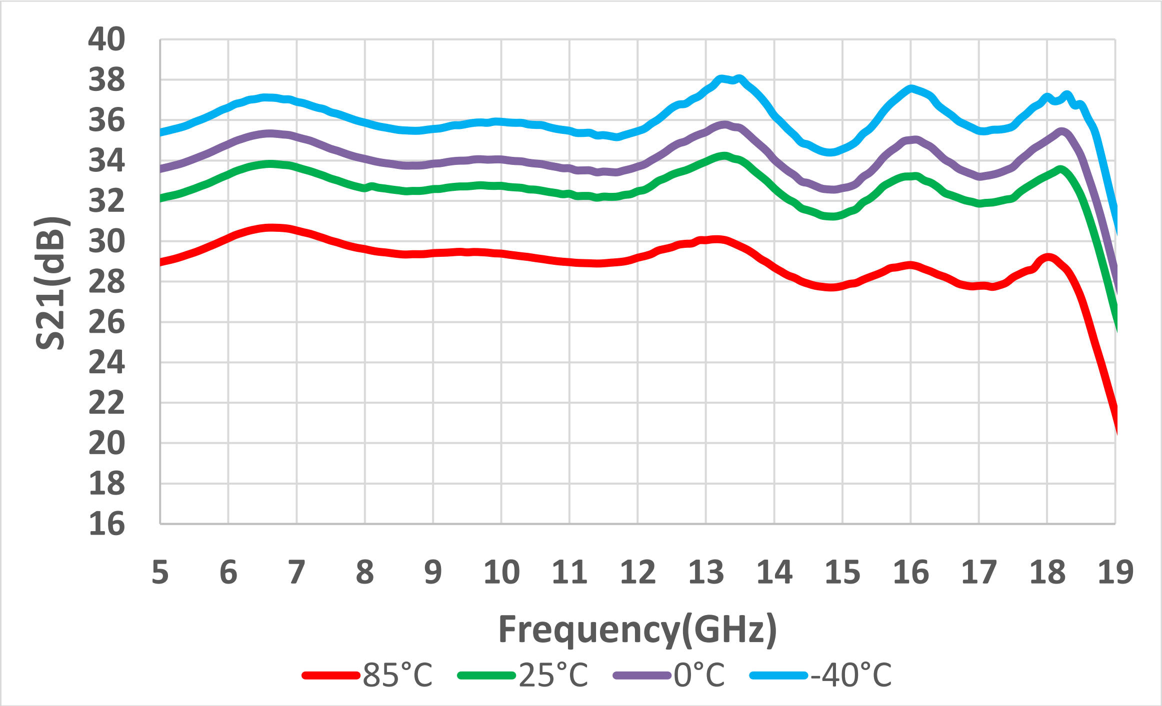
Typical Test Fixture Measurements: Small Signal Performances

CW measurements: Tb.= 25°C/0°C/-40°C/+85°C, Vd = +20V

Linear Gain versus Frequency
Idq=350mA @25°C



Linear Gain versus Frequency
Idq=350mA (kept constant versus temperature)



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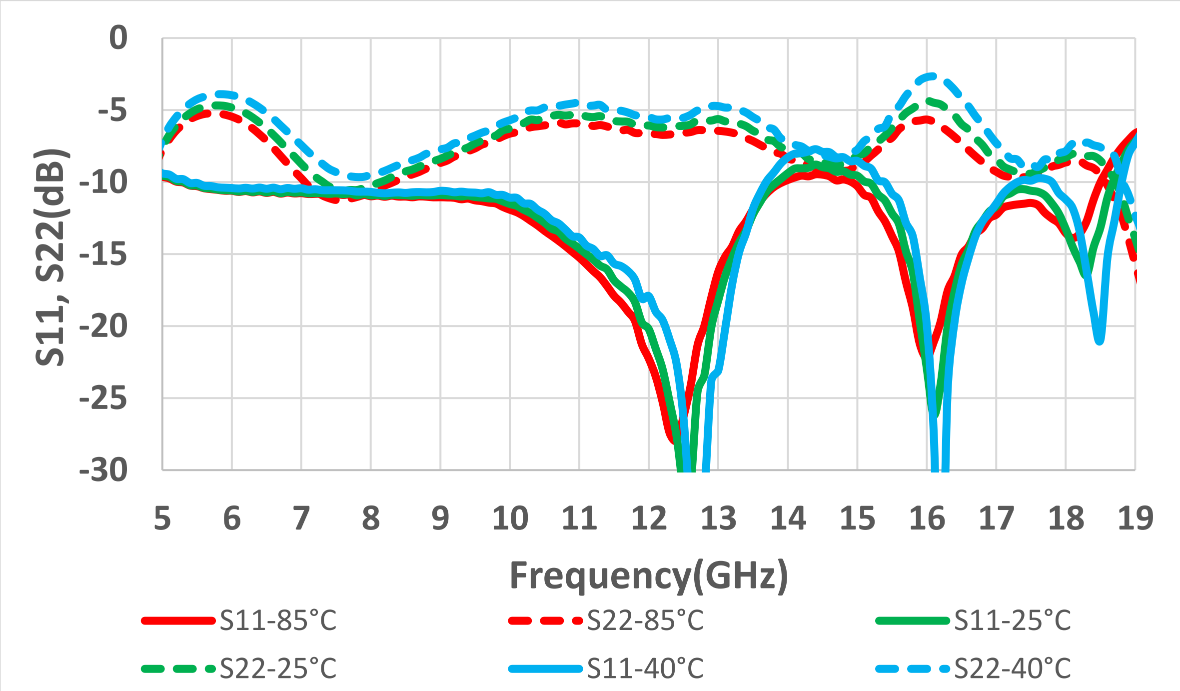
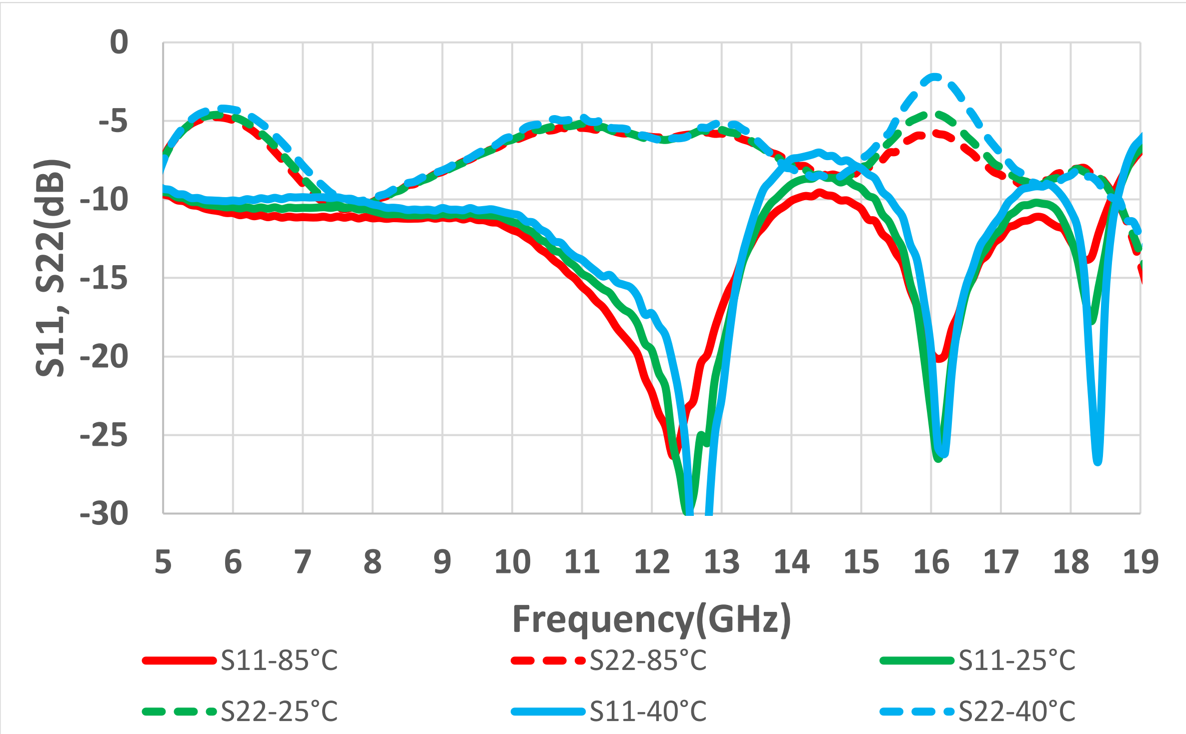
Typical Test Fixture Measurements: Small Signal Performances

CW measurements: Tb.= +25°C/+85°C/-40°C, Vd = +18V

Input Return Loss / output Return Loss versus Frequency
Idq = 530mA @25°C



Input Return Loss / output Return Loss versus Frequency
Idq = 530mA (kept constant versus temperature)



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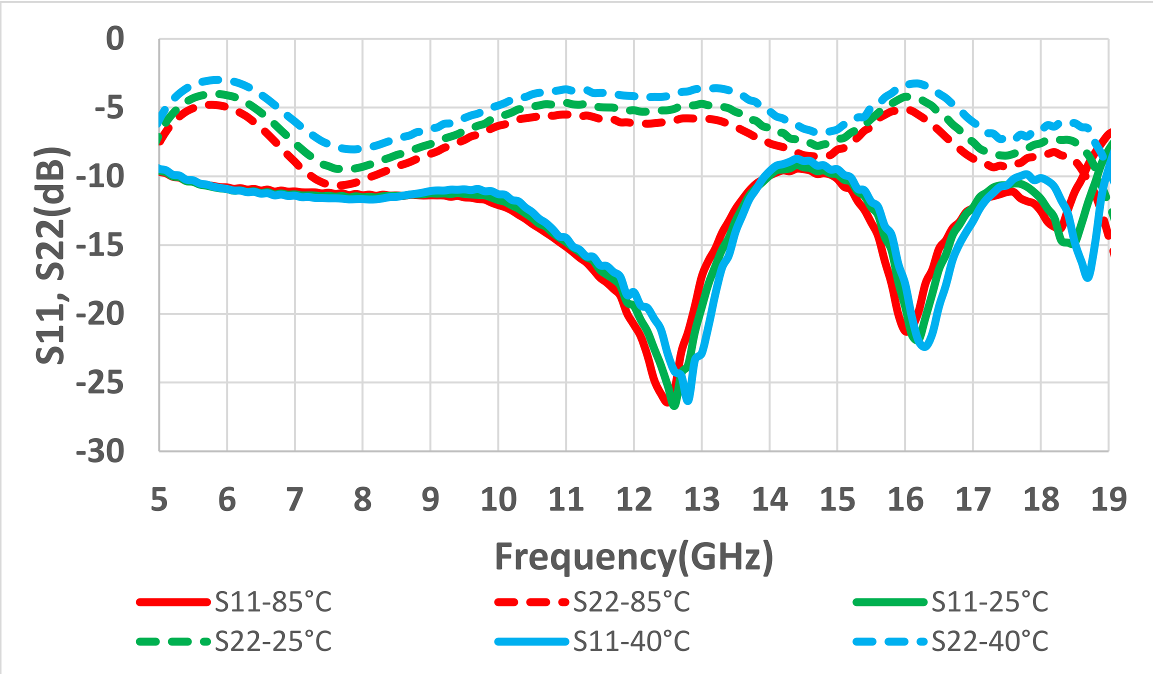
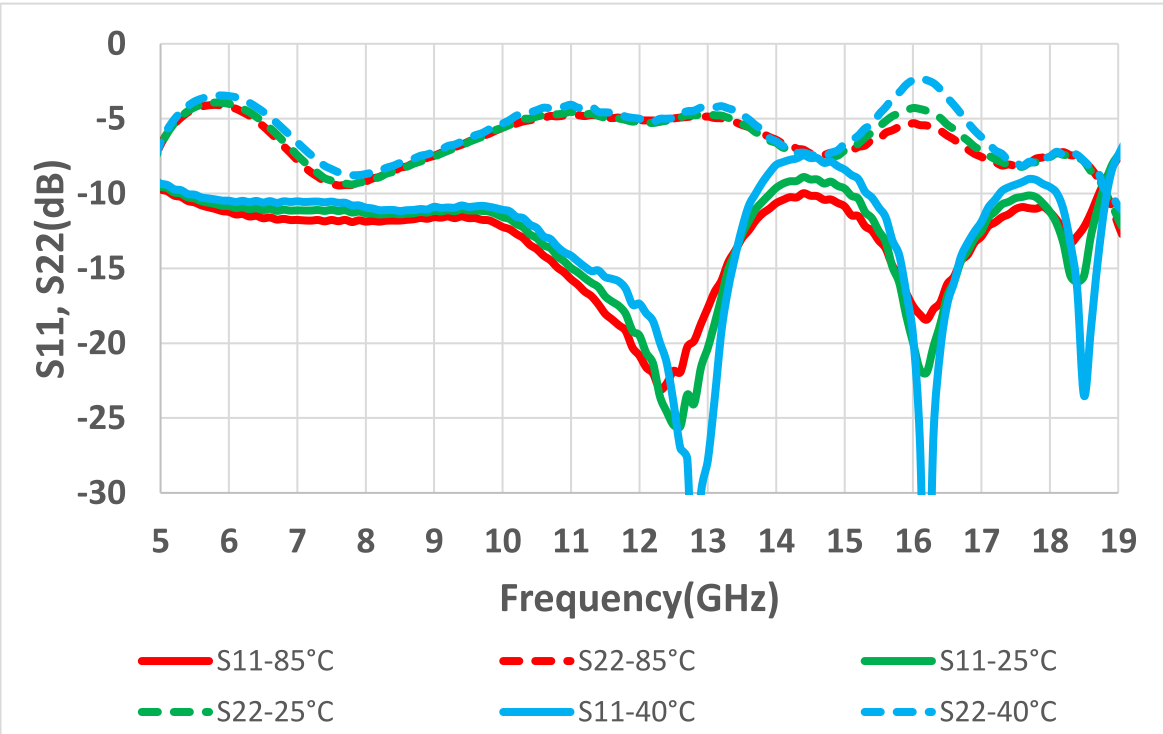
Typical Test Fixture Measurements: Small Signal Performances

CW measurements: Tb.= +25°C/+85°C/-40°C, Vd = +20V

Input Return Loss / output Return Loss versus Frequency
Idq = 350mA @25°C



Input Return Loss / Output Return Loss versus Frequency
Idq = 350mA (kept constant versus temperature)



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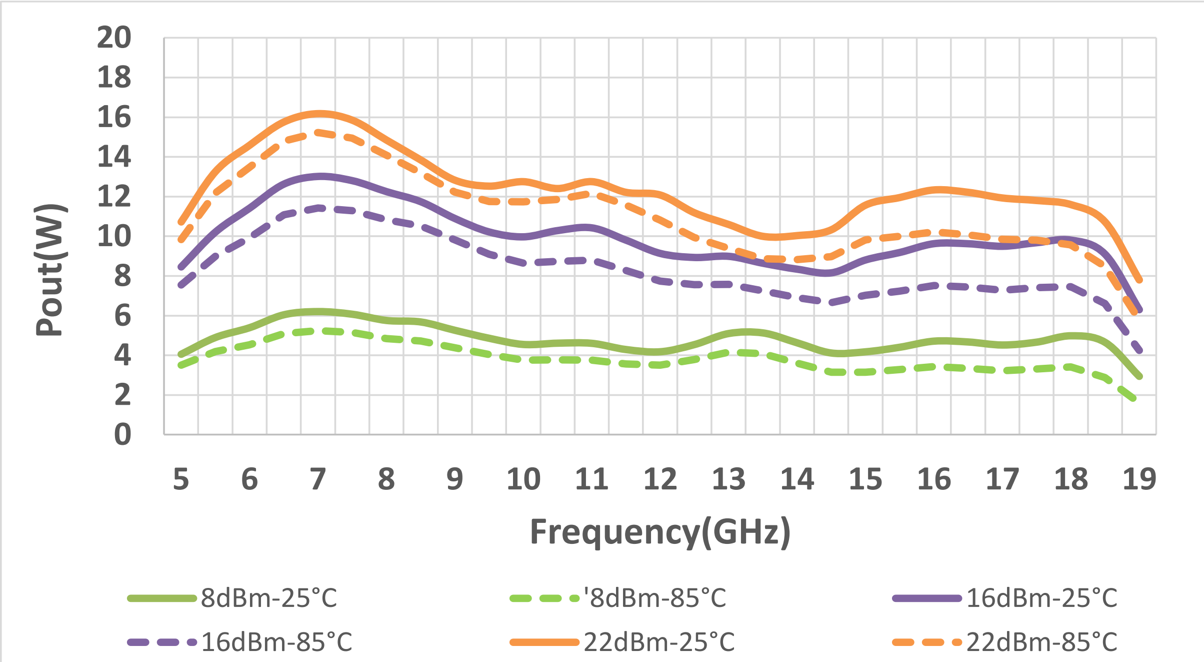
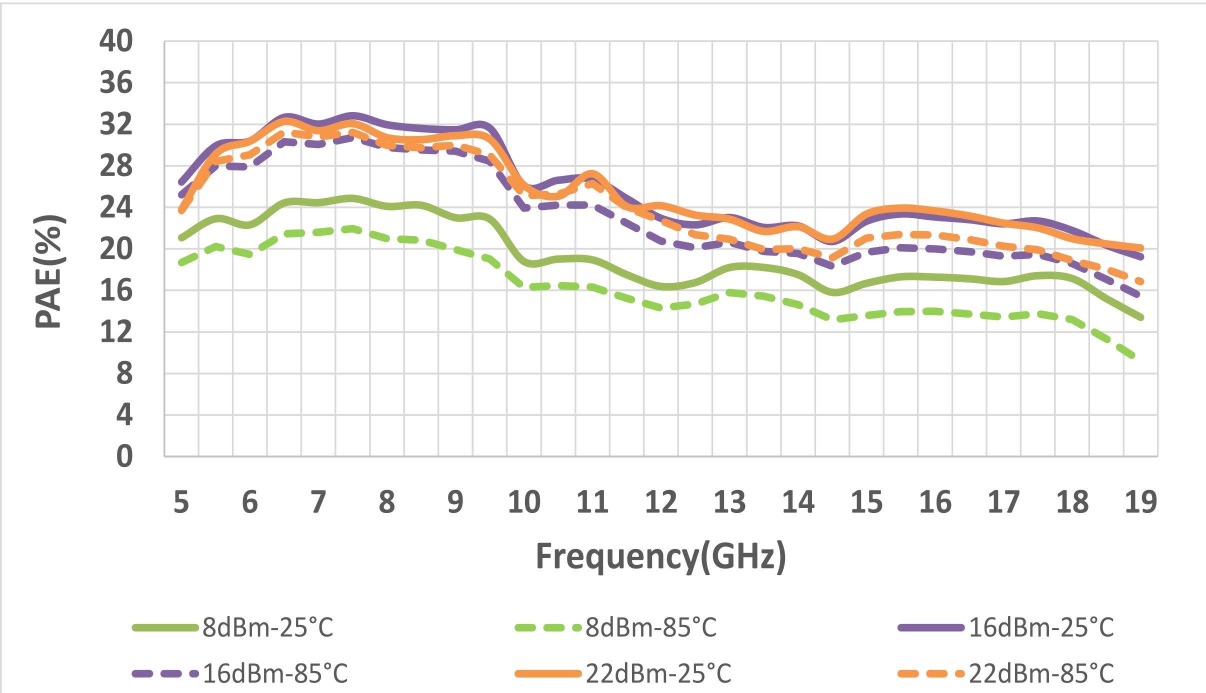
Typical Test Fixture Measurements: Non-linear performances

CW measurements: Tb=+25°C/+85°C, Vd = +18V, Idq = 530mA @25°C

Output Power versus Frequency



Power Added Efficiency versus Frequency



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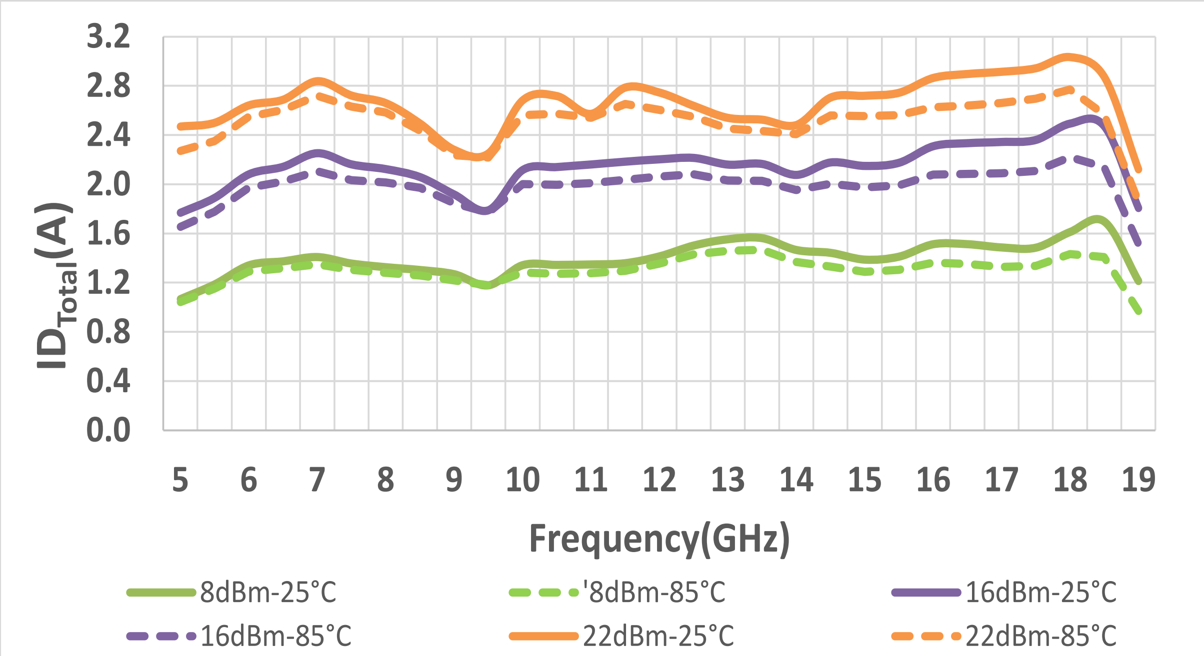
Typical Test Fixture Measurements: Non-linear performances

CW measurements: Tb=+25°C/+85°C, Vd = +18V, Idq = 530mA @25°C

Drain Current (Total ID) versus Frequency



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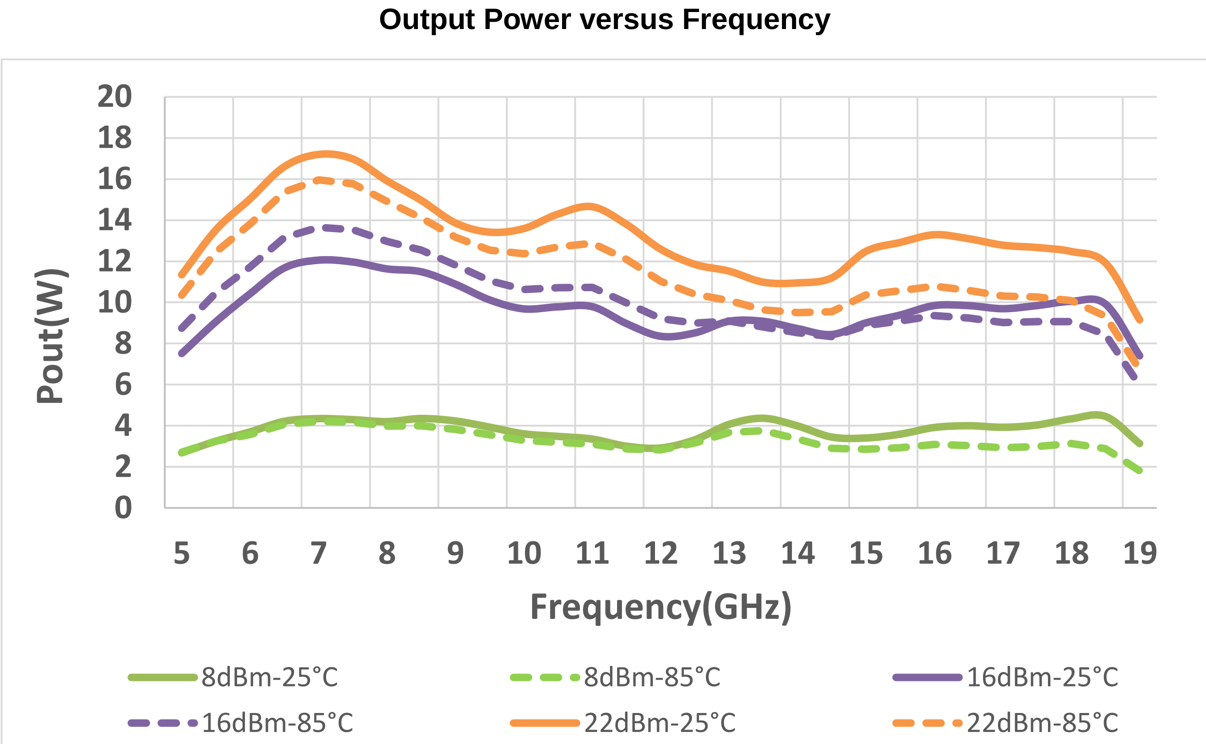
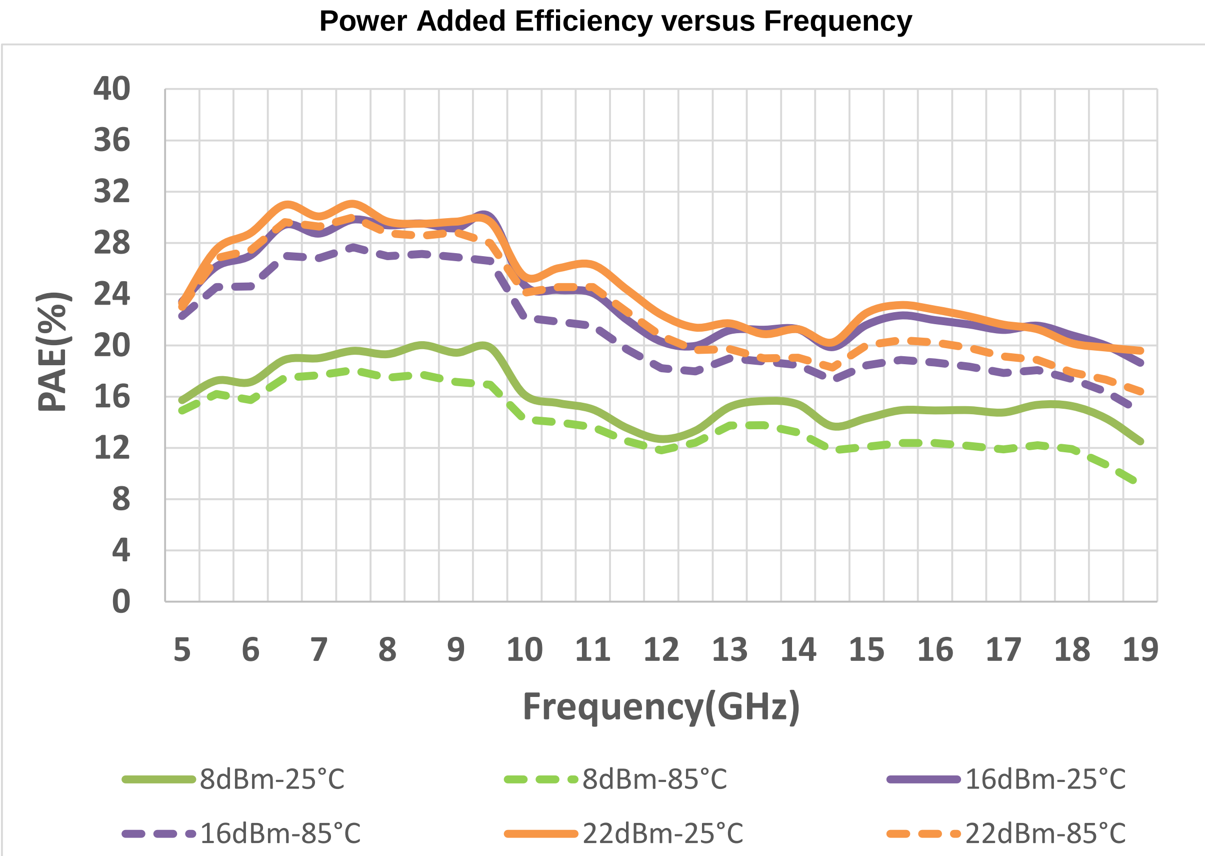
CW measurements: Tb=+25°C/+85°C, Vd = +20V, Idq = 350mA @25°C





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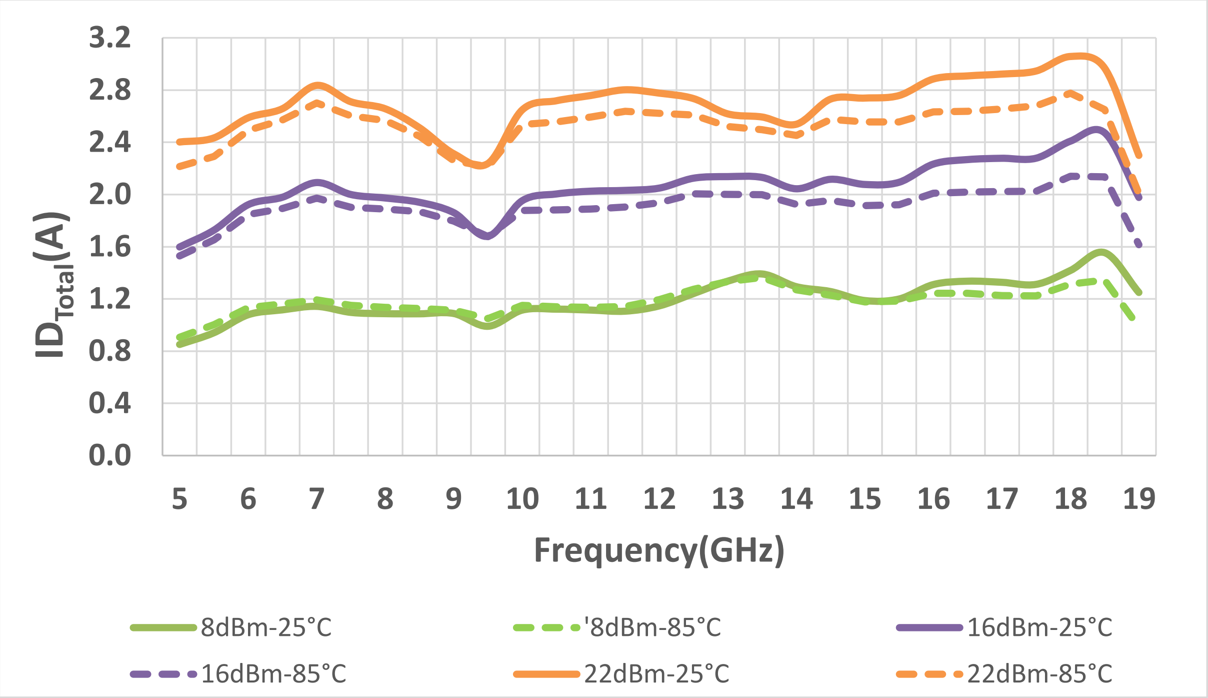

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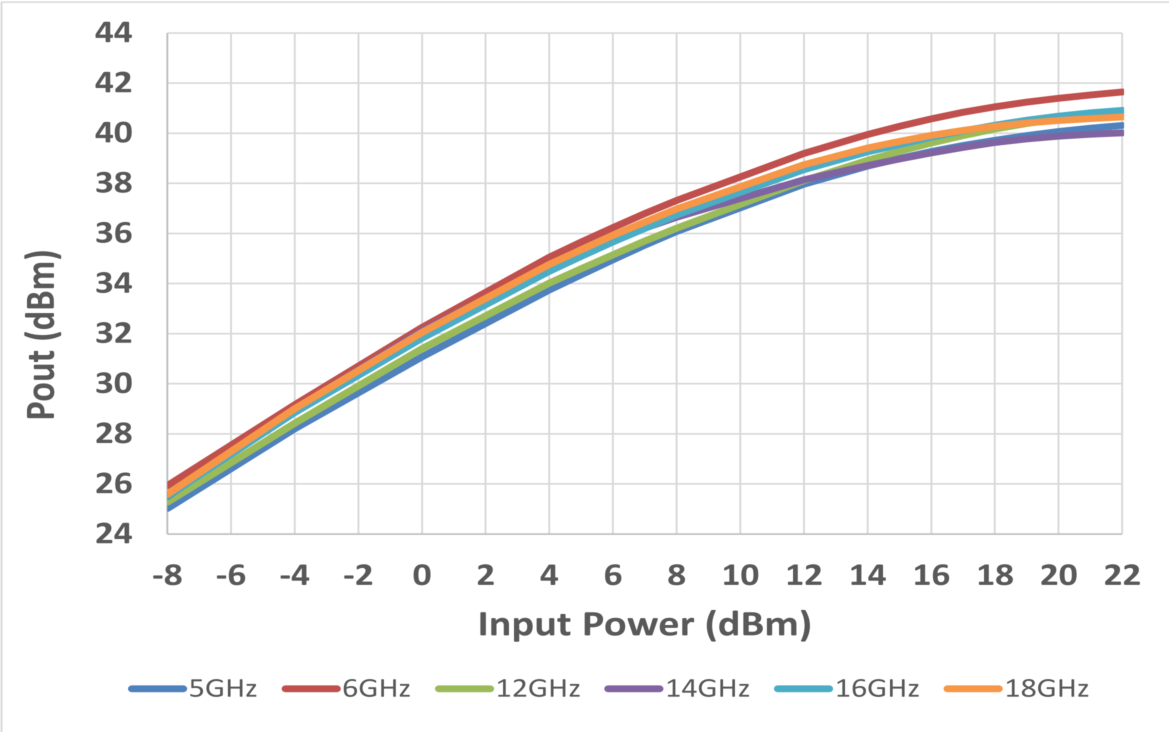
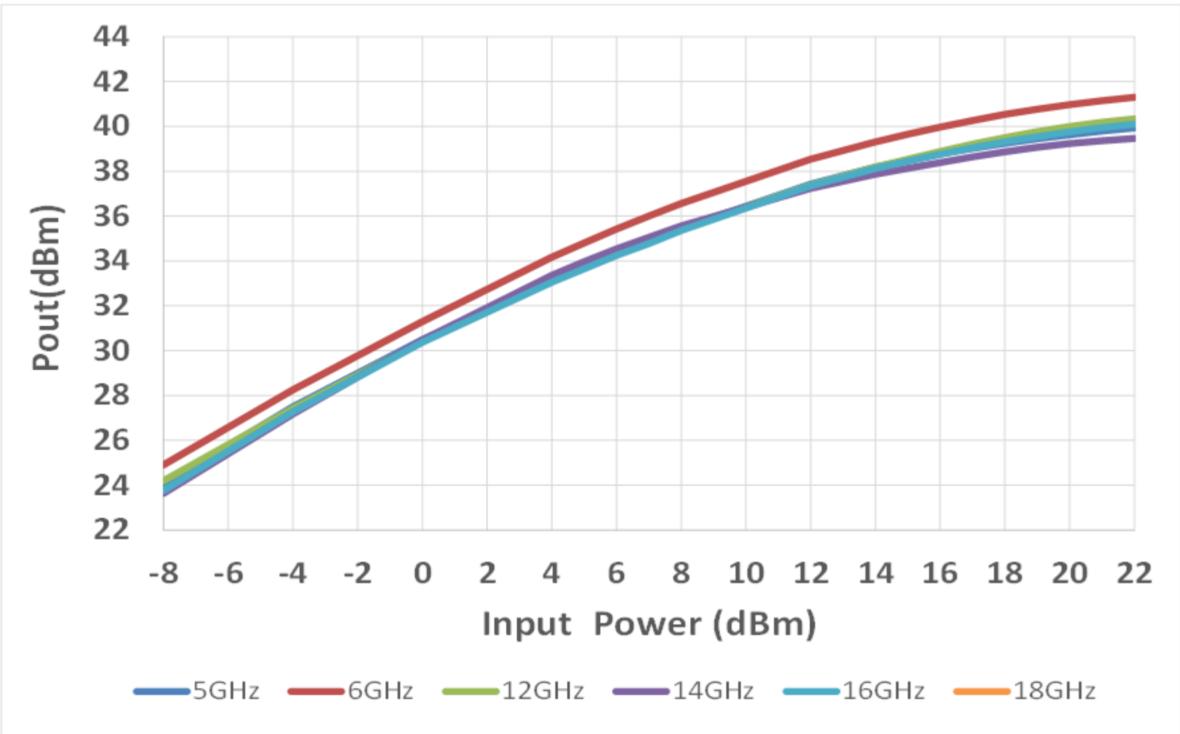
Typical Test Fixture Measurements: Non-linear Performances

CW measurements:Vd = +18V, Idq=530mA
Frequency: 5GHz, 6GHz, 12GHz, 14GHz, 16GHz, 18GHz

Pout versus Input Power Tb.= 25°C



Pout versus Input Power



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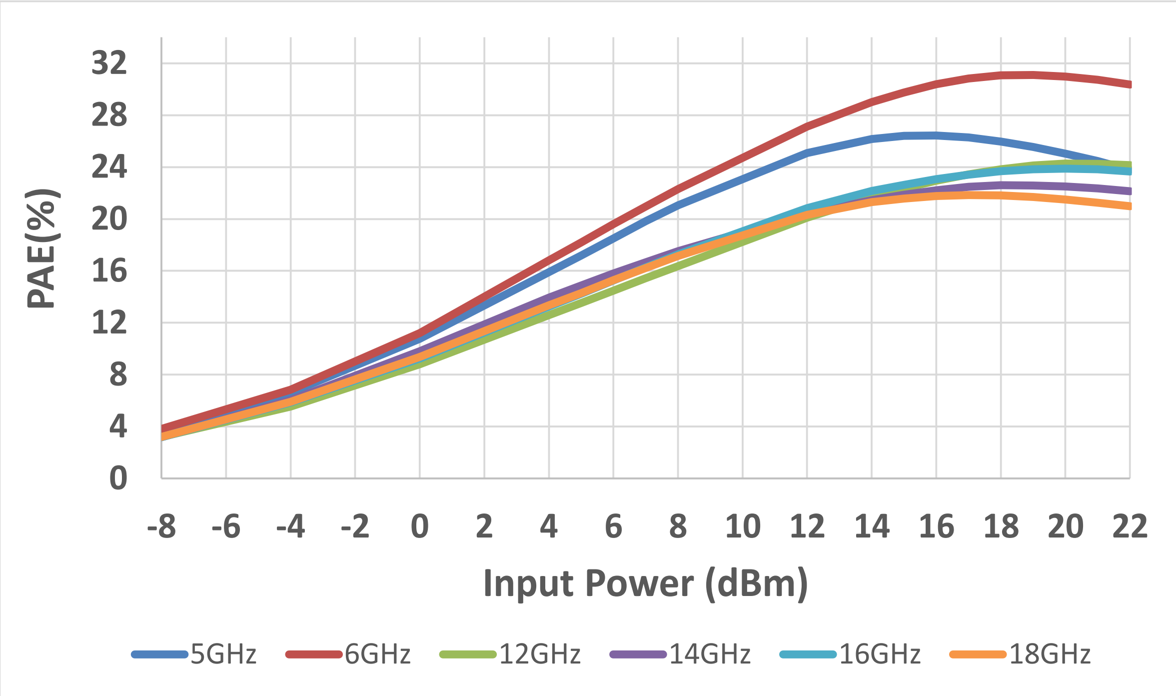
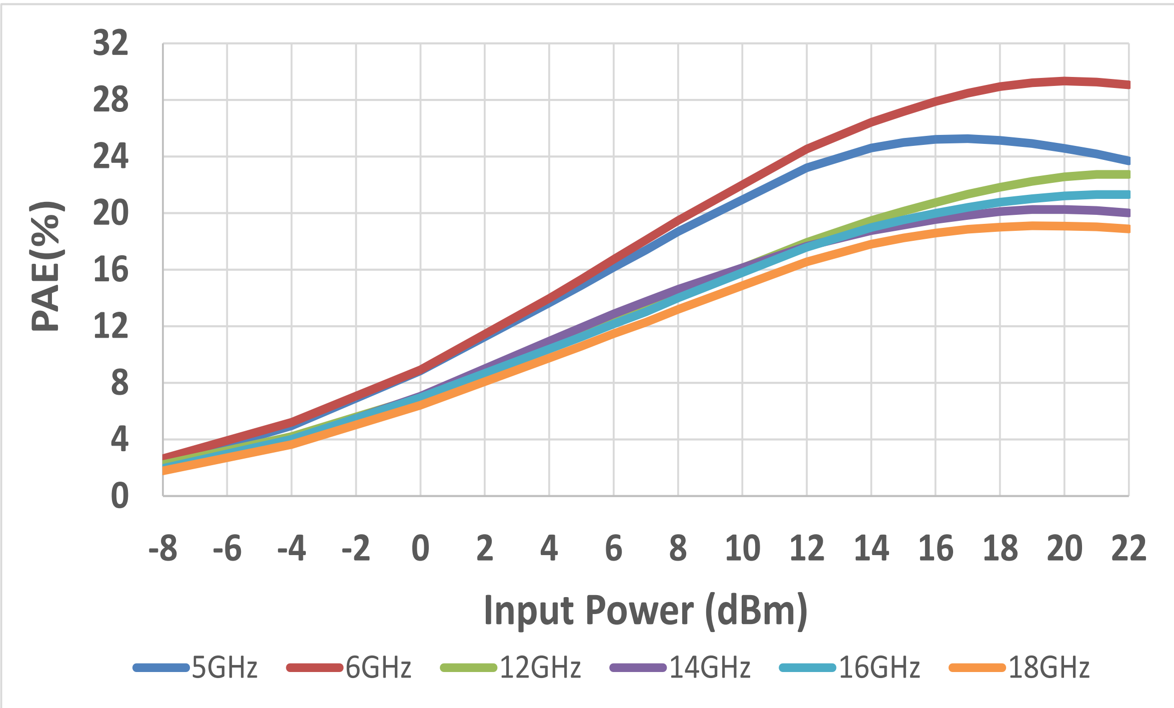
Typical Test Fixture Measurements: Non-linear Performances

CW measurements: Vd = +18V, Idq=530mA
Frequency: 5GHz, 6GHz, 12GHz, 14GHz, 16GHz, 18GHz

Power Added Efficiency versus Input Power Tb.= 25°C



Power Added Efficiency versus Input Power Tb.= 85°C



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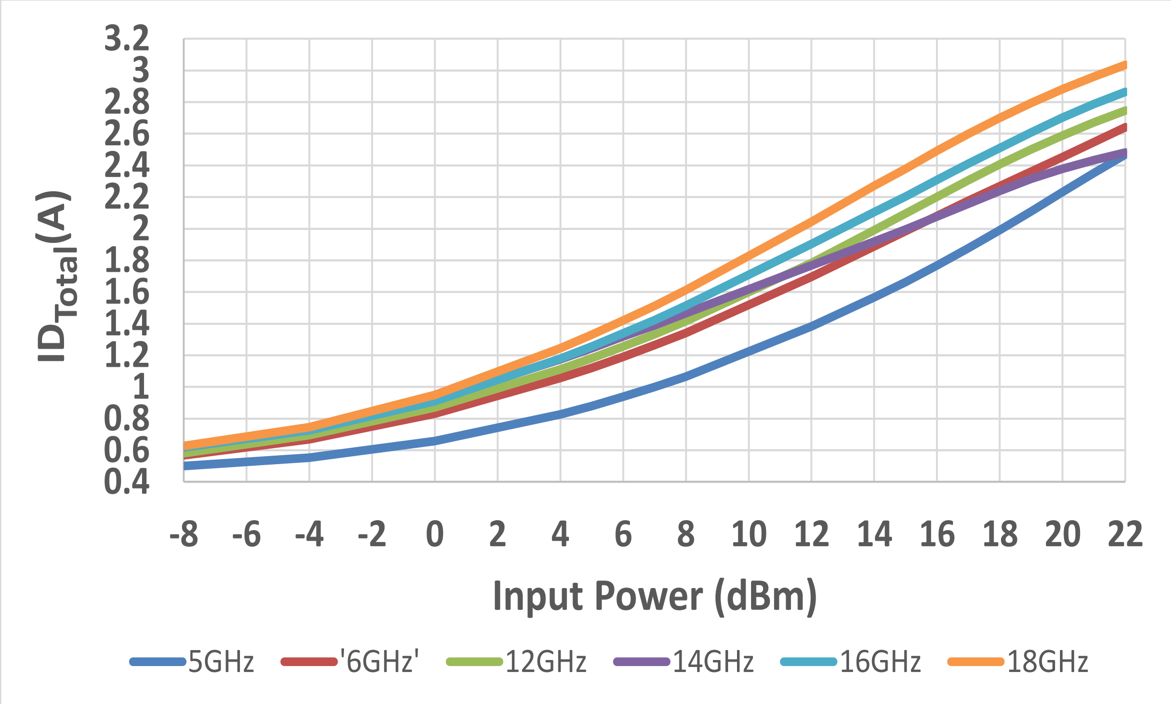
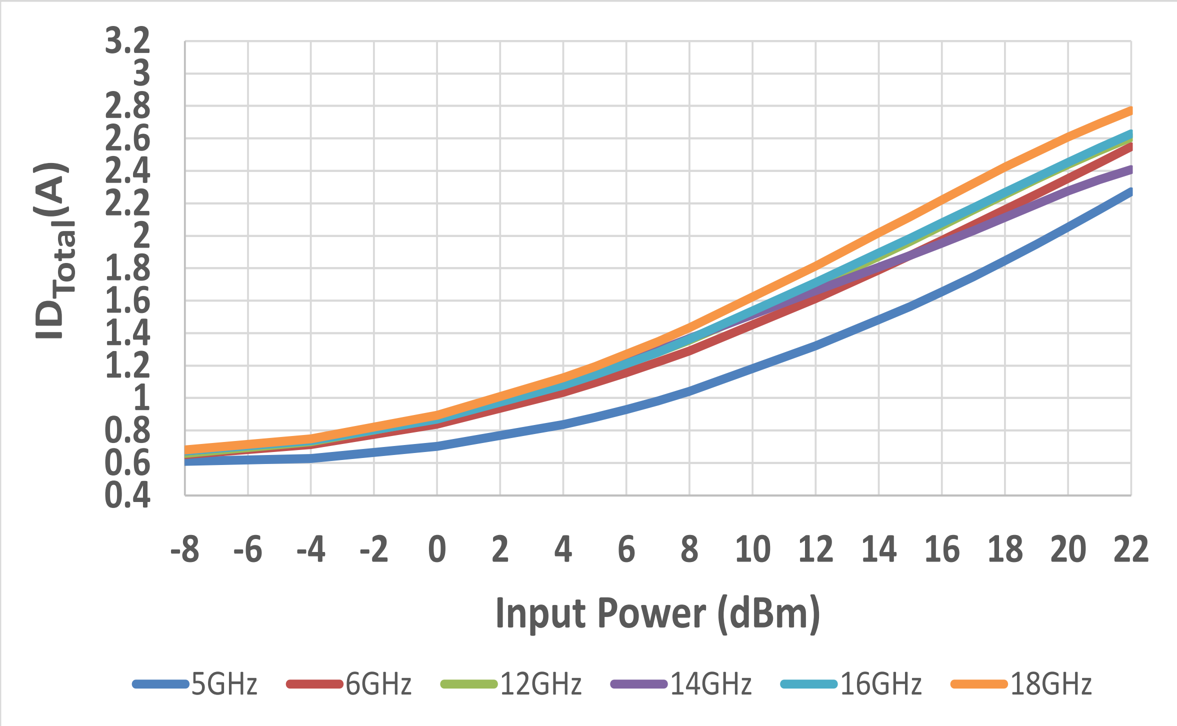
Typical Test Fixture Measurements: Non-linear Performances

CW measurements:Vd = +18V, Idq=530mA
Frequency: 5GHz, 6GHz, 12GHz, 14GHz, 16GHz, 18GHz

Drain current (Total ID) versus Input Power Tb.= 25°C



Drain current (Total ID) versus Input Power Tb.= 85°C



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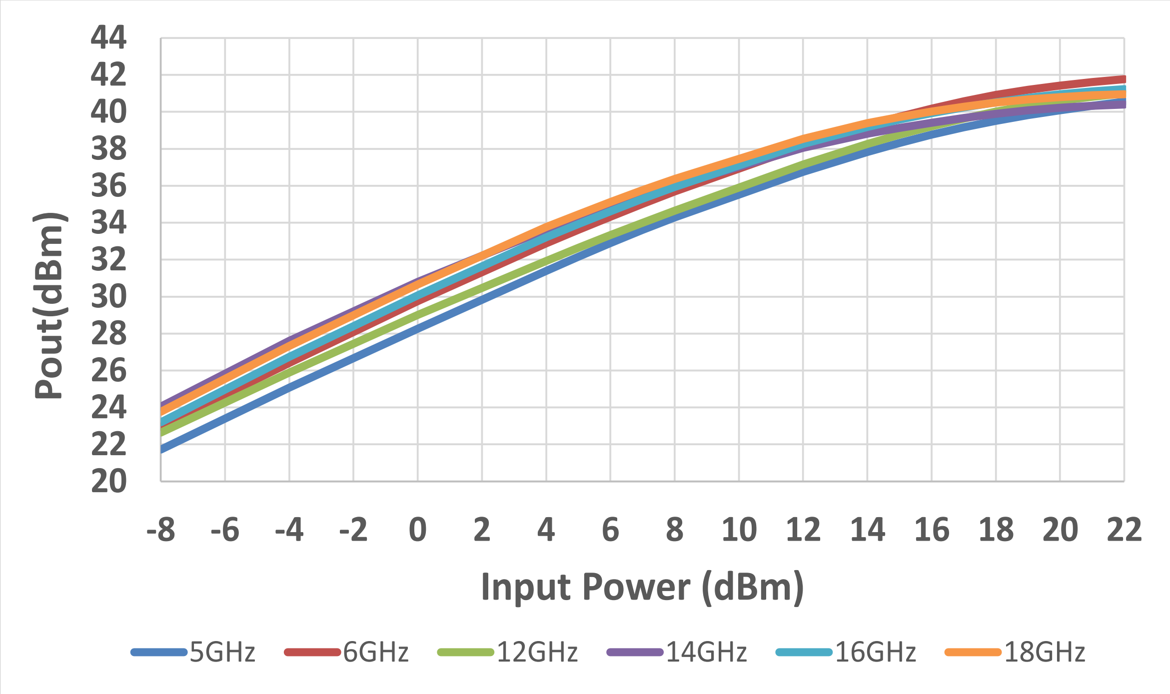
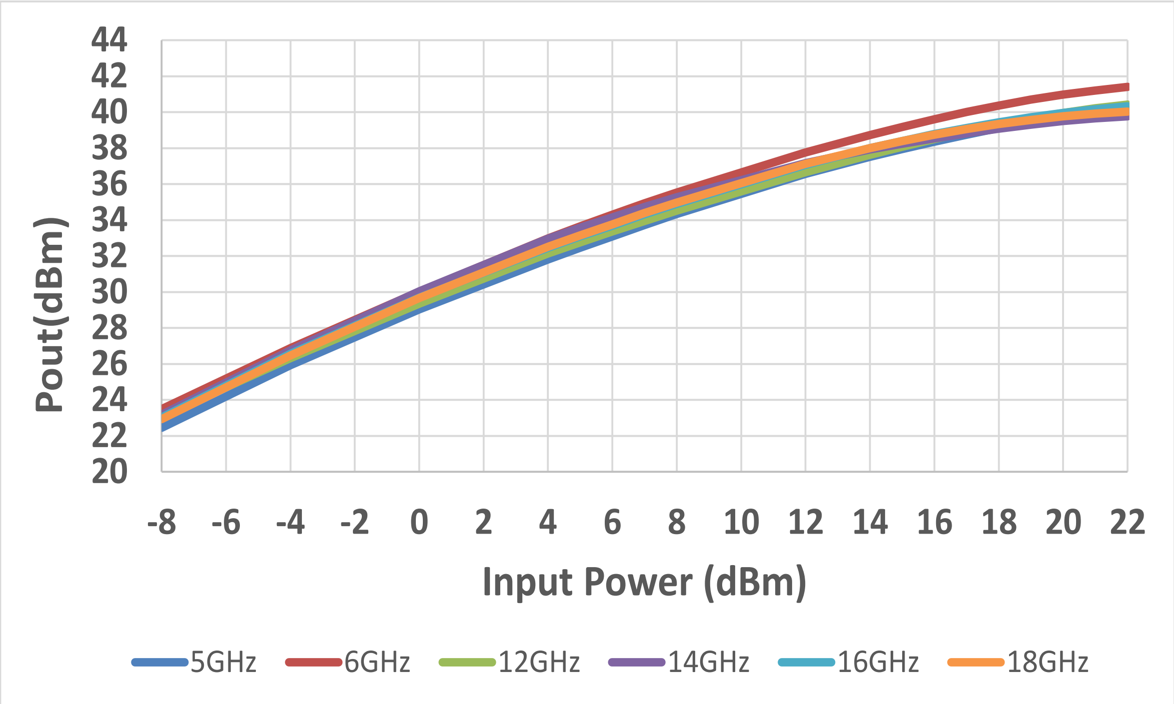
Typical Test Fixture Measurements: Non-linear Performances

CW measurements: Vd = +20V, Idq=350mA
Frequency: 5GHz, 6GHz, 12GHz, 14GHz, 16GHz, 18GHz

Pout versus Input Power Tb.= 25°C



Pout versus Input Power Tb.= 85°C



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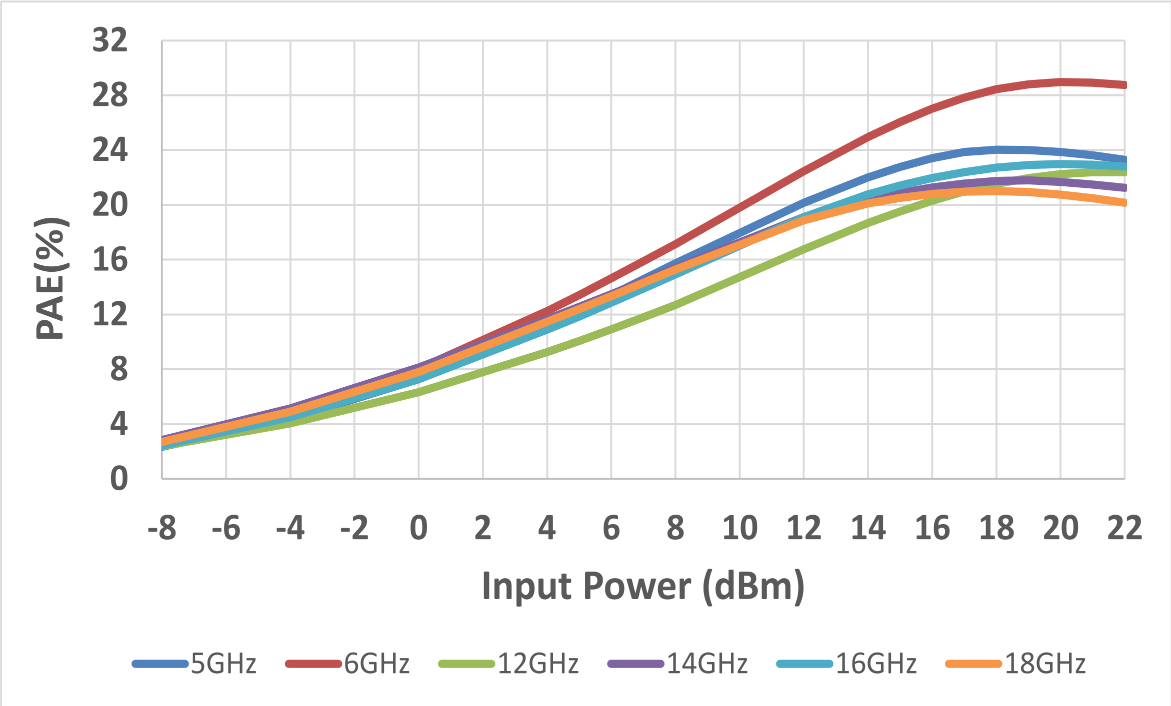
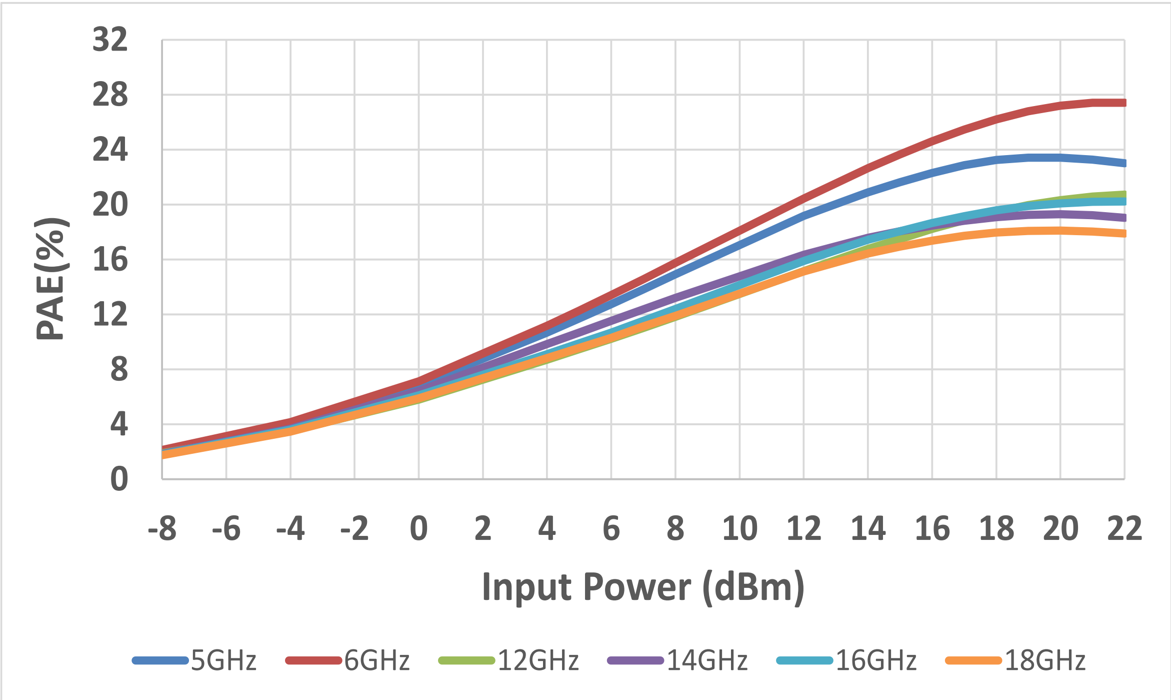
Typical Test Fixture Measurements: Non-linear Performances

CW measurements: Vd = +20V, Idq=350mA
Frequency: 5GHz, 6GHz, 12GHz, 14GHz, 16GHz, 18GHz

Power Added Efficiency versus Input Power Tb.= 25°C



Power Added Efficiency versus Input Power Tb.= 85°C,



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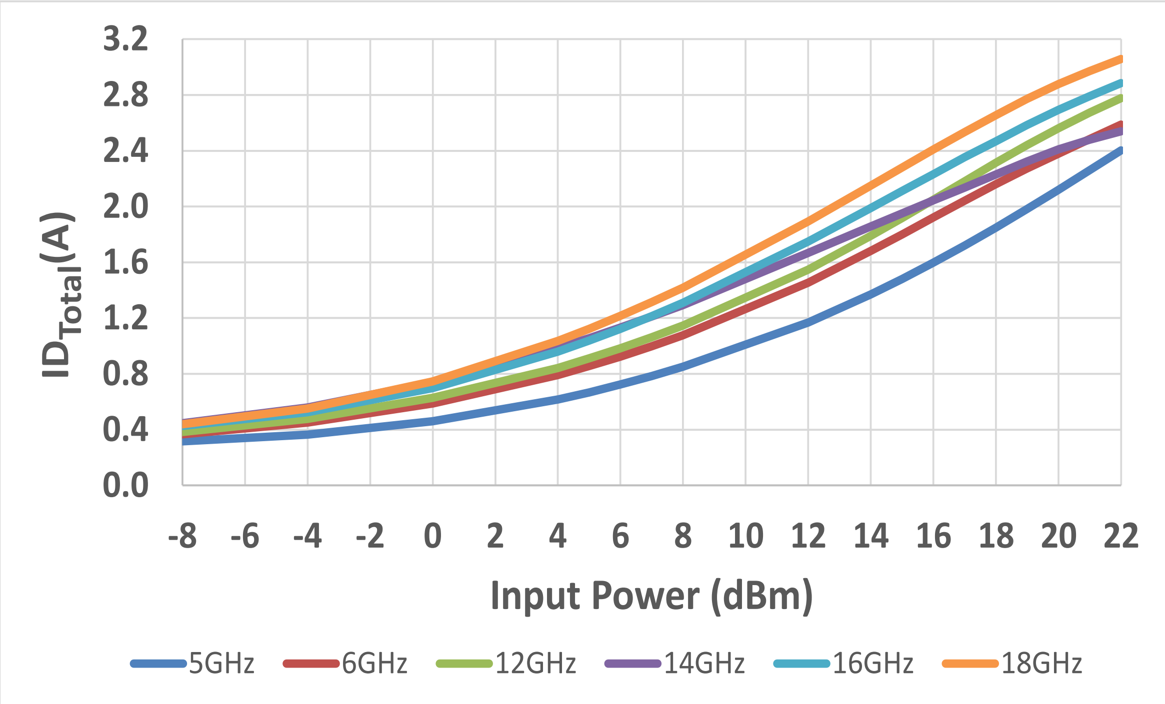
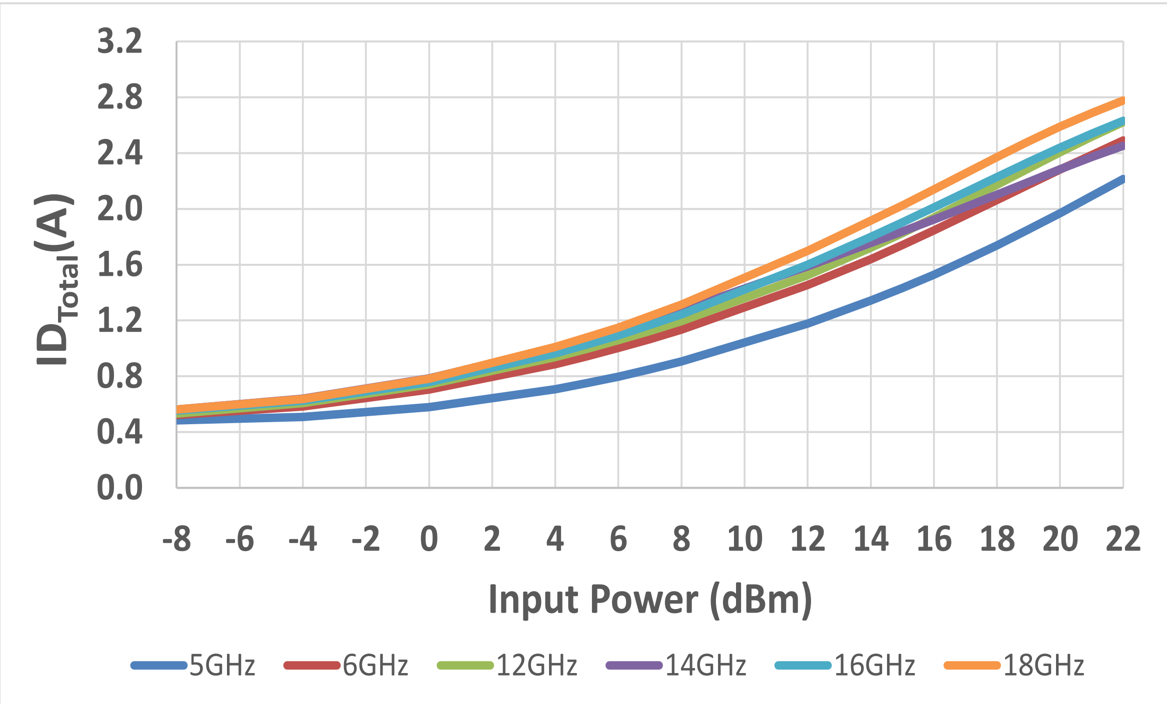
Typical Test Fixture Measurements: Non-linear Performances

CW measurements: Vd = +20V, Idq=350mA
Frequency: 5GHz, 6GHz, 12GHz, 14GHz, 16GHz, 18GHz

Drain current (Total ID) versus Input Power Tb.= 25°C



Drain current (Total ID) versus Input Power Tb.= 85°C



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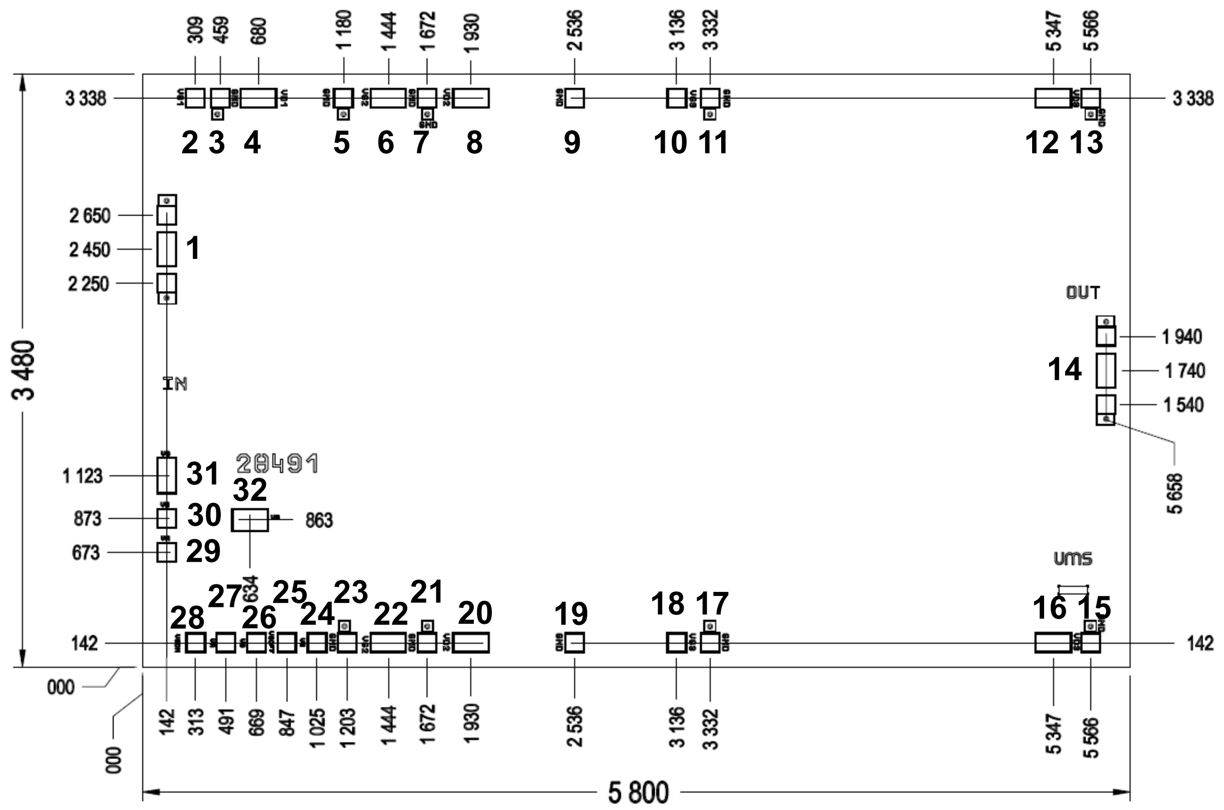
Chip Mechanical data



Chip size = 5800x3480 ±50µm
Chip thickness = 70µm ±10µm

Chip width and length are given with a tolerance of ±50µm
RF pads (1, 14) = 208 x 118µm²

DC pads (2, 3, 5, 7, 9, 10, 11, 13, 15, 17, 18, 19, 21, 23, 24, 25, 26, 27, 29, 30) = 118 x 118µm²
DC pads (4, 8, 12, 16, 20) = 218 x 118µm²
DC pads (6, 22, 31) = 214 x 118µm²

PAD Number	Name	Description
1	IN	Input RF port
3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23	GND	Ground (NC)
2	VG1	Negative supply voltage (gate of stage 1)
6, 22	VG2	Negative supply voltage (gate of stage 2)
10, 18	VG3	Negative supply voltage (gate of stage 3)
4	VD1	Positive supply voltage (drain of stage 1)
8, 20	VD2	Positive supply voltage (drain of stage 2)
12, 16	VD3	Positive supply voltage (drain of stage 3)
14	OUT	Output RF port
24, 25, 26, 27, 28, 29, 30, 31, 32	NC	NC

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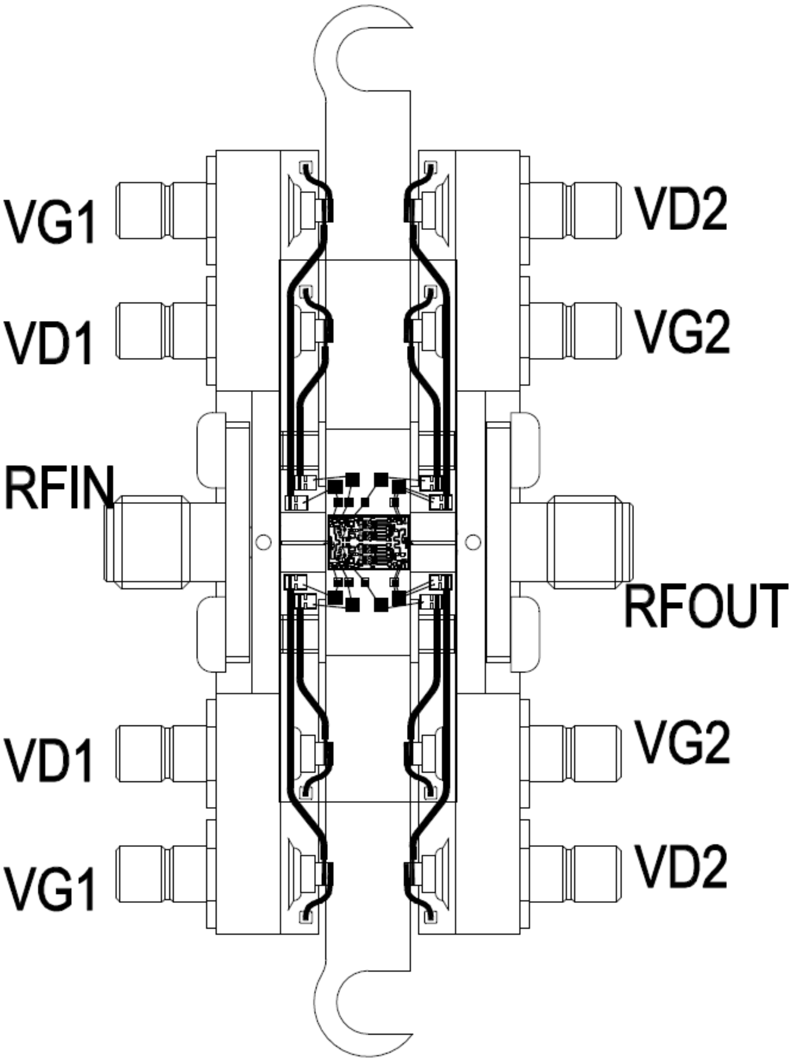
Recommended Test Jig



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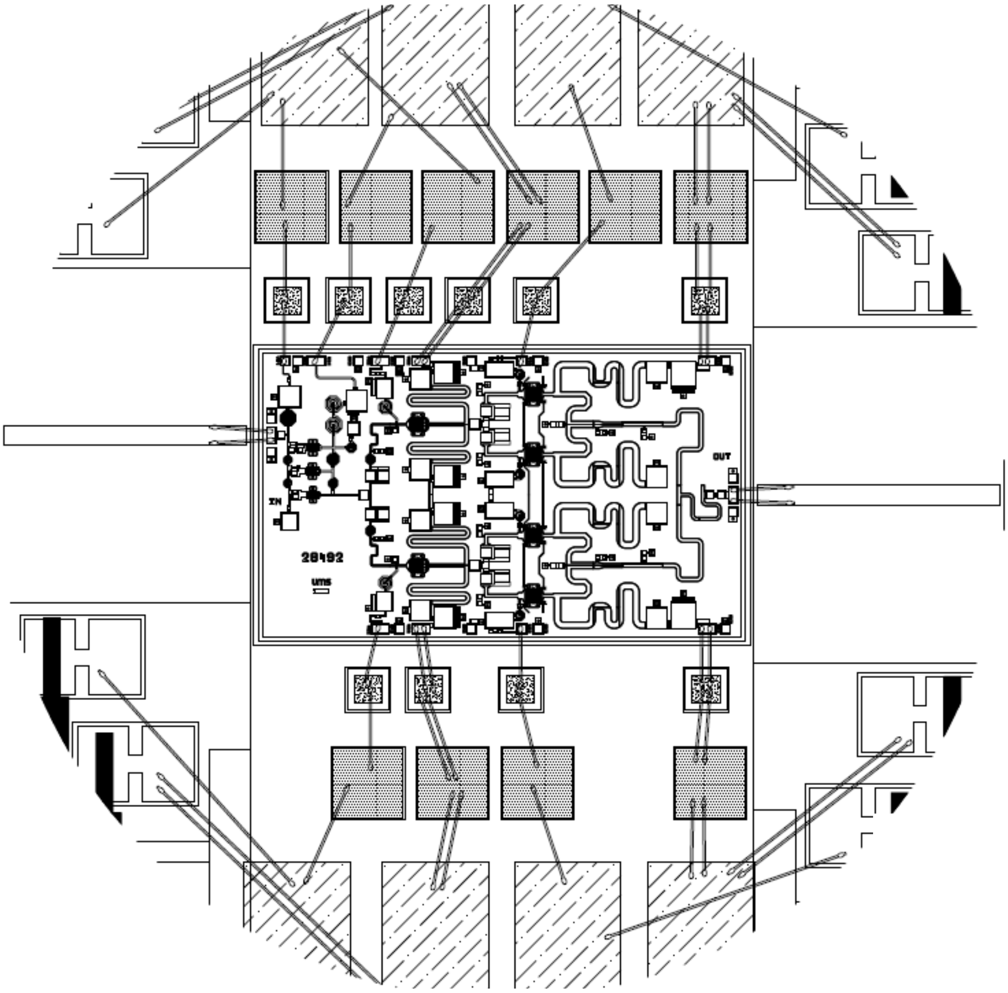
Recommended assembly plan



3 levels of decoupling capacitor have been used:
First level of capacitor is 120pF, second level is 10nF and third level is 100nF.

Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended reflow process assembly

Refer to the application note AN0001 available at https://www.ums-rf.com for die attach.

Ordering Information

Chip form:	CHA7618-99F/00

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