United Monolithic Semiconductors

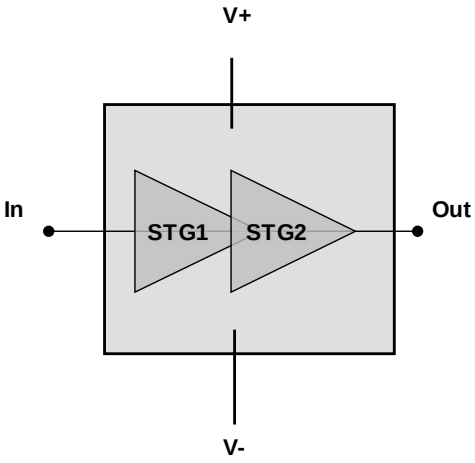
CHA8054-99F

20W X-Band High Power Amplifier

GaN Monolithic Microwave IC

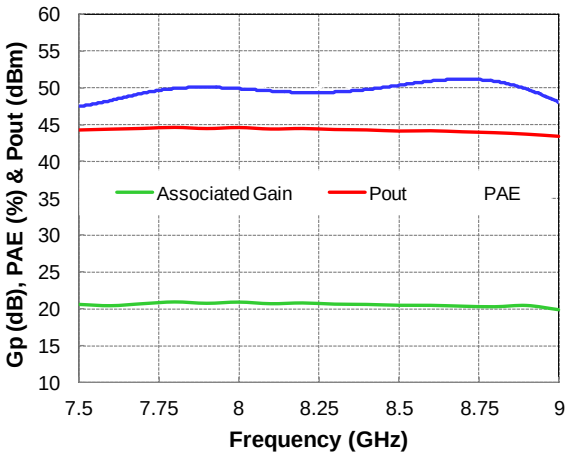
Description

The CHA8054-99F is a two stage High Power Amplifier operating between 7.7 and 8.6GHz and typically providing 20W of saturated output power and 50% of Power Added Efficiency.
It is designed for a wide range of applications, from space, military to commercial communication systems.
The circuit is manufactured with a GaN HEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Main Features

- Frequency range: 7.7-8.6GHz
- High output power: 23W
- High PAE: 50%
- Linear Gain: 27dB
- DC bias: Vd=28Volt @ Idq=0.9A
- Chip size 5.14x4.22x0.1mm
- Available in bare die



Main Electrical Characteristics

Vd = +28V, Idq = 900mA, Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	7.7		8.6	GHz
Gain	Linear Gain		27		dB
Pout	Output Power		23		W
PAE	Associated Power Added Efficiency		50		%

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Electrical Characteristics (CW mode)

Vd = +28V, Idq = 900mA at Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	7.7		8.6	GHz
Gain	Linear Gain		27		dB
Pout	Output Power (Pin=24dBm)		23		W
PAE	Associated Power Added Efficiency (Pin=24dBm)		50		%
Id	Associated current (Pin=24dBm)		2		A
IRL	Input Return Loss		12		dB
ORL	Output Return Loss		10		dB
Idq	Quiescent Current		0.9		A
Vd	Drain Voltage		28		V
Vg	Gate Voltage		-3.3		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	40	V
Pin	Maximum peak input power overdrive	33	dBm
Pdiss	Maximum dissipated power at Tb_{chip} =85°C	80	W
Tj	Junction temperature	230	°C
Ta	Operating temperature range	-40 to +100	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
Vd	Vd1, Vd2	Drain voltage	28	V
Vg	Vg1, Vg2	Gate voltage		
		HPA on (pulsed mode)	-3.3	V
		HPA on (CW mode)	-3.3	V
		HPA off	-8 to -5	V

Bias-up Procedure

1. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5V)
2. Apply Vds bias voltage (Typically: Vd = 28V)
3. Increase Vgs up to quiescent bias drain current Idq (pulsed applied on the gate)
4. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5V)
3. Turn Vds bias voltage to 0V
4. Turn Vgs bias voltage to 0V

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Typical on-wafer Sij parameters (Pulsed mode)

Vd = +28V, Idq = 970mA at Tamb.= +25°C

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
0.50	-0.05	-11.30	-97.67	-71.21	-25.83	102.16	-0.02	-16.83
1.00	-0.13	-22.12	-100.03	-151.34	-24.25	16.39	-0.06	-33.32
1.50	-0.20	-33.12	-109.71	-155.36	-25.05	6.14	-0.04	-49.36
2.00	-0.29	-44.20	-92.02	35.60	-21.92	-5.22	-0.06	-65.35
2.50	-0.38	-55.62	-87.95	-4.96	-18.33	-31.39	-0.04	-80.91
3.00	-0.62	-67.19	-87.91	-118.73	-20.31	-62.48	-0.06	-96.76
3.50	-0.96	-78.99	-85.24	175.26	-19.13	-24.99	-0.09	-112.50
4.00	-1.30	-90.02	-91.69	166.19	-9.69	-48.44	-0.16	-129.13
4.50	-1.65	-101.90	-85.31	152.18	-4.53	-83.22	-0.24	-147.03
5.00	-2.14	-114.94	-80.65	155.72	0.22	-116.14	-0.44	-168.01
5.50	-2.85	-129.39	-76.59	120.57	5.38	-152.80	-0.84	165.58
6.00	-3.84	-146.07	-72.45	67.70	11.06	163.86	-1.80	129.40
6.50	-5.45	-167.37	-68.09	6.51	16.96	109.41	-3.78	77.39
7.00	-8.48	161.80	-62.02	-71.13	22.62	41.83	-6.75	5.15
7.50	-16.11	109.16	-55.40	-164.11	27.14	-45.63	-12.07	-72.24
7.75	-21.83	73.05	-53.73	145.29	27.92	-94.84	-19.12	-80.47
8.00	-21.28	36.28	-52.94	100.71	27.78	-141.81	-18.17	-33.22
8.25	-15.92	8.99	-52.23	59.55	27.47	174.12	-13.87	-33.99
8.50	-11.41	-19.18	-51.08	17.97	27.52	128.46	-12.08	-36.29
8.75	-9.57	-56.13	-50.15	-33.11	27.48	72.03	-9.00	-30.17
9.00	-15.11	-89.87	-51.93	-93.72	24.73	5.53	-4.81	-44.70
9.25	-16.86	-12.21	-56.72	-139.31	19.08	-48.56	-3.43	-64.95
9.50	-9.77	-16.00	-61.83	-169.22	13.14	-87.93	-3.05	-78.34
10.00	-4.94	-41.03	-70.03	166.98	2.20	-147.05	-2.56	-95.53
10.50	-2.94	-61.05	-74.55	149.96	-8.04	165.81	-2.08	-107.95
11.00	-1.92	-76.95	-79.55	92.85	-18.31	126.35	-1.66	-118.64
11.50	-1.33	-89.98	-77.40	-44.71	-29.26	93.69	-1.33	-128.16
12.00	-1.00	-100.98	-69.86	-92.51	-42.53	69.13	-1.07	-136.81
12.50	-0.78	-110.54	-62.82	-143.67	-66.46	149.93	-0.90	-145.00
13.00	-0.64	-118.85	-60.83	179.96	-52.07	-112.32	-0.79	-153.27
13.50	-0.53	-126.51	-60.19	152.02	-47.03	-175.84	-0.70	-159.92
14.00	-0.48	-133.53	-57.48	127.59	-47.84	154.30	-0.63	-166.76
14.50	-0.45	-140.05	-56.63	104.86	-50.77	134.58	-0.61	-173.25
15.00	-0.43	-146.23	-55.49	81.16	-50.74	107.35	-0.60	-179.71
15.50	-0.41	-151.94	-54.80	56.23	-49.40	73.53	-0.58	174.14
16.00	-0.39	-157.53	-53.72	35.16	-50.32	48.20	-0.58	167.78
16.50	-0.40	-162.74	-53.52	6.70	-49.94	14.61	-0.59	161.42
17.00	-0.40	-167.87	-53.94	-9.39	-50.69	-5.36	-0.63	154.84
17.50	-0.40	-172.86	-52.69	-32.50	-48.28	-26.47	-0.62	148.44
18.00	-0.40	-177.83	-53.83	-64.83	-48.27	-67.94	-0.54	141.61
18.50	-0.43	177.34	-55.85	-96.10	-51.19	-108.67	-0.44	18.50
19.00	-0.44	173.02	-59.48	-100.50	-52.86	-113.60	-0.44	19.00
19.50	-0.45	168.55	-59.89	-88.32	-53.84	-121.94	-0.49	19.50
20.00	-0.45	164.20	-57.54	-89.91	-52.32	-123.01	-0.57	20.00

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Device thermal information

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA8054-99F is manufactured (GaN Power HEMT 0.25µm).
The temperature Tb_{chip} is defined as the chip back side temperature. The thermal resistance (Rth_eq) is given for the full circuit, and assumes CW operation mode is given in the table.

Thermal Resistance(1)	Rth_eq	Tb_{chip} =100°C, Vd=28V, Id_drive=1.89A Pin=25dBm Pout=43.95dBm Pdiss=28.4W CW	1.14	°C/W
Junction Temperature	Tj		130	°C
Median Life	T50		$2.8x10^9$	Hrs

(1) Thermal resistance measured to back of the chip

Thermal Resistance(1)	Rth_eq	Tb_{chip} =65°C, Vd=28V, Id_drive=1.97A Pin=24dBm Pout=44.2dBm Pdiss=29.2W CW	1.03	°C/W
Junction Temperature	Tj		98	°C
Median Life	T50		$6.3x10^{10}$	Hrs

(1) Thermal resistance measured to back of the chip

Thermal Resistance(1)	Rth_eq	Tb_{chip} =35°C, Vd=28V, Id_drive=1.974A Pin=24dBm Pout=44.35dBm Pdiss=28.36W CW	0.91	°C/W
Junction Temperature	Tj		63	°C
Median Life	T50		$3.7x10^{12}$	Hrs

(1) Thermal resistance measured to back of the chip

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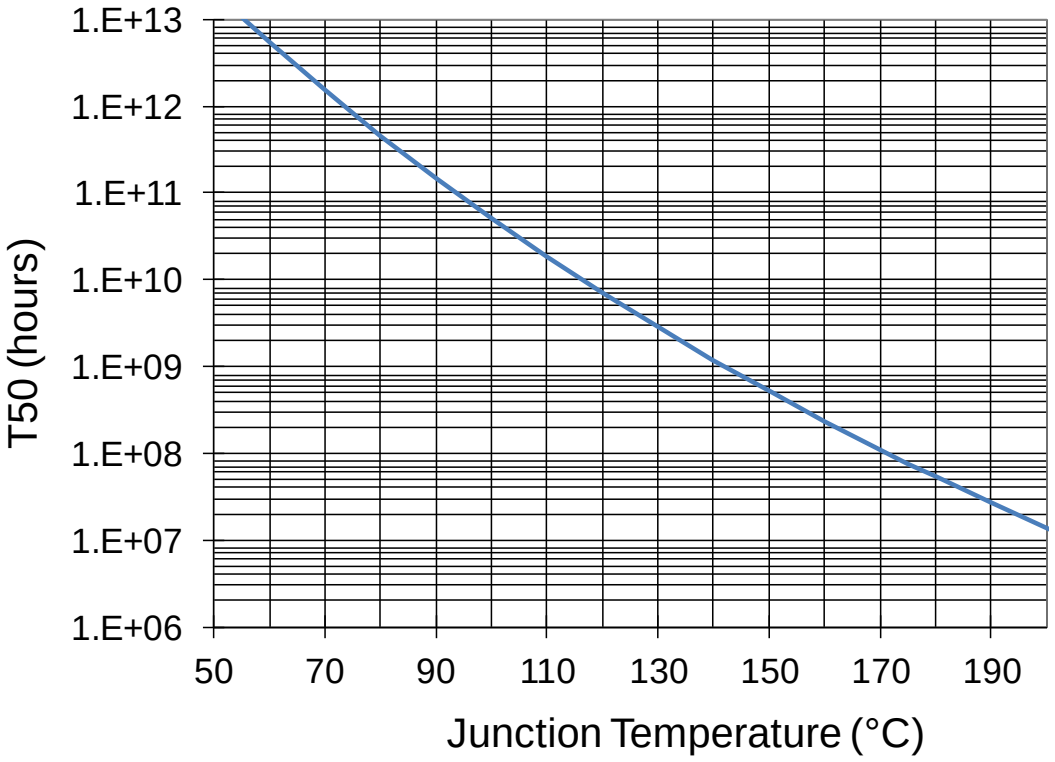
Median Life Time versus Junction Temperature



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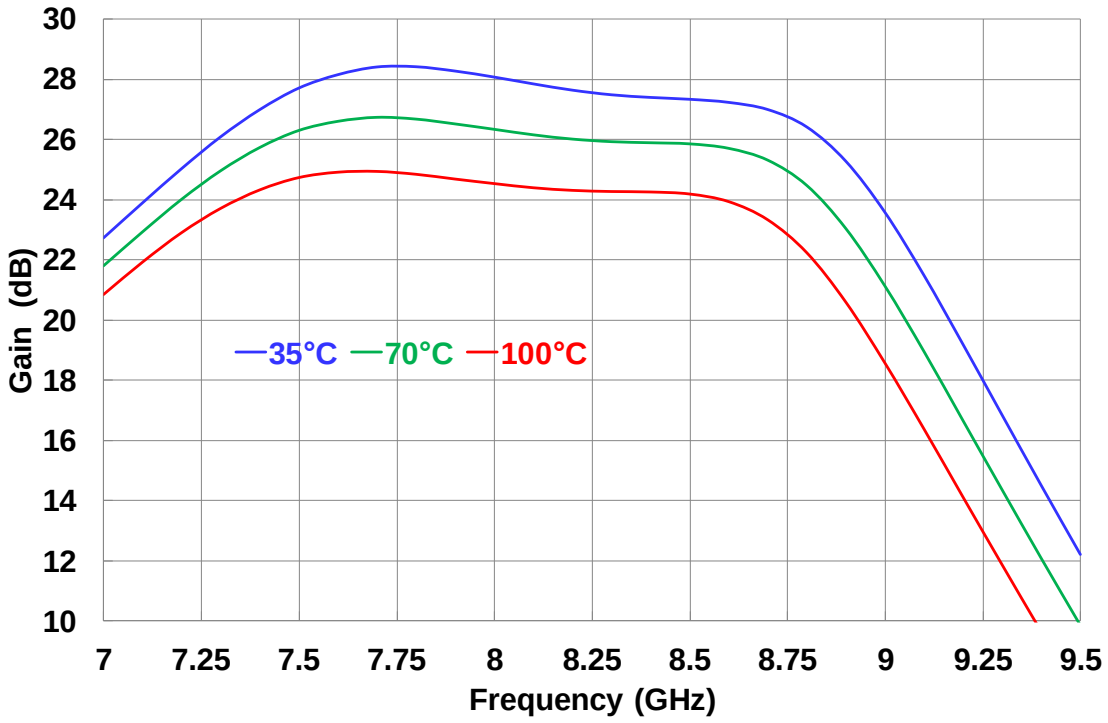
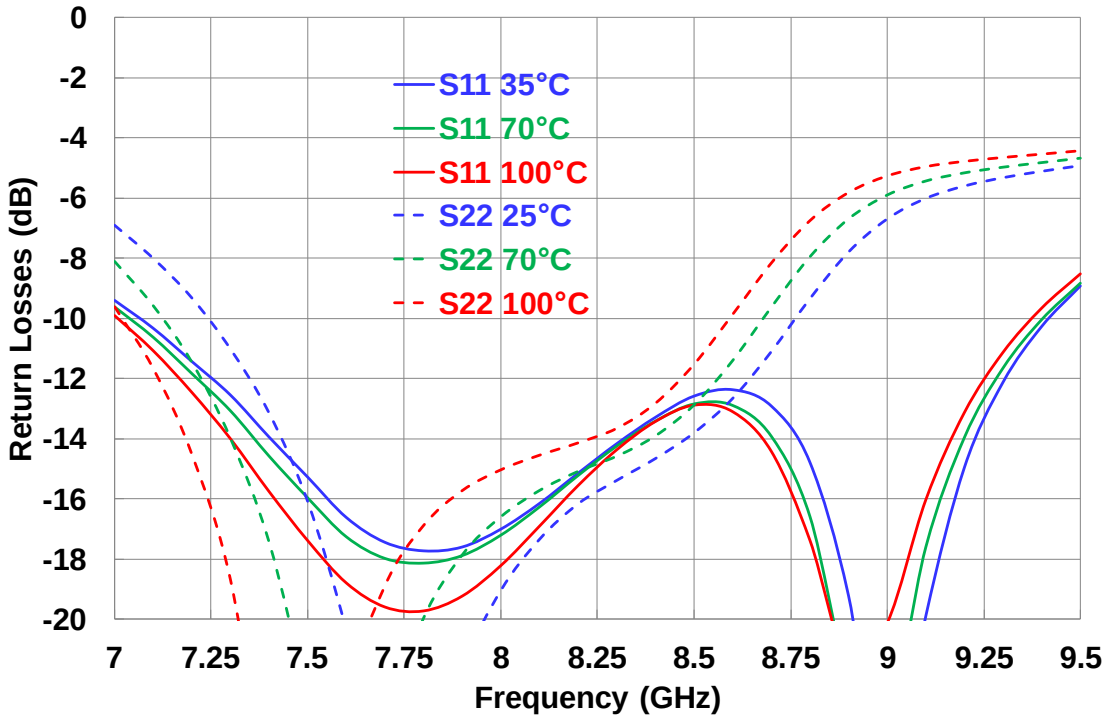
Typical Board Measurements (CW mode)

Vd = +28V, Idq = 900mA at Tamb.= +25°C, CW

Linear Gain versus Frequency (Temp.= +35 & +70 & +100 °C)



Return Losses versus Frequency (Temp.= +35 & +70 & +100 °C)



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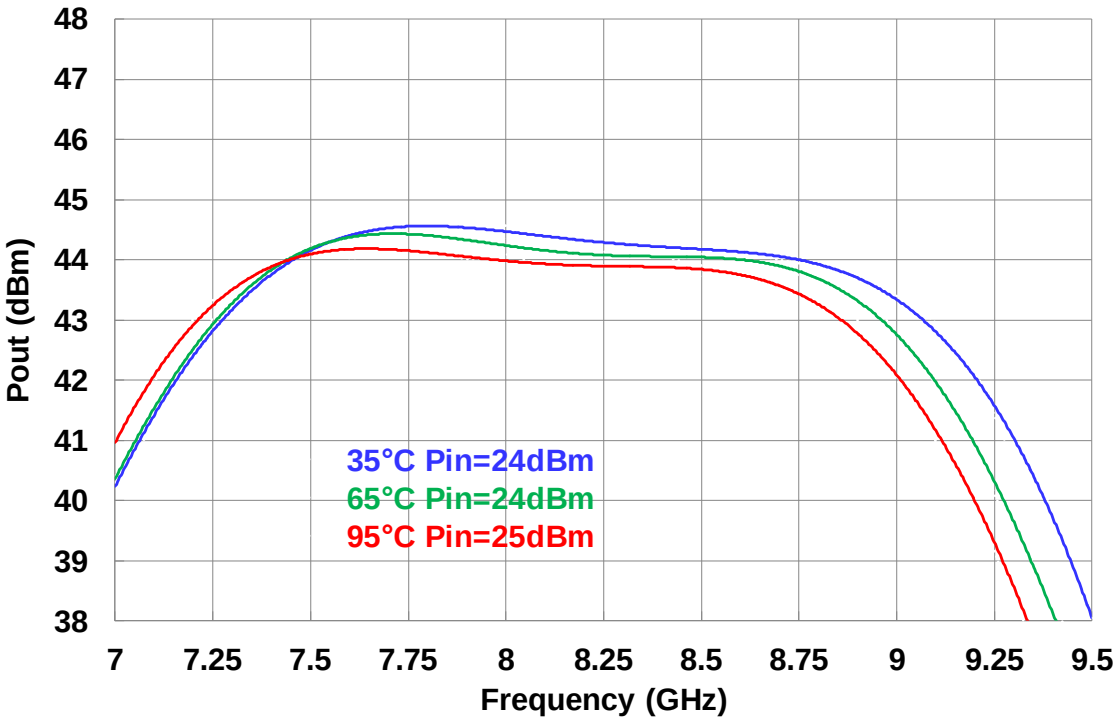
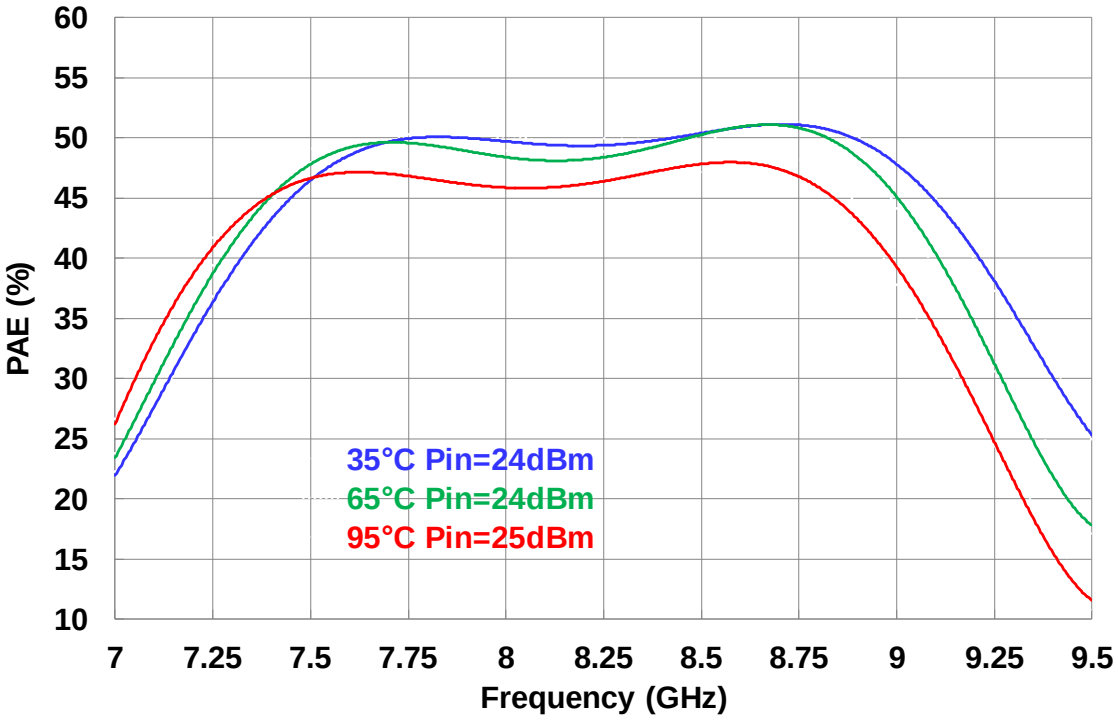
Typical Board Measurements (CW mode)

Vd = +28V, Idq = 900mA at Tamb.= +25°C, CW

Output Power versus Frequency (Temp.= +35 & +65 & +95 °C)



Power Added Efficiency versus Frequency (Temp.= +35 & +65 & +95 °C)



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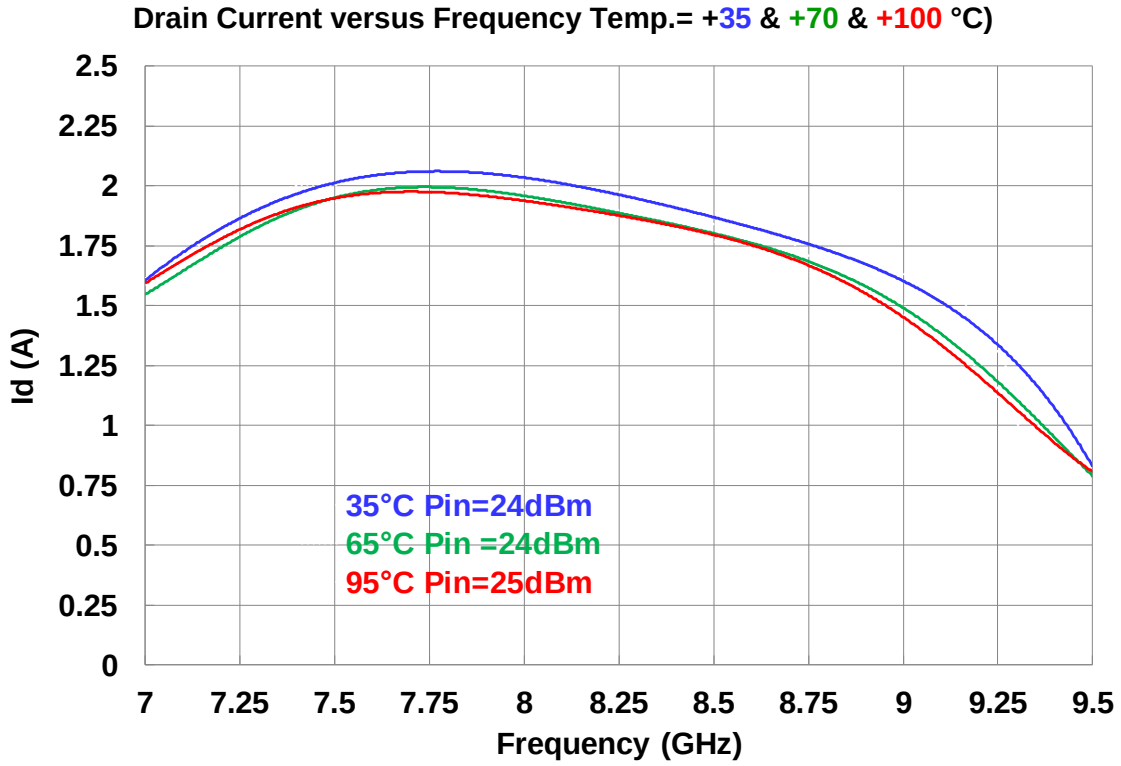
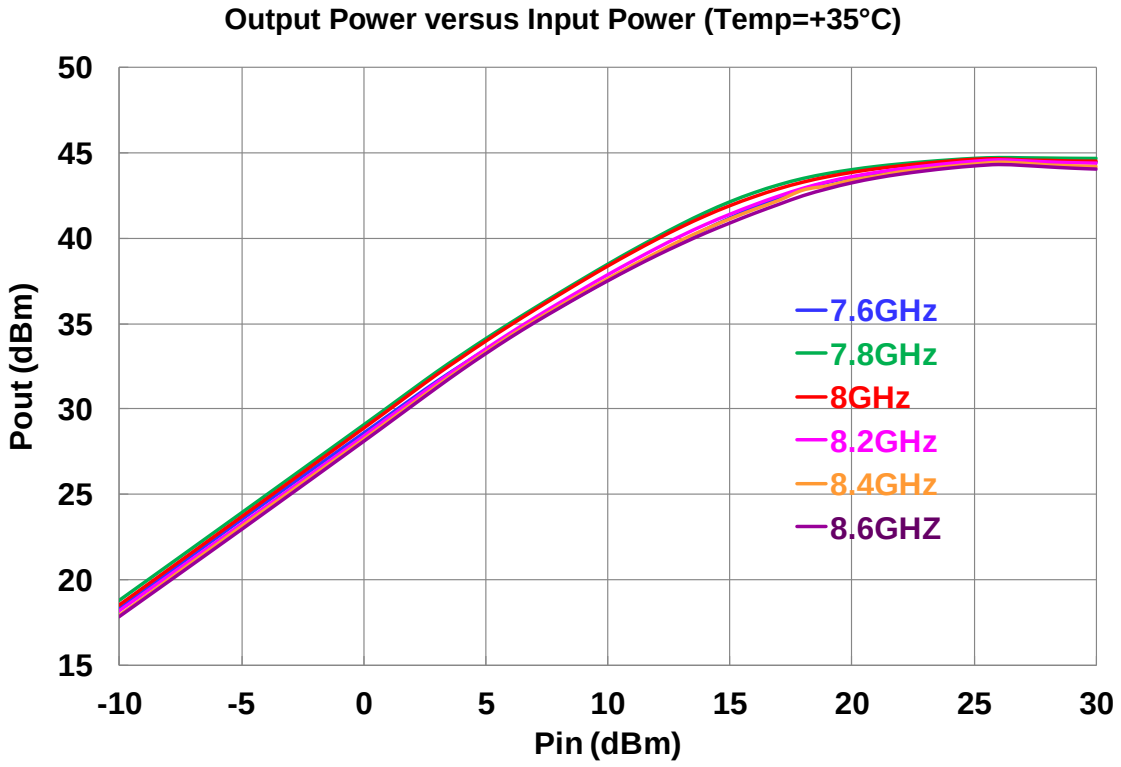
Typical Board Measurements (CW mode)

Vd = +28V, Idq = 900mA at Tamb.= +25°C, CW





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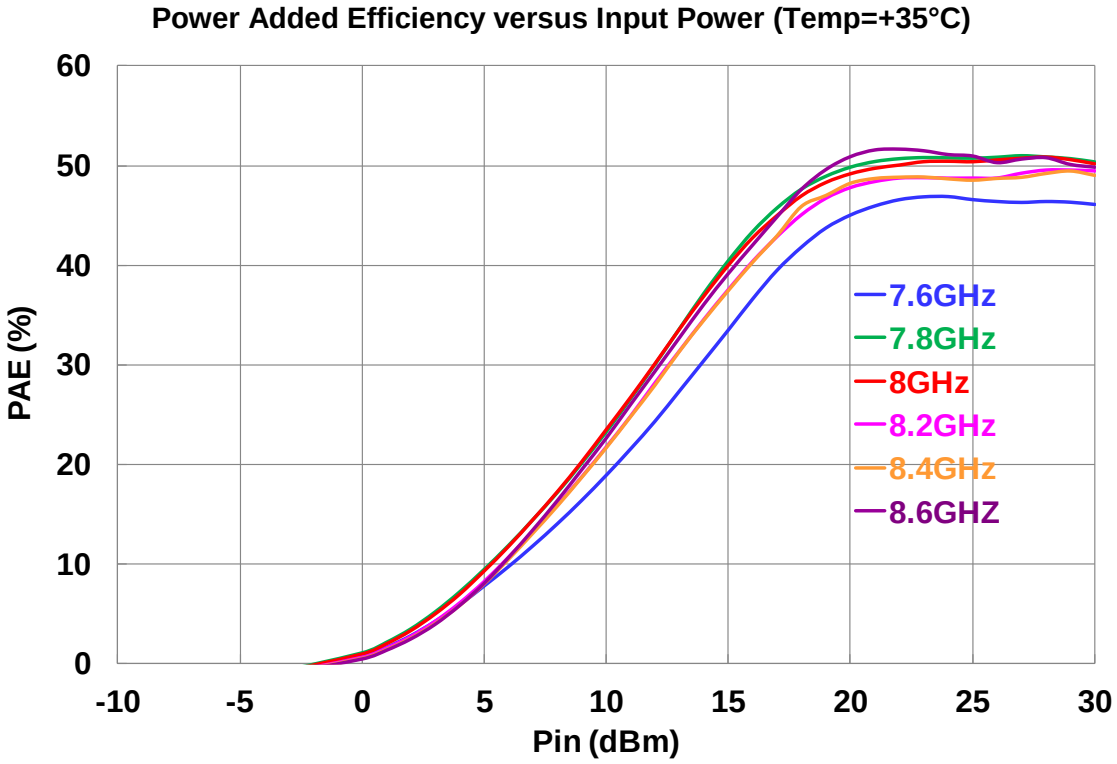
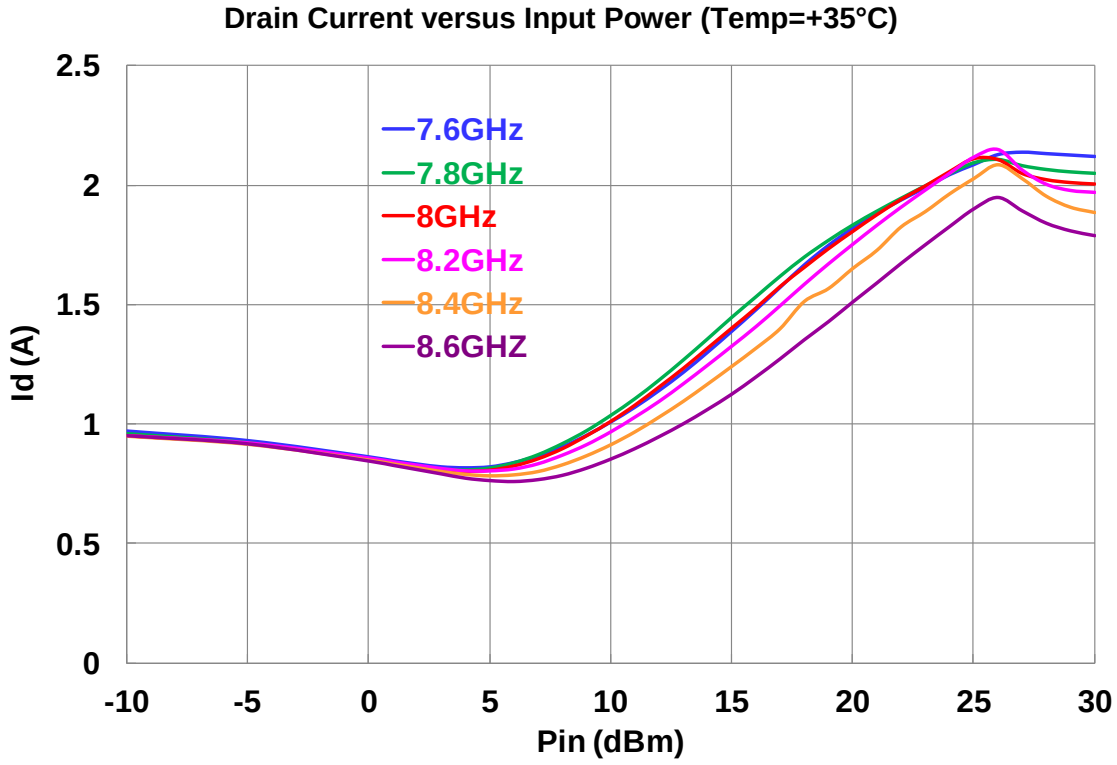
Typical Board Measurements (CW mode)

Vd = +28V, Idq = 900mA at Tamb.= +25°C, CW





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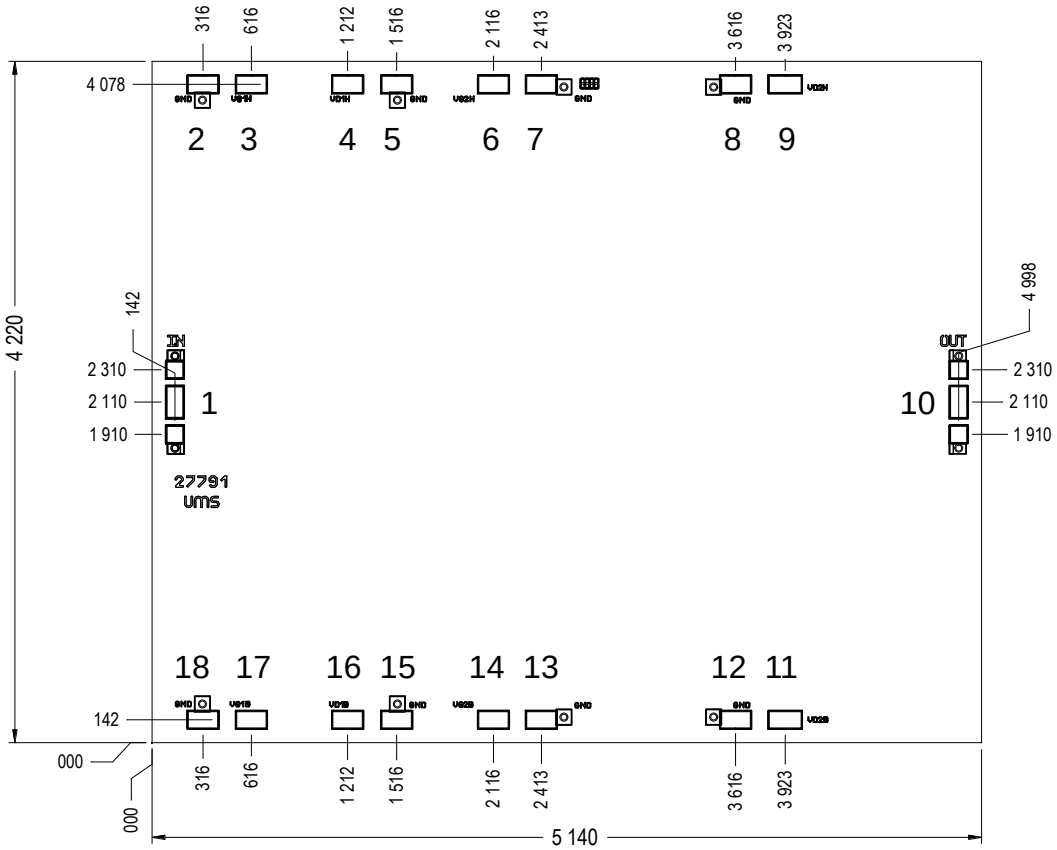
Mechanical data



All dimensions are in micrometers

Chip size = 5140x4220 ±50µm
Chip thickness = 100µm ±10µm
RF pads (1, 10) = 108 x 198µm²
DC pads (2, 3, 5, 7, 8, 11, 12, 13, 14, 15, 16, 17, 18) = 198 x 108µm²
Chip width and length are given with a tolerance of ±50µm

PAD Number	Name	Description
1	IN	Input RF port
2, 5, 7, 8, 12, 13, 15, 18	GND	Ground (NC)
3, 17	VG1	Negative supply voltage (gate of stage 1)
6, 14	VG2	Negative supply voltage (gate of stage 2)
4,16	VD1	Positive supply voltage (drain of stage 1)
9,11	VD2	Positive supply voltage (drain of stage 2)
10	OUT	Output RF port

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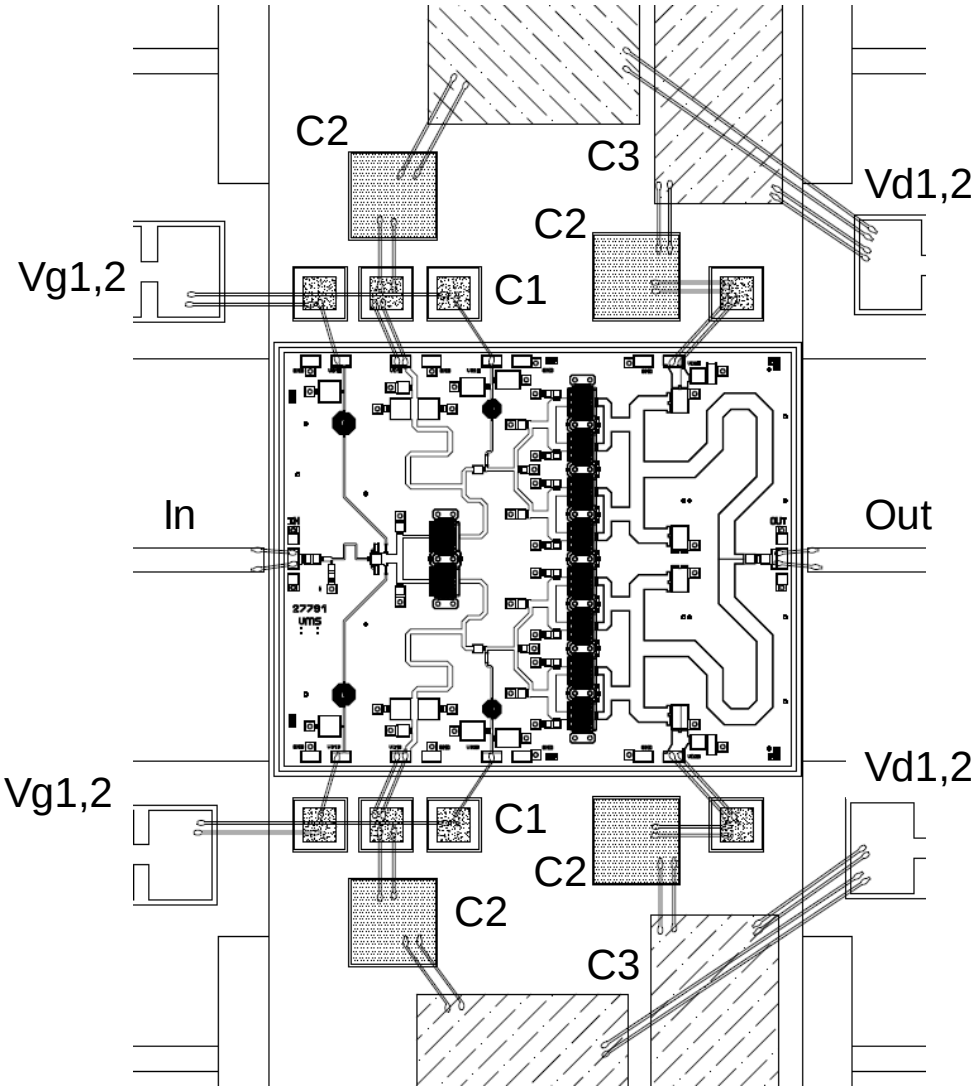
Recommended assembly plan in CW mode



Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Bill of Materials

Label	Value	Description
C1	RF	Capa 120pF ±10% 50V
C2	RF	Capa 10nF ±20% 50V
C3	RF	Capa 68nF ±20% 50V

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Recommended circuit bonding table

Label	Type	Decoupling	Comment
RFIN	RF	Not required	Inductance (Lbonding) = 0.3nH 2 gold wires with diameter of 25 µm (500µm)
RFOUT	RF	Not required	Inductance (Lbonding) = 0.3nH 2 gold wires with diameter of 25 µm (500µm)
Vd	DC	120pF, 10nF & 68nF	Inductance ≤ 1nH (mainly for first decoupling level) ⇒1.2mm length wires with a diameter of 25 µm
Vg	DC	120pF & 10nF & 68nF (for CW mode)	Inductance ≤ 1nH (mainly for first decoupling level) ⇒1.2mm length wires with a diameter of 25 µm

- The overall biasing network proposed is compliant with CW mode and with a DC pulse applied on the gate; it can be integrated differently depending on module technology and on modulation characteristics (gate or drain pulse, pulse length and Duty Cycle). However, the first decoupling level should always be kept, the second one should be adapted to modulator characteristics and the third one should be kept and optimized on the non-modulated ports.

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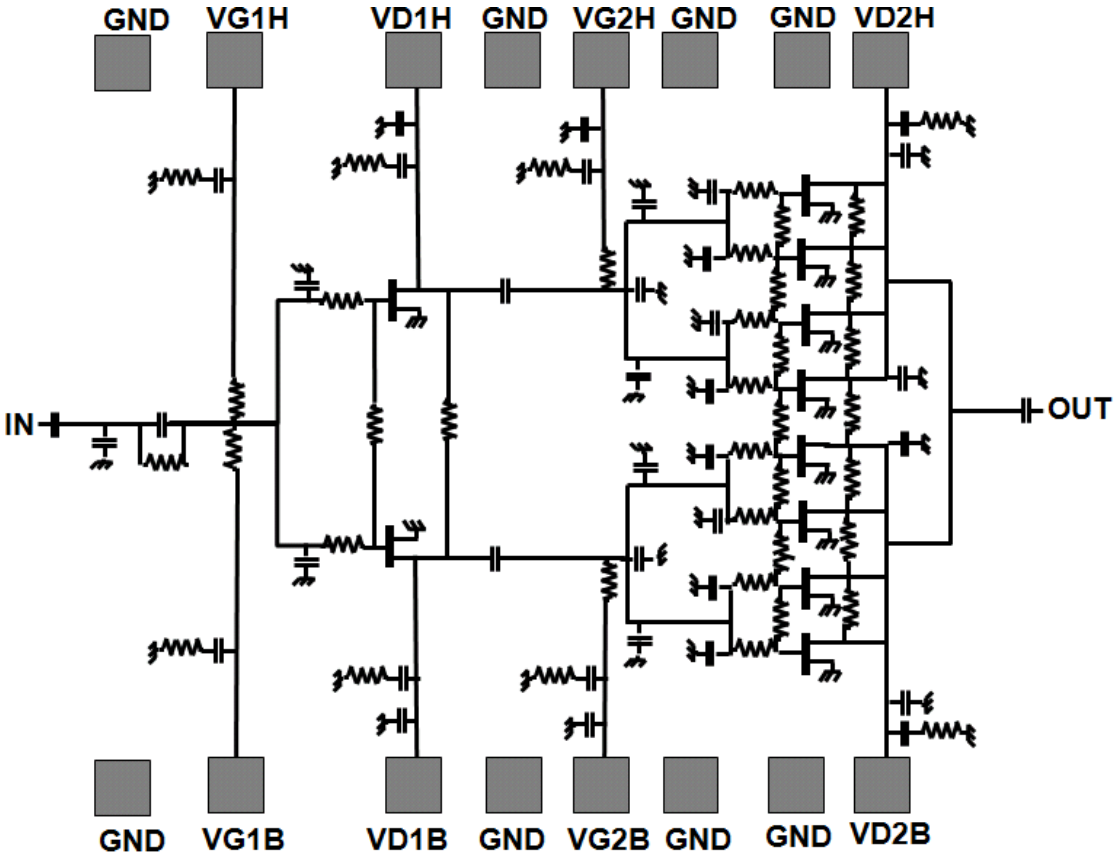
DC Schematic



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Note

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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Ordering Information

Chip form:	CHA8054-99F/00

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