

15W X Band High Power Amplifier

GaN Monolithic Microwave IC

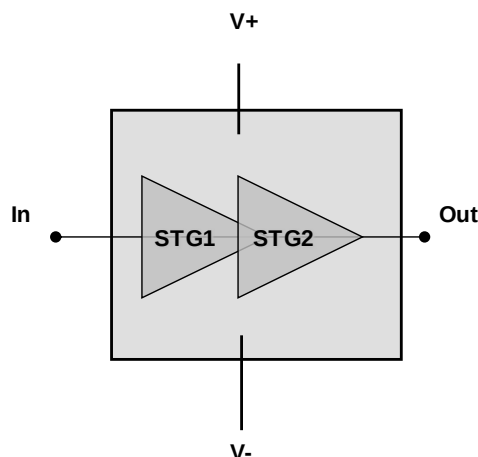
Description

The CHA8610-99F is a two stage High Power Amplifier operating between 8.5 and 11GHz and providing typically 15W of saturated output power and 40% of Power Added Efficiency.

It is designed for a wide range of applications, from military to commercial communication systems.

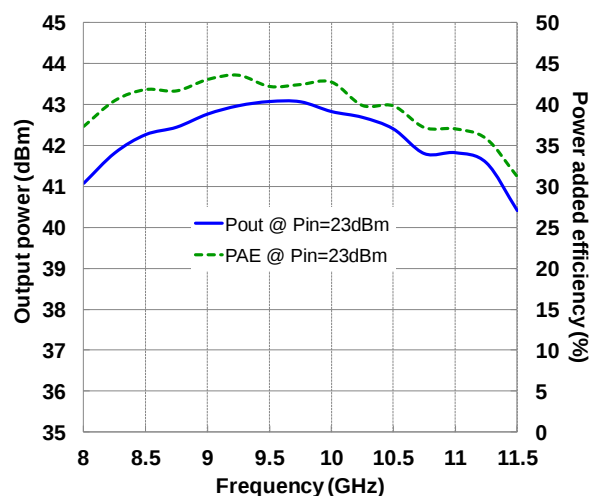
The circuit is manufactured with a pHEMT process, 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Main Features

- Frequency range: 8.5-11GHz
- High output power: 15W
- High PAE: 40%
- Linear Gain: 24dB
- DC bias: Vd=30Volt @Id=0.68A
- Chip size 5.08x2.75x0.1mm
- Available in bare die



Pout and PAE versus frequency for Pulsed mode

Main Electrical Characteristics (Pulsed mode)

Tamb.= +25°C; Vd = +30V Pulse width = 25 μ s Duty cycle = 10%

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	8.5		11	GHz
Gain	Linear Gain		24		dB
Pout	Output Power		15		W
PAE	Associated Power Added Efficiency.		40		%

Electrical Characteristics (Pulsed mode)

Tamb.= +25°C, Vd = +30V Pulse width = 25µs Duty cycle = 10%

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	8.5		11	GHz
Gain	Linear Gain		24		dB
Pout	Output Power (Pin=23dBm)		15		W
PAE	Associated Power Added Efficiency (Pin=23dBm)		40		%
Id	Associated current (Pin=23dBm)		1.5		A
IRL	Input Return Loss		10		dB
ORL	Output Return Loss		8		dB
Idq	Quiescent Current		0.68		A
Vd	Drain Voltage		30		V
Vg	Gate Voltage		-3.2		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

Electrical Characteristics (CW mode)

Tamb.= +25°C, Vd = +30V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	8.5		11	GHz
Gain	Linear Gain		23		dB
Pout	Output Power (Pin=24dBm)		14		W
PAE	Associated Power Added Efficiency (Pin=24dBm)		37.5		%
Id	Associated current (Pin=24dBm)		1.3		A
IRL	Input Return Loss		10		dB
ORL	Output Return Loss		8		dB
Idq	Quiescent Current		0.45		A
Vd	Drain Voltage		30		V
Vg	Gate Voltage		-3.5		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

Absolute Maximum Ratings ⁽¹⁾T_{amb.} = +25°C

Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	35V	V
P _{in}	Maximum peak input power overdrive	35	dBm
P _{diss}	Maximum dissipated power	55	W
T _j	Junction temperature	230	°C
T _a	Operating temperature range	-40 to +85	°C
T _{stg}	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above any one of these parameters may cause permanent damage.

Typical Bias ConditionsT_{amb.} = +25°C

Symbol	Pad N°	Parameter	Values	Unit
V _d	V _{d1} , V _{d2}	Drain voltage	25, 30	V
V _g	V _{g1} , V _{g2}	Gate voltage		
		HPA on (pulsed mode)	-3.2	V
		HPA on (CW mode)	-3.5	V
		HPA off	-8 to -5	V

Bias-up Procedure

1. Bias HPA gate voltage at V_g close to V_{pinch-off} (Typically: V_g ≈ -5V)
2. Apply V_{ds} bias voltage (Typically: V_d = 25V)
3. Increase slowly V_{gs} up to quiescent bias drain current I_{dq} (pulsed applied on the gate)
4. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Bias HPA gate voltage at V_g close to V_{pinch-off} (Typically: V_g ≈ -5V)
3. Turn V_{ds} bias voltage to 0V
4. Turn V_{gs} bias voltage to 0V

Typical on-wafer Sij parameters (Pulsed mode)

Tamb.= +25°C, Vd = +30V, Id = 680mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2.0	-1.03	-130.86	-84.60	-148.64	-41.86	-140.08	-0.19	-136.88
2.5	-1.49	-162.82	-76.54	91.66	-55.58	-170.00	-0.29	-171.20
3.0	-2.00	165.57	-77.59	72.93	-55.42	-118.62	-0.41	154.65
3.5	-2.58	134.24	-76.43	14.56	-45.17	-101.02	-0.50	120.59
4.0	-3.25	103.01	-75.27	-10.59	-36.73	-175.24	-0.62	86.30
4.5	-3.87	71.59	-73.10	-12.83	-42.81	152.80	-0.53	51.55
5.0	-4.72	40.20	-70.30	-44.98	-31.13	-177.22	-0.55	16.06
5.5	-5.83	8.73	-66.72	-82.15	-20.04	140.51	-0.59	-20.94
6.0	-7.46	-23.07	-68.60	-117.36	-9.91	88.62	-0.72	-60.44
6.5	-10.05	-54.20	-66.44	-152.64	0.89	26.18	-1.04	-104.04
7.0	-14.88	-71.93	-63.47	-178.69	13.09	-59.53	-2.12	-155.54
7.5	-15.52	-62.98	-61.98	84.46	21.90	171.10	-6.18	150.67
8.0	-13.04	-69.14	-60.38	-59.52	24.51	51.58	-12.88	99.10
8.5	-9.64	-111.20	-55.52	-161.77	26.45	-59.96	-18.37	-164.62
9.0	-10.83	-175.05	-54.69	108.03	26.96	-172.37	-8.79	125.57
9.5	-17.16	112.88	-60.27	14.46	25.95	81.49	-8.79	50.35
10.0	-21.00	-26.53	-64.42	-113.62	24.45	-17.23	-12.72	-28.35
10.5	-12.57	-108.09	-57.33	131.56	23.58	-114.34	-15.60	-127.95
11.0	-7.02	-174.86	-53.30	65.97	23.48	138.36	-12.09	151.12
11.5	-6.84	107.10	-54.93	7.46	21.87	9.09	-7.70	99.16
12.0	-10.98	108.86	-54.86	21.04	15.60	-133.30	-4.29	47.48
12.5	-3.40	51.85	-48.18	-36.18	2.80	95.09	-2.96	0.10
13.0	-3.29	-8.75	-48.85	-98.34	-12.83	1.03	-2.21	-40.14
13.5	-3.96	-54.77	-52.25	-137.54	-27.89	-68.80	-1.69	-77.61
14.0	-4.55	-93.88	-54.49	175.95	-42.29	-127.97	-1.34	-113.03
14.5	-4.94	-129.70	-58.08	159.62	-55.62	-168.12	-1.11	-147.21
15.0	-5.27	-162.36	-63.64	123.65	-69.56	-178.62	-0.95	-179.96
15.5	-5.61	165.77	-77.61	60.54	-66.15	-139.01	-0.85	147.98
16.0	-5.84	135.54	-74.57	-146.47	-72.47	-153.41	-0.77	116.58
16.5	-6.11	105.78	-64.77	-156.85	-62.71	-159.07	-0.72	85.92
17.0	-6.34	75.82	-60.45	-170.95	-60.45	-175.29	-0.69	55.89
17.5	-6.56	47.25	-57.49	159.51	-57.34	167.51	-0.67	26.71
18.0	-6.90	18.84	-55.51	139.32	-55.52	134.52	-0.66	-2.23
18.5	-7.18	-9.59	-54.89	115.46	-54.42	113.65	-0.64	-30.90
19.0	-7.59	-37.61	-51.56	103.31	-51.75	102.60	-0.64	-59.43
19.5	-8.14	-66.11	-47.44	69.64	-47.27	68.46	-0.65	-87.78
20.0	-8.76	-95.81	-46.38	14.77	-46.36	15.13	-0.68	-116.54

Device thermal information

The device thermal performances below are based on UMS rules to evaluate the junction temperature.

This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA8610-99F is manufactured (GaN Power HEMT 0.25 μ m).

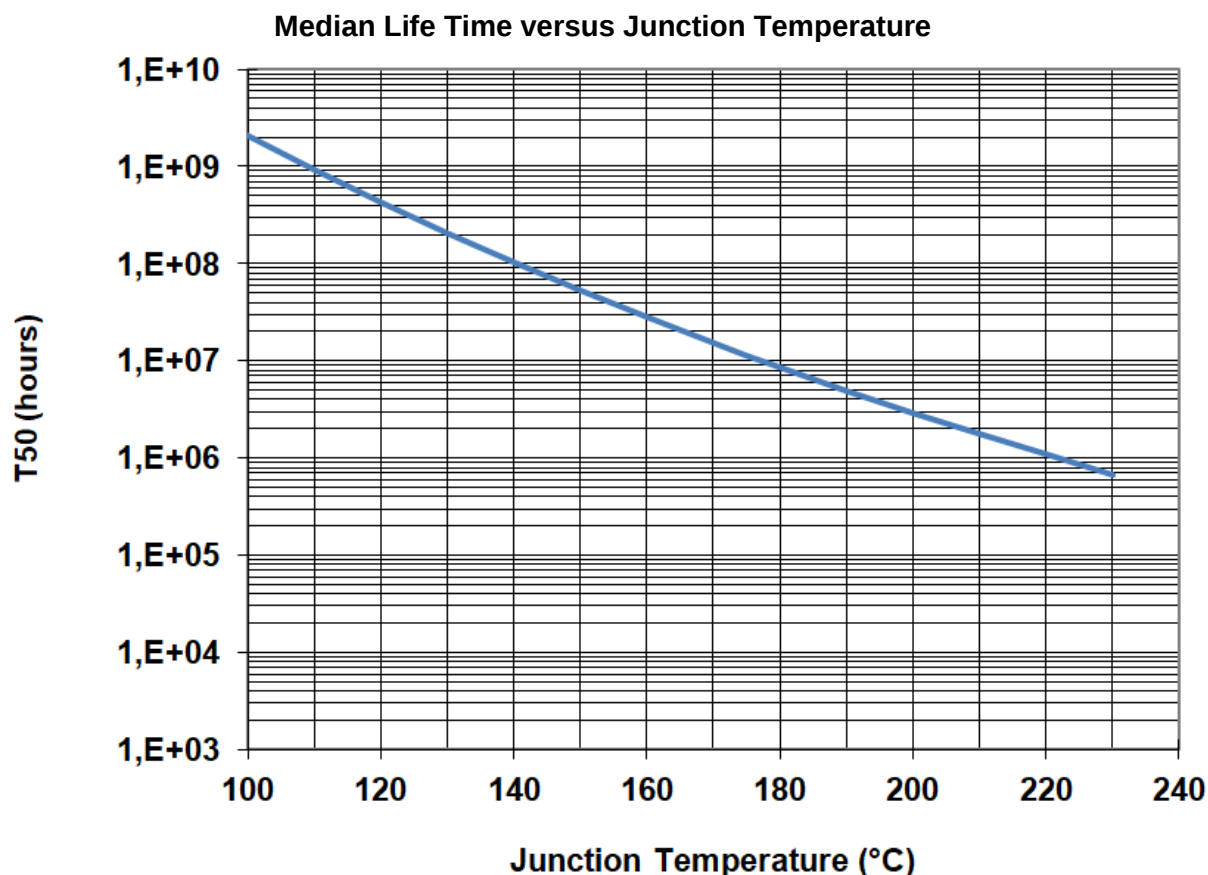
The temperature $T_{b_{chip}}$ is defined as the chip back side temperature and $T_{b_{carrier}}$ is defined as the carrier back side temperature. The thermal resistance (R_{th_eq}) is given for the full circuit, and assumes CW and pulsed operation mode are given in the table.

Thermal Resistance ⁽¹⁾	R_{th_eq}	$T_{b_{chip}} = 85^{\circ}\text{C}$, $V_d = 30\text{V}$, $I_{d_drive} = 1.3\text{A}$	2.6	$^{\circ}\text{C/W}$
Junction Temperature	T_j	$P_{in} = 24\text{dBm}$ $P_{out} = 40.7\text{dBm}$	153	$^{\circ}\text{C}$
Median Life	T50	$P_{diss} = 26\text{W}$ CW	5×10^7	Hrs

⁽¹⁾ Thermal resistance measured to back of the chip

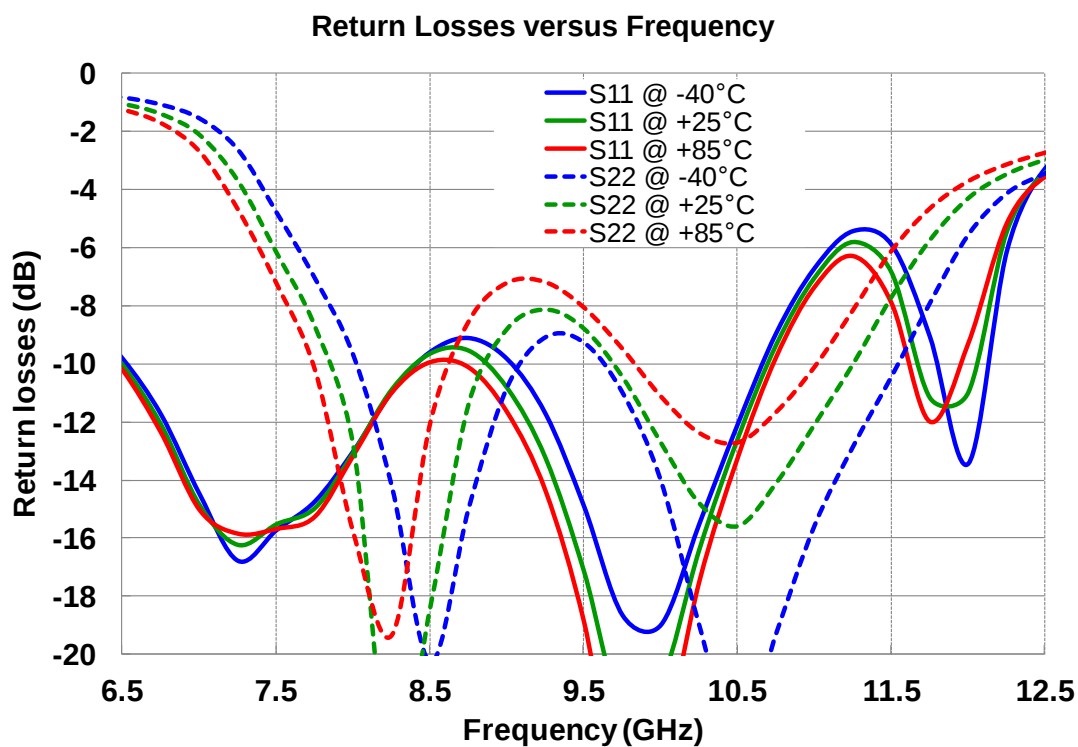
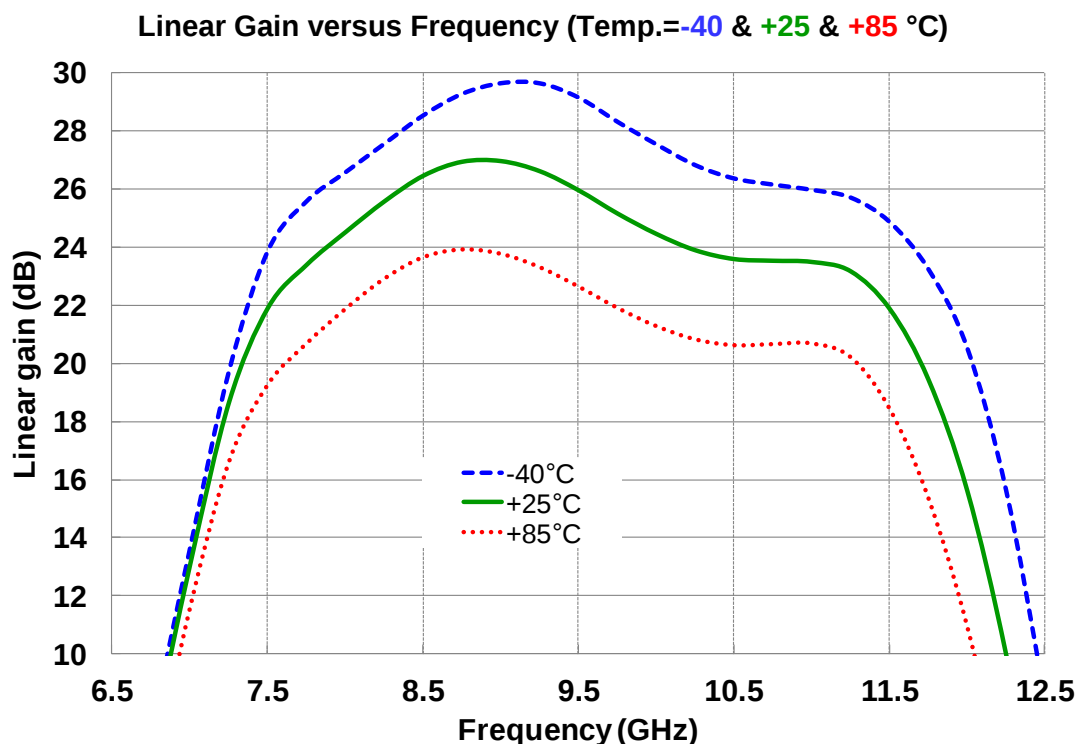
Thermal Resistance ⁽²⁾	R_{th_eq}	$T_{b_{carrier}} = 85^{\circ}\text{C}$, $V_d = 30\text{V}$, $I_{d_drive} = 1.35\text{A}$	3.4	$^{\circ}\text{C/W}$
Junction Temperature	T_j	$P_{in} = 24\text{dBm}$ $P_{out} = 40.7\text{dBm}$	175	$^{\circ}\text{C}$
Median Life	T50	$P_{diss} = 26\text{W}$ CW	1×10^7	Hrs

⁽²⁾ Thermal resistance measured to back of carrier plate (20 μ m Au/Sn soldering + 1.4mm Cu/Mo/Cu). Thermal analysis is highly recommended, more details are available on request.



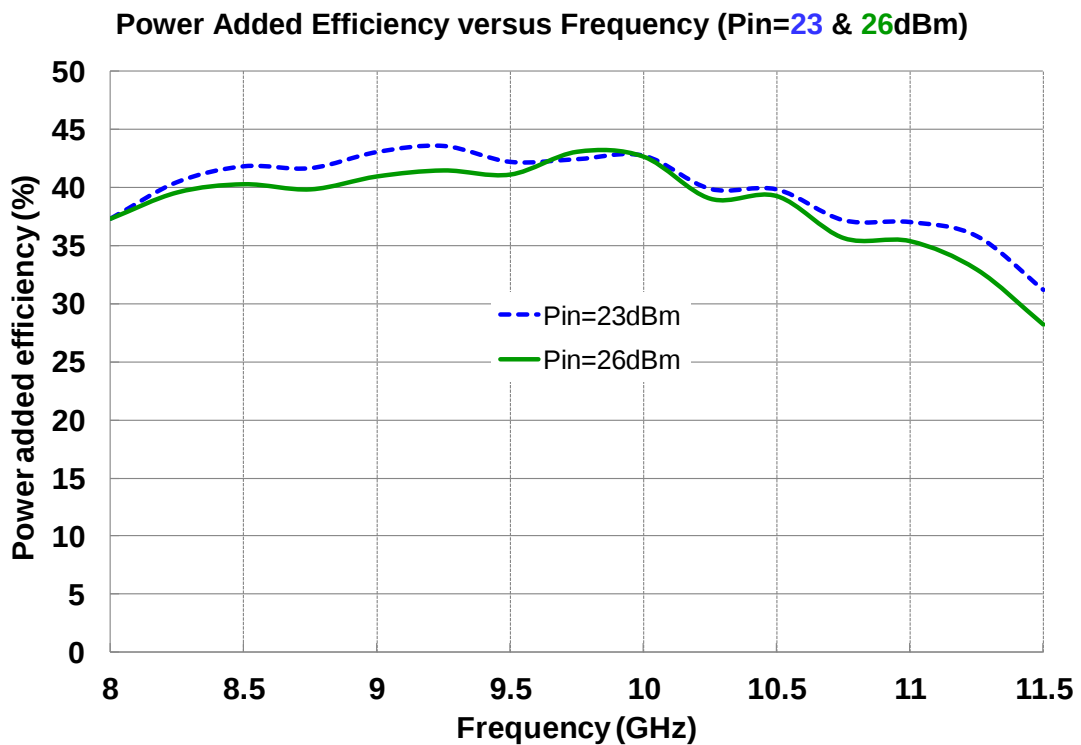
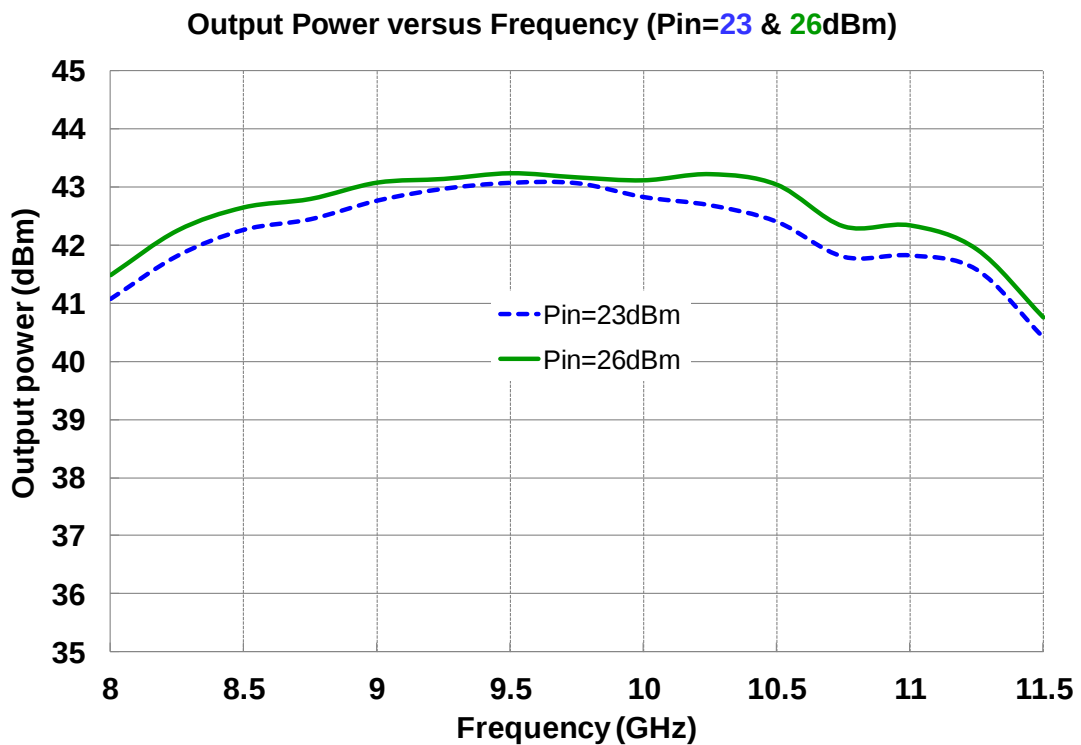
Typical Board Measurements (Pulsed mode)

Vd = +30V, Idq = 680mA at Tamb=+25°C, Pulse width=25μs, Duty cycle =10%



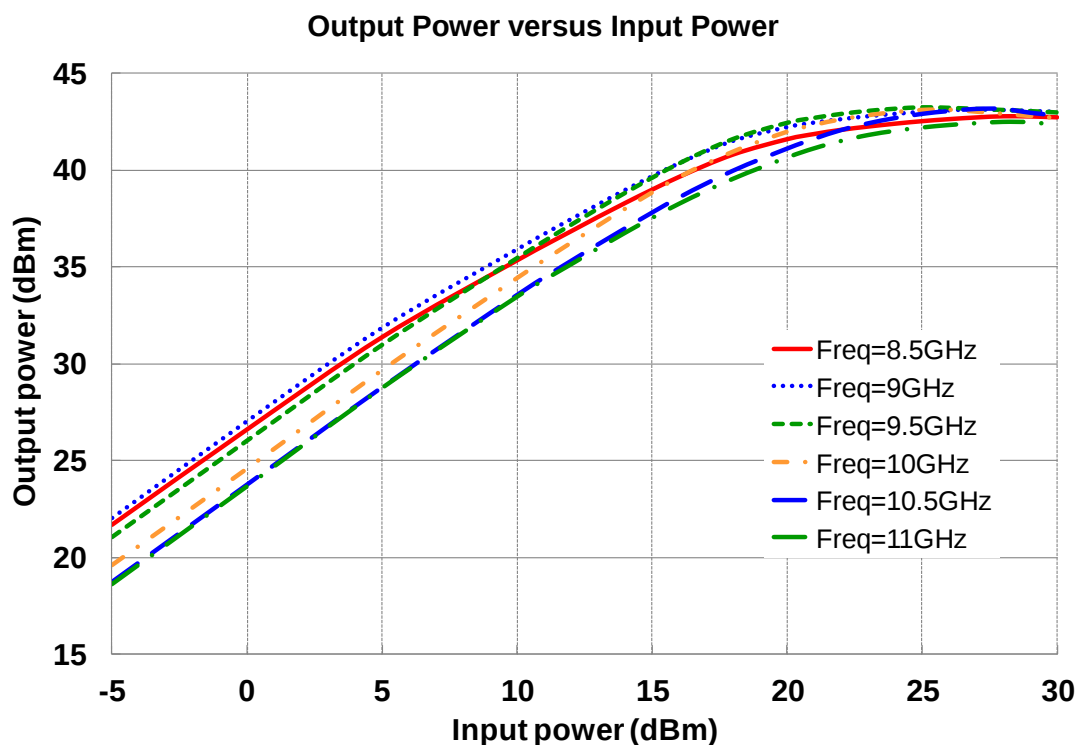
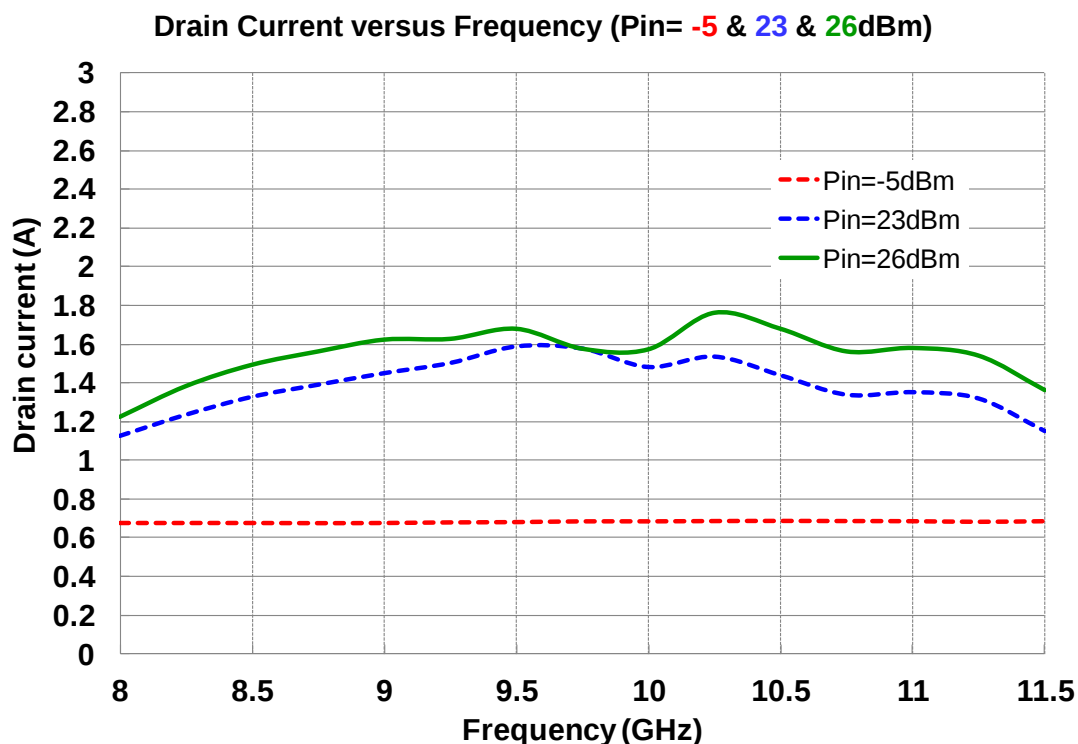
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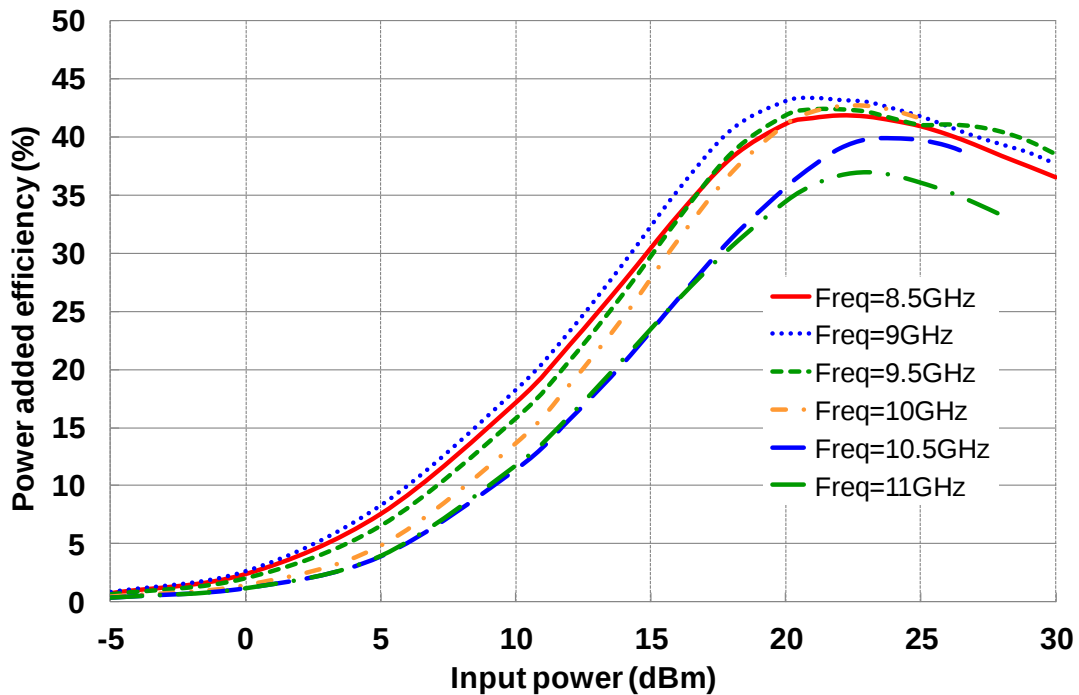
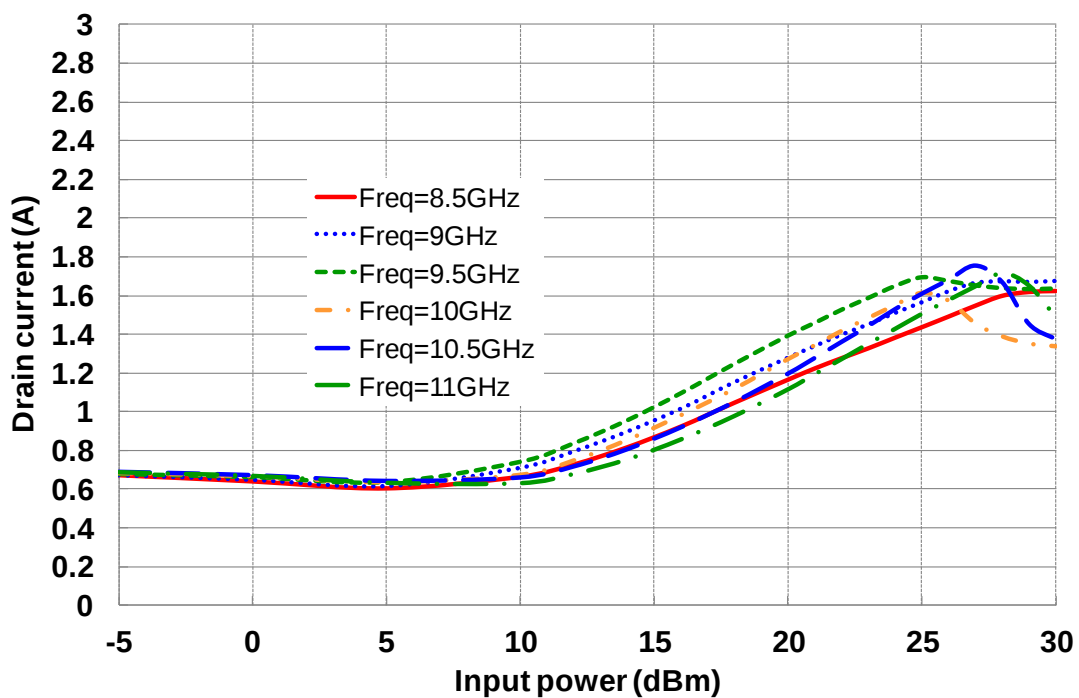
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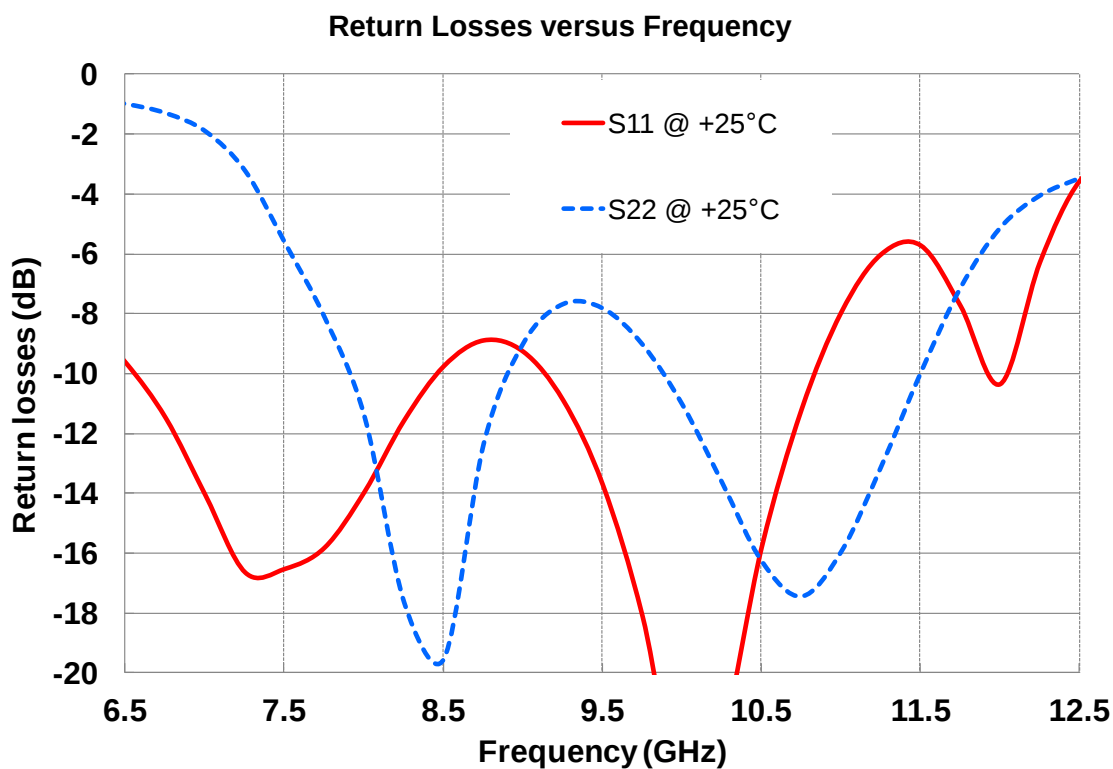
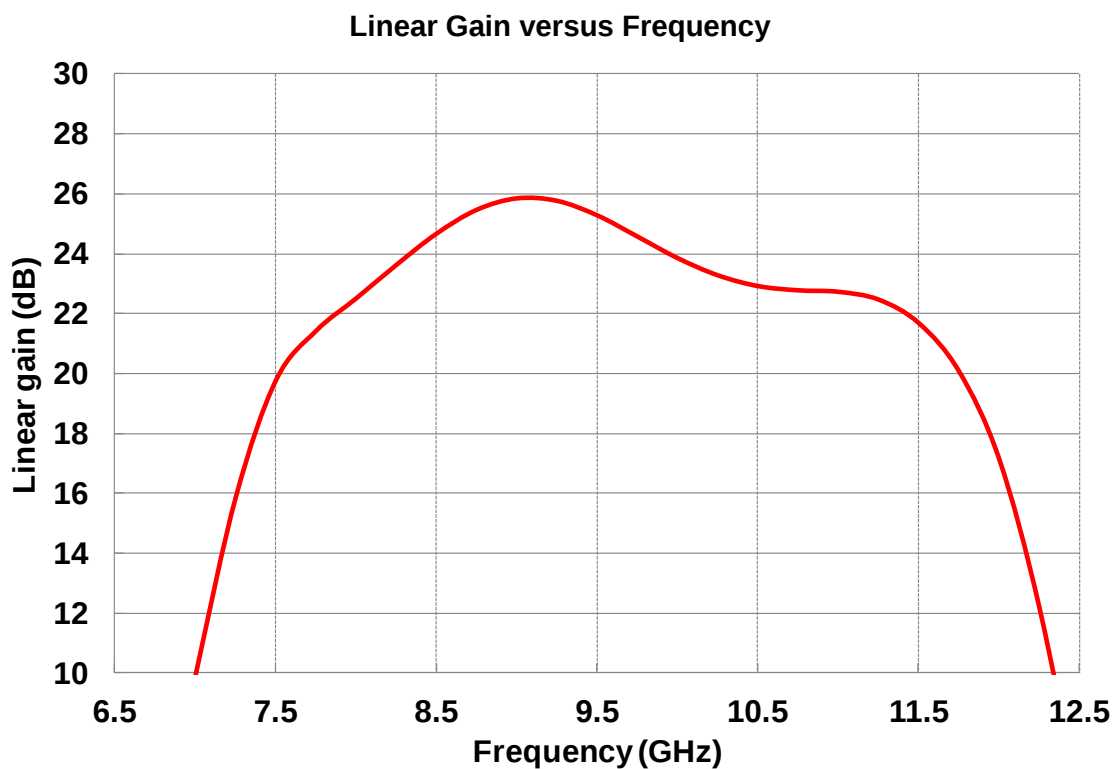
Typical Board Measurements (Pulsed mode)

Tamb= +25°C, Vd= +30V, Idq= 680mA at Tamb=+25°C, Pulse width=25µs, Duty cycle =10%

Power Added Efficiency versus Input Power**Drain Current versus Input Power**

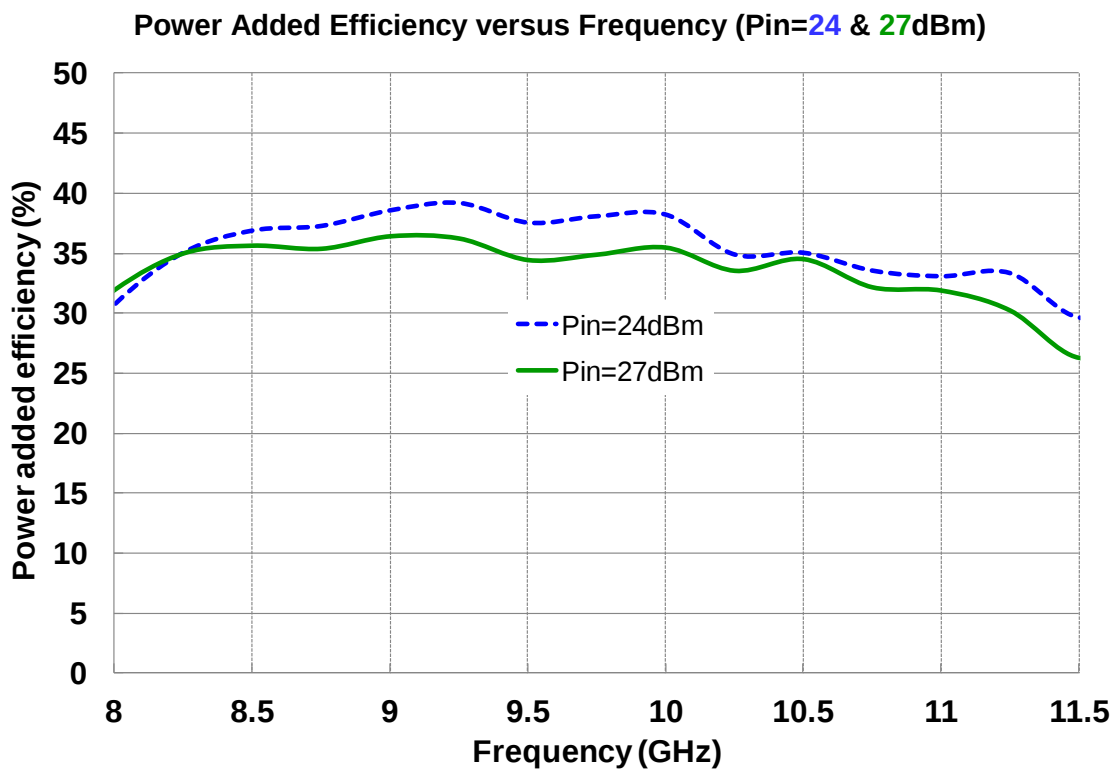
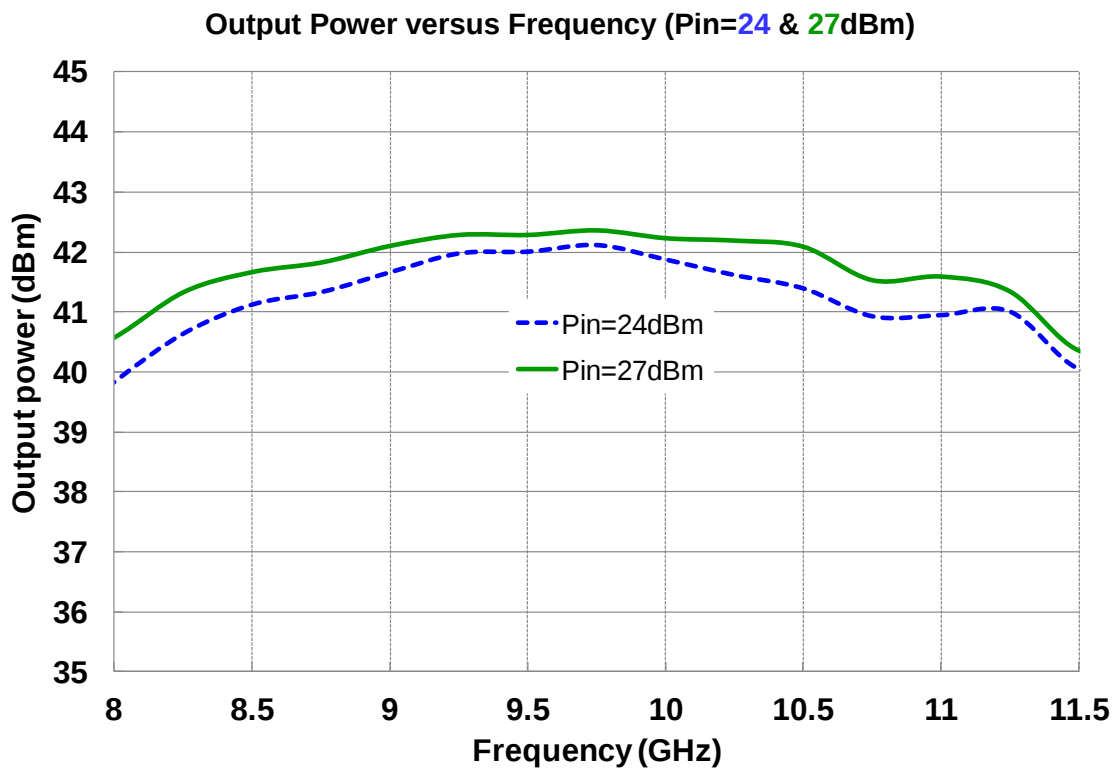
Typical Board Measurements (CW mode)

Tamb = +25°C, Vd = +30V, Idq = 450mA @ Tamb = +25°C



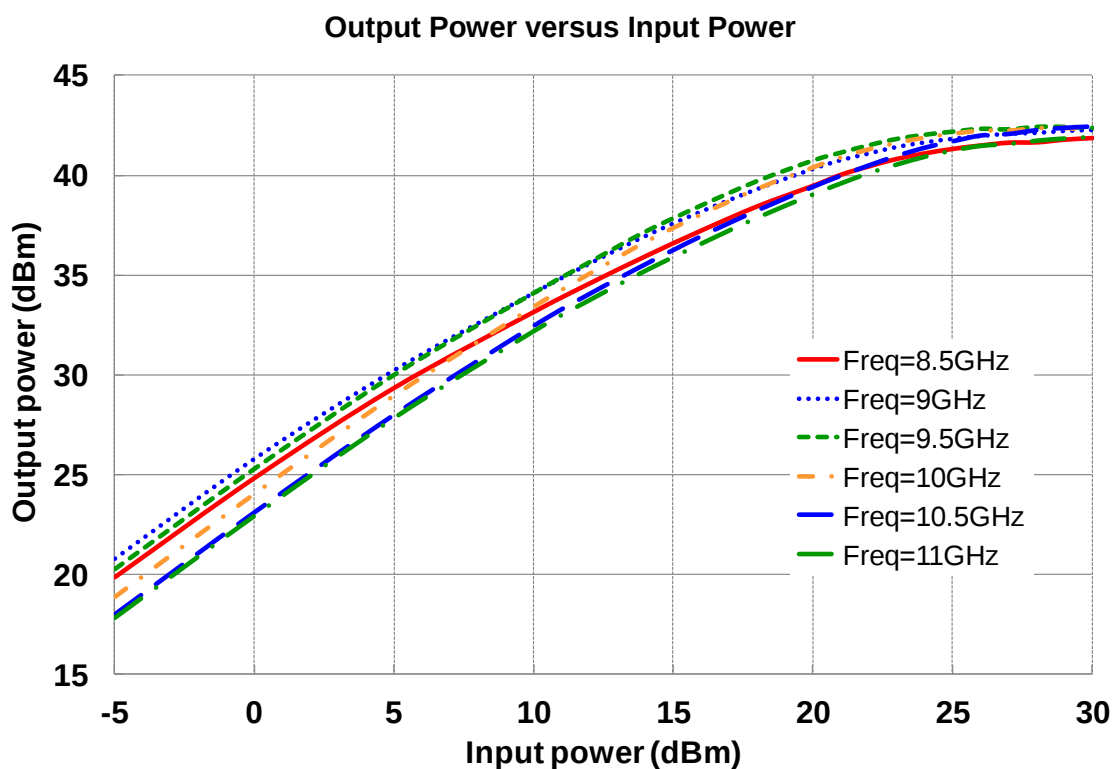
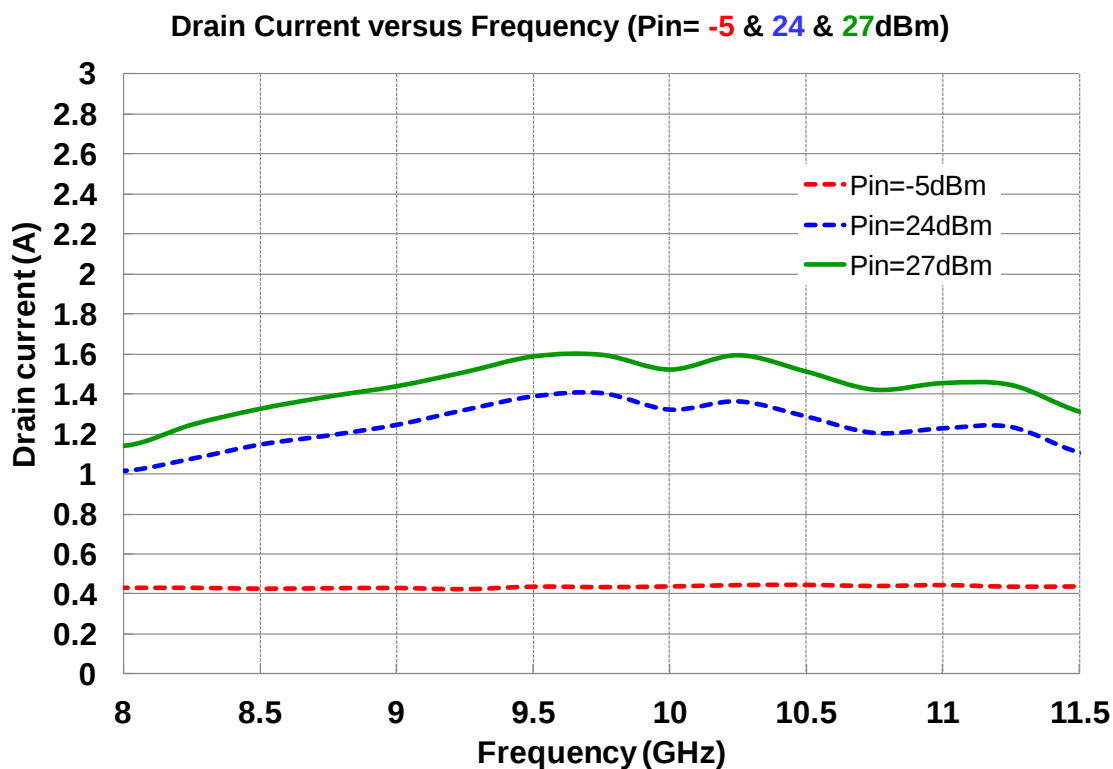
Typical Board Measurements (CW mode)

Tamb.= +25°C, Vd = +30V, Idq = 450mA @ Tamb = +25°C



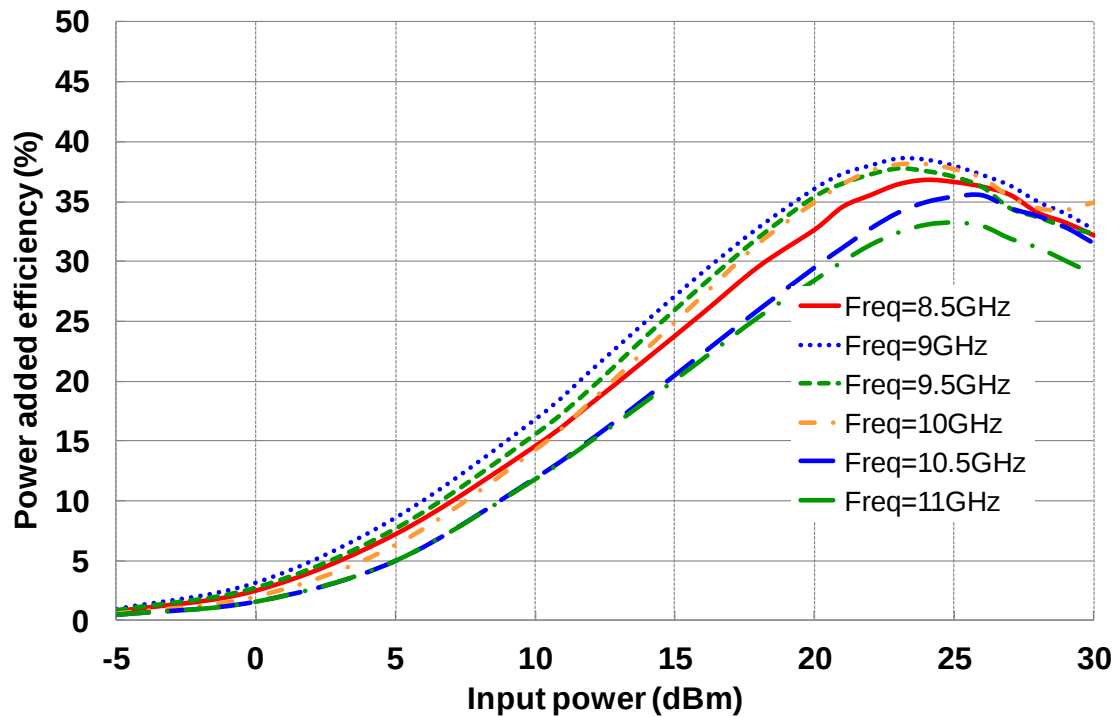
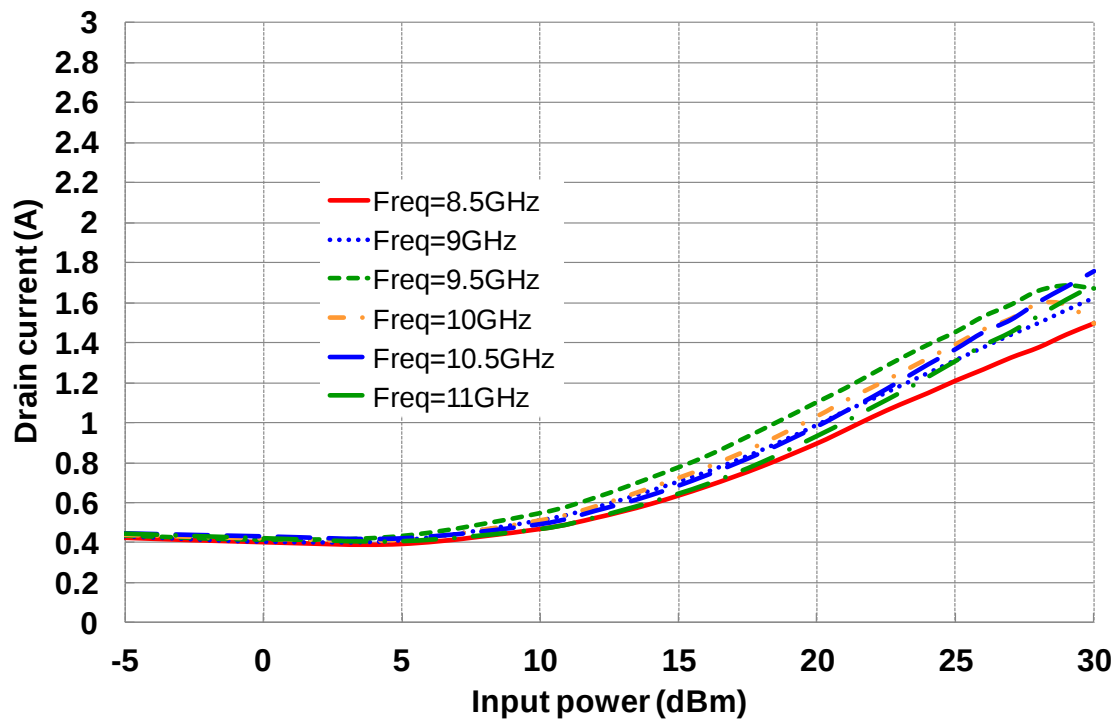
Typical Board Measurements (CW mode)

Tamb.= +25°C, Vd = +30V, Idq = 450mA @ Tamb = +25°C

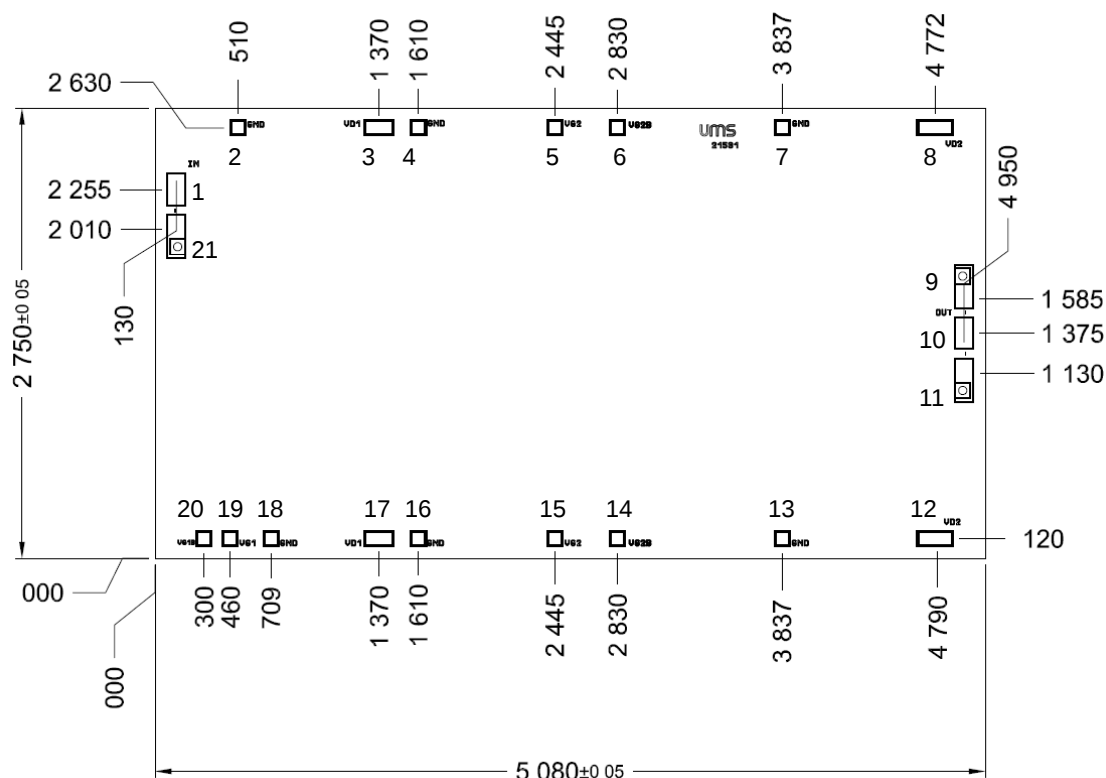


Typical Board Measurements (CW mode)

Tamb. = +25°C, Vd = +30V, Idq = 450mA @ Tamb = +25°C

Power Added Efficiency versus Input Power**Drain Current versus Input Power**

Mechanical data



All dimensions are in micrometers

Chip size = 5080μm x 2750μm (dicing streets included) ±50μm

Chip thickness = 100μm

RF pads (1, 10) = 120 x 200μm²

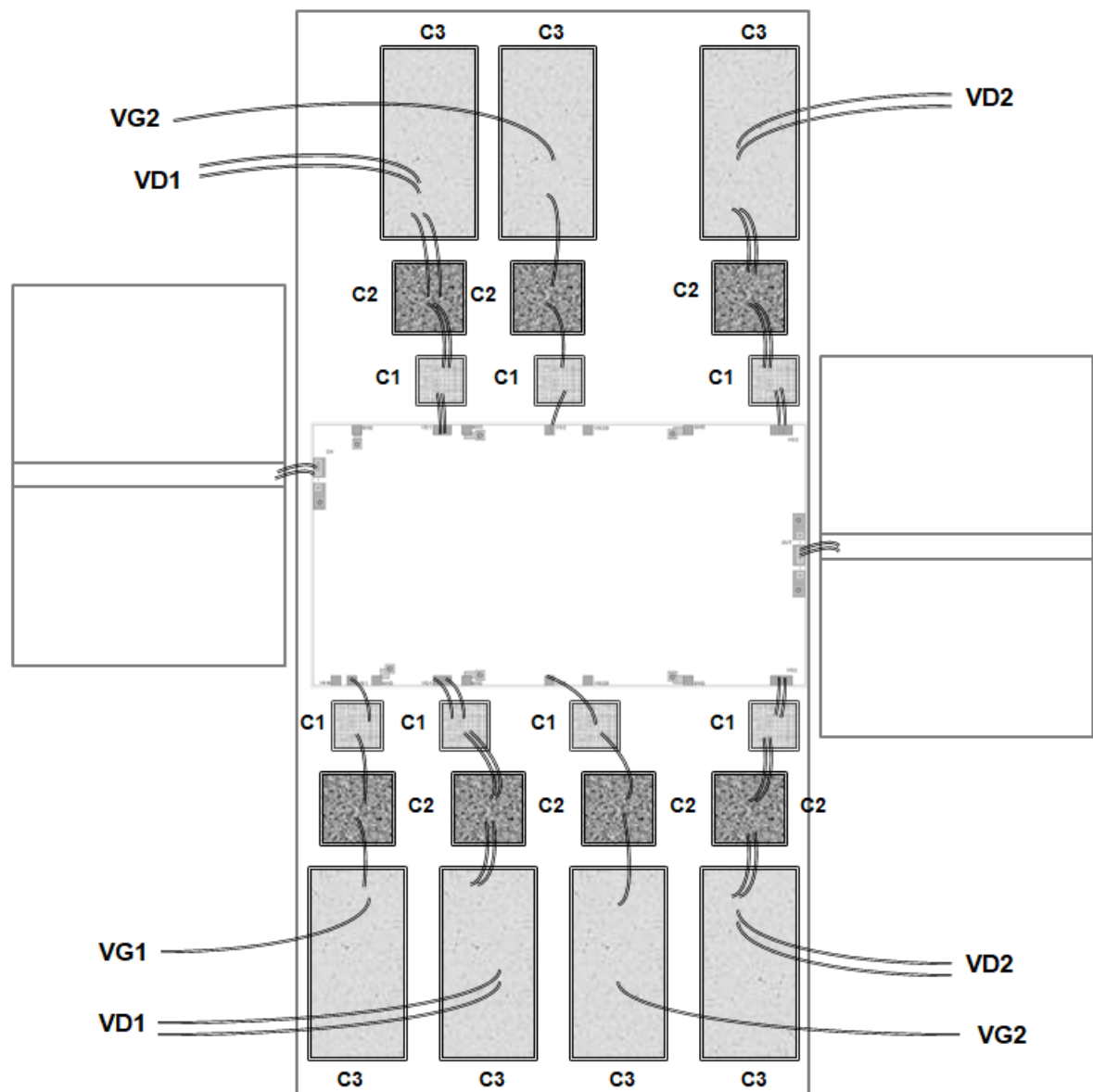
DC pads (5, 6, 14, 15, 19, 20) = 100 x 100μm²

DC pads (3, 17) = 185 x 100μm²

DC pads (8, 12) = 225 x 100μm²

PAD Number	Name	Description
1	IN	Input RF port
2, 4, 7, 9, 11, 13, 16, 18, 21	GND	Ground (NC)
19	VG1	Negative supply voltage (gate of stage 1)
5, 15	VG2	Negative supply voltage (gate of stage 2)
3, 17	VD1	Positive supply voltage (drain of stage 1)
8, 12	VD2	Positive supply voltage (drain of stage 2)
10	OUT	Output RF port
20	VG1B	Negative supply voltage (gate of stage 1) without series resistor (non-connected)
6, 14	VG2B	Negative supply voltage (gate of stage 2) without series resistor (non-connected)

Recommended assembly plan in CW mode

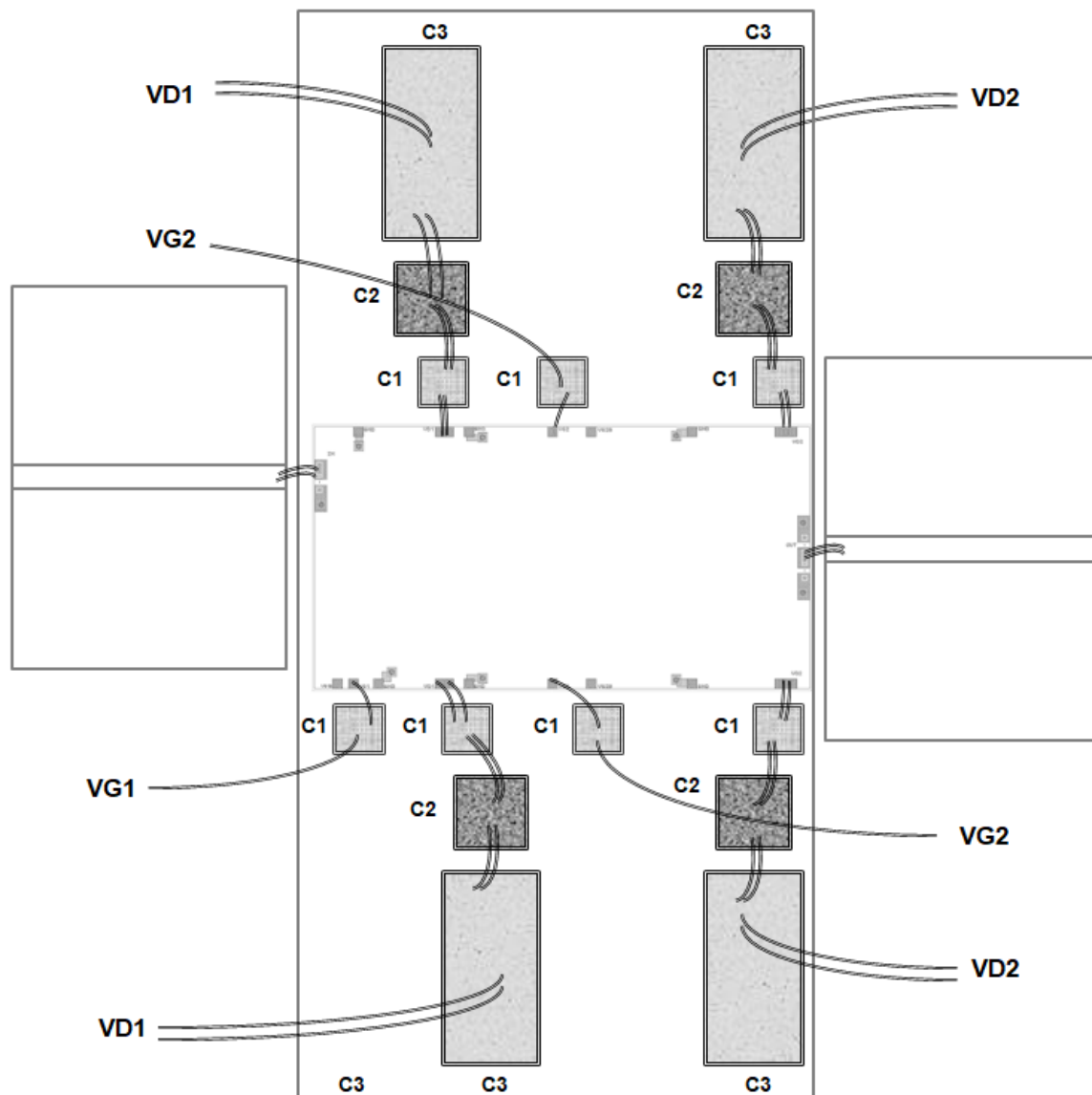


Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Bill of Materials

Label	Value	Description
C1	120pF	RF Capa ±10% 50V
C2	10nF	RF Capa ±20% 50V
C3	68nF	RF Capa ±20% 50V

Recommended assembly plan in gate pulsed mode



Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Bill of Materials

Label	Value	Description
C1	120pF	RF Capa ±10% 50V
C2	10nF	RF Capa ±20% 50V
C3	68nF	RF Capa ±20% 50V

Recommended circuit bonding table

Label	Type	Decoupling	Comment
RFIN	RF	Not required	Inductance (Lbonding) = 0.3nH 2 gold wires with diameter of 25 μ m (500 μ m)
RFOUT	RF	Not required	Inductance (Lbonding) = 0.3nH 2 gold wires with diameter of 25 μ m (500 μ m)
Vd	DC	100pF & 10F & 68nF	Inductance $\leq$ 1nH (mainly for first decoupling level) $\Rightarrow$ 1.2mm length wires with a diameter of 25 μ m
Vg	DC	100pF	Inductance $\leq$ 1nH (mainly for first decoupling level) $\Rightarrow$ 1.2mm length wires with a diameter of 25 μ m

- The overall biasing network proposed is compliant with a DC pulse applied on the gate; it can be integrated differently depending on module technology and on modulation characteristics (gate or drain pulse, pulse length and Duty Cycle). However, the first decoupling level should always be kept, the second one should be adapted to modulator characteristics and the third one should be kept and optimized on the non-modulated ports.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Ordering Information

Chip form:

CHA8610-99F/00

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