

DESCRIPTION

The CHD408L is a family of low voltage, low power 4Mbit static RAMs organized as 512K-words by 8-bit, designed with Cascade's patent pending SuperT-SRAM™ technology, fabricated with low-power 0.18μm process technology.

The CHD408LVS is designed specifically for low-power applications such as mobile cellular phones, personal digital assistants and other battery-operated products.

CHD408LVS -55,70 is packaged in sTSOP-I packages, with normal and reverse lead-bending. sTSOP-I packages are available in dimensions of 8x12mm and 8x20mm.

FEATURES

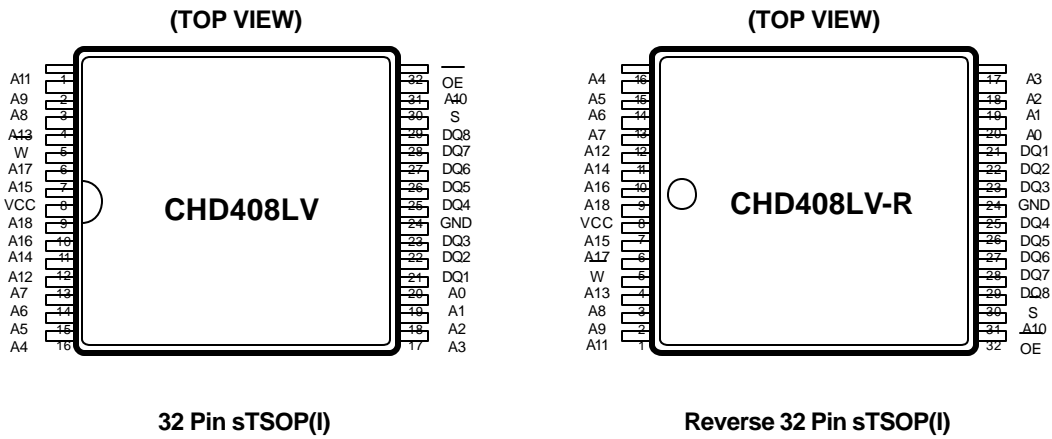
- Low power
 - Low active and standby power for hand-held applications.
 - Single power supply.
- High Performance
 - 55ns or 70ns access time
- Compatibility
 - 100% compatible with JEDEC asynchronous SRAM.
 - No clocks, no refresh.
 - No timing restrictions.
 - No special power-up sequence requirement.
 - Direct TTL compatibility for all inputs and outputs.
- Technology
 - Designed with Cascade's patent pending SuperT-SRAM™ technology.
 - Fabricated with low-power 0.18μm process technology.
- Extended temperature range -40 ~ 85°C.

PART NAME TABLE & KEY SPEC SUMMARY

| Power Supply | Part Name | Max. Access Time @ 2.7V | Standby Icc Max @ 3.0V 85°C | Active Icc 3.0V 10MHz |
|--------------|--------------|-------------------------|-----------------------------|-----------------------|
| 2.7V ~ 3.6V | CHD408LVx-70 | 70ns | 35 μA | 8mA |
| 3.0V ~ 3.6V | CHD408LVx-55 | 55ns | 35 μA | 8mA |

PART SELECTION TABLE

| Part Name | Package | Lead Bending |
|-------------------|----------------|--------------|
| CHD408LVS-55,70 | 8x12mm STSOP-I | Normal |
| CHD408LVS-55,70-R | 8x12mm STSOP-I | Reverse |
| CHD408LVW-55,70 | 8x20mm STSOP-I | Normal |
| CHD408LVW-55,70-R | 8x20mm STSOP-I | Reverse |

PIN CONFIGURATION


| Pin | Function |
|-----------------|---------------------|
| A0~A18 | Address input |
| DQ1 ~ DQ8 | Data input / output |
| \overline{S} | Chip select input |
| \overline{W} | Write control input |
| \overline{OE} | Output enable input |
| VCC | Power supply |
| GND | Ground supply |

FUNCTIONAL DESCRIPTION

CHD408LVS-55/70(-R) is organized as 512K-words by 8-bit. These devices operate on a single power supply, and are directly TTL compatible to both input and output. The design uses fully asynchronous static circuits, requiring no clocks, no refresh, and no special power-up sequence.

The operation modes are determined by a combination of the device control inputs \overline{S} , \overline{W} and \overline{OE} . Each mode is summarized in the function table.

A write operation is executed whenever the low level \overline{W} overlaps with the low level \overline{S} . The address (A0~A18) must be set up before the write cycle and must be stable during entire cycle.

A read operation is executed by setting \overline{W} at a high level and \overline{OE} at a low level while \overline{S} is in an active state.

When setting \overline{S} at a high level, the chip is in a non-select mode. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips.

When \overline{OE} is at a high level, the output stage is in a high-impedance state.

FUNCTION TABLE

| \overline{S} | \overline{OE} | \overline{W} | DQ1-8 | Mode | Power |
|----------------|------------------|----------------|------------------|-----------------|---------|
| H | X ⁽¹⁾ | X | Z ⁽²⁾ | Deselected | Standby |
| L | H | H | Z | Output disabled | Active |
| L | L | H | Data out | read | Active |
| L | X | L | Data in | write | Active |

Notes : (1) X means don't-care, but must drive to either high or low.

(2) Z means high impedance state.

ABSOLUTE MAXIMUM RATINGS

| Parameter | Value | Unit | Notes |
|--------------------------------------|----------------------------|------|----------------------------|
| VCC Power Supply Voltage | -0.4 to 4.6 | V | |
| VI Input Voltage | -0.4* to VCC+0.5 (max 4.6) | V | * -3V for AC pulse (<30ns) |
| VO Output Voltage | 0 to VCC | V | |
| PD Power Dissipation | 0.5 | W | |
| Tsolder Soldering Temperature | 260 | °C | |
| Tstor Storage Temperature | -65 to 150 | °C | |
| Tope Operating Temperature | -40 to 85 | °C | |

DC ELECTRICAL CHARACTERISTICS (T = -40 to 85°C)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---------|-----|---------|-------|
| VCC Power Supply Voltage | | 2.7/3.0 | - | 3.6 | V |
| VIH Input High Voltage | | 2.2 | - | VCC+0.4 | V |
| VIL Input Low Voltage | | -0.4* | - | 0.6 | V |
| VOH High-Level Output Voltage | I _{OH} = -1 mA | VCC-0.4 | - | - | V |
| VOL Low-level Output Voltage | I _{OL} = 2 mA | - | - | 0.4 | V |
| I_I Input Leakage Current | V _I = 0~VCC | - | - | ±1 | μA |
| I_O Output Leakage Current | Output disabled. V _{IO} = 0~VCC | - | - | ±1 | μA |

* -3V for AC pulse (<= 30ns)

POWER CONSUMPTION CHARACTERISTICS

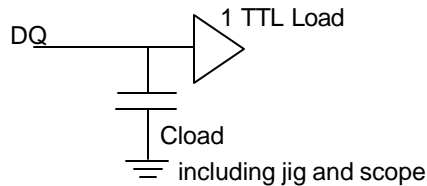
| Parameter | Conditions | Typ | Max (3.0V) | Max (3.6V) | Units |
|-------------------|--|-----|------------|------------|-------|
| ICC1 10MHz | Output open. All inputs = 0.2V or VCC-0.2V | - | 8 | 10 | mA |
| ICC1 1MHz | Output open. All inputs = 0.2V or VCC-0.2V | - | 2 | 3 | mA |
| ICC2 10MHz | Output open. All inputs = VIL or VIH | - | 9 | 11 | mA |
| ICC2 1MHz | Output open. All inputs = VIL or VIH | - | 3 | 4 | mA |
| ISB1 | S = VCC-0.2V All other inputs = 0.2 or VCC-0.2V | - | 35 | 60 | μA |
| ISB2 | S = VIH All other inputs = VIH or VIL | - | 0.3 | - | mA |

CAPACITANCE

| | Parameter | Min | Typ | Max | Notes |
|-----------|--------------------|-----|-----|-----|-------|
| CI | Input Capacitance | | | 8pF | |
| CO | Output Capacitance | | | 8pF | |

AC ELECTRICAL CHARACTERISTICS
(1) TEST CONDITIONS

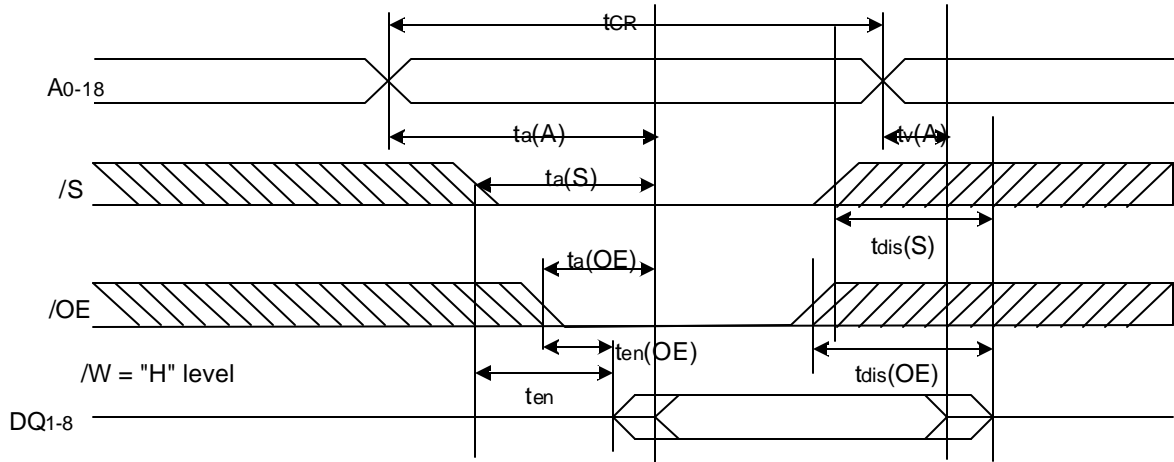
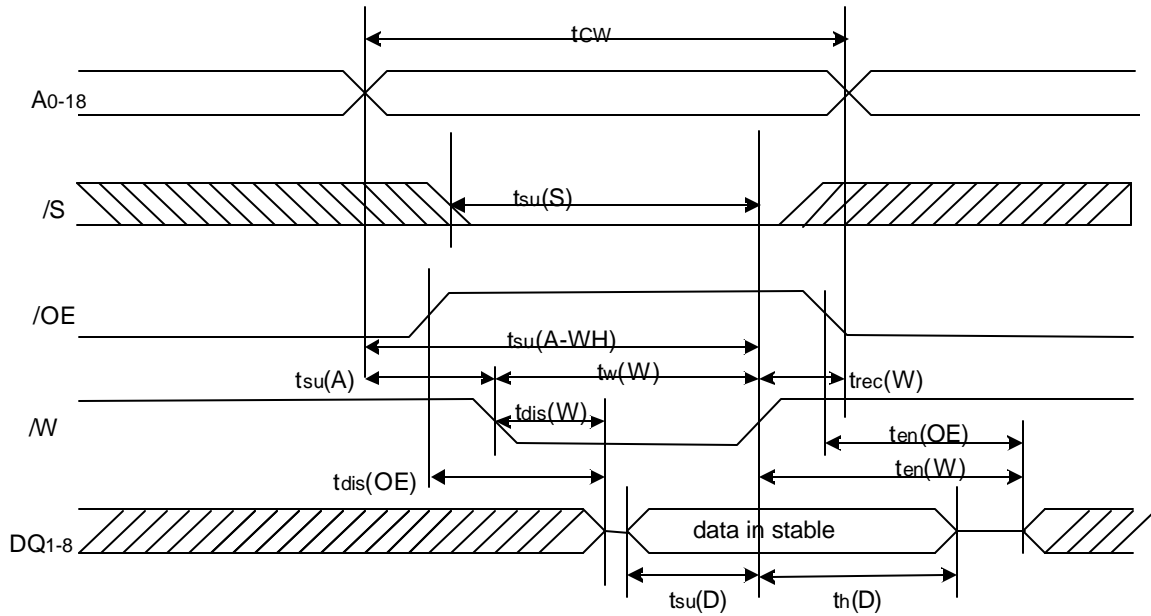
| Parameter | Value | Notes |
|--------------------------|--|-------------------------|
| VCC | 2.7-3.6V | |
| Input pulse level | V _{IH} =2.4V, V _{IL} =0.4V | |
| Input rise and fall time | 5ns | |
| Reference level | V _{OH} =V _{OL} =1.5V | |
| Output loads | 30pF | Plus one TTL input load |

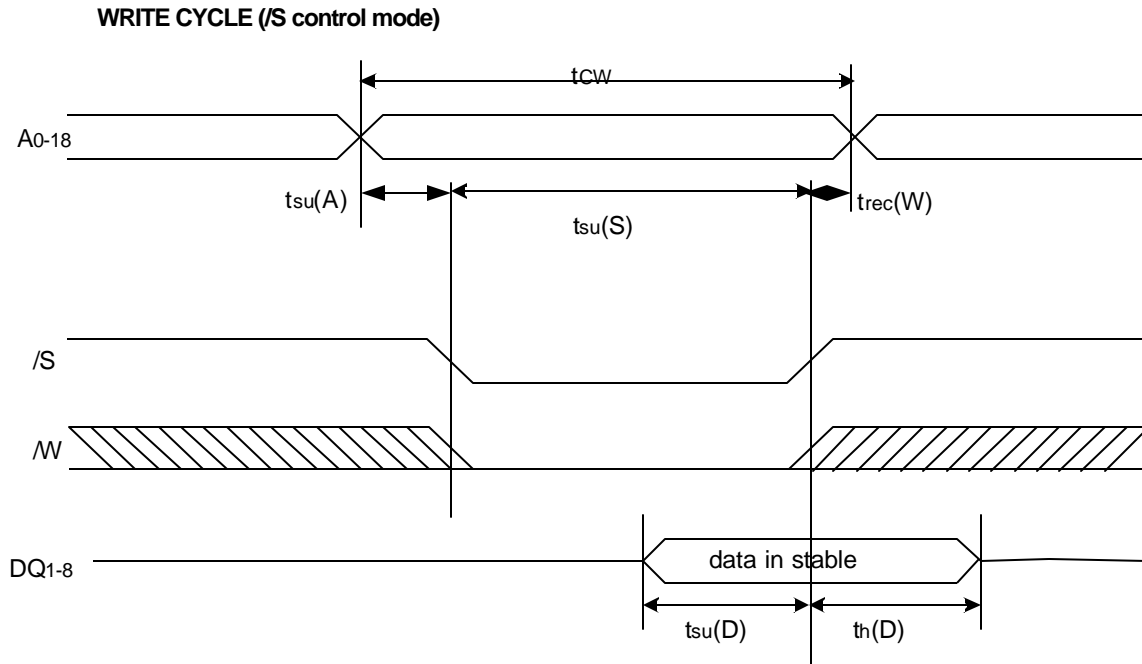

(2) READ CYCLE

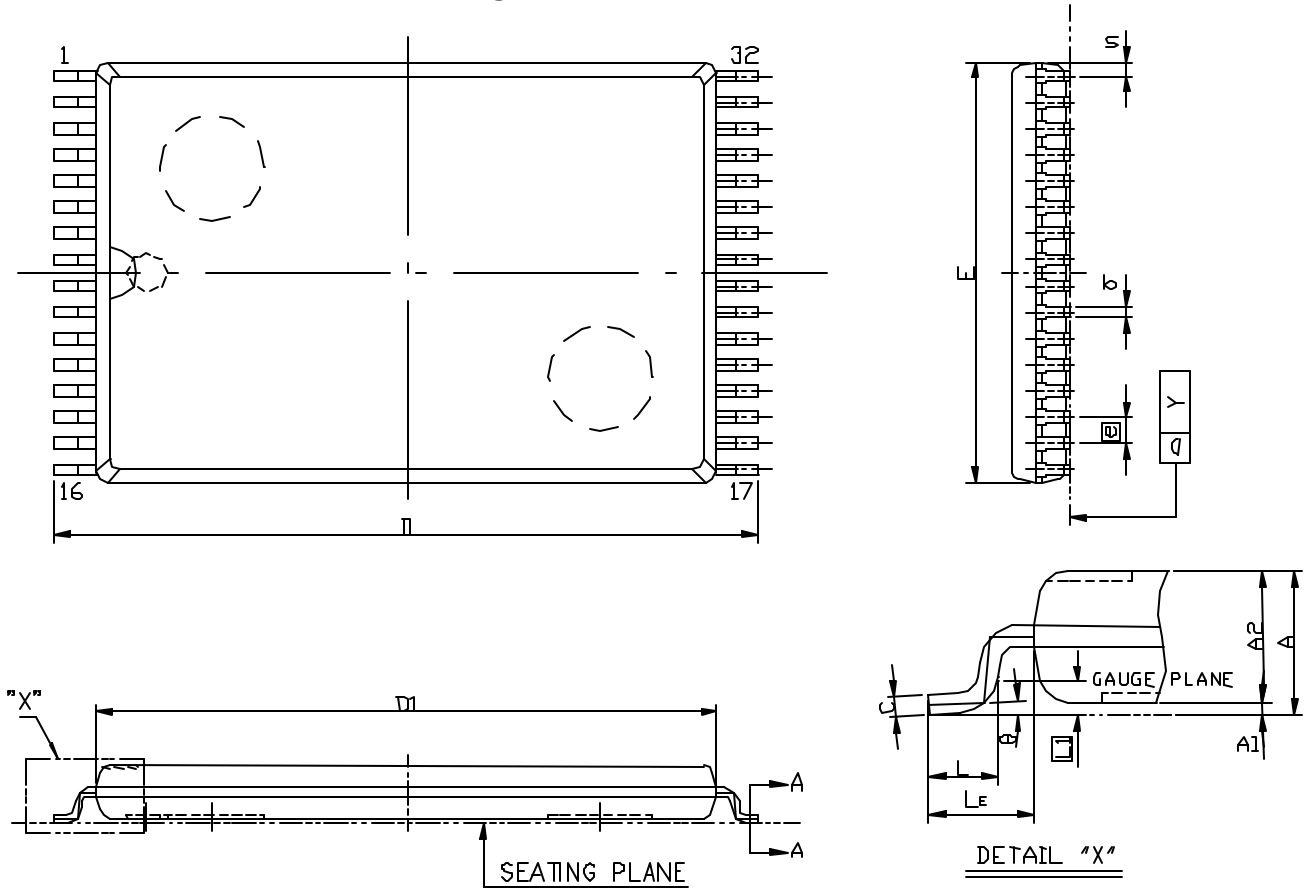
| | Parameter | CHD408LVS-55(-R) | | CHD408LVS-70(-R) | |
|----------------------|--------------------------------|------------------|-----|------------------|-----|
| | | Min | Max | Min | Max |
| t _{CR} | Read cycle time (ns) | 55 | - | 70 | - |
| t _{a(A)} | Address access time (ns) | - | 55 | - | 70 |
| t _{a(S)} | Chip select access time (ns) | - | 55 | - | 70 |
| t _{a(OE)} | Output enable access time (ns) | - | 25 | - | 35 |
| t _{dis(S)} | Output disable after /S (ns) | - | 15 | - | 25 |
| t _{dis(OE)} | Output disable after /OE (ns) | - | 15 | - | 25 |
| t _{en(S)} | Output enable after /S (ns) | 5 | - | 5 | - |
| t _{en(OE)} | Output enable after /OE (ns) | 5 | - | 5 | - |
| t _{v(A)} | Data valid time after address | 10 | - | 10 | - |

(3) WRITE CYCLE

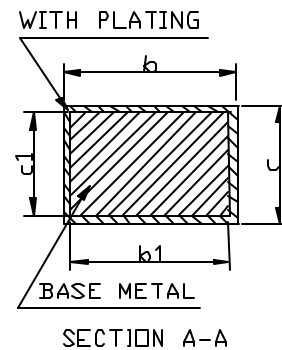
| | Parameter | CHD408LVS-55(-R) | | CHD408LVS-70(-R) | |
|----------------|-------------------------------|------------------|-----|------------------|-----|
| | | Min | Max | Min | Max |
| t_{CW} | Write cycle time (ns) | 55 | - | 70 | - |
| $t_{W(W)}$ | Write pulse width (ns) | 45 | - | 55 | - |
| $t_{su(A)}$ | Address setup time (ns) | 0 | - | 0 | - |
| $t_{su(A-WH)}$ | Add setup to Write high (ns) | 45 | - | 55 | - |
| $t_{su(S)}$ | Chip select setup time (ns) | 45 | - | 55 | - |
| $t_{su(D)}$ | Data setup time (ns) | 25 | - | 25 | - |
| $t_h(D)$ | Data hold time (ns) | 0 | - | 0 | - |
| $t_{rec(W)}$ | Write recovery time (ns) | 0 | - | 0 | - |
| $t_{dis(W)}$ | Output disable after /W (ns) | - | 25 | - | 25 |
| $t_{dis(OE)}$ | Output disable after /OE (ns) | - | 25 | - | 25 |
| $t_{en(W)}$ | Output enable after /W (ns) | 5 | - | 5 | - |
| $t_{en(OE)}$ | Output enable after /OE (ns) | 5 | - | 5 | - |

(4) TIMING DIAGRAMS
READ CYCLE

WRITE CYCLE (/W control mode)


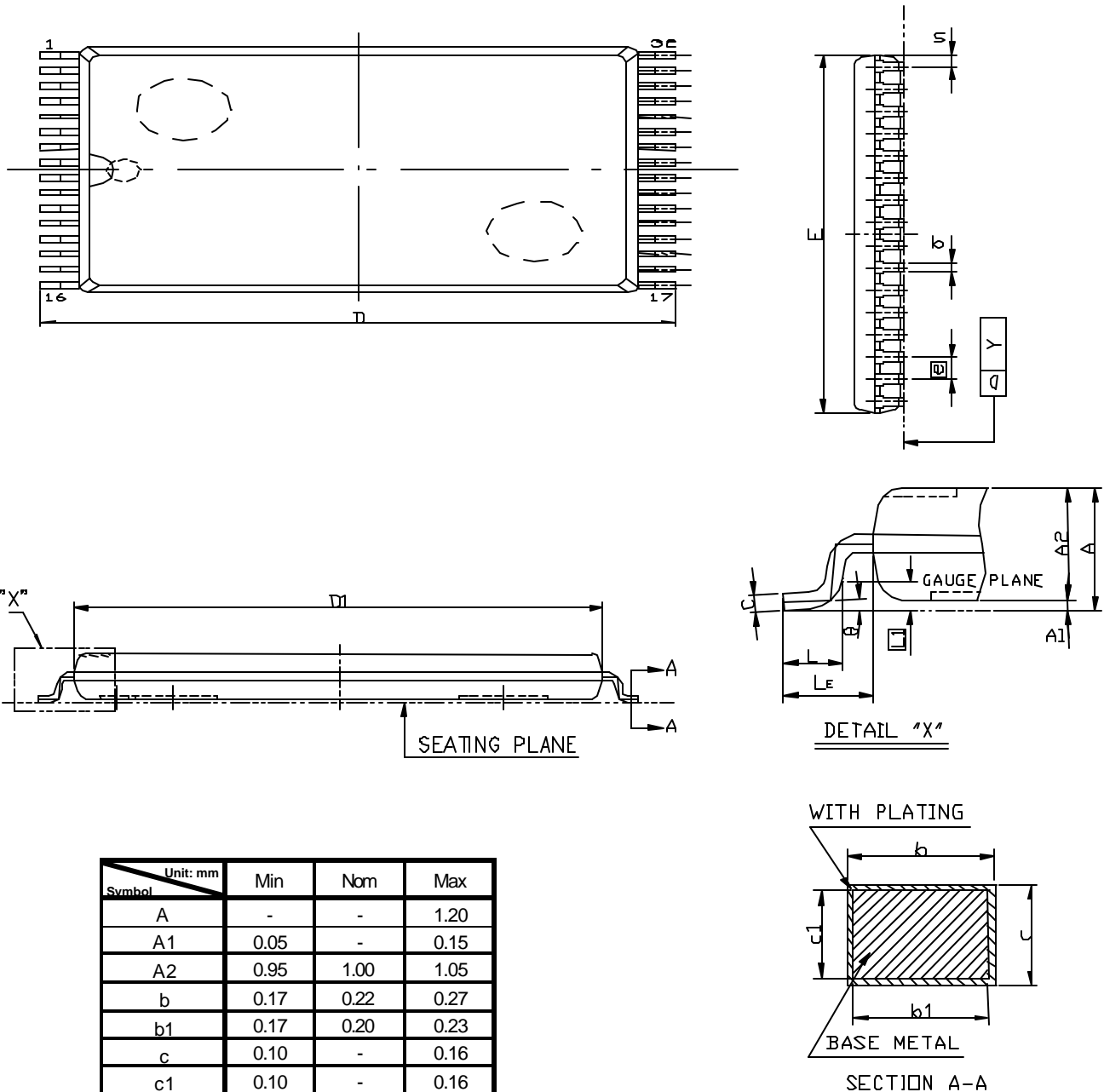


32-Pin 8x12mm sTSOP-I Package Dimensions


| Unit: mm | Min | Nom | Max |
|---------------|-------|-------|-------|
| Symbol | | | |
| A | - | - | 1.25 |
| A1 | 0.05 | - | - |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.17 | 0.22 | 0.27 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.10 | - | 0.21 |
| c1 | 0.142 | 0.150 | 0.158 |
| D | 13.20 | 13.40 | 13.60 |
| D1 | 11.70 | 11.80 | 11.90 |
| E | 7.90 | 8.00 | 8.10 |
| e | - | 0.50 | - |
| L1 | - | 0.25 | - |
| L | 0.30 | 0.50 | 0.70 |
| LE | 0.675 | - | - |
| θ | 0 | 3° | 5° |
| y | - | - | 0.075 |
| s | - | 0.278 | - |


NOTE:

- 1.D1 and E do not include mold protrusion. Allowable mold protrusion on E is 0.15mm per side and on D1 is 0.25mm per side
- 2.Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm.

32-Pin 8x20mm sTSOP-I Package Dimensions


| Symbol | Unit: mm | Min | Nom | Max |
|--------|----------|----------|-------|-------|
| A | | - | - | 1.20 |
| A1 | | 0.05 | - | 0.15 |
| A2 | | 0.95 | 1.00 | 1.05 |
| b | | 0.17 | 0.22 | 0.27 |
| b1 | | 0.17 | 0.20 | 0.23 |
| c | | 0.10 | - | 0.16 |
| c1 | | 0.10 | - | 0.16 |
| D | | 19.80 | 20.00 | 20.20 |
| D1 | | 18.20 | 18.40 | 18.60 |
| E | | 7.80 | 8.00 | 8.20 |
| e | | - | 0.50 | - |
| L | | 0.50 | 0.60 | 0.70 |
| LE | | 0.80 REF | | |
| θ | | 0 | 3° | 5° |
| y | | - | - | 0.075 |
| s | | - | 0.278 | - |

NOTE:

- 1.D1 and E do not include mold protrusion. Allowable mold protrusion on E is 0,15mm per side and on D1 is 0,25mm per side
- 2.Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0,08mm.

4M SuperT-SRAM™ CHD408LVx-55,70 Datasheet Revision History

| | | | |
|-----------------|---------|----|--|
| Preliminary 0.1 | 2/21/02 | WC | Preliminary initial version |
| Rev 1.0 | 6/13/02 | SC | Added more detailed DC parameters and test conditions; fixed some DC parameter numbers. Added figure for output load |
| Rev 1.1 | 1/2/03 | SC | Updated A17/A18 assignment to be consistent with industry convention. |
| Rev 2.0 | 3/20/03 | JG | Added -55 grade |
| Rev 2.1 | 7/11/03 | WC | Added 8x20mm TSOP-I package |
| Rev 2.2 | 7/22/03 | WC | Renamed LVS-70W to LVW-70, to be consistent with naming convention. |

- The information contained herein is subject to change without notice.