CHT-ADC10 Datasheet

Version: 1.6
8-Jul-14
(Last Modification Date)

High-Temperature Ultra-low-power 10-bit ADC

General Description

The CHT-ADC10 is a high-temperature, ultra-low-power, highly stable analog-to-digital converter. This successive approximation ADC is based on an R-2R network and features 10 bits of resolution and a strictly monotonic characteristic from -55°C up to +225°C. An optional internal clock generator is included to provide stand-alone operation. It includes Sample&Hold and µP interface with possibility of serial data transfer. Both parallel and serial interfaces can be used simultaneously. A special control line allows for doubling the frequency of the internal clock generator for reduced throughput time. The maximum sampling rate is 25kS/s. Several input ranges are available from -15V up to +10V. It only requires a +5V supply and an external +5V reference.
The CHT-ADC10 is latch-up free and the fabrication technology guarantees a high reliability at extreme temperatures.

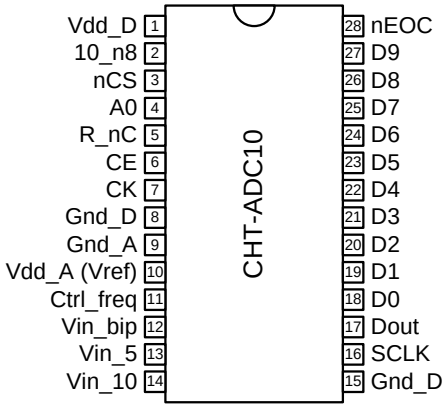
Features

- 10 bit-resolution with optional internal clock, Sample/Hold, µC interface with parallel or serial data transfer
- Up to 25kS/s
- +5V power supply only
- Low total supply current (<250 µA)
- Operational from -55 to +225°C with very low drift
- Validated at 225°C for 20000 hours (and still on-going)
- Available in die, CDIL28 and CSOIC28

Applications

- Oil&Gas, Industrial, Automotive, Aeronautics & Aerospace
- Electric Power Conversion

Package Configurations[1]

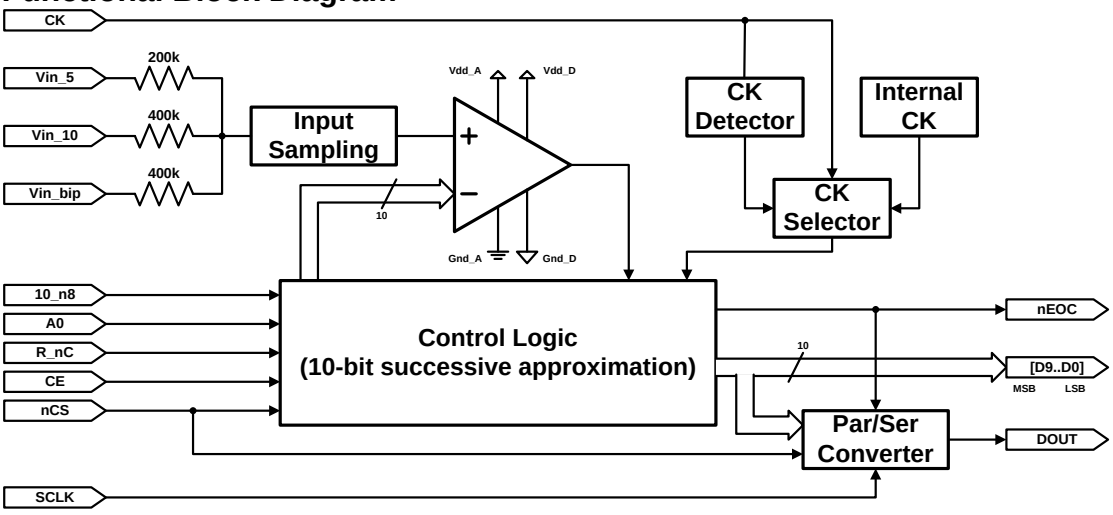


[1] Pinout is identical for CDIL28 and CSOIC28. Other packages available upon request.

Ordering Information

Ordering Reference	Package	Temperature Range	Marking
CHT-ADC10-CDIL28-T	Ceramic DIL28	-55°C to +225°C	CHT-ADC10
CHT-ADC10-CSOIC28-T	Ceramic SOIC28	-55°C to +225°C	CHT-ADC10

Functional Block Diagram



Pin Description

Pin#	Symbol	Type[1]	Function
1	**Vdd_D**	SD	+5V digital supply (+/- 5%).
2	**10_n8**	DI	Determines whether output data is to be organized as two 8-bit words (low) or a single 10-bit word (high).
3	**nCS**	DI	(active low) Chip Select.
4	**A0**	DI	During the read cycle, if 10_n8 is low, A0 low enables the 8 MSBs (D9…D2) while A0 high enables (D1,D0) and sets (D7…D2)=0.
5	**R_nC**	DI	Read/Convert. Active high for Read and low for write.
6	**CE**	DI	(active high) Chip Enable.
7	**CK**	DI	Optional clock input. Must be grounded if not used. If used, should preferably be high during 12µs after the starting of conversion for noise reasons. Range: 10kHz and 500kHz ; duty-cycle:10% to 90%.
8	**Gnd_D**	SD	Digital ground.
9	**Gnd_A**	SA	Analog ground.
10	**Vdd_A (Vref)**	SA	Analog supply voltage. It is also used as internal voltage reference. Must be a precise and noiseless 5V supply (current <200µA). The accuracy of this reference directly affects the ADC gain error.
11	**Ctrl_ freq**	DI	Should be high for normal operation. If low, it doubles the internal oscillator frequency (~500kHz) at cost of a lower precision.
12	**Vin_bip**	AI	Analog signal input. It is connected to an internal 400kΩ resistor. See Static Characteristics table for possible input ranges.
13	**Vin_5**	AI	Analog signal input. It is connected to an internal 200kΩ resistor. See Static Characteristics table for possible input ranges.
14	**Vin_10**	AI	Analog signal input. It is connected to an internal 400kΩ resistor. See Static Characteristics table for possible input ranges.
15	**Gnd_D**	SD	Digital ground.
16	**SCLK**	DI	Must be low whilst CS is active with a conversion in progress. After End-of-Conversion, each SCLK falling edge shifts data out through DOUT. Maximum SCLK frequency is 10MHz.
17	**Dout**	DO	Tri-state serial data output. When nCS is high, Dout is in high-impedance state. When nCS is low, Dout is low during conversion and goes high at end of conversion. After this rising edge, new data (starting from MSB) go out at each falling edge of SCLK.
18	**D0 (LSB)**	DO	Tri-state parallel data output.
19	**D1**	DO	
20	**D2**	DO	
21	**D3**	DO	
22	**D4**	DO	
23	**D5**	DO	
24	**D6**	DO	
25	**D7**	DO	
26	**D8**	DO	
27	**D9(MSB)**	DO	
28	**nEOC**	DO	Represents the End-of-Conversion (active low) flag.

[1] *Type: **S**=Supply, **A**=Analog; **D**=Digital; **I**=input; **O**=output*

Absolute Maximum Ratings

Supply Voltage V_{DD} to GND	-0.5 to 5.5V
Voltage on any Pin to GND	-0.5 to V_{DD}+0.5V

ESD Rating (expected)

Human Body Model (expected)	<1kV

Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability.

Operating Conditions

Supply Voltage V_{DD} to GND	5V ± 5%
Junction temperature	-55°C to +225°C

Electrical Characteristics

Unless otherwise stated: V_{DDD}=5V±5%, T_j=25°C, output data rate=10 kS/s. **Bold** figures indicate values over the whole temperature range (-55°C < T_j <225°C).

Parameter	Condition	Min	Typ	Max	Units
Digital Supply voltage (V_{DDD})		**4.75**	**5.00**	**5.25**	V
Analog Supply voltage (V_{DDA})	Used as internal voltage reference		**5**		V
Current consumption (analog part)	-55°C 225°C		134 164		µA
Current consumption (digital part)	Using external CK		55		µA
	Using internal CK		70		µA

Static characteristics

Unless otherwise stated: V_{DDD}=5V±5%, T_j=25°C. **Bold** figures indicate values over the whole temperature range (-55°C < T_j <225°C). Units are referred to 10 bit word. Selected input range=0 to 5V.

Parameter	Condition	Min	Typ	Max	Units
Resolution		**10**			Bits
DNL[1]			**1.3**	**1.5**	LSB
INL[1]			**1.3**	**1.5**	LSB
Missing code			**0**	**1**	
Monotonicity			**OK**		
Offset[2]			17		LSB [1]
Gain Error[2]			1.5		%
Temperature Drift (d/dT°) - Offset - Gain Error			**-0.023** **-19**		LSB/°C ppm/°C
Selectable Analog Input Ranges	**Vin_5 / Vin_10 / Vin_bip** gndA / in / gndA in / gndA / gndA in / in / gndA in / in / in in / in / vddA in / gndA / vddA gndA / in / vddA in / vddA / vddA vddA / in / gndA vddA / in / vddA	 **0** **0** **0** **0** **-1.67** **-2.5** **-5** **-5** **-10** **-15**		 **10** **5** **3.33** **2.5** **1.67** **2.5** **5** **0** **0** **-5**	V
Input Impedance - Sample phase - Hold phase	For [0…5V] range. Can change up to a factor of 2 for other ranges.	 **144** **288**	 **200** **400**	 **245** **490**	kΩ

[1] Value extracted with code density method, using 200kHz external clock.

[2] For [0…5]V range, DAC transfer function is: **D**=Offset+(1024/5)***A***(1-(Gain Error/100))

Timing Characteristics

Unless otherwise stated: V_{DDD}=5V±5%, T_j=25°C, output data rate=10 kS/s. **Bold** figures indicate values over the whole temperature range (-55°C < T_j <225°C).

Parameter	Condition	Min	Typ	Max	Units
External CK frequency	Duty cycle between 10% and 90%	10	250	500	kHz
Output data rate		0.8	16	25	kS/s
Data Output Delay (clock edge to valid data)	TBD				ns
Sampling time before Hold	When conversion starts, actual sampling occurs after this sampling time.	8	10	12	µs
Data latency	Occurs when S/H goes to hold state.		13		cycles
Conversion time (t_C)	Cfr figure 12 for timing diagram		58		µs
NEOC delay from CE (t_{DSC})	Cfr figure 12 for timing diagram		15		ns
CE pulse width (t_{HEC})	Cfr figure 12 for timing diagram	40			ns
nCS to CE high setup time (t_{SSC})	Cfr figure 12 for timing diagram	40			ns
nCS to CE high hold time (t_{HSC})	Cfr figure 12 for timing diagram	40			ns
R_nC to CE high setup time (t_{SRC})	Cfr figure 12 for timing diagram	40			ns
R_nC to CE high hold time (t_{HRC})	Cfr figure 12 for timing diagram	40			ns
A0 to CE high setup time (t_{SAC})	Cfr figure 12 for timing diagram	5			ns
A0 to CE high hold time (t_{HAC})	Cfr figure 12 for timing diagram	40			ns
Access time (t_{DD})	Cfr figure 13 for timing diagram		9		ns
Data valid to CE low hold time (t_{HD})	Cfr figure 13 for timing diagram		6		ns
Output float after CE faling edge (t_{HL})	Cfr figure 13 for timing diagram		11		ns
nCS to CE high setup time (t_{SSR})	Cfr figure 13 for timing diagram	40			ns
R_nC to CE high setup time (t_{SRR})	Cfr figure 13 for timing diagram	40			ns
A0 to CE high setup time (t_{SAR})	Cfr figure 13 for timing diagram	40			ns
nCS to CE low hold time (t_{HSR})	Cfr figure 13 for timing diagram		0		ns
R_nC to CE low hold time (t_{HRR})	Cfr figure 13 for timing diagram		0		ns
A0 to CE low hold time (t_{HAR})	Cfr figure 13 for timing diagram	40			ns
D<9..0> delay from SCLK falling edge	Cfr figure 15 for timing diagram	4	10	25	ns

AC Characteristics

Unless otherwise stated: V_{DDD}=5V±5%, T_j=25°C, 13.2kSamples/s, analog input of 4.9V_{pp} at 1kHz; V_{DDD}=5V

Parameter	Condition	Min	Typ	Max	Units
Signal to Noise and distortion ratio (ENOB)	T_j=25°C ; external CK 200kHz T_j=225°C ; external CK 200kHz T_j=25°C ; internal CK T_j=225°C ; internal CK	9.1 - - -	9.47 9.35 9.30 9.13	9.6 - - -	dB
ENOB	T_j=25°C; external CK 200kHz -Vddd=4.75V -Vddd=5.00 -Vddd=5.25V		 9.31 9.47 9.55		dB

Analog to Digital transfer function can be generalized to all input ranges defining:

D= Digital value
A= Analog input value
Amin=lowest value of selected analog input range from

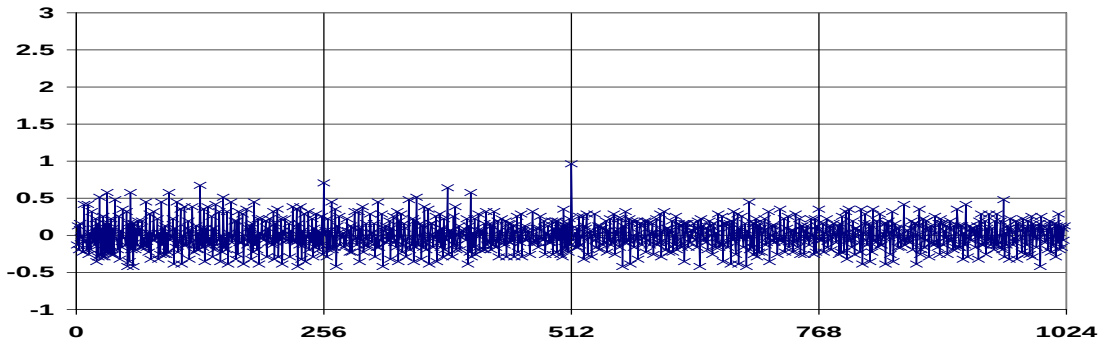
Ama_x=highest value of selected analog input range from
Offset= value of D when A=Amin. Offset value is independent of range.
GE=Gain-Error (in %). GE value is independent of range.

$$D=Offset+(A-A_{min})*(1024/(A_{max}-A_{min}))*(1-GE/100).$$

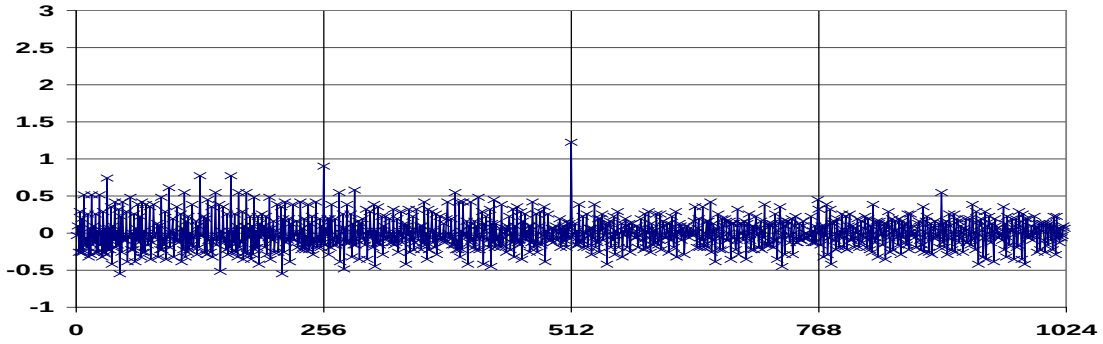
Equation 1

Typical Performance Characteristics

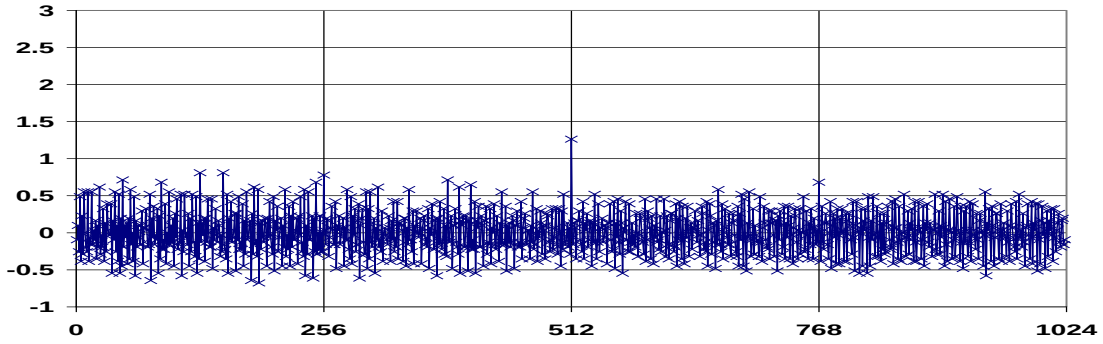
Typical DNL Characteristics (using external clock at 200kHz)



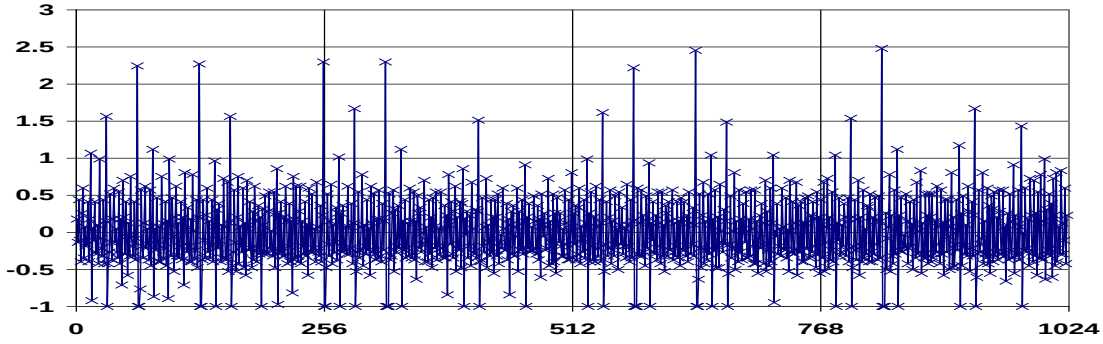
DNL [LSB] vs. digital code; -55°C – (external CK)



DNL [LSB] vs. digital code; 25°C – (external CK)



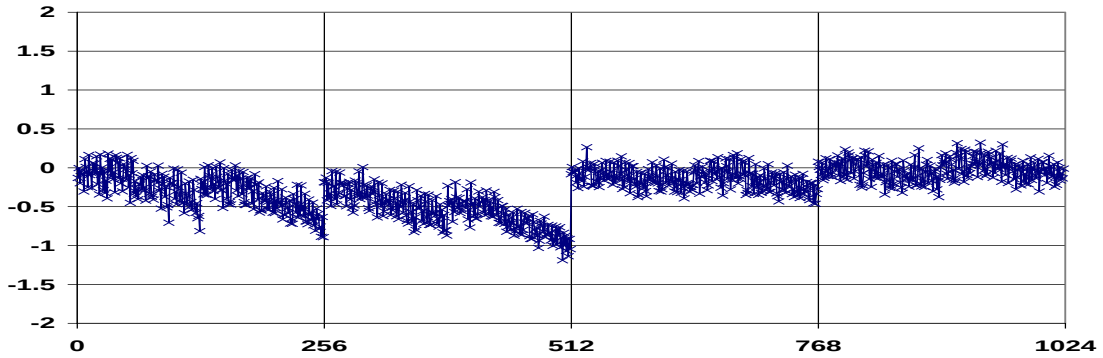
DNL [LSB] vs. digital code; 225°C – (external CK)



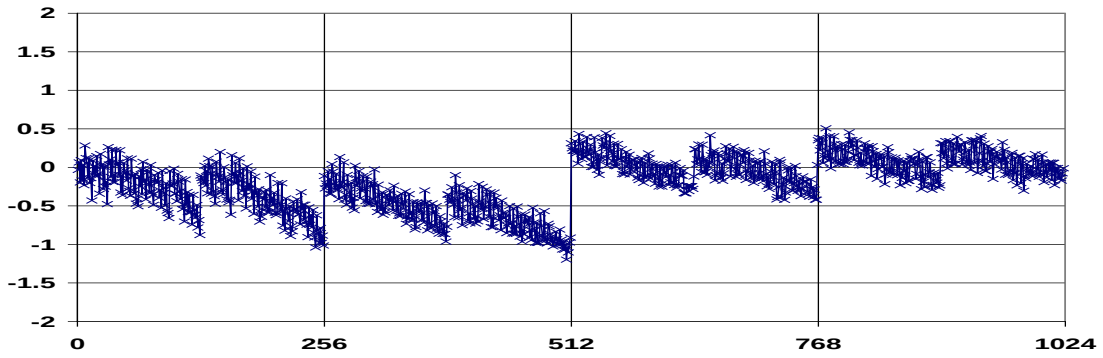
DNL [LSB] vs. digital code; 300°C – (external CK)

Figure 1

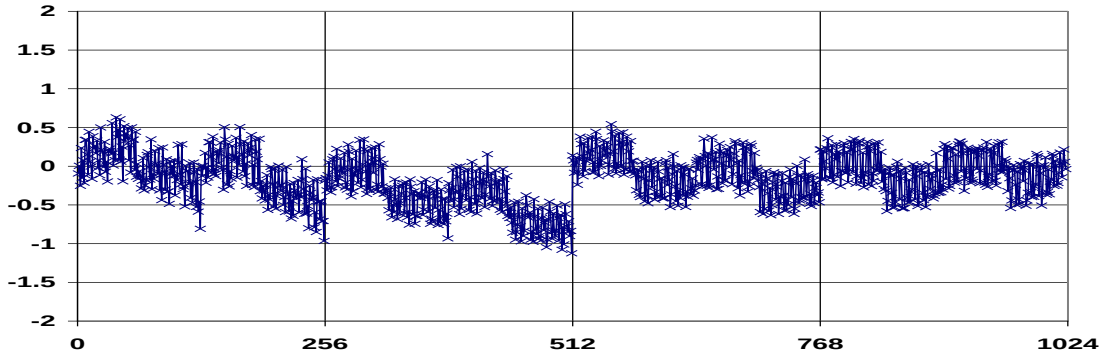
Typical INL Characteristics (using external clock at 200kHz)



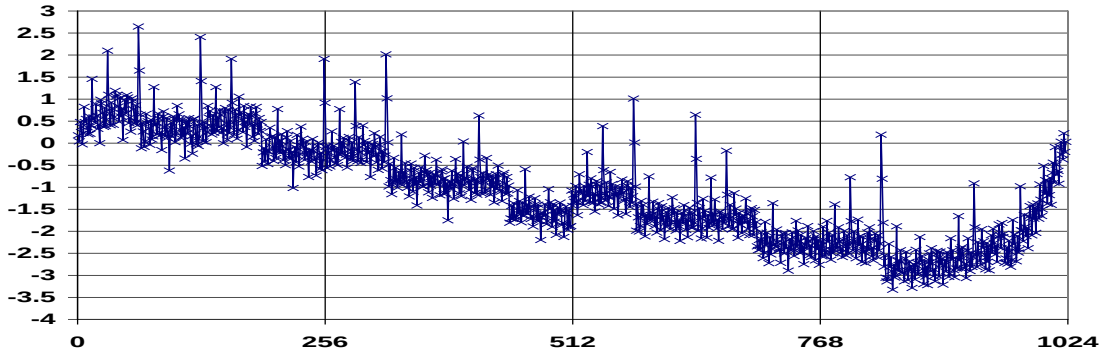
INL [LSB] vs. digital code; -55°C – (external CK)



INL [LSB] vs. digital code; 25°C – (external CK)



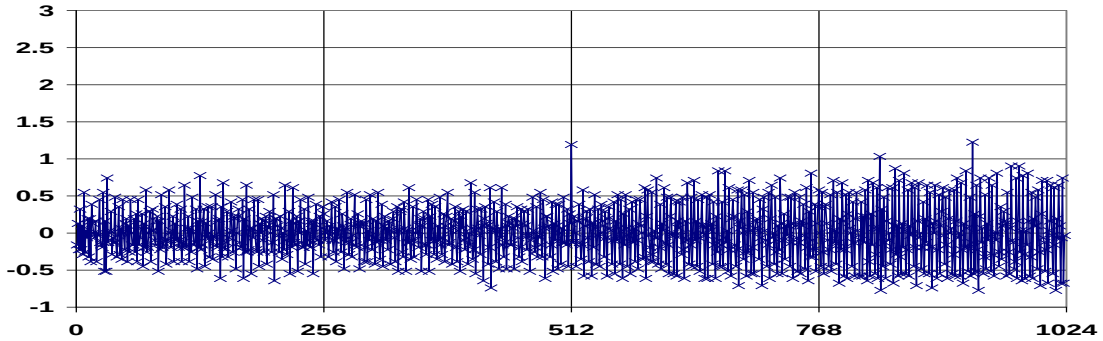
INL [LSB] vs. digital code; 225°C – (external CK)



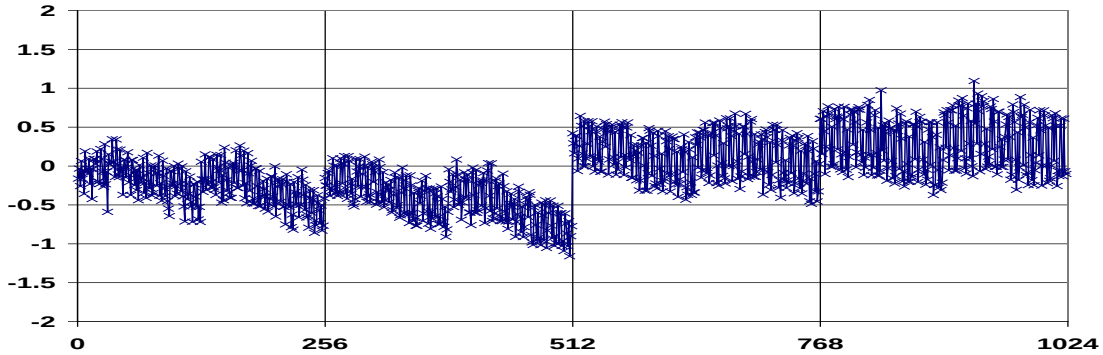
INL [LSB] vs. digital code; 300°C – (external CK)

Figure 2

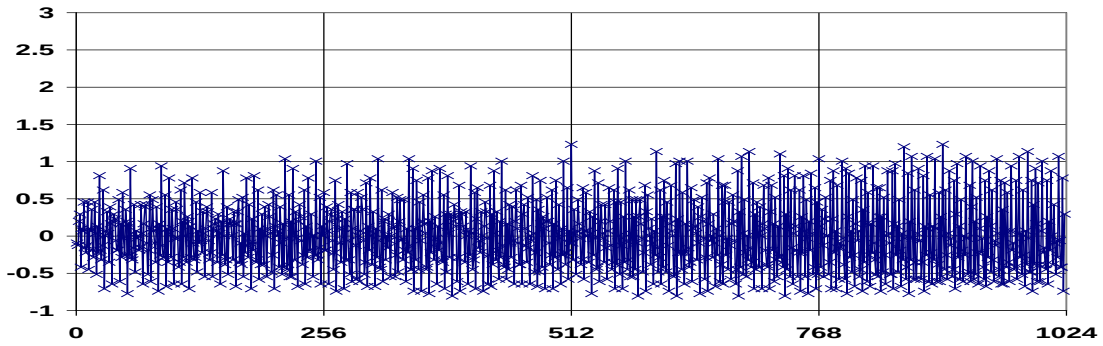
Typical DNL & INL Characteristics (using internal clock)



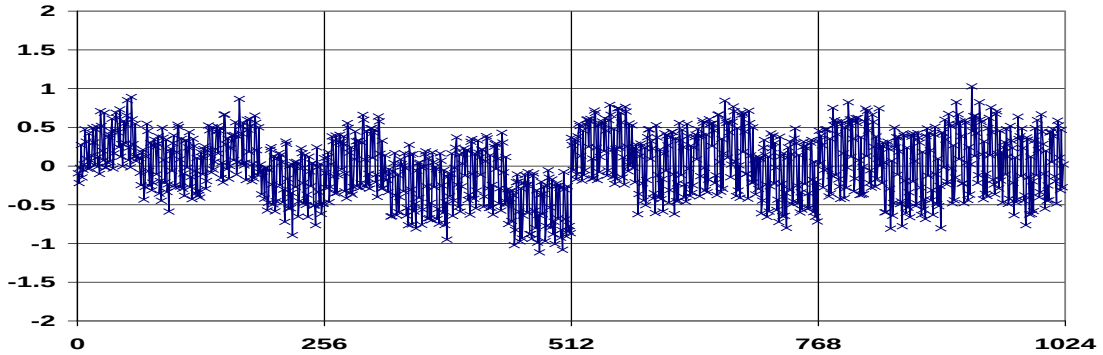
DNL [LSB] vs. digital code; 25°C – (internal CK)



INL [LSB] vs. digital code; 25°C – (internal CK)



DNL [LSB] vs. digital code; 225°C – (internal CK)



INL [LSB] vs. digital code; 225°C – (internal CK)

Figure 3

Static Characteristics

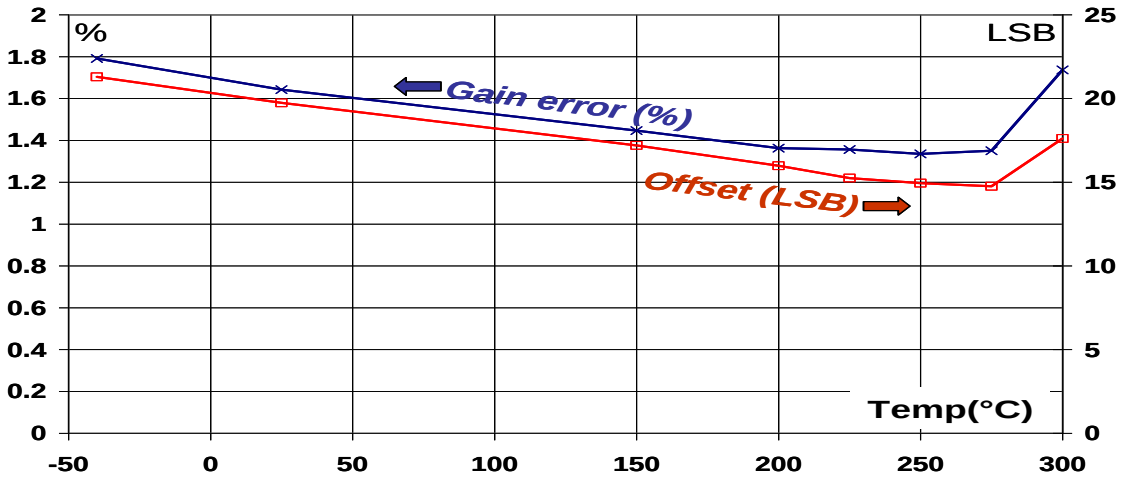


Figure 4: Typical Gain Error (%) and Offset (LSB) over temperature in [0…5]V range. External CK=200kHz

ADC transfer function is: D=Offset+A*(1024/5)*(1-(GainError/100))

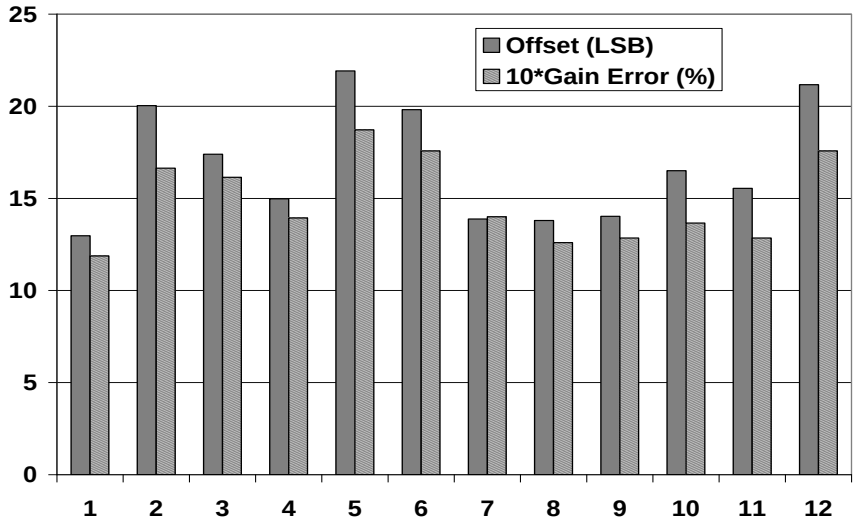


Figure 5: Gain Error (*10) and Offset (LSB) measured at 25°C on 12 samples from 2 different wafer batches. External CK=200kHz.

AC Characteristics

-Internal clock; [0…5]V range, input @1kHz; 4.9V_{pp}.

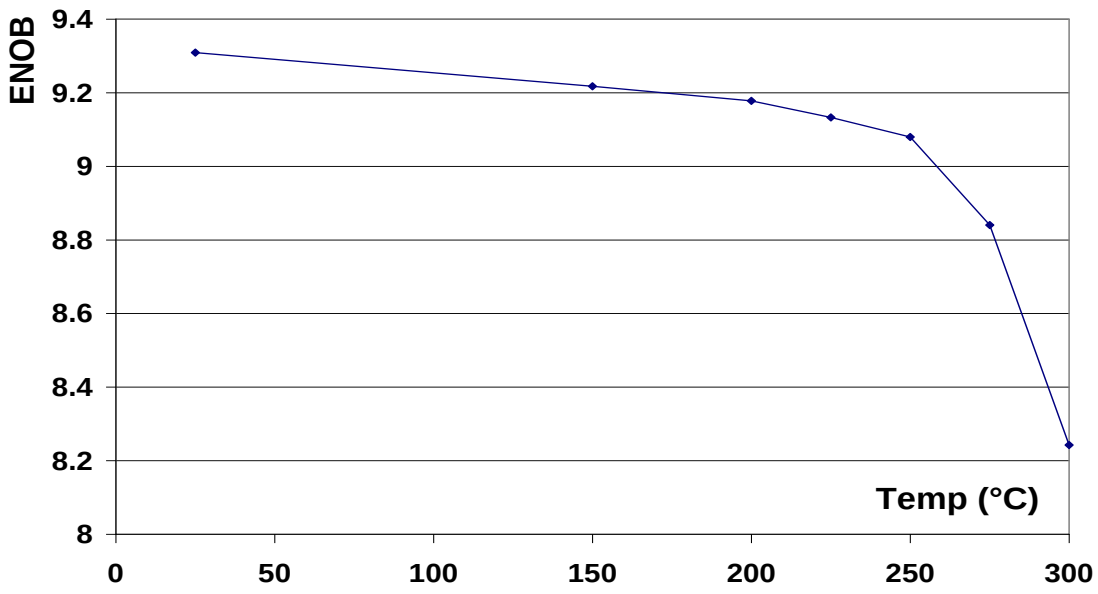


Figure 6: Typical ENOB (=S/(N+D)) over temperature; VDDD=5V

-External clock at 200kHz; [0…5]V range, input @1kHz; 4.9V_{pp}.

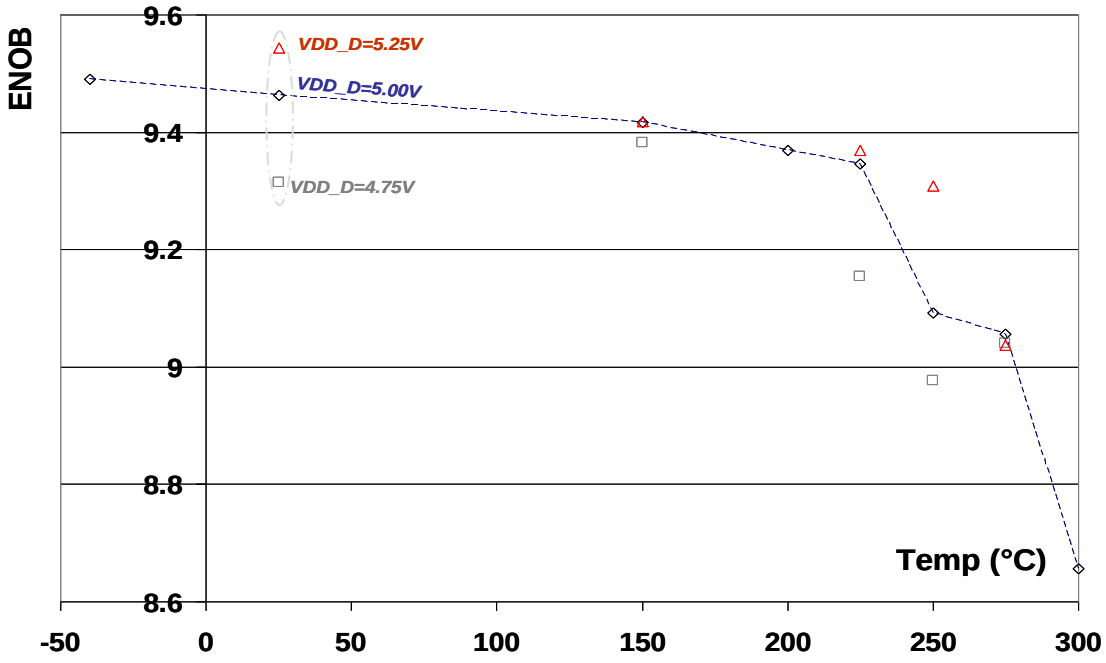


Figure 7: Typical ENOB over temperature; VDDD=4.75V; 5V; 5.25V

AC Characteristics

-External clock; [0…5]V range, input @1kHz; 4.9V_{pp}; V_{DDD}=5V

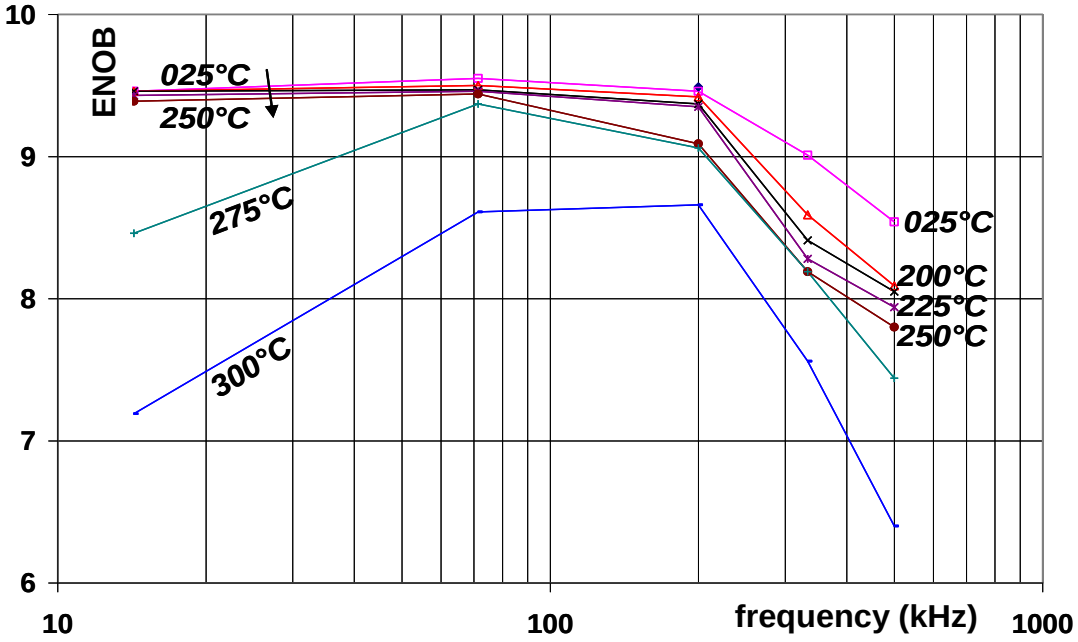


Figure 8: Typical ENOB over Temperature vs. external CK frequency

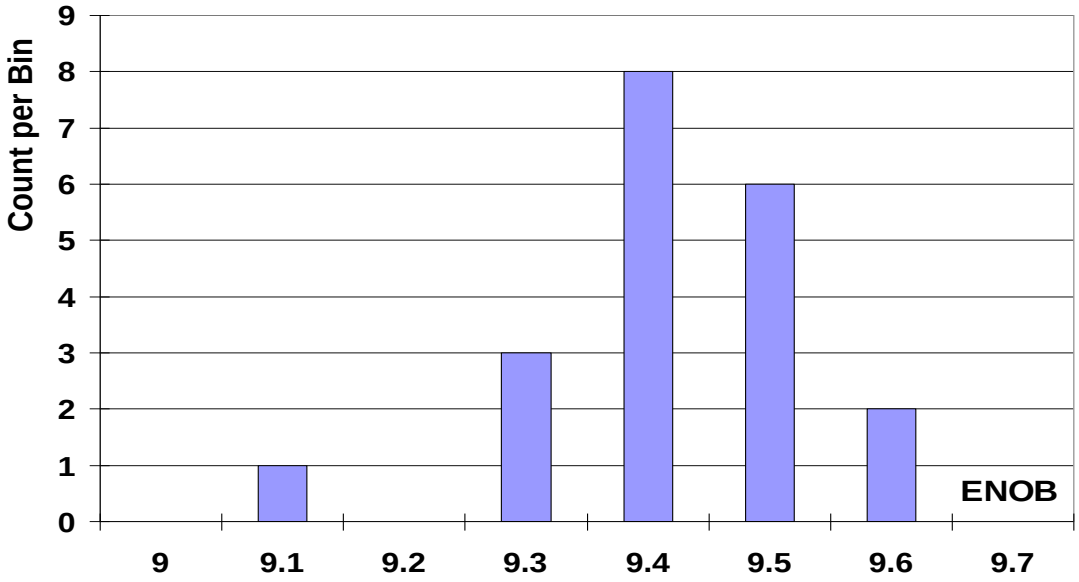
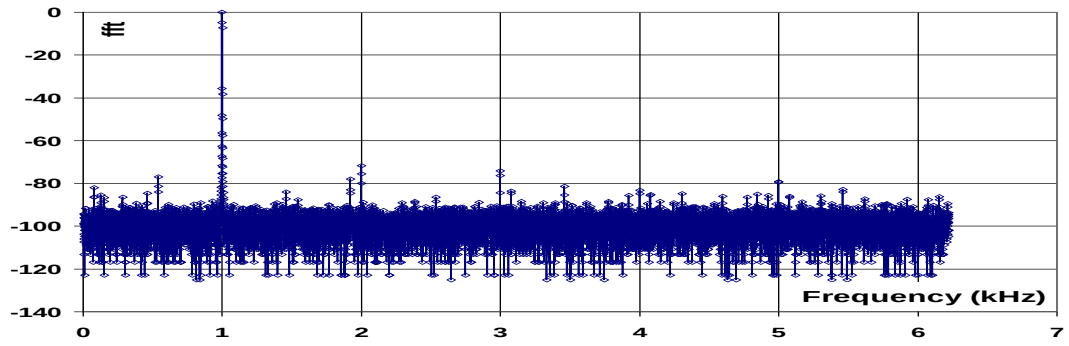


Figure 9: ENOB distribution measured at 25°C on 20 samples from 2 different wafer batches

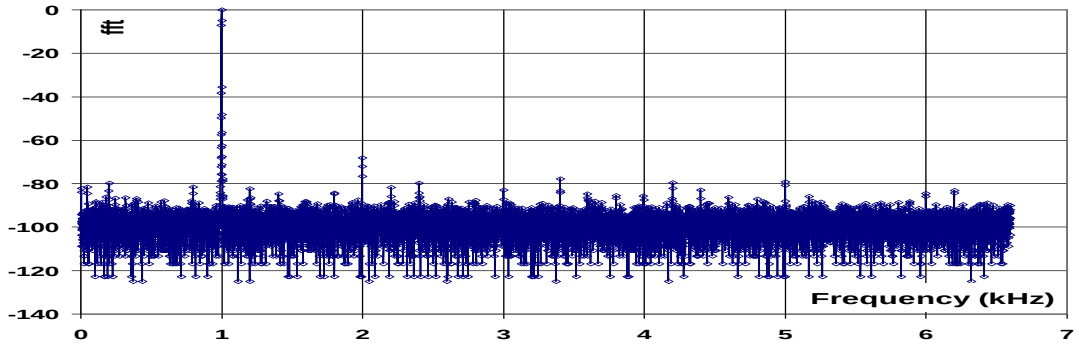
External CK=200kHz; 13.1kS/s

AC Characteristics

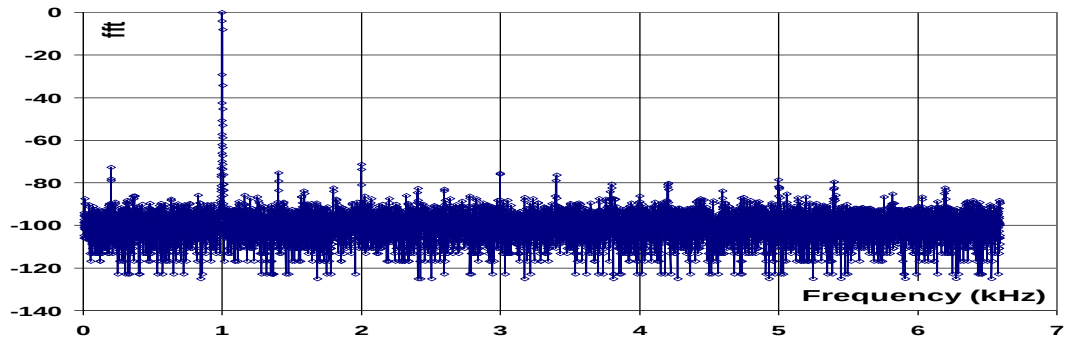
-External clock at 200kHz; [0…5]V range, input @1kHz; 4.9V_{pp}.



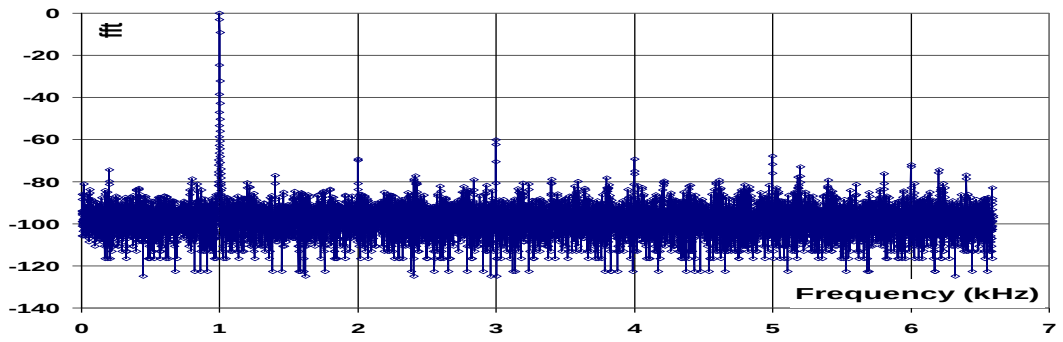
Normalized fft (dB) @ -55°C – 12.4kS/s (external CK)



Normalized fft (dB) @ 25°C – 13.1kS/s (external CK)



Normalized fft (dB) @ 225°C – 13.1kS/s (external CK)

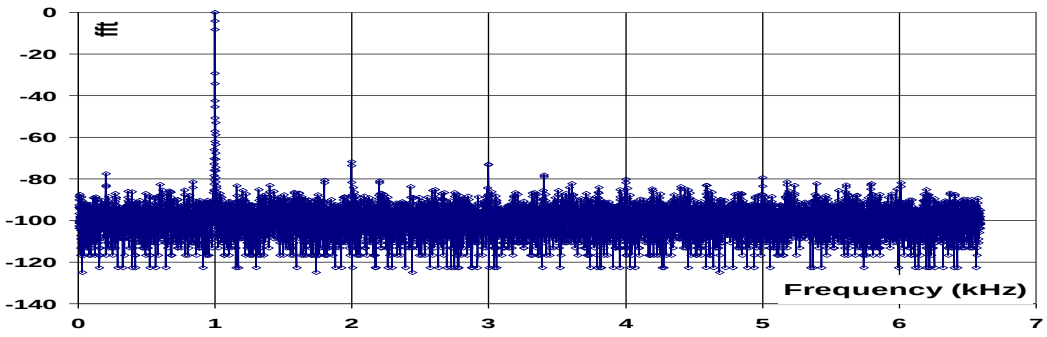


Normalized fft (dB) @ 300°C – 13.1kS/s (external CK)

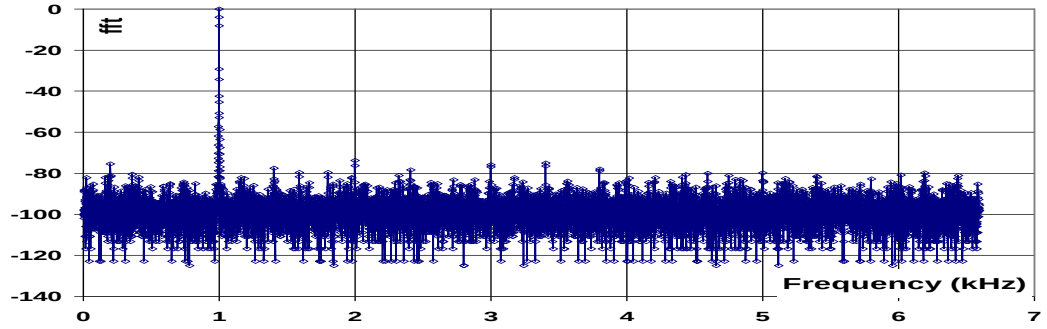
Figure 10

AC Characteristics

-Internal clock; [0…5]V range, input @1kHz; 4.9V_{pp}.



Normalized fft (dB) @ 25°C – 13.1kS/s (internal CK)



Normalized fft (dB) @ 225°C – 13.1kS/s (internal CK)

Figure 11

Circuit Functionality

Operating conditions

The CHT-ADC10 has been qualified for digital supply voltages from 4.75V to 5.25V and for an accurate and noise-free analog supply voltage of 5V.
The qualification temperature range extends from -55°C to +225°C, though functionality above +250°C is achieved with some derating of the characteristics.

Input scaling

The CHT-ADC10 allows operating with several possible input voltage ranges by properly connecting its 3 analog inputs (Vin_5; Vin_10; Vin_bip). Connecting them to the analog input voltage to be sampled, to Gnd_A or to Vdd_A allows setting different input voltage dynamic ranges. For a standard 0-5V range for example, the analog input is “Vin_5” pin whereas both other pins “Vin_10” and “Vin_bip” must be grounded. For other input ranges, please refer to the **Static Characteristics** table.

Circuit control

The CHT-ADC10 control logic includes standard protocol control signals (nCS, R_nC, CE, A0 and 10_n8) for communication with most µC. The CHT-ADC10 may operate in full µC control or in stand-alone mode. Full control protocols for the “conversion” and “read” cycles are shown in the figures below.

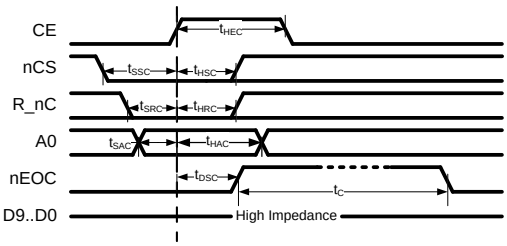


Figure 12. Conversion cycle timing.

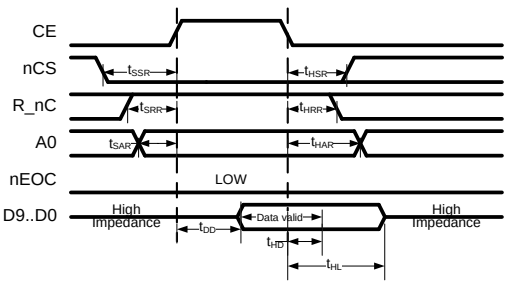


Figure 13. Read cycle timing.

In the stand-alone mode of operation, the converter is controlled only by means of the control signal R_nC. Signal CE must be connected to Vdd_D and signal nCS must be connected to Gnd_D. Control signals A0 and 10_n8 can be driven as desired or be hardwired according to the final application specifications.
The table below presents all possible operations based on all control lines combination.

CE	nCS	R_nC	10_n8	A0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiates a 10-bit conversion
↑	0	0	X	1	Initiates a 8-bit conversion
1	↓	0	X	0	Initiates a 10-bit conversion
1	↓	0	X	1	Initiates a 8-bit conversion
1	0	↓	X	0	Initiates a 10-bit conversion
1	0	↓	X	1	Initiates a 8-bit conversion
1	0	1	1	X	Enables 10-bit output
1	0	1	0	0	Enables 8 MSBs only
1	0	1	0	1	Enables 2 LSBs plus 6 trailing zeroes

Clock source selection

Either an external or the internal clock sources can be used. The external CK input must be grounded if the internal clock is used. If an external clock is used, it is strongly recommended to synchronize this external clock signal with the µC conversion request in order to avoid switching noise during the sampling period. In this case, CK should be kept “high” during the internal 10µs sampling period (see below). The presence of the external clock is automatically detected by an internal block, preventing the internal clock from starting. The external clock should be faster than 10kHz in order to avoid erroneous starting of internal clock. Also, at high temperature, slow clocks can lead to excessive discharge of the sampling capacitor over the conversion time. On the other side, external clocks faster than 500kHz strongly affects the ADC DNL.

Sampling period

The input sampling block includes a monostable set to 10µs (+/- 2µs). When an external µC initiates a conversion at time t0, the input voltage is sampled on an internal capacitor during 10µs. This means that the actual sampling always occurs after a constant delay of 10µs after the µC conversion request. During this 10µs sampling period, any noise on supplies should be avoided. If the internal (~250kHz) clock is used, this clock is only activated after this 10µs sampling period and delivers only 13 clock periods before going back to sleep-mode. If the serial interface is used, it is also recommended to turn off the ex-

ternal serial clock SCLK during the sampling and conversion periods.
During the 10µs sampling period, the "input sampling" block sets its input to 2.5V. This means that input impedance during this time period is about 200kΩ for [0-5V] input range setting. After the 10µs sampling period, the input sampling block can be considered as an open circuit, leading to an input impedance of about 400kΩ. Absolute impedance values can change up to 30% over temperature and from lot to lot. This is not critical for the ADC as it is based on ratios between resistors and not on their absolute values.

Conversion cycle

A conversion cycle is started whenever the following logic condition occurs:

(CE=HIGH)&(nCS=LOW)&(R_nC=LOW)

Conversion start is asserted by the rising edge of the condition above. Once the condition is set, conversion is not restarted provided that there is no new rising edge of the condition.
Depending on the value of A0 at the moment where the conversion start condition is asserted, either a 10bit (A0=LOW) or an 8bit (A0=HIGH) conversion cycle is executed. If an 8-bit conversion cycle is performed, the result is present in the 8 MSBs, with the remaining two LSBs set to zero. The value of A0 is latched with the rising edge of the conversion start condition.
During the conversion cycle, nEOC is HIGH and the parallel output bus is set to high-impedance state. Depending on the value of nCS, the serial data output can be at LOW (nCS=LOW) or high-impedance (nCS=HIGH) state.
Once the conversion cycle has finished nEOC returns to LOW and the conversion result is stored in the internal parallel and serial registers.

Reading output data

Once the conversion cycle ends, data can be read out through either any or both parallel and serial ports. Both parallel and serial output interfaces are always active together and can be used simultaneously.
To use the parallel port control signal 10_n8 must be accordingly set. If 10_n8 is HIGH, all 10 output lines are enabled at the same time allowing full data word transfer to a bus of at least 10bits. In this case A0 has no influence on the read data. If 10_n8 is LOW, output data is presented as a two 8-bit words. In this case only the output data bus must be set as in Figure 14. When A0=LOW, the 8 MSBs are presented to the bus. When A0=HIGH, the two remaining ADC LSBs are presented to the two MSBs of the data bus, with trailing zeroes on the 6 LSBs.

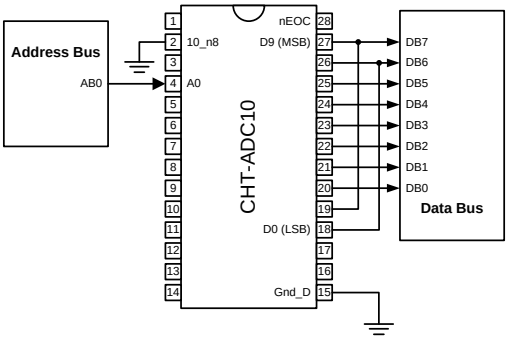


Figure 14. Left-justified 8-bit data bus.

To read the results of a conversion cycle through the serial port, the protocol shown in Figure 15 must be used. The protocol shown initiates a conversion cycled at the end of which the serial interface is used to read the results data.

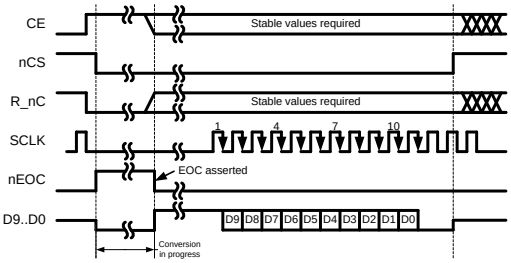


Figure 15. Conversion cycle and serial read protocol.

When using the series interface, SCLK should be stopped during the sampling and conversion periods. Once EOC is asserted, any falling edge on SCLK will produce the series register to shift data out starting by D9 (MSB). Once D0 (LSB has been shifted out of the register, any SCLK falling edge will continue to shift zeroes out of the series register until nCS returns back to HIGH state. Once a conversion has been finished, any falling edge on nCS reloads the series shift register with the result from the previous conversion as shown in next figure.

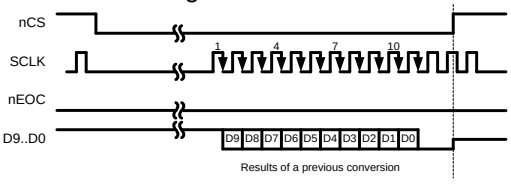
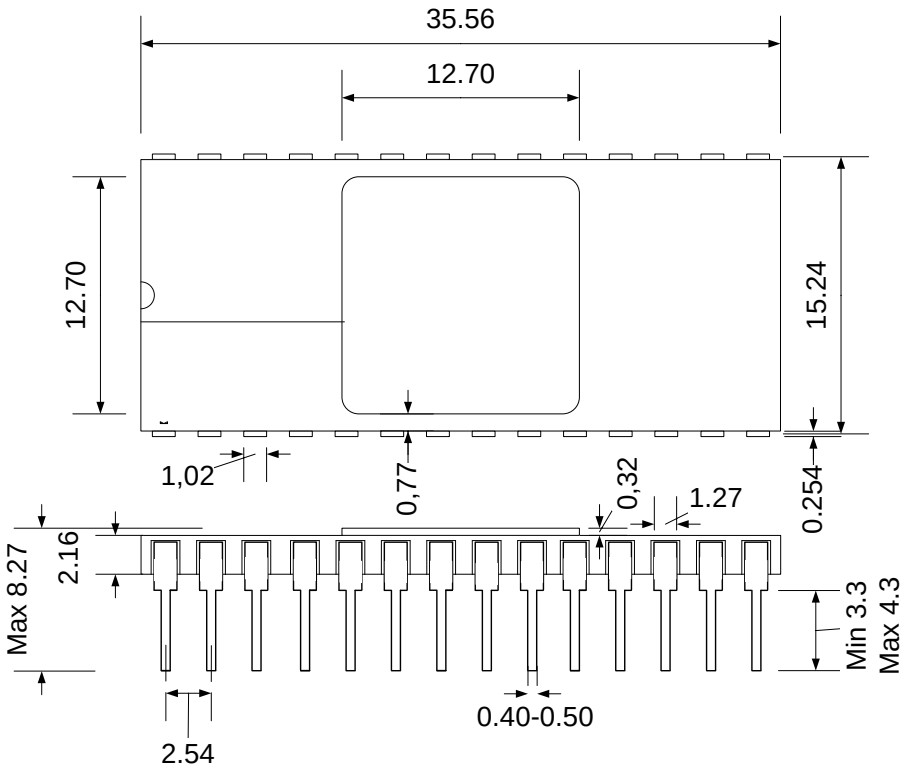
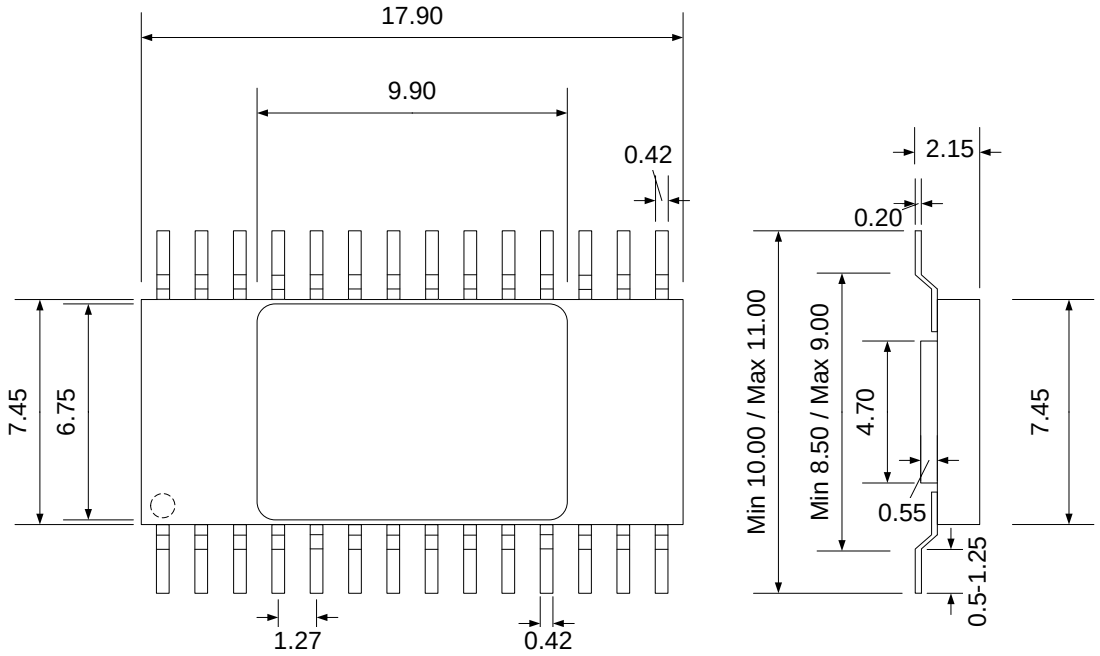


Figure 16. Reloading the results of a previous conversion.

Package Dimensions



Drawing CDIL28 (mm +/-10%)



Drawing CSOIC28 (mm +/-10%)

Contact & Ordering

CISSOID S.A.

Headquarters and contact EMEA:	CISSOID S.A. – Rue Francqui, 3 – 1435 Mont Saint Guibert - Belgium T : +32 10 48 92 10 - F: +32 10 88 98 75 Email: sales@cissoid.com
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