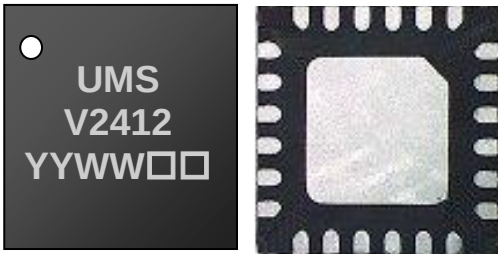
Fully integrated HBT K-Band VCO

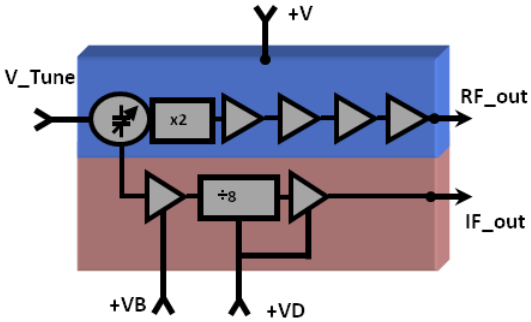
Description

The CHV2412-QDG is a monolithic multifunction for frequency generation. It integrates an X-band "push-push" oscillator with frequency control (VCO) thanks to base-collector diodes used as varactors, a K-band buffer amplifiers and a divider by 8. All the active devices are internally self-biased.

The circuit is delivered in a 24 Leads RoHS compliant QFN4x4 package.

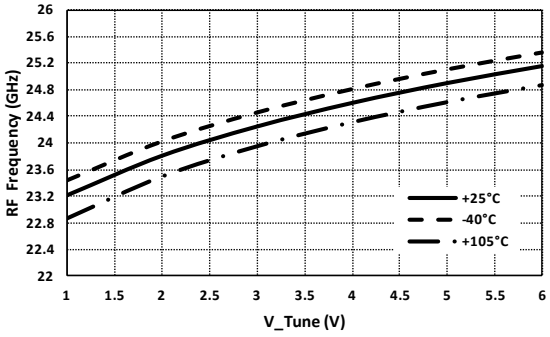


Plastic package



Main Features

- K-band VCO+K bufffers+Prescaler/8
- Fully integrated VCO (no need for external resonator)
- Low phase noise
- High temperature range
- High frequency stability
- On chip self-biased devices
- Standard SMD package: 24L-QFN4x4
- MSL1



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_out	Output frequency range on RF_out port	24.0	24.125	24.25	GHz
F_vco	VCO frequency	F_out/2			GHz
IF_out	Output Intermediate frequency	F_out/16			GHz
P_out	Output power on RF_out port	13	16		dBm
PFI	Output power at Intermediate freq. (IF)	-3	0		dBm
PN	SSB Phase Noise @F_out@100KHz		-90	-80	dBc/Hz

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Electrical Characteristics

VCO & buffer section

Symbol	Parameters	Min	Typ	Max	Unit
F_out	Output Frequency range (Operating band)	24		24.25	GHz
F_vco	VCO frequency		F_out/2		GHz
V_Tune	Voltage Tuning range	1		6	V
	Tuning sensitivity	250	400	725	MHz/V
	Frequency drift rate		5		MHz/°C
H1	Harmonics 1/2F_out			-40	dBc
H3	Harmonics 3/2 F_out			-40	dBc
H4	Harmonics 2 F_out			-20	dBc
PN	SSB Phase Noise given @ F_out @ 100 KHz		-90	-80	dBc/Hz
	Main Output (RF_Out) VSWR		2:1		
L_Pull	Load Pulling into 2:1 VSWR for all phases			8	MHz
PB_Pull	Prescaler & 12GHz buffer switching pulling		3		MHz
	Pushing @ within the V_tune range			250	MHz/V
P_out	Output Power on RF_out port @ 5V supply	13	16	19	dBm
	Positive supply current		140	170	mA

Prescaler section

Symbol	Parameters	Min	Typ	Max	Unit
IF_out	IF Output Frequency		F_out/16		GHz
	Output Power	-3	0		dBm
+ID	Prescaler positive supply current	15	26	40	mA
	Prescaler Output (IF) VSWR		2:1		
+IB	12GHz prescaler's buffer positive supply current	2	4	6	mA

General section

Symbol	Parameters	Min	Typ	Max	Unit
+V	Positive supply voltage (VB,V1,VB1,V2,VB2,VD)		5		V
+I	Total Positive supply current (IB+IB1+IB2+I1+I2+ID)		170	216	mA
Top	Operating temperature range	-40		+105	°C

All the parameters are specified between 1V and 6V of Tuning Voltage

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameters	Values	Unit
V_tune	Positive Tuning voltage	10	V
+V	Positive supply voltage Minimum supply voltage	6 -0.3	V
+ID	Positive supply current (Prescaler)	45	mA
+IB1 / +IB2	Positive supply current (buffers 2 & 3)	50 / 55	mA
+I1 / +I2	Positive supply current (VCO+ buffer 1)	35 / 50	mA
+IB	Positive supply current (prescaler's buffer)	7	mA
Top	Operating temperature range (2)	-40 to +105	°C
TcaseMax	Absolute maximum rating Tcase temperature (2)	115	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Temperature of the back side of the QFN package

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

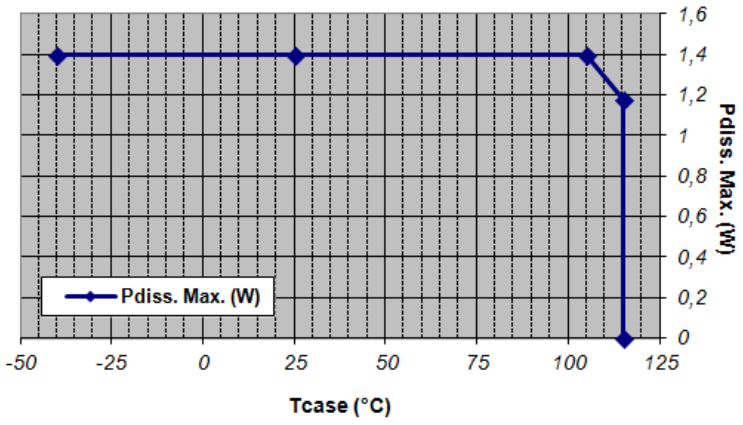
A derating must be applied on the dissipated power if the Tcase temperature cannot be maintained below the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

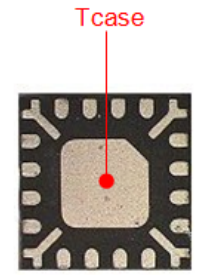
DEVICE THERMAL SPECIFICATION : CHV2412-QDG			
Recommended max. junction temperature (Tj max)		:	168 °C
Junction temperature absolute maximum rating		:	175 °C
Max. continuous dissipated power @ Tcase=	105 °C	:	1,4 W
=> Pdiss derating above Tcase(1)=	105 °C	:	22 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)		:	<44 °C/W
Minimum Tcase operating temperature(3)		:	-40 °C
Maximum Tcase operating temperature(3)		:	105 °C
Absolute maximum rating Tcase temperature(3)		:	115 °C
Minimum storage temperature		:	-55 °C
Maximum storage temperature		:	150 °C

(1) Derating at junction temperature constant = Tj max

*(2) Rth J-C is calculated for a worst case where the **hottest junction** of the MMIC is considered.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temeprature reference point (Tcase) on package's bottom side

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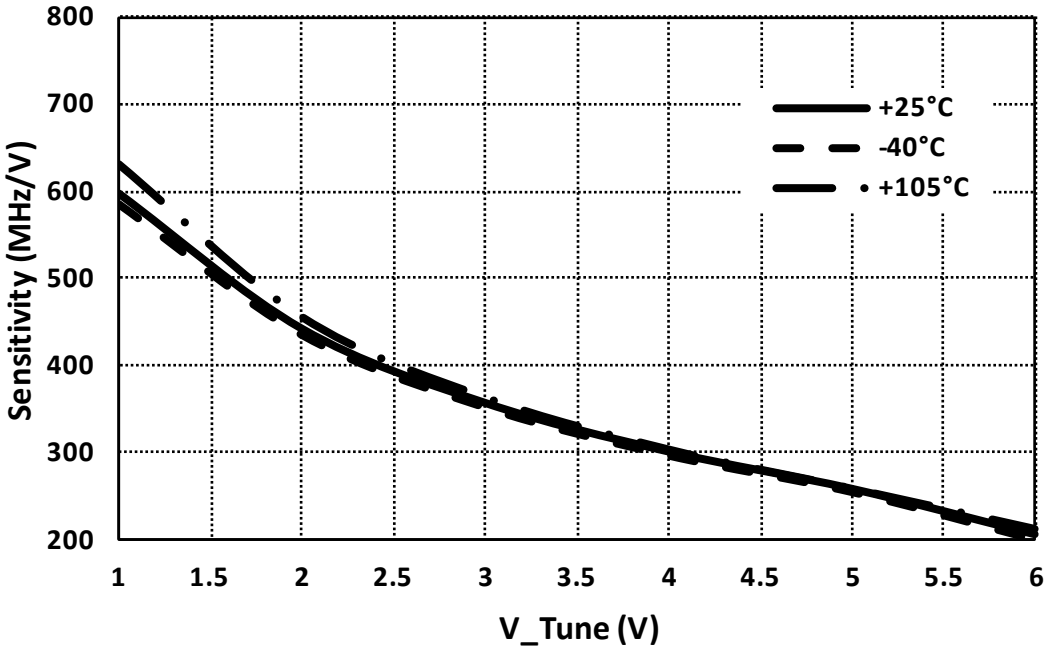
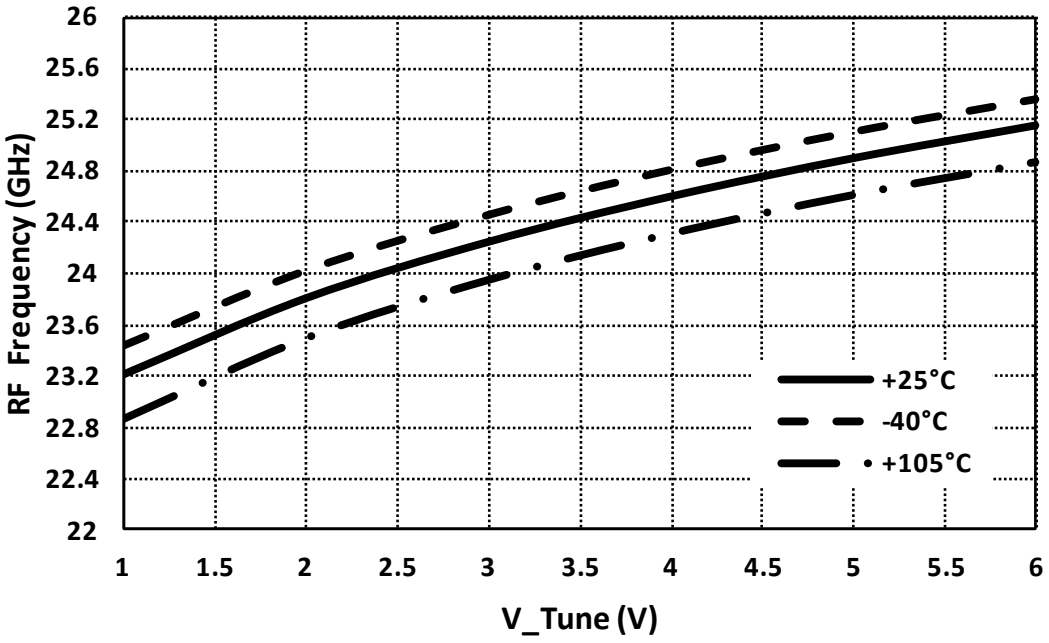
Typical QFN Measurements on board 500865 (at QFN accesses)

Note: The temperature mentioned below is taken at the back side of the QFN package

Sensitivity versus V-tune



RF Output Frequency versus V-tune



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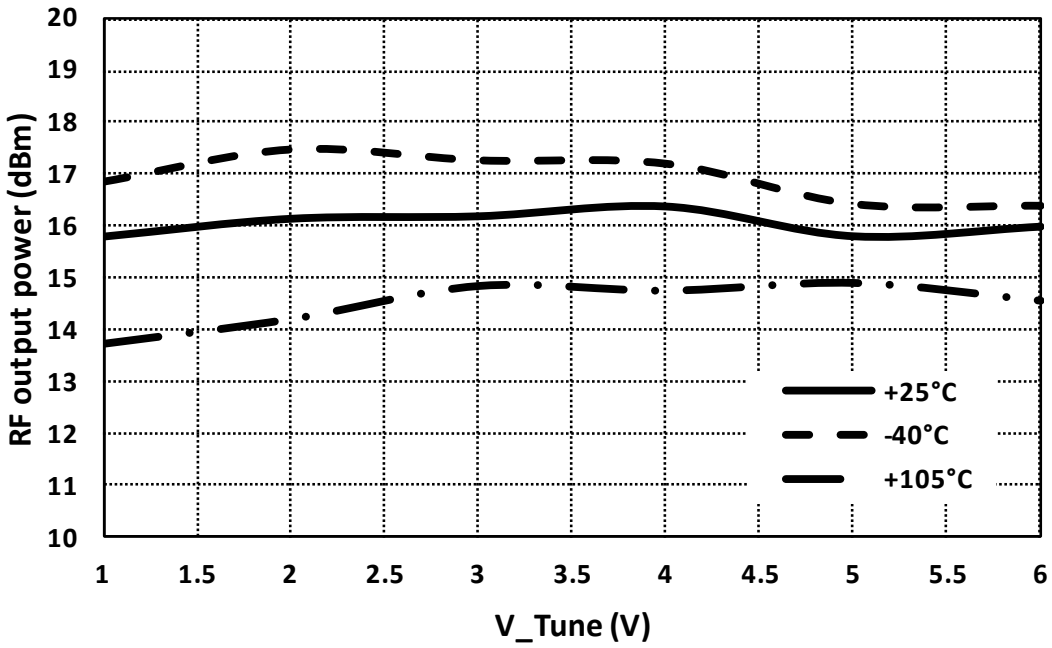
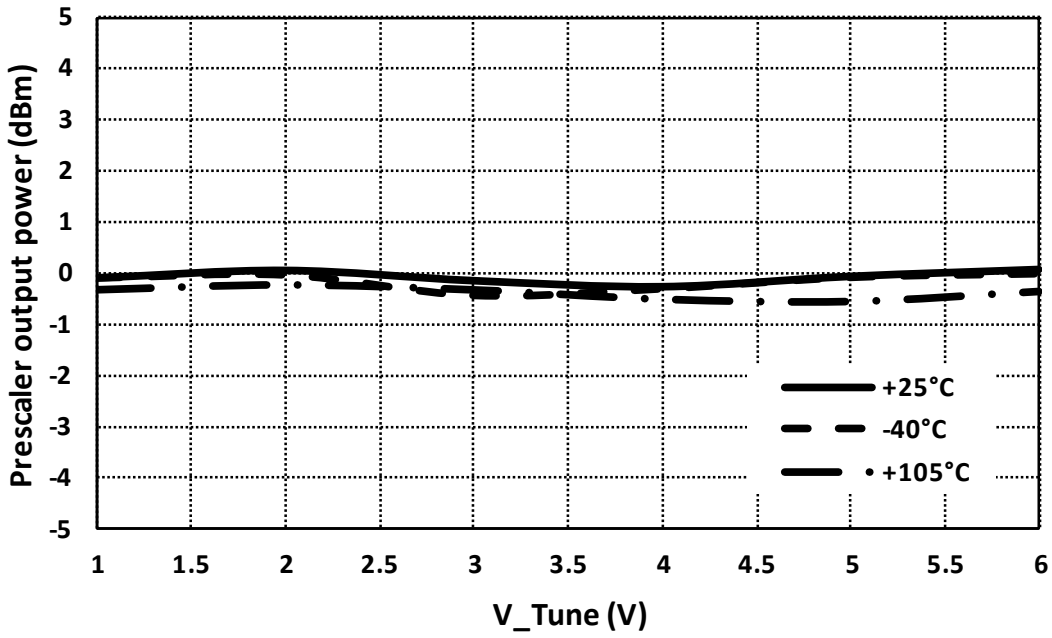
Typical QFN Measurements on board 500865 (at QFN accesses)

RF Output Power versus V-tune



IF Output Power versus V-tune



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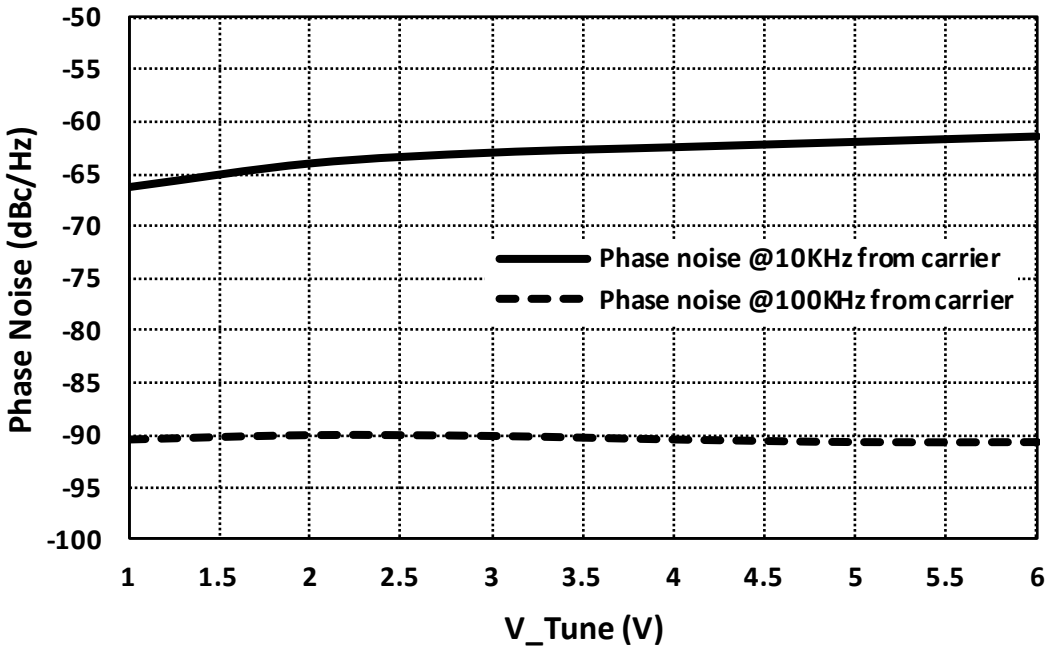
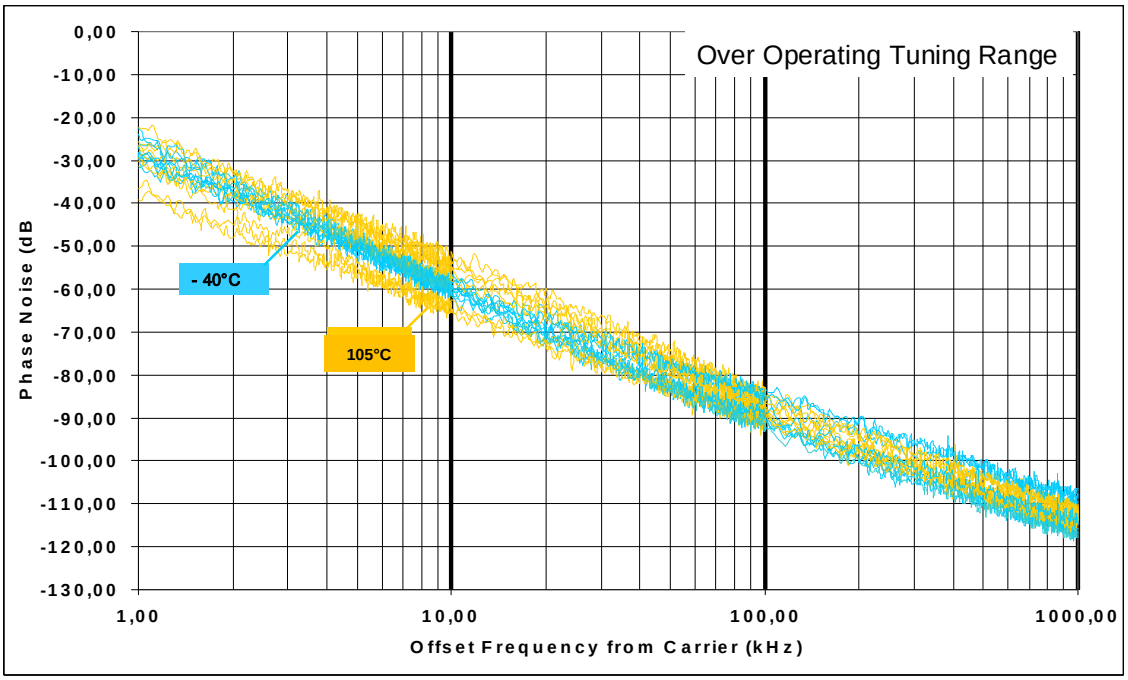
Typical QFN Measurements on board 500865 (at QFN accesses)

Phase Noise versus V-tune



Phase Noise versus Offset frequency



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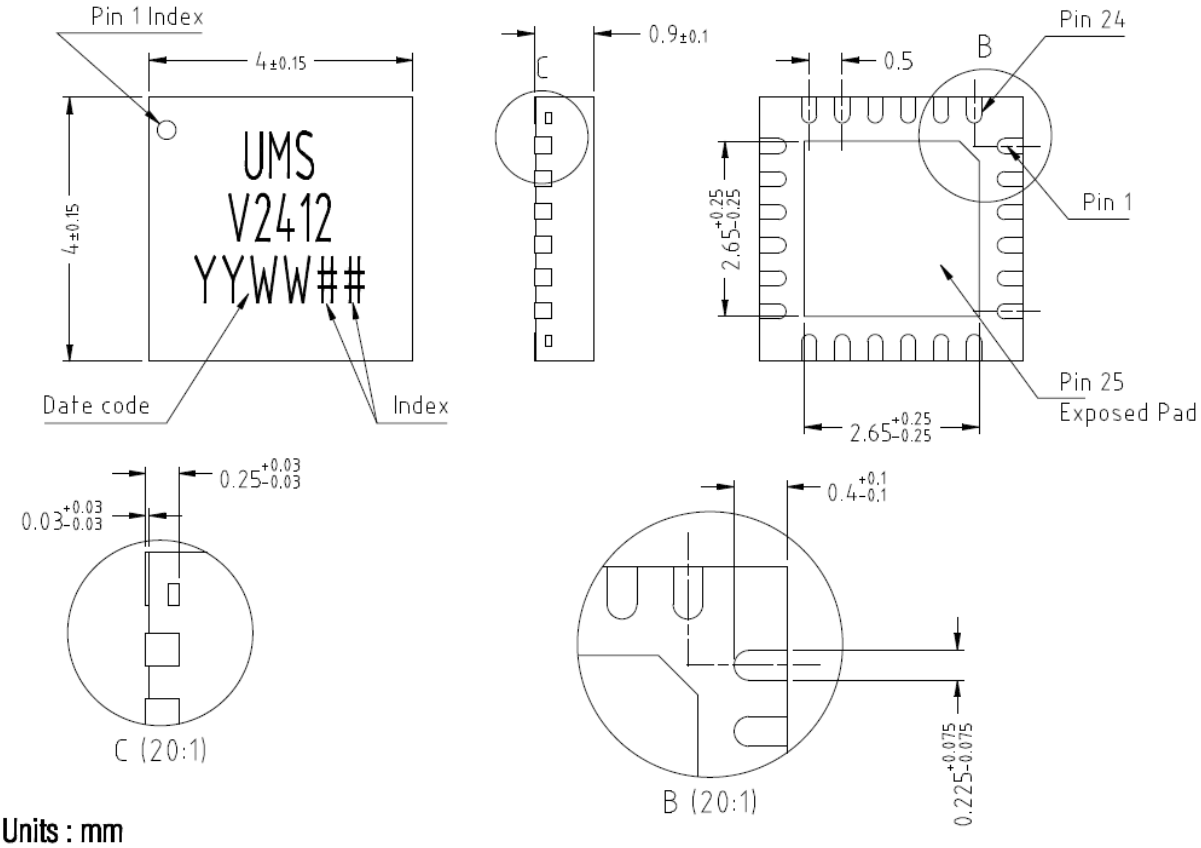
Package outline [1]



Units : mm
From the standard : JEDEC MO-220 [VGGD]

1- Nc	9- Nc	17- Gnd	25- Gnd
2- P	10- NC	18- Nc	
3- Nc	11- V1	19- Nc	
4- VT	12- Nc	20- VB2	
5- VB	13- VB1	21- V2	
6- Nc	14- Nc	22- Nc	
7- Nc	15- Gnd	23- VD	
8- Nc	16- RF	24- Nc	

[1]The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

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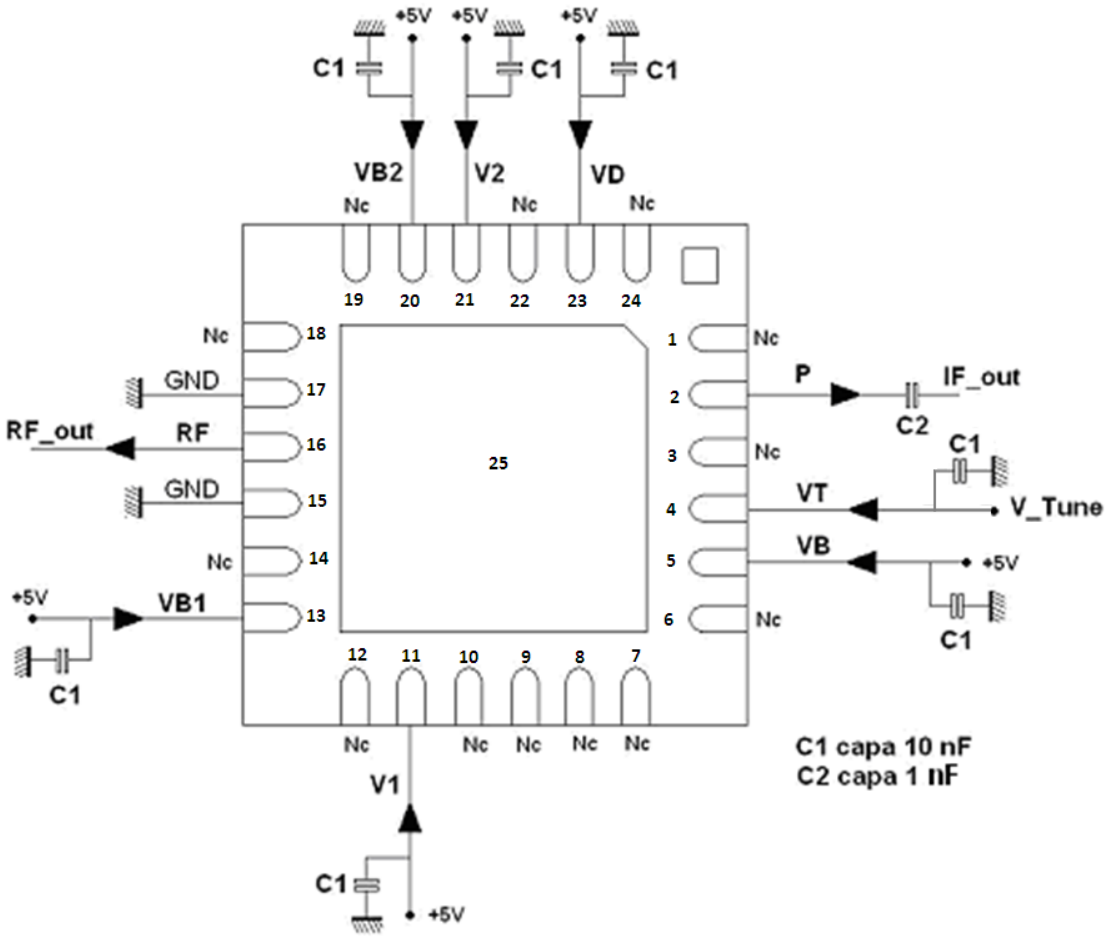
QFN Pin-out description

Pin number	Pin name	Symbol	Description
15,17	GND		Ground
2	P	IF_out	IF output at 1.5GHz
4	VT	V_Tune	Frequency Tuning Port
5, 11, 13, 20, 21, 23	VB, V1, VB1, VB2, V2, VD	+V	Positive supply voltage
5	VB		Positive supply voltage of 12GHz prescaler's buffer
11,21	V1,V2		Positive supply voltage of the VCO core +1st stage of the 24GHZ buffers
13	VB1		Positive supply voltage of the 2nd & 3rd stages of the 24GHZ buffers
16	RF	RF_out	RF output at 24GHz
1, 3, 6, 7, 8, 9, 10, 12, 14, 18, 19, 22, 24	Nc		Not connected

External Components and bias configuration (recommended)



Important: Need for a capacitor on the prescaler output port as a DC block (C2).

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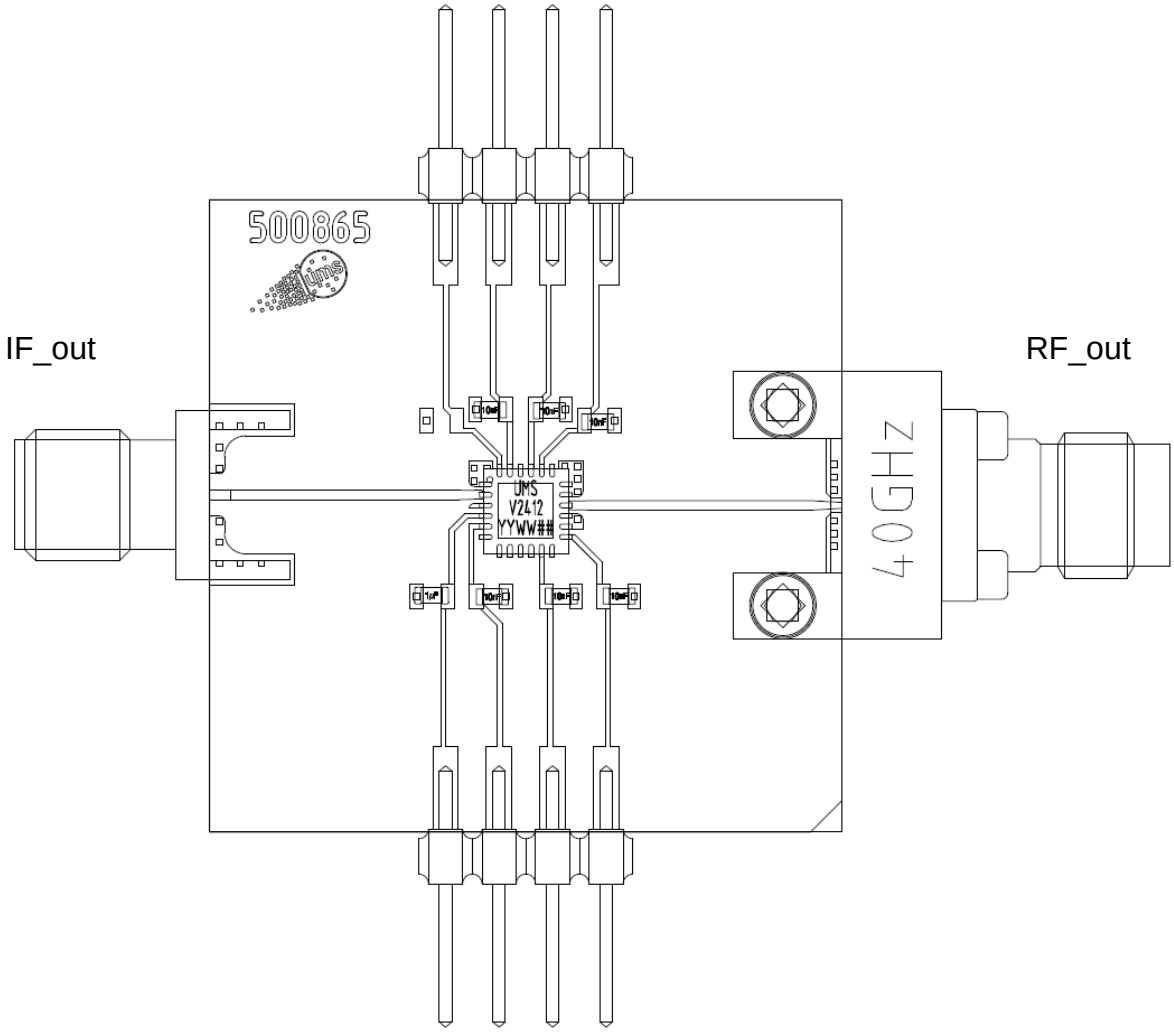
Evaluation mother board:

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.

Recommended Test Fixture (Ref. 500865) for measurements over Temperature Range



6 capacitors 0603 X7R (10nF)
1 capacitor 0603 X5R (1µF)

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:	CHV2412-QDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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