

13.5-40.5GHz Frequency Multiplier

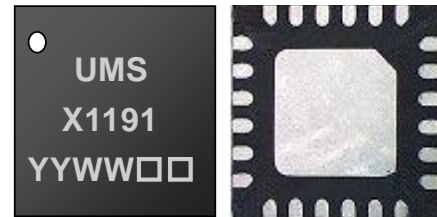
GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHX1191-QDG is a packaged monolithic time three multiplier which integrates input and output buffer.

This circuit is a very versatile multiplier for telecommunication and specifically for E-band LO chain. Moreover it is proposed in standard surface mount package and integrates ESD protection. The overall power supply is of +5V/ 80mA.

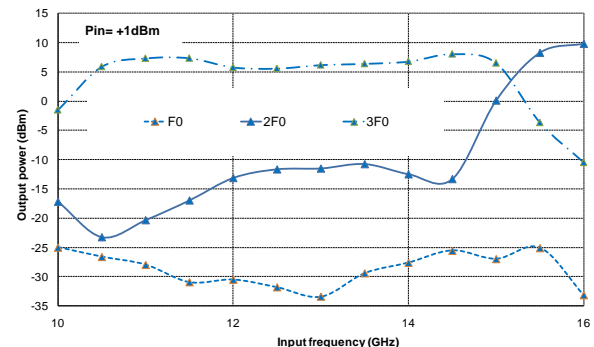
It is developed on a robust 0.15 μ m gate length pHEMT process, and will be available in a standard SMD package.



Main Features

Broadband performances: 11-14.5GHz

- 6dBm Pout for +1dBm input power
- DC bias: V+=5 Volts, V- = -5V@Id=80mA
- 24L-QFN4x4



Main Electrical Characteristics

Tamb.= +25°C

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------|---------------------------|-----|-----|------|------|
| Fin | Input frequency range | 11 | | 14.5 | GHz |
| Fout | Output frequency range | 33 | | 43.5 | GHz |
| Pin | Input power | | +1 | | dBm |
| Pout_H3 | 3rd harmonic output power | | 6 | | dBm |

Electrical Characteristics

Tamb.= +25°C, Vd = +5.0V

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------|---------------------------|------|-----|------|------|
| Fin | Input frequency range | 11.0 | | 14.5 | GHz |
| Fout | Output frequency range | 33.0 | | 43.5 | GHz |
| Pin | Input power | | +1 | | dBm |
| Pout_H3 | 3rd harmonic output power | | 6 | | dBm |
| Rej_H1 | Fundamental rejection | | 35 | | dBc |
| Rej_H2 | 2nd harmonic rejection | | 16 | | dBc |
| RL_in | Input return loss | | -12 | | dB |
| RL_out | Output return loss | | -14 | | dB |
| V+ | DC positive voltage | | +5 | | V |
| V- | DC negative voltage | | -5 | | V |
| Id | DC current | | 80 | | mA |

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

| Symbol | Parameter | Values | Unit |
|--------|-----------------------------|-------------|------|
| V+ | Positive bias voltage | 5.5 | V |
| V- | Negative bias current | -6 | V |
| Id | DC current | 120 | mA |
| Pin | Maximum input power | +6 | dBm |
| Tj | Junction temperature | 175 | °C |
| Ta | Operating temperature range | -40 to +95 | °C |
| Tstg | Storage temperature range | -55 to +150 | °C |

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).

The temperature is monitored at the package back-side interface (T_{case}) as shown below.

The system maximum temperature must be adjusted in order to guarantee that T_{case} remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

A derating must be applied on the dissipated power if the T_{case} temperature can not be maintained below than the maximum temperature specified (see the curve $P_{diss. Max.}$) in order to guarantee the nominal device life time (MTTF).

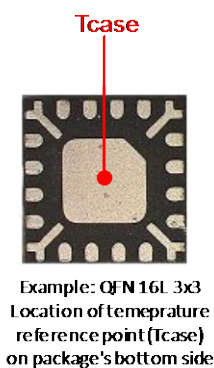
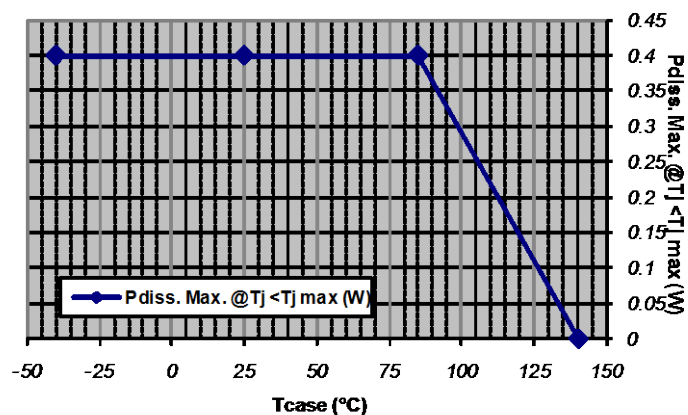
DEVICE THERMAL SPECIFICATION : CHX1191-QDG

| | |
|--|-------------|
| Recommended max. junction temperature (T_J max) | : 140 °C |
| Junction temperature absolute maximum rating | : 175 °C |
| Max. continuous dissipated power ($P_{diss. Max.}$) | : 0.4 W |
| => $P_{diss. Max.}$ derating above $T_{case}^{(1)} = 85$ °C | : 7 mW/°C |
| Junction-Case thermal resistance ($R_{th J-C}$) ⁽²⁾ | : <138 °C/W |
| Minimum T_{case} operating temperature ⁽³⁾ | : -40 °C |
| Maximum T_{case} operating temperature ⁽³⁾ | : 85 °C |
| Minimum storage temperature | : -55 °C |
| Maximum storage temperature | : 150 °C |

(1) Derating at junction temperature constant = T_J max.

(2) $R_{th J-C}$ is calculated for a worst case considering the **hottest junction** of the M M IC and all the devices biased.

(3) T_{case} = P package back side temperature measured under the die-attach-pad (see the drawing below).



6.4

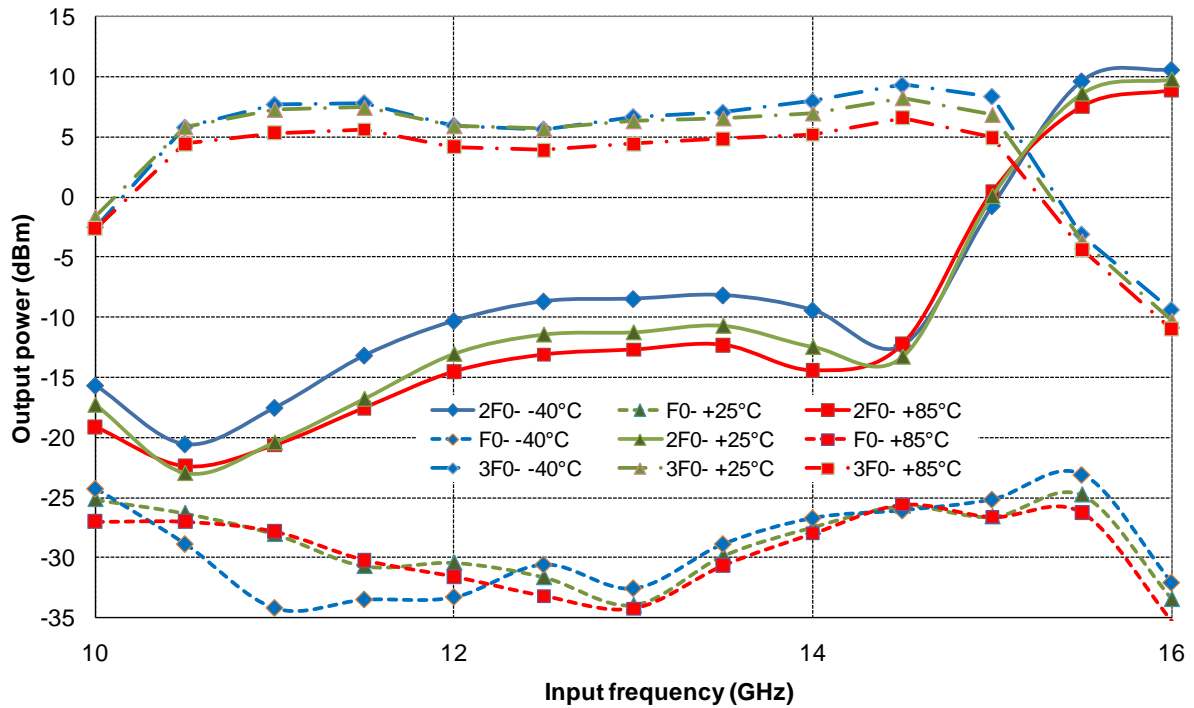
Typical Board Measurements

Tamb.= +25°C, V+ = +5.0V, Id = 80mA

Results are given in the package access planes

Harmonic output power versus frequency

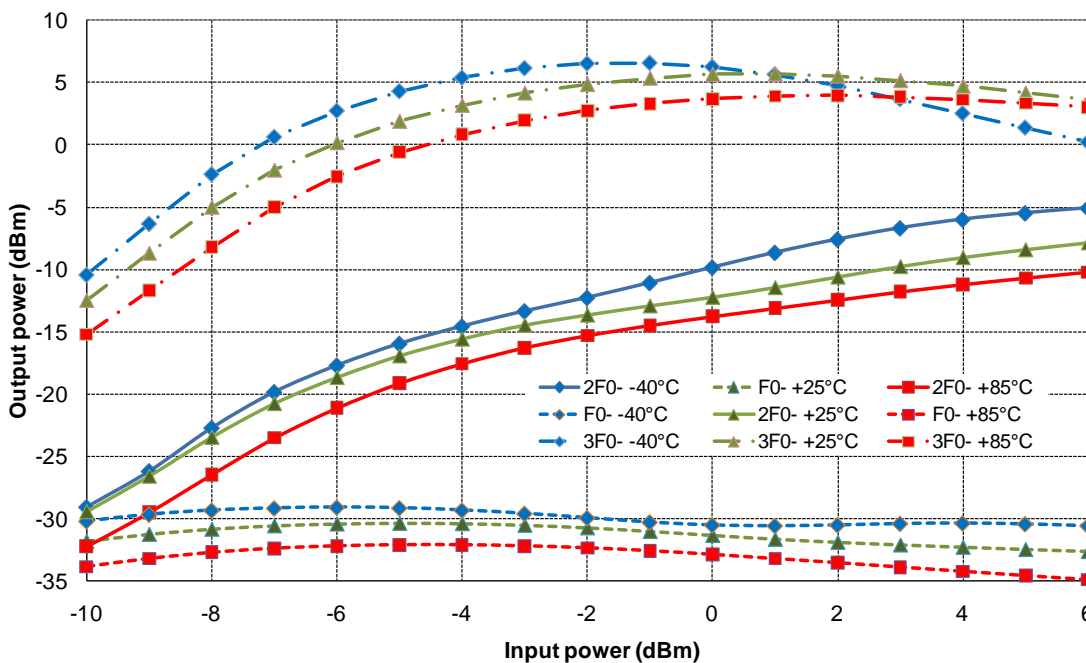
Pin= +1dBm



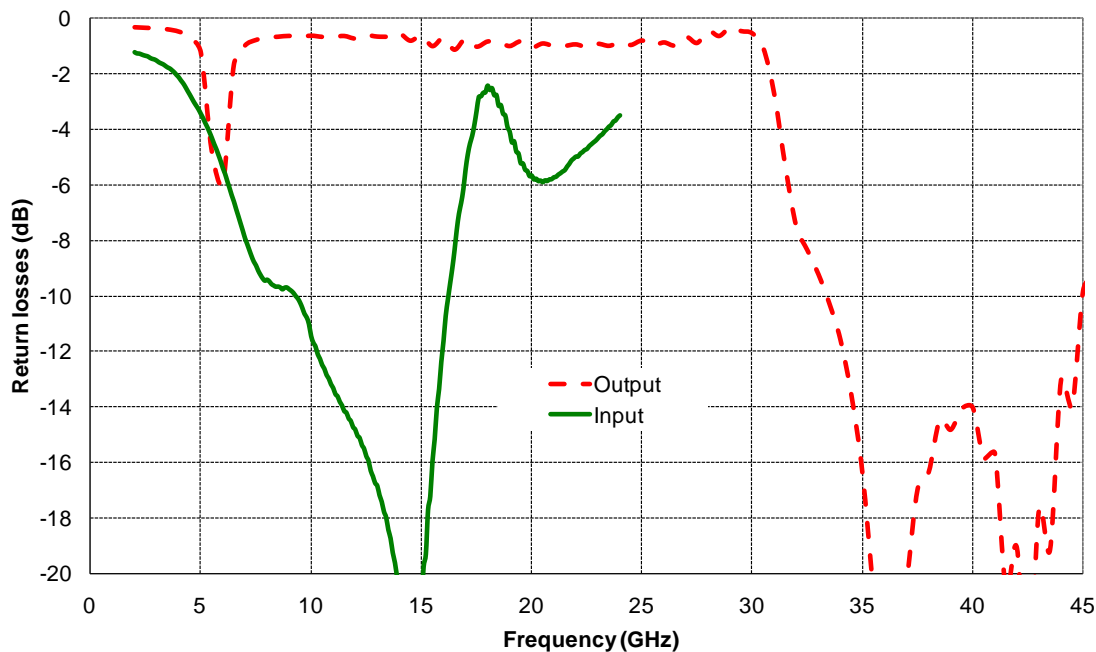
Typical Board Measurements

Tamb.= +25°C, V+ = +5.0V, Id = 80mA

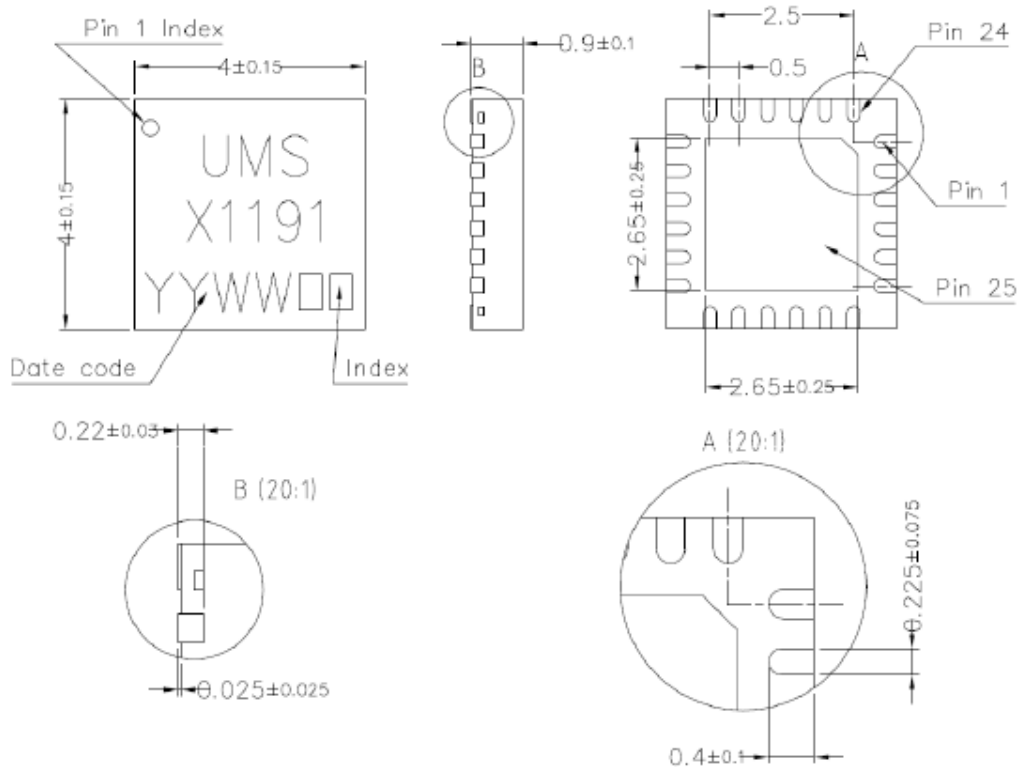
Harmonic output power versus input power
F0=12.5GHz



Input & Output return loss



Package outline ⁽¹⁾



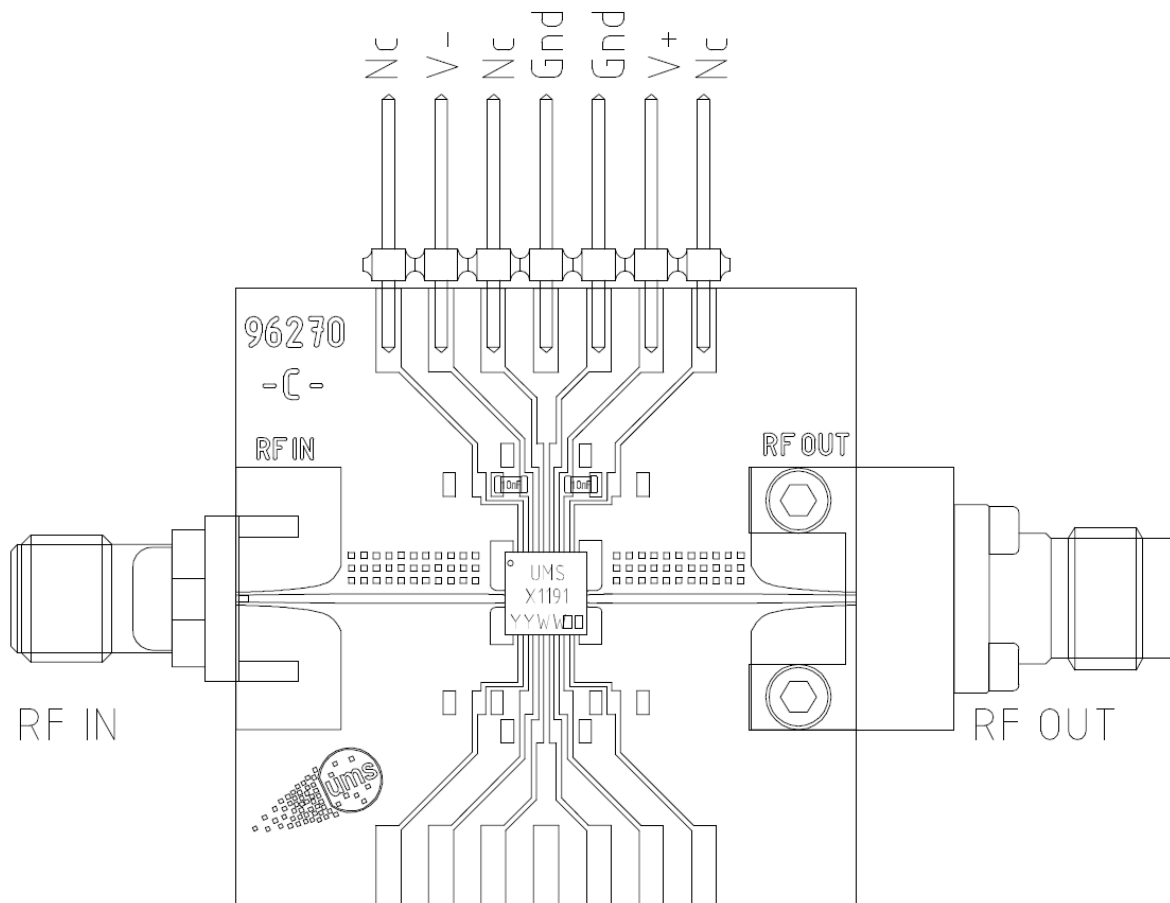
| | | | | |
|---------------------|------------------------|-----------------------|------------------------|------------------------|
| Matt tin, Lead Free | (Green) | 1- Nc | 9- Nc | 17- Gnd ⁽²⁾ |
| Units : | mm | 2- Gnd ⁽²⁾ | 10- Nc | 18- Nc |
| From the standard : | JEDEC MO-220 (VGGD) | 3- Gnd ⁽²⁾ | 11- Nc | 19- Nc |
| | 25- GND | 4- RF in | 12- Nc | 20- V+ |
| | | 5- Gnd ⁽²⁾ | 13- Gnd ⁽²⁾ | 21- Gnd ⁽²⁾ |
| | | 6- Gnd ⁽²⁾ | 14- Gnd ⁽²⁾ | 22- Nc |
| | | 7- Nc | 15- RF out | 23- V- |
| | | 8- Nc | 16- Gnd ⁽²⁾ | 24- Nc |

⁽¹⁾ The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<https://www.ums-rf.com>) for exact package dimensions.

⁽²⁾ It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

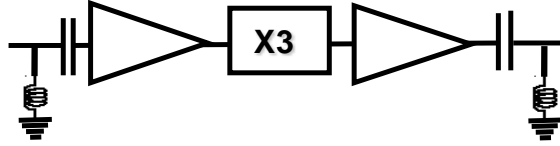
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF \pm 10% are recommended for all DC accesses.
- See application note AN0017 for details.



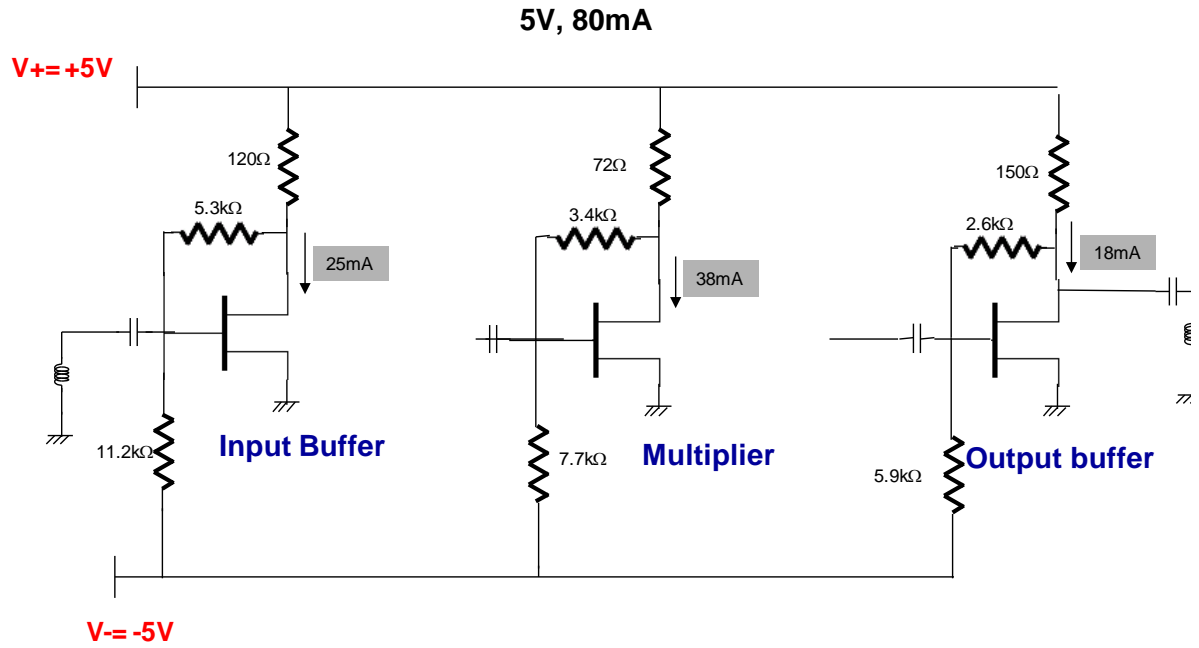
Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (10nF) on the PC board, as close as possible to the package.

DC Schematic



Recommended package footprint

Refer to the application note AN0017 available at <https://www.ums-rf.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:

CHX1191-QDG/XY

Stick: XY = 20

Tape & reel: XY = 21

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