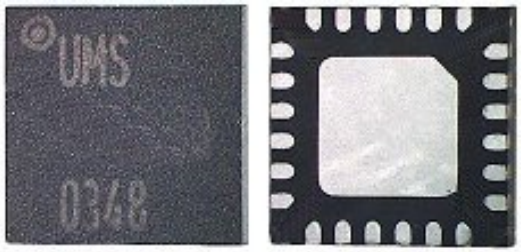
CHX2090-QDG

12-24GHz Frequency Multiplier

GaAs Monolithic Microwave IC in SMD leadless package

Description

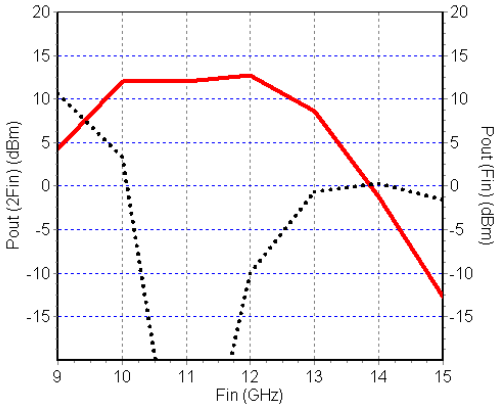
The CHX2090-QDG is a cascadable frequency doubler monolithic circuit, which integrate an output buffer amplifier that produces a constant output power over a range of input powers. It is designed for a wide range of applications, from military to commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 11-13GHz
- 13dBm output power for +14dBm input power
- DC bias: Vd=3.5Volt@Id=65mA
- 24L-QFN4x4 SMD package

Typical Measurement



Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	11		13	GHz
Fout	Output frequency range	22		26	GHz
Pin	Input power		14		dBm
Pout	Output power for +14dBm input power		13		dBm

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

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Electrical Characteristics

Tamb = +25°C, Vd = 3.5V, Vg1 = -0.9V, Vg2 tuned for Id=65mA.

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	11		13	GHz
Fout	Output frequency range	22		26	GHz
Pin	Input power		14		dBm
Pout 2Fin	2Fin Output power for (11 < Fin < 12GHz) for Fin = 13GHz		12 9		dBm dBm
Is/Fin	Fin level at the output for (11 < Fin < 12) for Fin = 13GHz		-10 0		dBm dBm
Is/3Fin	3Fin level at the output		-15		dBm
VSWRin	Input VSWR			2.0:1	
VSWRout	Output VSWR			2.5:1	
Vd	Drain voltage		3.5		V
Id	Bias current		65	75	mA

Absolute Maximum Ratings

Tamb.= 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	5V	V
Id	Drain bias current	120	mA
Vg	Gate bias voltage	-2 to +0.4	V
Tj	Junction temperature (2)	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Thermal Resistance channel to ground paddle =249°C/W for Tamb. = +85°C with 3.5V & 65mA.

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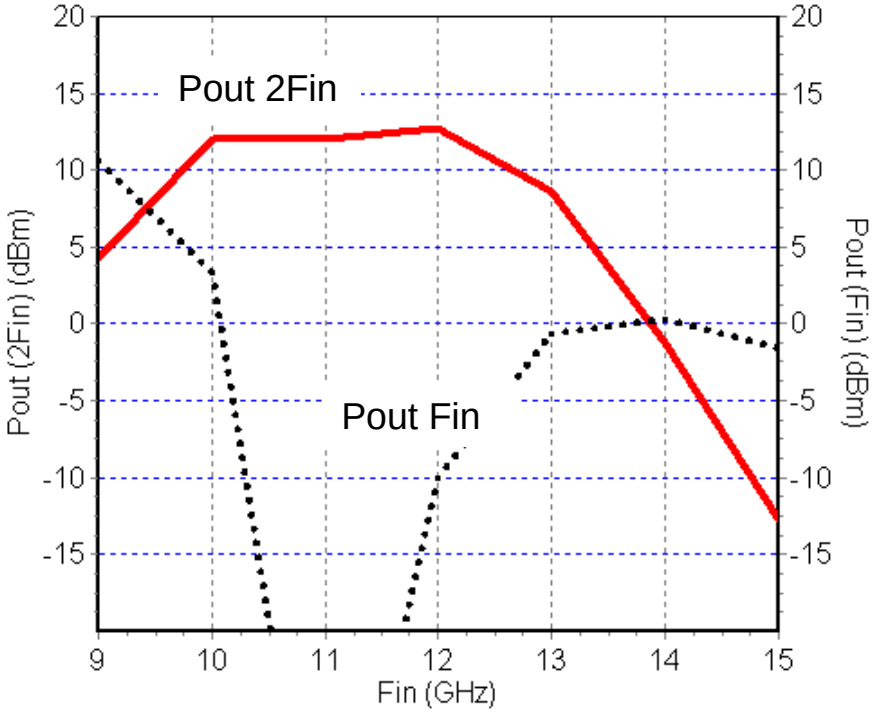
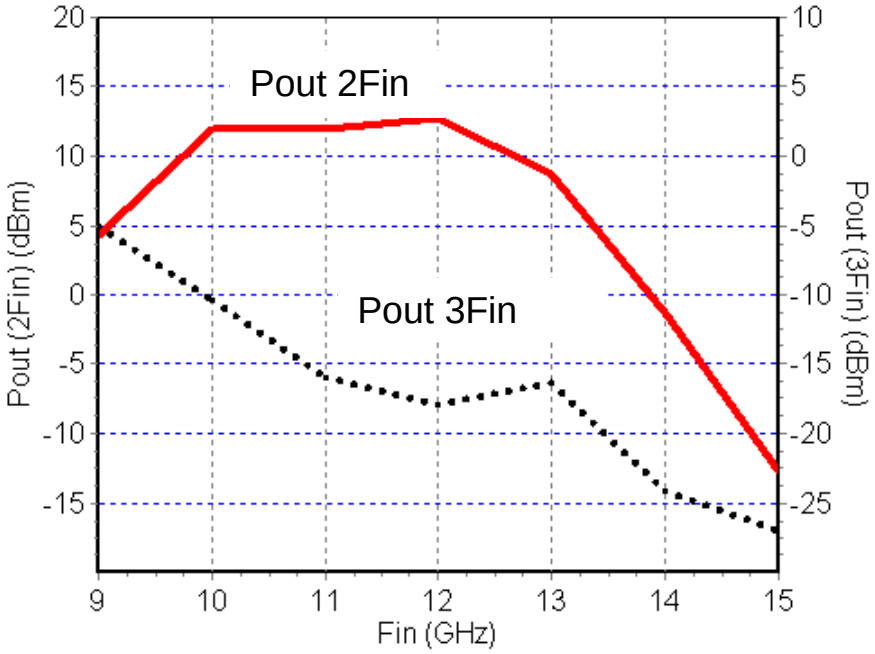
Typical Measured performances

Measurements in the connector access planes, using the proposed land pattern & board 96270.
Bias conditions : Vd = 3,5V, Vg1 = -0.9V, Vg2 tuned for Id# 65mA.

Pout (2Fin) & Pout (Fin) vs Fin for Pin=14 dBm



Pout (2Fin) & Pout (3Fin) vs Fin for Pin=14 dBm



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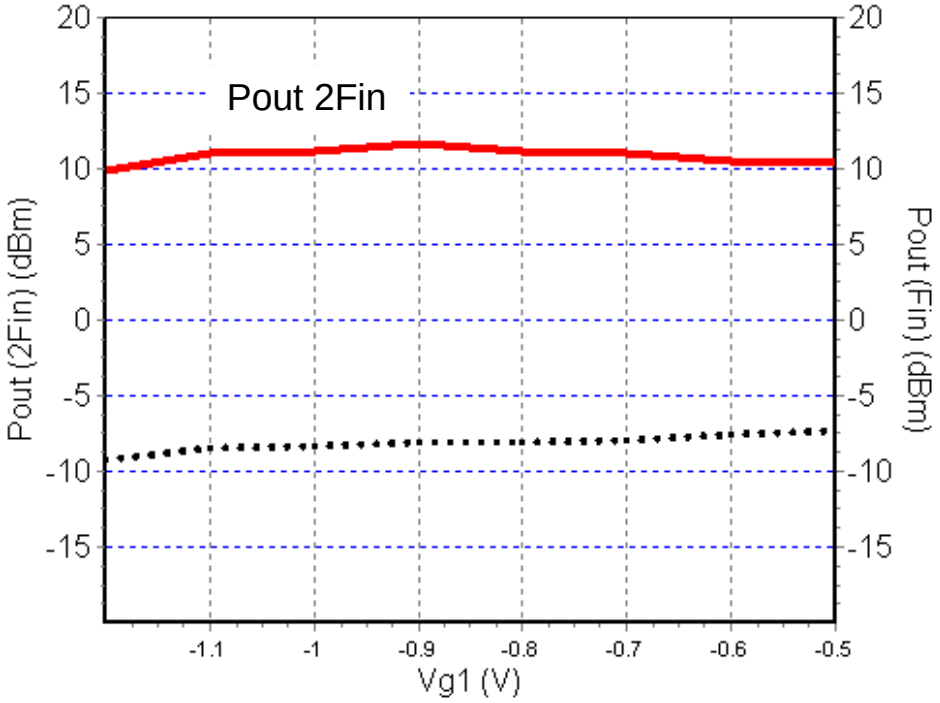
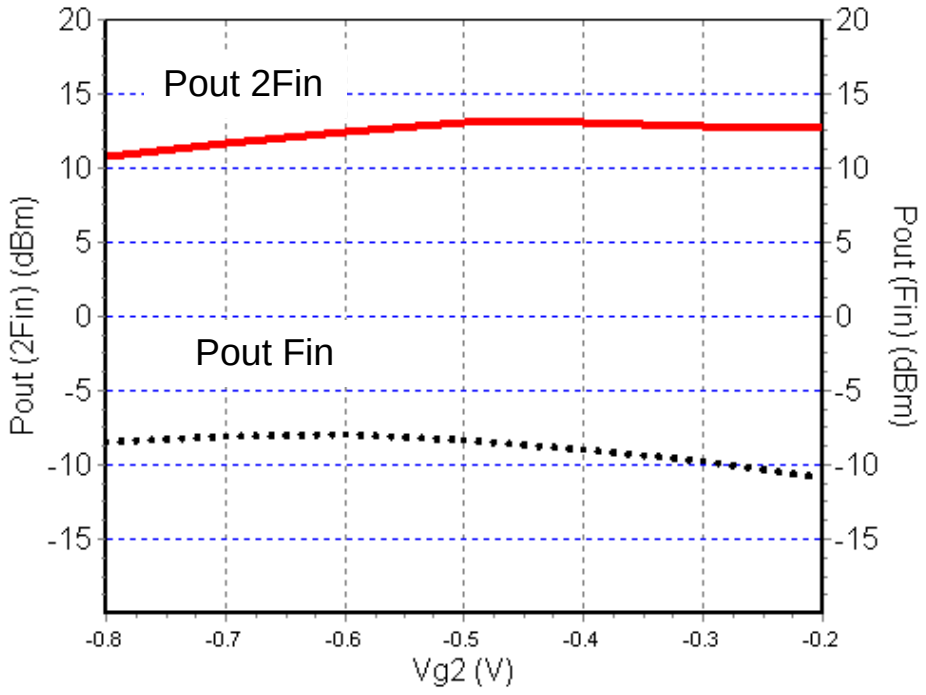
Pout (2Fin) & Pout (Fin) vs Vg1 for Fin = 12 GHz, Pin=14dBm & Vg2= -0,7V



Pout (2Fin) & Pout (Fin) vs Vg2 for Fin = 12 GHz, Pin=14dBm & Vg1= -0,9V



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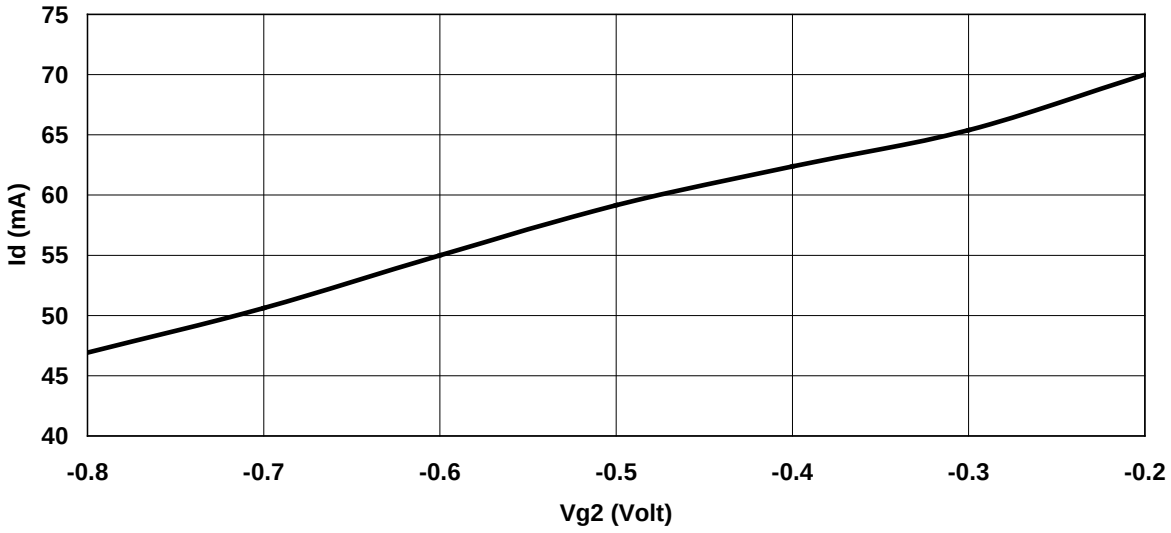
Drain current versus Vg2, for Fin=12GHz, Pin=14dBm, Vd=3.5V and Vg1=-0.9V



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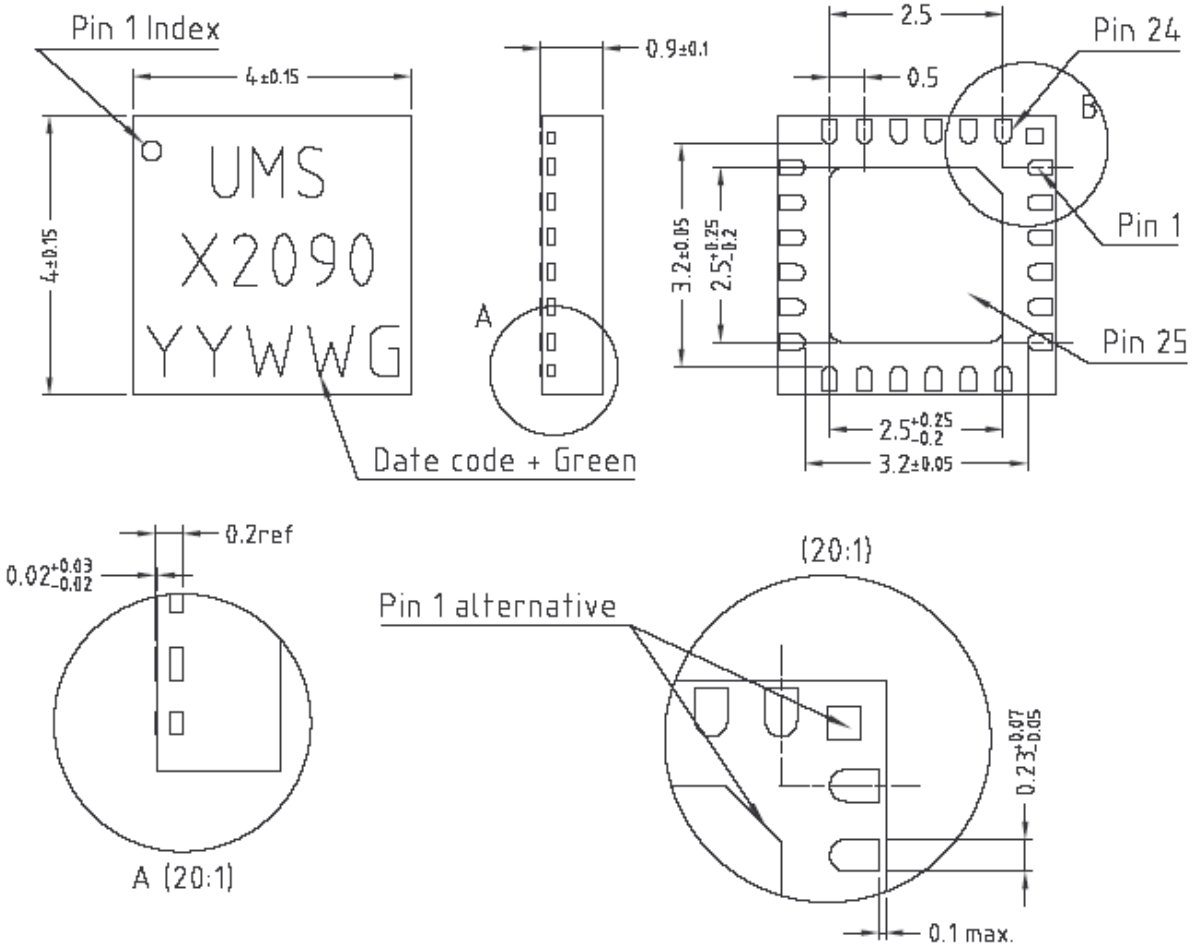
Package outline



Matt tin, Lead Free	(Green)	1-	NC	13-	NC
Units	mm	2-	NC	14-	GND
From the standard	JEDEC MO-220	3-	GND	15-	RF OUT
Pin 25 (paddle)	GND	4-	RF IN	16-	GND
		5-	GND	17-	NC
		6-	NC	18-	NC
		7-	NC	19-	NC
		8-	NC	20-	Vd
		9-	NC	21-	NC
		10-	NC	22-	Vg2
		11-	NC	23-	Vg1
		12-	NC	24-	NC

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Application note

The design of the motherboard has a strong impact on the over all performance since the transition from the motherboard to the package is comparably large. In case of the SMD type packages of United Monolithic Semiconductors the motherboard should be designed according to the information given in the following to achieve good performance. Other configurations are also possible but can lead to different results. If you need advise please contact United Monolithic Semiconductors for further information.

SMD type packages of UMS should allow design and fabrication of micro- and mm-wave modules at low cost. Therefore, a suitable motherboard environment has been chosen. All tests and verifications have been performed on Rogers RO4003. This material exhibits a permittivity of 3.38 and has been used with a thickness of 200µm [8 mils] and a 1/2oz or less copper cladding. The corresponding 50Ohm transmission line has a strip width of about 460µm [approx. 18 mils].

The contact areas on the motherboard for the package connections should be designed according to the footprint given above. The proper via structure under the ground pad is very important in order to achieve a good RF and lifetime performance. All tests have been done by using a grid of plenty plated through vias with a diameter of less than 300µm [12 mils] and a spacing of less than 700µm [28 mils] from the centres of two adjacent vias. The via grid should cover the whole space under the ground pad and the vias closest to the RF ports should be located near the edge of the pad to allow a good RF ground connection. Since the vias are important for heat transfer, a proper via filling should be guaranteed during the mounting procedure to get a low thermal resistance between package and heat sink. For power devices the use of heat slugs in the motherboard instead of a grid of via’s is recommended.

For the mounting process the SMD type package can be handled as a standard surface mount component. The use of either solder or conductive epoxy is possible. The solder thickness after reflow should be typical 50µm [2 mils] and the lateral alignment between the package and the motherboard should be within 50µm [2 mils]. Caution should be taken to obtain a good and reliable contact over the whole pad areas. Voids or other improper connections, in particular, between the ground pads of motherboard and package will lead to a deterioration of the RF performance and the heat dissipation. The latter effect can reduce drastically reliability and lifetime of the product.

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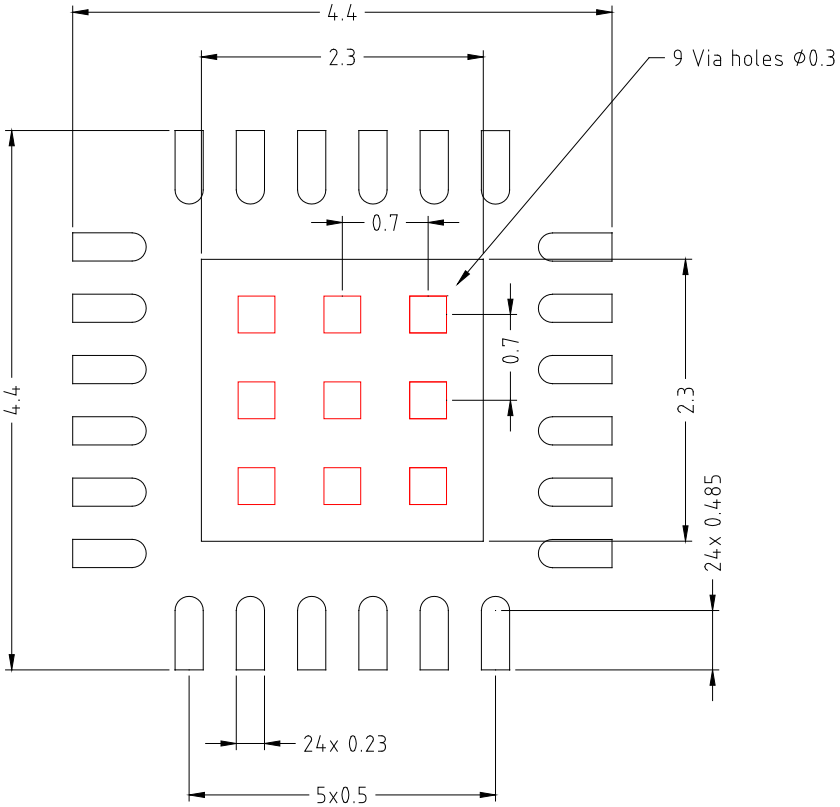

(For production, design must be adapted
with regard to PCB tolerances and assembly process)

Basic footprint for a 24L-QFN4x4 (all units mm)
(Please, refer to the UMS proposed footprint for optimum
operation in the following “Proposed Assembly board” section)

The RF ports are DC blocked on chip. The DC connection (Vd) does not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

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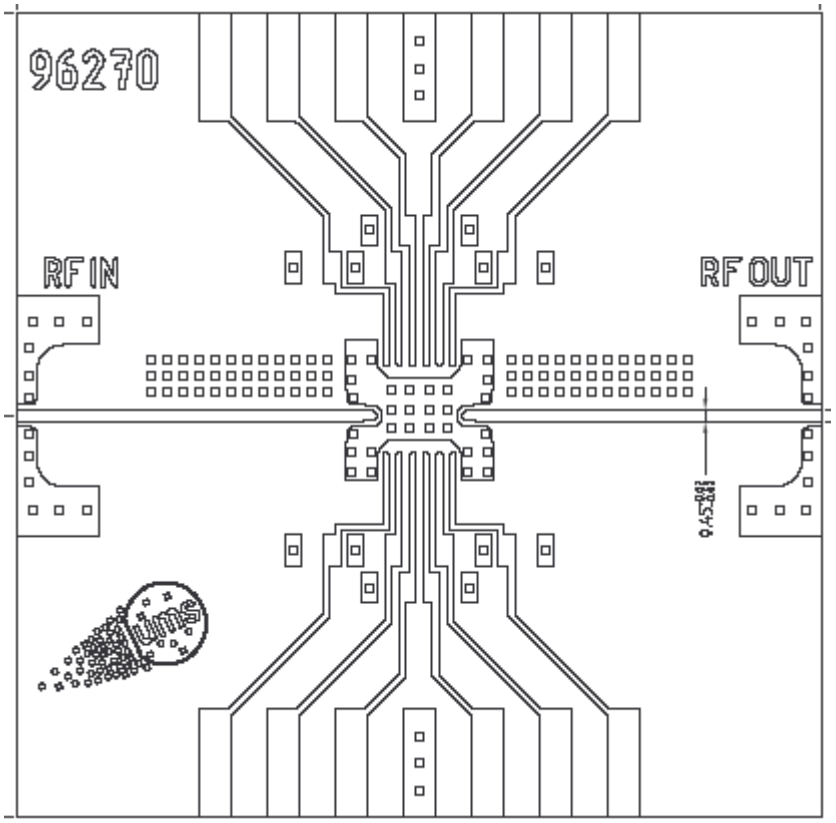
Proposed Assembly board “96270” for the 24L-QFN4x4 products characterization.

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.



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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

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For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Recommended environmental management

Refer to the application note AN0019 available at https://www.ums-rf.com for environmental data on UMS package products.

Ordering Information

QFN 4x4 RoHS compliant package:	CHX2090-QDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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