

## 15W L-Band Driver

GaN HEMT on Sic in SMD leadless package

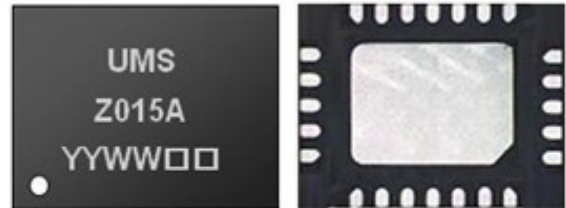
### Description

The CHZ015A-QEG is an input matched packaged Gallium Nitride High Electron Mobility Transistor.

It allows broadband solutions for a variety of RF power applications in L-band. The circuit is well suited for pulsed radar application.

The CHZ015A-QEG is proposed on a 0.5 $\mu$ m gate length GaN HEMT process. It is based on Quasi MMIC technology.

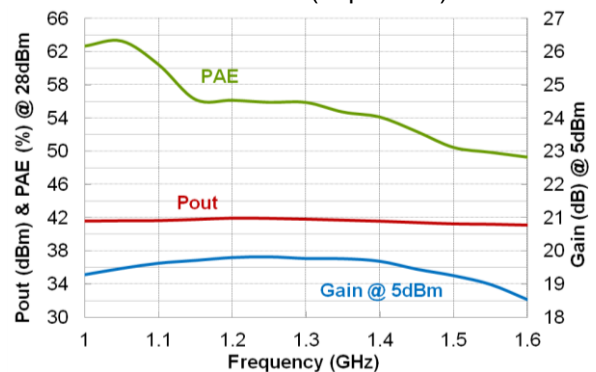
It is supplied in RoHS compliant SMD package.



### Main Features

- Wide band capability: 1.2 - 1.4GHz
- Pulsed operating mode
- High power: > 15W
- High PAE: up to 55%
- DC bias:  $V_{DS}=45V$  @  $I_{D,Q}=100mA$
- Low cost package: 24L-QFN4x5
- MTTF > 10<sup>6</sup> hours @  $T_j=200^{\circ}C$

$V_{DS} = 45V$ ,  $I_{D,Q} = 100mA$ ,  $P_{in} = 28dBm$   
Pulsed mode (25 $\mu$ s-10%)



Performances on the connector access planes

### Main Electrical Characteristics

$T_{amb.} = +25^{\circ}C$ , pulsed mode

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	1.2		1.4	GHz
$G_{SS}$	Small Signal Gain	18	19.5		dB
$P_{OUT}$	Output Power	39.5	41.5	43	dBm
PAE	Max Power Added Efficiency	45	55		%
$I_{D,SAT}$	Saturated Drain Current		650		mA

## Recommended DC Operating Ratings

T<sub>amb</sub>. = +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V <sub>DS</sub>	Drain to Source Voltage	20	45	50	V	
V <sub>GS_Q</sub>	Gate to Source Voltage		-1.9		V	V <sub>DS</sub> =45V, I <sub>D_Q</sub> =100mA
I <sub>D_Q</sub>	Quiescent Drain Current		100	350	mA	V <sub>DS</sub> =45V
I <sub>D_MAX</sub>	Drain Current		650	(1)	mA	V <sub>DS</sub> =45V, Compressed mode
I <sub>G_MAX</sub>	Gate Current (forward mode)		0	8	mA	Compressed mode
P <sub>W</sub>	Pulse width			1.5	ms	
D <sub>C</sub>	Duty cycle		10		%	
T <sub>J_MAX</sub>	Junction temperature			200	°C	

(1) Limited by dissipated power.

## DC Characteristics

T<sub>amb</sub>. = +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V <sub>P</sub>	Pinch-Off Voltage	-3	-2	-1	V	V <sub>DS</sub> =45V, I <sub>D</sub> =I <sub>DSS</sub> /100
I <sub>D_SAT</sub> <sup>(2)</sup>	Saturated Drain Current		2.7		A	V <sub>DS</sub> =7V, V <sub>G</sub> =2V <sup>(1)</sup>
I <sub>G_Leak</sub>	Gate Leakage Current (reverse mode)	-1			mA	V <sub>D</sub> =45V, V <sub>G</sub> =-7V <sup>(1)</sup>
V <sub>BDS</sub>	Drain-Source Break-down Voltage		200		V	V <sub>G</sub> =-7V <sup>(1)</sup>
R <sub>TH</sub>	Thermal Resistance		5.5		°C/W	1ms – 10%

(1) Parameters extrapolated from unit cell measurement.

(2) For information, limited by I<sub>D\_MAX</sub>, see on Absolute Maximum Ratings.

**RF Characteristics** <sup>(1)</sup>

T<sub>amb</sub>. = +25°C, pulsed mode <sup>(2)</sup>, on board 61501358<sup>(1)</sup>, V<sub>DS</sub>=45V, I<sub>D,Q</sub>=100mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	1.2		1.4	GHz
G <sub>SS</sub>	Small Signal Gain	18	19.5		dB
dG <sub>SS</sub>	Small Signal Gain flatness		+/-0.3		dB
P <sub>SAT</sub>	Saturated Output Power	39.5	41.5	43	dBm
PAE	Power Added Efficiency	45	55		%
I <sub>DSAT</sub>	Saturated Drain Current		650		mA
R <sub>lin</sub>	Input Return Loss		-12	-10	dB

<sup>(1)</sup> Measured on evaluation board 61501358 on the connector access planes.

<sup>(2)</sup> Input RF and gate voltage are pulsed. Conditions are 25µs width, 10% duty cycle and 1µs offset between RF and DC pulse.

## Absolute Maximum Ratings

T<sub>amb.</sub> = +25°C <sup>(1), (2), (3)</sup>

Symbol	Parameter	Rating	Unit	Note
V <sub>DS</sub>	Drain-Source Voltage	-0.5, +60	V	
V <sub>GS_Q</sub>	Gate-Source Voltage	-10, +2	V	(4), (6)
I <sub>G_MAX</sub>	Maximum Gate Current in forward mode	25	mA	
I <sub>G_MIN</sub>	Maximum Gate Current in reverse mode	-4	mA	
I <sub>D_MAX</sub>	Maximum Drain Current	2	A	(4)
P <sub>IN</sub>	Maximum Input Power	32	dBm	(5)
P <sub>W_MAX</sub>	Pulse width	3	ms	
D <sub>C_MAX</sub>	Duty cycle	20	%	
Top	Operating temperature range	-40 to +85	°C	
T <sub>j</sub>	Junction Temperature	220	°C	
T <sub>STG</sub>	Storage Temperature	-55 to +150	°C	

(1) Operation by this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

(3) The given values have not to be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may take place.

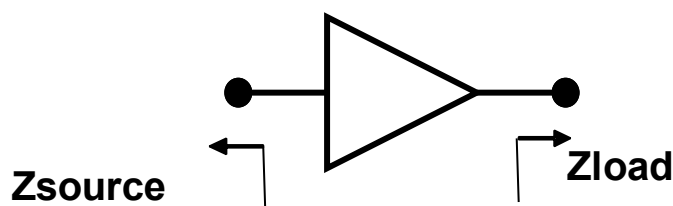
(4) Max junction temperature has to be considered.

(5) Linked to and limited by I<sub>G\_MAX</sub> & I<sub>G\_MIN</sub> values.

(6) V<sub>GS\_Q</sub> max limited by I<sub>D\_MAX</sub> and I<sub>G\_MAX</sub> values.

## Simulated Source and Load Impedance

V<sub>DS</sub> = 45V, I<sub>D\_Q</sub> = 100mA



Frequency (GHz)	Source	Load
Typical [1.2-1.4]	50 - j0	54.0 + j29.6

These values are defined at the package interface with PCB.

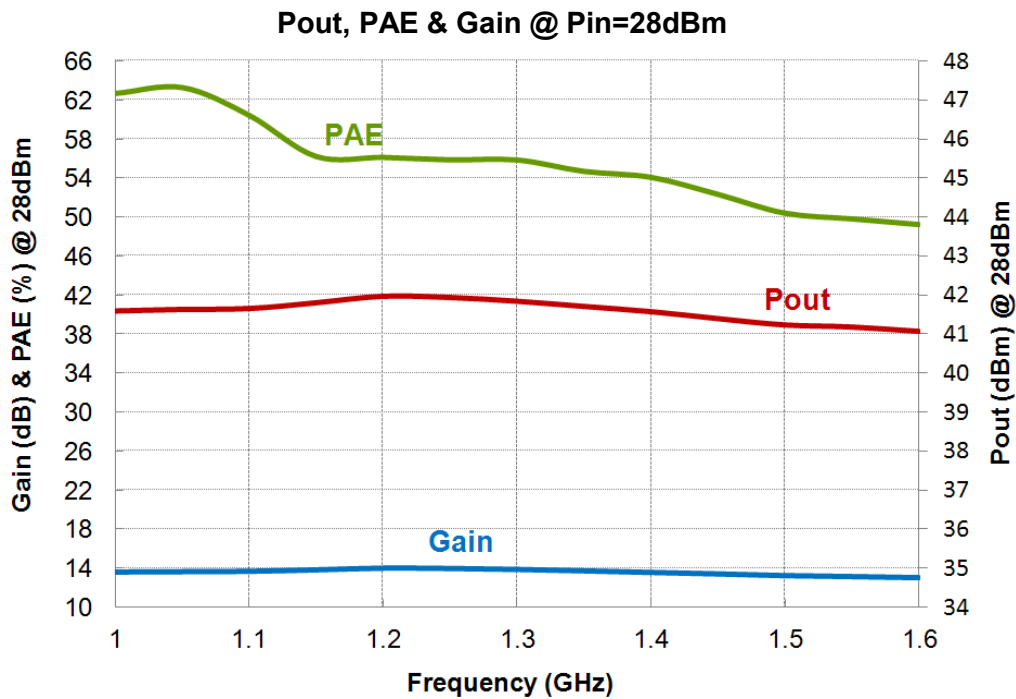
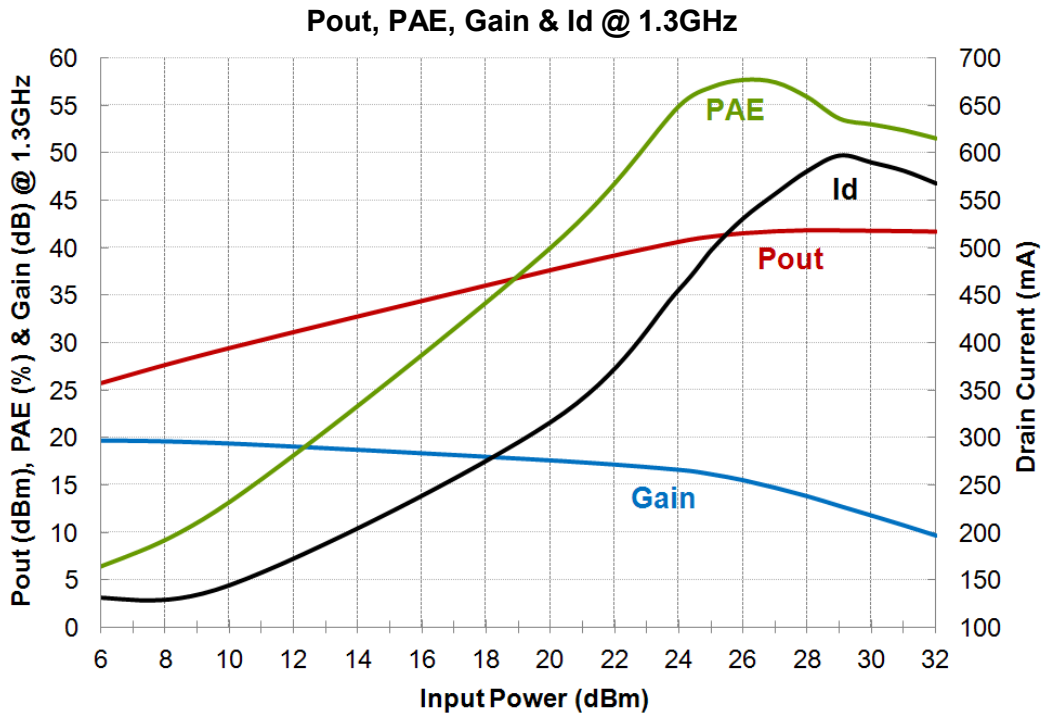
**Typical Package Sij parameters (simulation)**Tamb.= +25°C, CW mode, V<sub>DS</sub>=45V, I<sub>DQ</sub>=100mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
0.1	-0.04	-7.9	-60.47	103.6	9.48	-166.5	-5.44	-20.3
0.2	-0.09	-16.0	-53.53	85.8	10.39	175.2	-5.98	-24.1
0.3	-0.18	-24.6	-49.33	73.7	11.07	162.7	-5.87	-30.2
0.4	-0.32	-34.3	-46.02	62.1	11.89	150.8	-5.54	-37.3
0.5	-0.55	-45.4	-43.13	49.7	12.84	138.1	-5.05	-45.1
0.6	-0.95	-58.6	-40.54	35.9	13.87	123.9	-4.56	-55.3
0.7	-1.65	-75.1	-38.09	20.3	14.98	108.0	-4.58	-63.1
0.8	-2.86	-95.8	-35.88	2.2	16.04	89.6	-4.22	-69.9
0.9	-4.89	-122.7	-34.01	-18.2	16.90	68.8	-3.87	-77.5
1.0	-7.93	-159.0	-32.58	-40.3	17.43	46.3	-3.63	-85.0
1.1	-11.14	150.1	-31.59	-63.0	17.60	23.4	-3.47	-91.8
1.2	-12.04	92.7	-30.92	-85.3	17.53	0.7	-3.31	-97.8
1.3	-11.73	49.2	-30.40	-107.3	17.37	-21.6	-3.09	-103.7
1.4	-12.88	16.9	-29.97	-130.0	17.17	-44.7	-2.86	-110.1
1.5	-18.12	-9.9	-29.71	-154.4	16.86	-69.4	-2.81	-117.3
1.6	-27.14	129.5	-29.80	179.7	16.22	-95.7	-3.09	-124.1
1.7	-12.71	113.3	-30.37	153.4	15.15	-122.3	-3.62	-128.1
1.8	-8.17	93.3	-31.25	128.0	13.80	-148.0	-3.94	-128.7
1.9	-6.07	77.4	-32.19	102.7	12.41	-173.7	-3.63	-128.3
2.0	-5.06	66.4	-33.21	74.7	10.98	158.0	-2.80	-131.5
2.1	-4.28	60.6	-34.91	41.9	8.87	124.8	-2.22	-140.8
2.2	-3.14	55.2	-38.21	8.4	5.20	91.0	-2.78	-151.7
2.3	-2.20	47.6	-42.76	-17.7	0.29	64.6	-4.06	-156.8
2.4	-1.65	39.9	-47.60	-35.4	-4.89	46.5	-5.11	-156.4
2.5	-1.32	33.3	-52.31	-47.3	-9.91	34.2	-5.68	-153.9
2.6	-1.11	27.7	-56.83	-55.3	-14.75	25.9	-5.87	-151.4
2.7	-0.96	22.7	-61.24	-60.4	-19.45	20.5	-5.85	-149.6
2.8	-0.84	18.3	-65.64	-62.7	-24.12	17.8	-5.72	-148.5
2.9	-0.75	14.4	-70.11	-61.8	-28.86	18.4	-5.54	-148.0
3.0	-0.68	10.8	-74.72	-55.7	-33.73	24.1	-5.34	-148.0
3.1	-0.62	7.5	-79.12	-40.7	-38.37	38.7	-5.14	-148.3
3.2	-0.57	4.4	-82.10	-16.7	-41.58	62.4	-4.94	-148.9
3.3	-0.53	1.5	-82.89	6.3	-42.59	85.0	-4.75	-149.6
3.4	-0.49	-1.3	-82.61	20.6	-42.52	99.0	-4.56	-150.5
3.5	-0.46	-3.9	-82.26	27.9	-42.38	105.9	-4.39	-151.5
3.6	-0.43	-6.4	-82.13	31.5	-42.45	109.1	-4.22	-152.5
3.7	-0.40	-8.8	-82.20	32.9	-42.71	110.2	-4.06	-153.6
3.8	-0.38	-11.1	-82.44	33.2	-43.13	110.1	-3.92	-154.8
3.9	-0.36	-13.4	-82.81	32.8	-43.67	109.3	-3.78	-156.0
4.0	-0.34	-15.5	-83.27	32.1	-44.29	108.2	-3.65	-157.2

## Typical Performance on Evaluation Board (ref 61501358)

Calibration and measurements are done on the connector access planes of the evaluation boards.

Tamb.= +25°C, pulsed mode <sup>(1)</sup>, V<sub>DS</sub>=45V, I<sub>D,Q</sub>=100mA

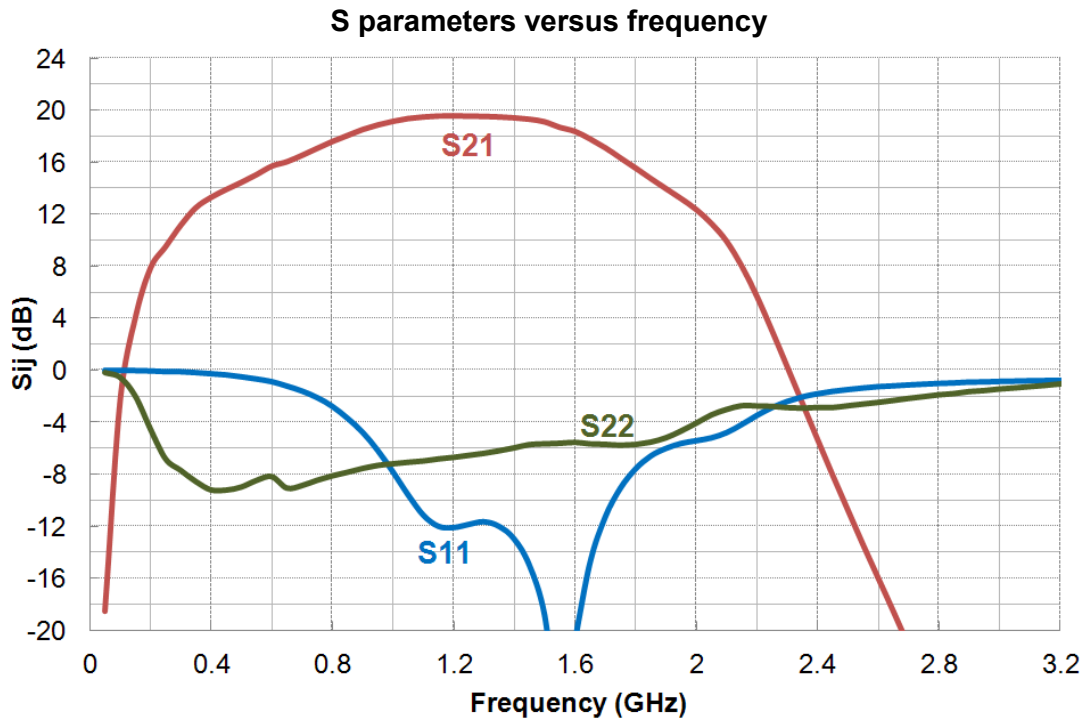


<sup>(1)</sup> Input RF and gate voltage are pulsed. Conditions are 25µs width, 10% duty cycle and 1µs offset between DC and RF pulse.

**Typical Performance on Evaluation Board (ref 61501358)**

Calibration and measurements are done on the connector access planes of the evaluation boards.

T<sub>amb.</sub> = +25°C, **pulsed mode** <sup>(1)</sup>, V<sub>DS</sub>=45V, I<sub>D\_Q</sub>=100mA

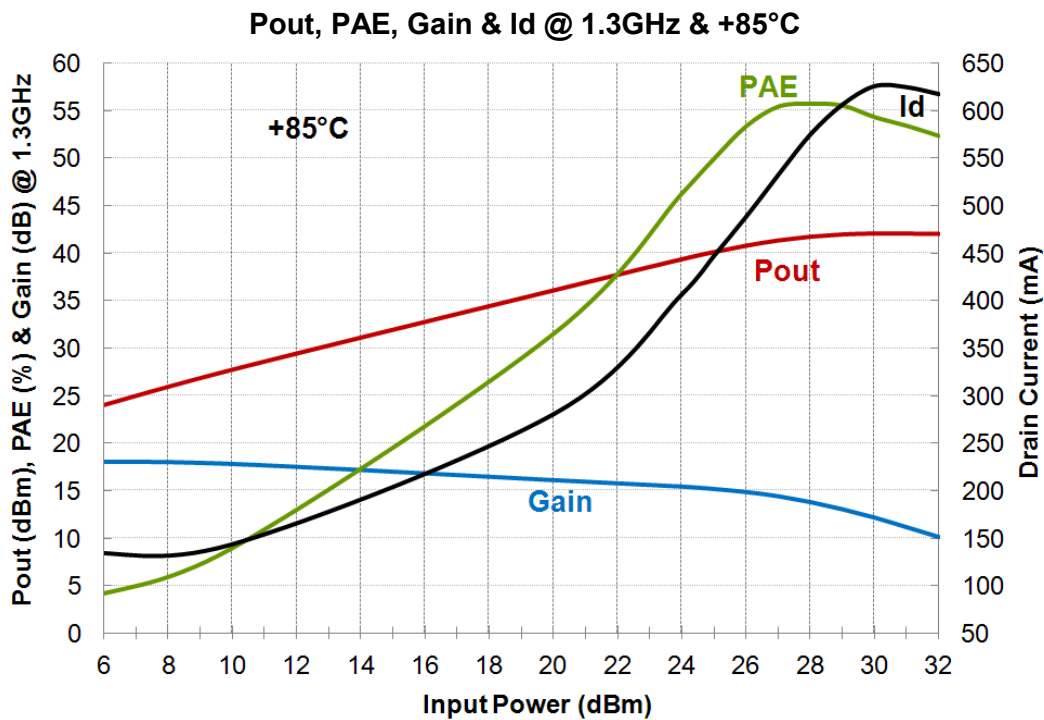
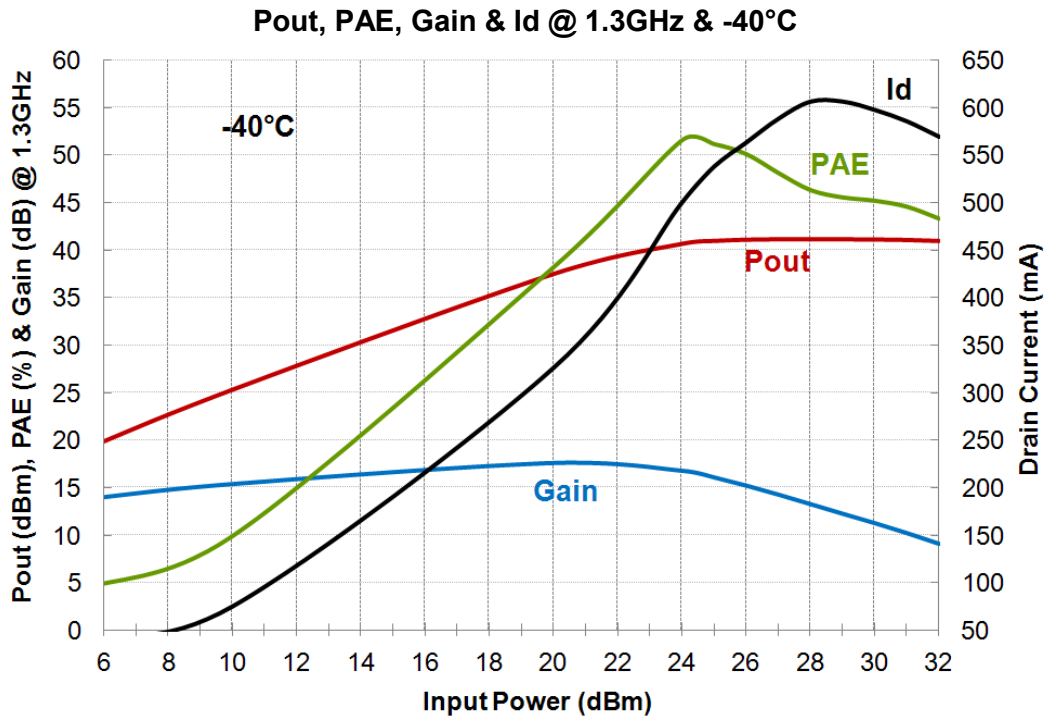


<sup>(1)</sup> Input RF and gate voltage are pulsed. Conditions are 25µs width, 10% duty cycle and 1µs offset between DC and RF pulse.

## Typical Performance in Temperature (on evaluation board)

Calibration and measurements are done on the connector access planes of the evaluation boards (ref 61501358).

Tamb.= -40°C, +25°C, +85°C, **pulsed mode** <sup>(1)</sup>, V<sub>DS</sub>=45V, V<sub>gs</sub> fixed (I<sub>D,Q</sub>=100mA @ +25°C)



<sup>(1)</sup> Input RF and gate voltage are pulsed. Conditions are 25µs width, 10% duty cycle and 1µs offset between DC and RF pulse.

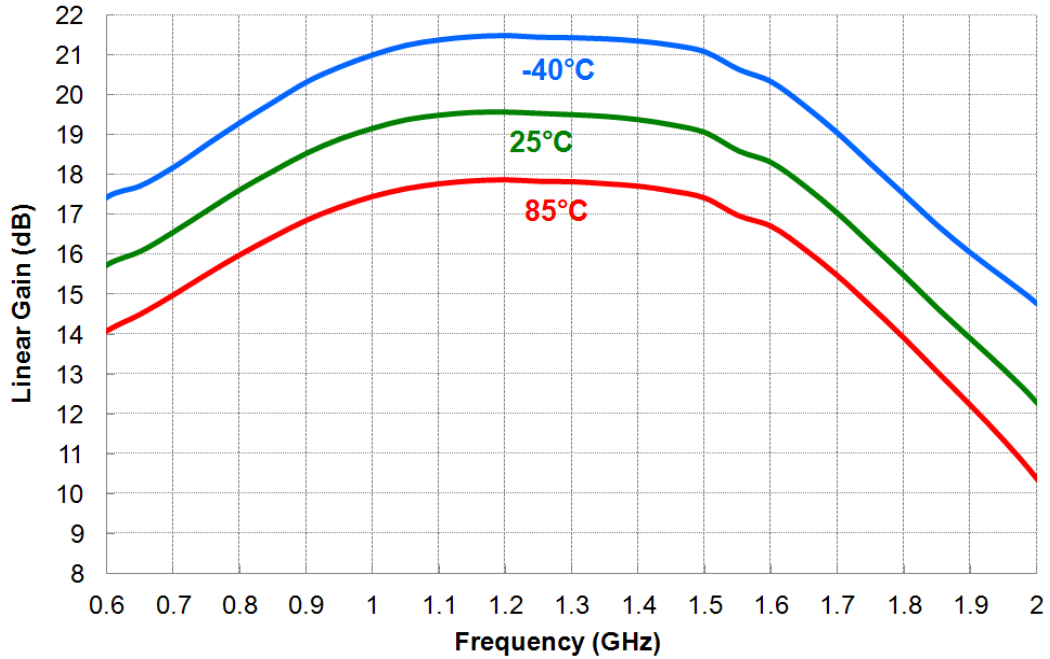


**Typical Performance in Temperature (on evaluation board)**

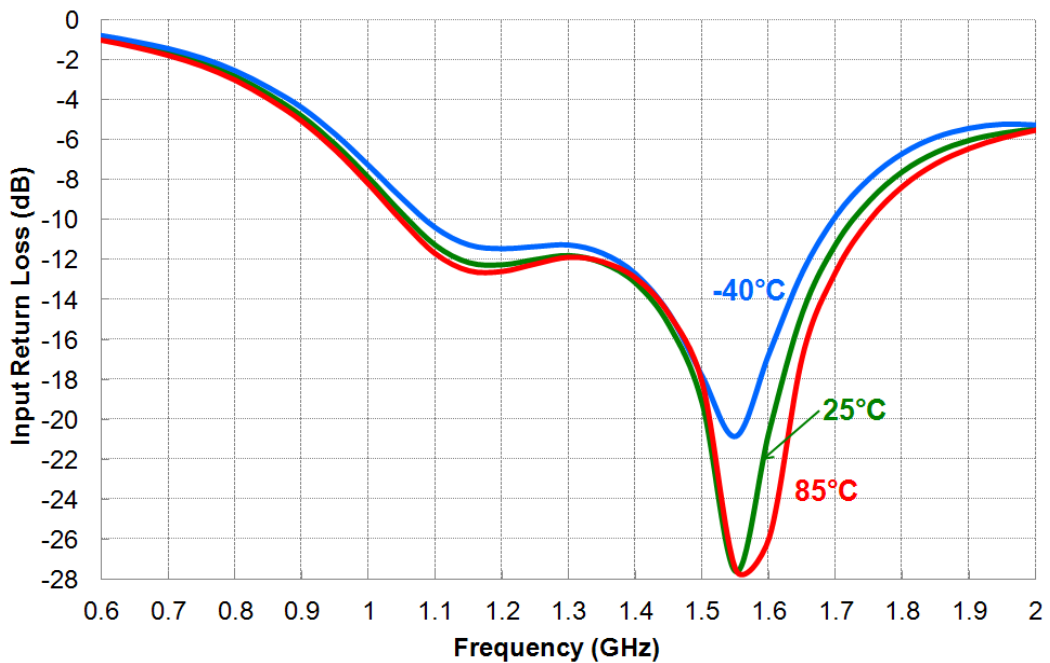
Calibration and measurements are done on the connector access planes of the evaluation boards (ref 61501358).

Tamb.= -40°C, +25°C, +85°C, pulsed mode <sup>(1)</sup>, V<sub>DS</sub>=45V, I<sub>D\_Q</sub>=100mA (fixed @ +25°C)

**Linear Gain versus temperature with ID\_Q fixed @ +25°C (100mA)**

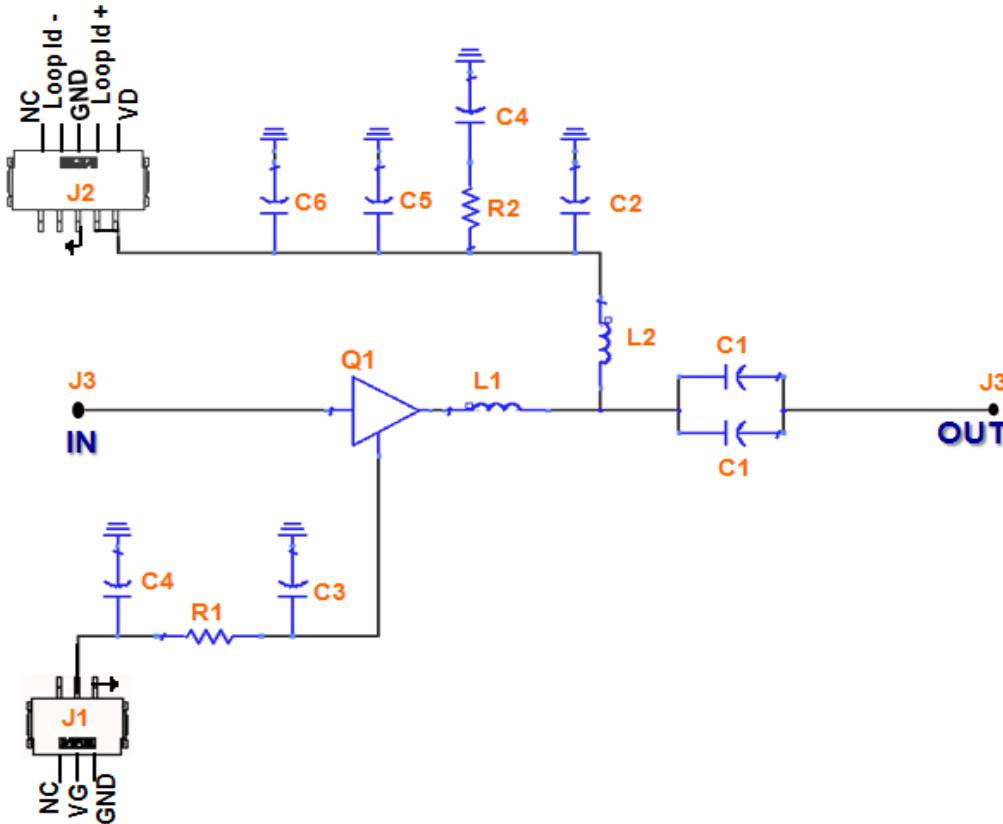


**Input Return Loss versus temperature with ID\_Q fixed @ +25°C (100mA)**



<sup>(1)</sup> Input RF and gate voltage are pulsed. Conditions are 25µs width, 10% duty cycle and 1µs offset between DC and RF pulse.

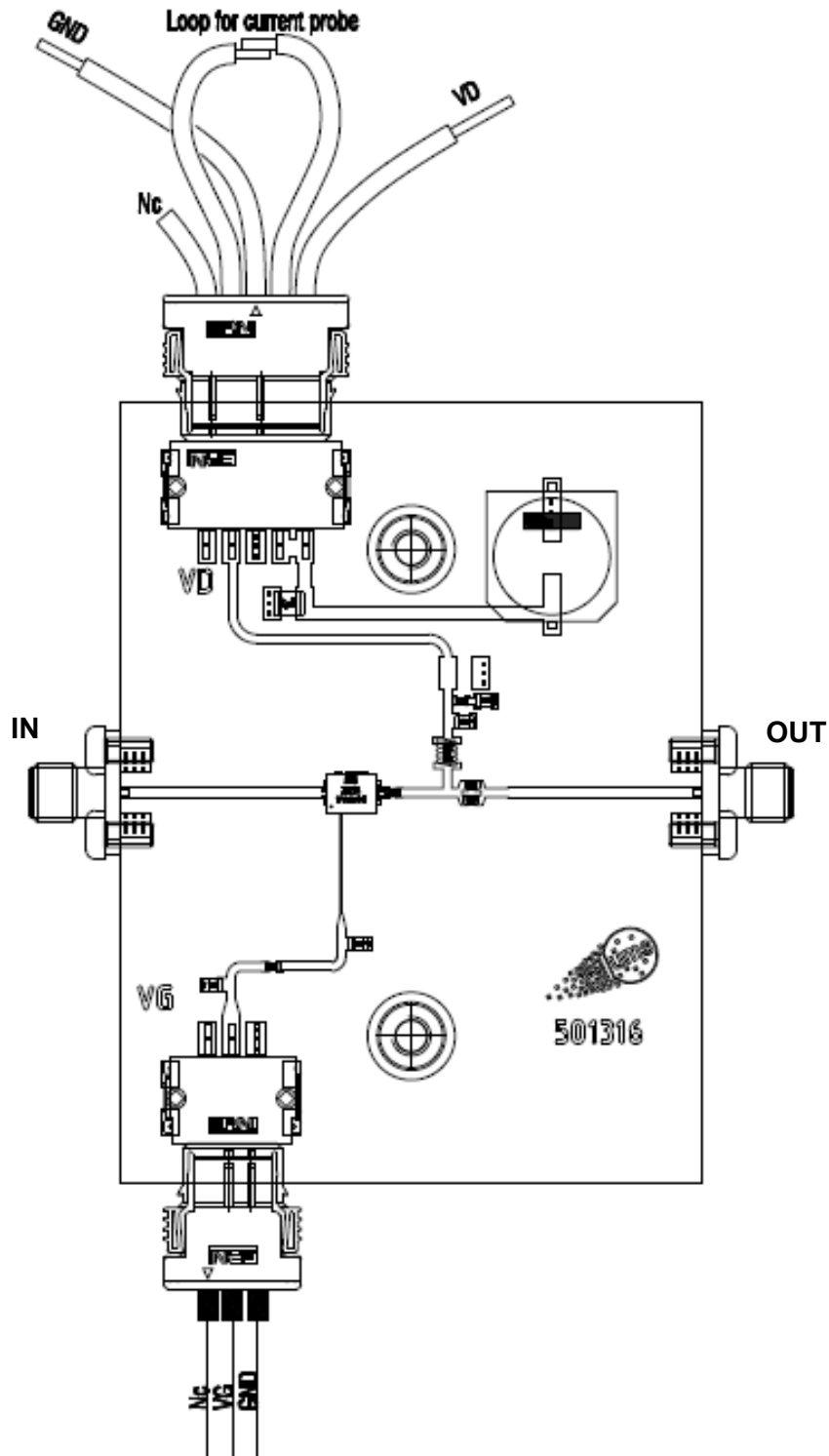
## Demonstration Amplifier Low Frequency Equivalent Schematic (ref 61501358)



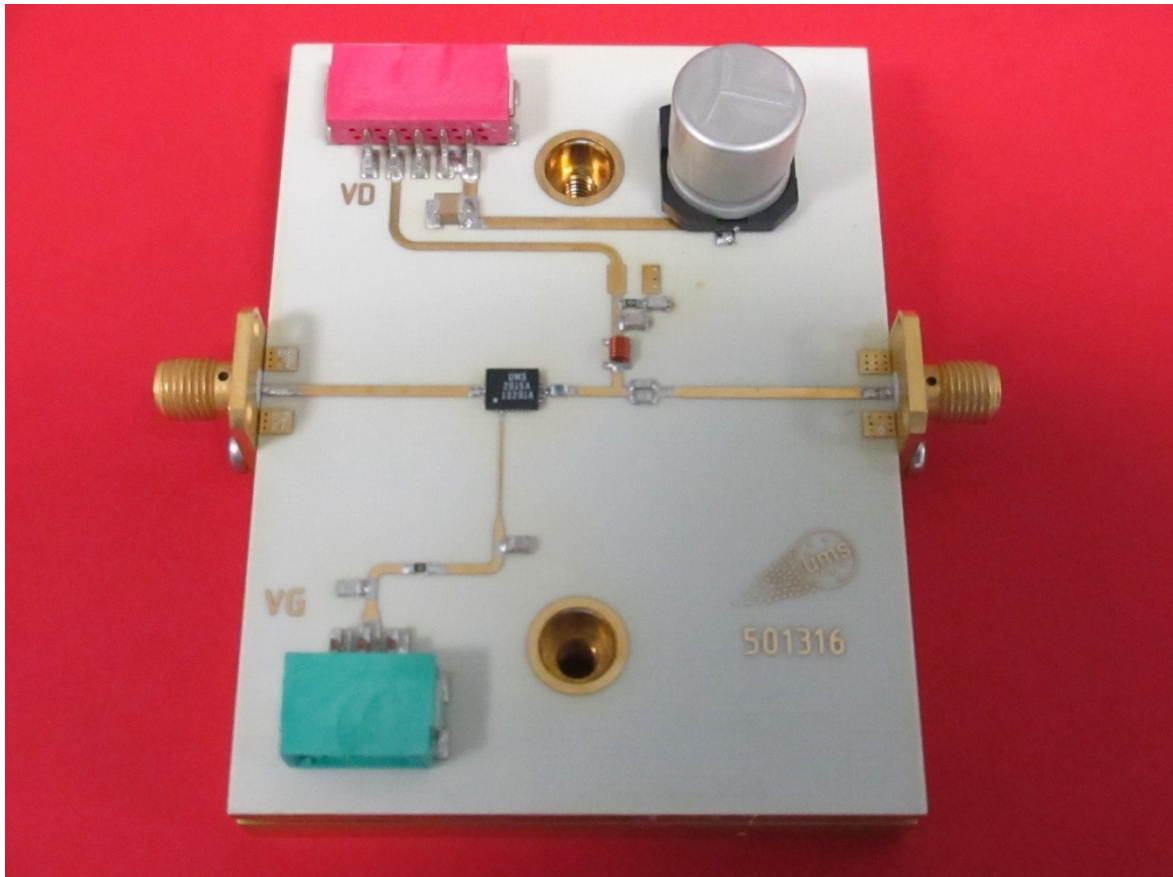
## Demonstration Amplifier (ref 61501358) / Bill of Materials

Designator	Type	Value - Description	Qty
L1	Inductor for output pre-matching	3.6nH, +/- 5%, 0603	1
L2	Inductor	22nH, +/- 5.2%, 0908	1
C1	Capacitor	10pF, +/- 5%, 0603	2
C2	Capacitor	120pF, +/- 5%, 0805	1
C3	Capacitor	220pF, +/- 5%, 0805	1
C4	Capacitor	1nF, +/- 5%, 0805	2
C5	Capacitor	1μF, +/- 10%, 1210	1
C6	Capacitor	68μF, +/- 20%, H13	1
R1	Jumper	Jumper 0 Ω, 0603	1
R2	Resistor	3Ω, +/- 1%, 0603	1
J1	Connector	SMD 3 contacts	1
J2	Connector	SMD 5 contacts	1
J3	Connector	SMA	2
Q1	Driver	CHZ015A-QEG	1
-	PCB	RO4003, Er=3.55, h=508μm	-

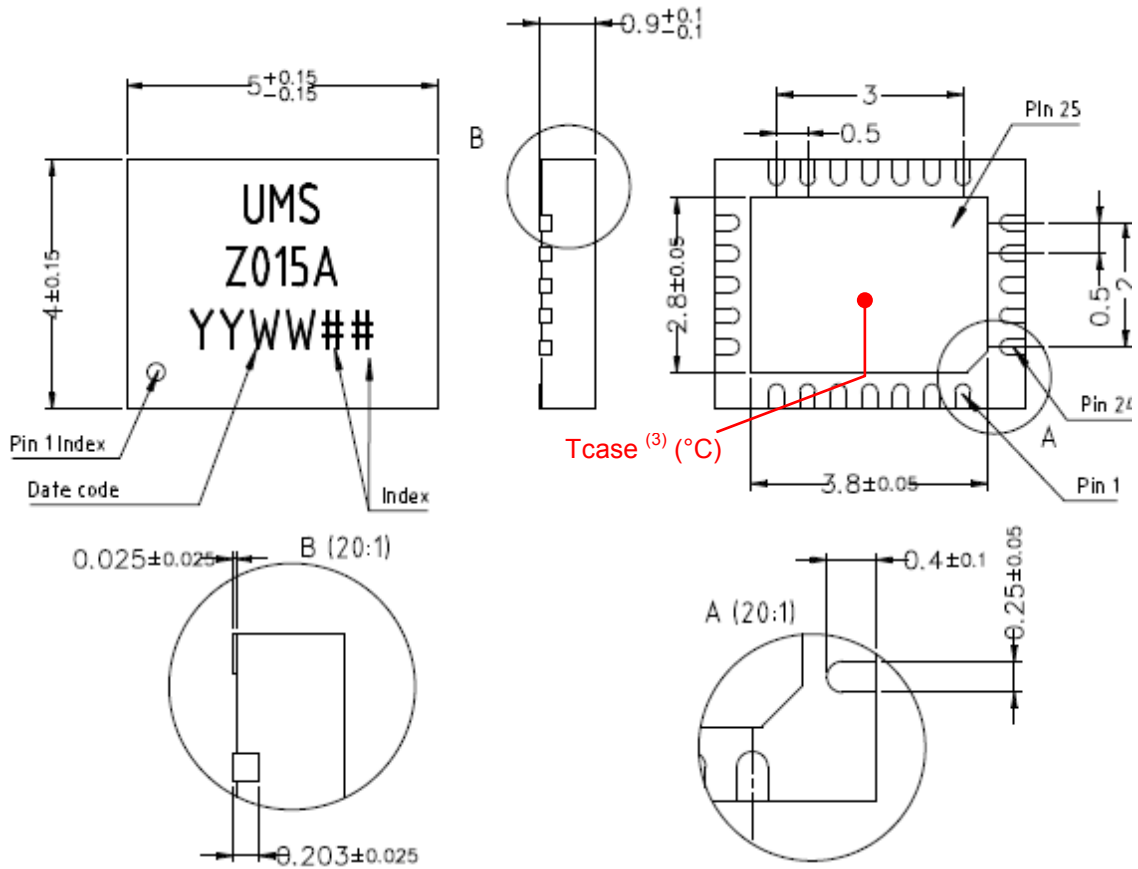
Amplifier Demonstration Board (ref 61501358)



## Amplifier Demonstration Board (ref 61501358)



Package outline <sup>(1)</sup>



Matt tin, Lead Free (Green)	1- Nc	9- OUT	17- Nc
Units : mm	2- DC	10- Nc	18- GND <sup>(2)</sup>
From the standard : JEDEC MO-220 (VGHD)	3- Nc	11- OUT	19- Nc
25- GND	4- Nc	12- Nc	20- Nc
	5- GND <sup>(2)</sup>	13- Nc	21- GND <sup>(2)</sup>
	6- GND <sup>(2)</sup>	14- GND <sup>(2)</sup>	22- IN
	7- Nc	15- Nc	23- GND <sup>(2)</sup>
	8- Nc	16- Nc	24- Nc

<sup>(1)</sup> The package outline drawing included in this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

<sup>(2)</sup> It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

<sup>(3)</sup> The temperature is monitored at the package back-side interface (Tcase) as shown above.

## Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

## SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

## Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

## Ordering Information

QFN 4x5 package:

CHZ015A-QEG/XY

Stick: XY = 20

Tape & reel: XY = 21

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