

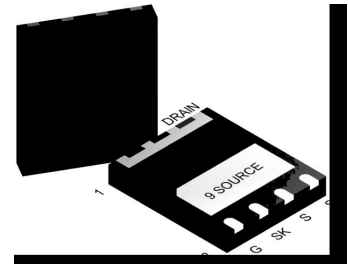
## GaN Enhancement-mode Power Transistor

### General description

650V GaN-on-Silicon Enhancement-mode Power Transistor in Dual Flat No-lead Package (DFN) with 5 mm × 6 mm Size

### Features

- Enhancement-mode transistor - normally-OFF power switch
- Ultra-high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC standards
- ESD safeguard
- RoHS, Pb-free

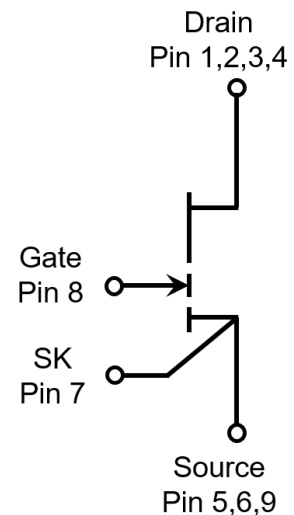


### Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High-density power conversion
- High-efficiency power conversion

**Table 1 Key Performance Parameters at  $T_j = 25\text{ }^\circ\text{C}$**

Parameters	Values	Units
$V_{DS, \max}$	650	V
$R_{DS(on), \max}$	200	m $\Omega$
$Q_G, \text{typ}$	2.3	nC
$I_D, \text{Pulse}$	18	A
$Q_{OSS} @ 400\text{ V}$	22	nC
$Q_{rr}$	0	nC



Gate	8
Drain	1, 2, 3, 4
Kelvin Source	7
Source	5, 6, 9

**Table 2 Ordering Information**

Type/Ordering Code	Package	Marking
CID10N65D5	DFN 5x6, 2500 pcs/reel	10N65

## 1 Maximum ratings

at  $T_j = 25\text{ °C}$  unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Tokmas sales office.

**Table 3 Maximum rating**

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Drain-source voltage	$V_{DS, max}$	-	-	650	V	$V_{GS} = 0\text{ V}$ , $I_D = 10\text{ }\mu\text{A}$
Drain-source voltage transient <sup>1</sup>	$V_{DS, transient}$	-	-	750	V	$V_{GS} = 0\text{ V}$ , $V_{DS} = 750\text{ V}$
Continuous current, drain-source	$I_D$	-	-	10	A	$T_c = 25\text{ °C}$
Pulsed current, drain-source <sup>2</sup>	$I_{D, pulse}$	-	-	18	A	$T_c = 25\text{ °C}$ ; $V_G = 6\text{ V}$
Pulsed current, drain-source <sup>2</sup>	$I_{D, pulse}$	-	-	10	A	$T_c = 125\text{ °C}$ ; $V_G = 6\text{ V}$
Gate-source voltage, continuous <sup>3</sup>	$V_{GS}$	-1.4	-	+7	V	$T_j = -55\text{ °C}$ to $150\text{ °C}$
Gate-source voltage, pulsed	$V_{GS, pulse}$	-	-	+10	V	$T_j = -55\text{ °C}$ to $150\text{ °C}$ ; $t_{Pulse} = 50\text{ ns}$ , $f = 100\text{ kHz}$ ; open drain
Power dissipation	$P_{tot}$	-	-	75	W	$T_c = 25\text{ °C}$
Operating temperature	$T_j$	-55	-	+150	°C	
Storage temperature	$T_{stg}$	-55	-	+150	°C	

1.  $V_{DS, transient}$  is intended for surge rating during non-repetitive events,  $t_{Pulse} < 1\text{ }\mu\text{s}$ .

2. Pulse width =  $10\text{ }\mu\text{s}$ .

3. The minimum  $V_{GS}$  is clamped by ESD protection circuit, as shown in Figure 8.

## 2 Thermal characteristics

**Table 4 Thermal characteristics**

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Thermal resistance, junction-case	$R_{thJC}$	-	-	1.65	°C/W	
Reflow soldering temperature	$T_{sold}$	-	-	260	°C	MSL3

### 3 Electrical characteristics

at  $T_j = 25\text{ }^\circ\text{C}$ , unless specified otherwise.

**Table 5 Static characteristics**

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	1.2	1.6	2.5	V	$I_D = 11\text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25\text{ }^\circ\text{C}$
		-	1.6	-		$I_D = 11\text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 125\text{ }^\circ\text{C}$
Drain-source leakage current	$I_{DSS}$	-	0.4	20	$\mu\text{A}$	$V_{DS} = 650\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$
		-	4	-		$V_{DS} = 650\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	-	200	$\mu\text{A}$	$V_{GS} = 6\text{ V}$ ; $V_{DS} = 0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	160	200	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$ ; $I_D = 3\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$
		-	330	-	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$ ; $I_D = 3\text{ A}$ ; $T_j = 125\text{ }^\circ\text{C}$
Gate resistance	$R_G$	-	3.5	-	$\Omega$	$f = 5\text{ MHz}$ ; open drain

**Table 6 Dynamic characteristics**

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	83	-	pF	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 400\text{ V}$ ; $f = 100\text{ kHz}$
Output capacitance	$C_{oss}$	-	27	-	pF	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 400\text{ V}$ ; $f = 100\text{ kHz}$
Reverse transfer capacitance	$C_{rss}$	-	0.4	-	pF	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 400\text{ V}$ ; $f = 100\text{ kHz}$
Effective output capacitance, energy related <sup>1</sup>	$C_{o(er)}$	-	35	-	pF	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 0\text{ to }400\text{ V}$
Effective output capacitance, time related <sup>2</sup>	$C_{o(tr)}$	-	54	-	pF	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 0\text{ to }400\text{ V}$
Output charge	$Q_{oss}$	-	22	-	nC	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 0\text{ to }400\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	2	-	ns	$V_{DS} = 400\text{ V}$ ; $I_D = 6\text{ A}$ ; $L = 318\text{ }\mu\text{H}$ ; $V_{GS} = 6\text{ V}$ ; $R_{on} = 10\text{ }\Omega$ ; $R_{off} = 2\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	4	-	ns	
Rise time	$t_r$	-	5	-	ns	
Fall time	$t_f$	-	6	-	ns	

1.  $C_{o(er)}$  is the fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V.

2.  $C_{o(tr)}$  is the fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V.

**Table 7 Gate charge characteristics**

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate charge	$Q_G$	-	2.3	-	nC	$V_{GS} = 0$ to 6 V; $V_{DS} = 400$ V; $I_D = 3$ A
Gate-source charge	$Q_{GS}$	-	0.2	-	nC	
Gate-drain charge	$Q_{GD}$	-	0.9	-	nC	
Gate plateau voltage	$V_{plat}$	-	2.4	-	V	$V_{DS} = 400$ V; $I_D = 3$ A

**Table 8 Reverse conduction characteristics**

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Source-drain reverse voltage	$V_{SD}$	-	2.5	-	V	$V_{GS} = 0$ V; $I_{SD} = 3$ A
Pulsed current, reverse	$I_{S, pulse}$	-	20	-	A	$V_{GS} = 6$ V
Reverse recovery charge	$Q_{rr}$	-	0	-	nC	$I_{SD} = 3$ A; $V_{DS} = 400$ V
Reverse recovery time	$t_{rr}$	-	0	-	ns	
Peak reverse recovery current	$I_{rrm}$	-	0	-	A	

## 4 Electrical characteristics diagrams

at  $T_j = 25\text{ }^\circ\text{C}$ , unless specified otherwise.

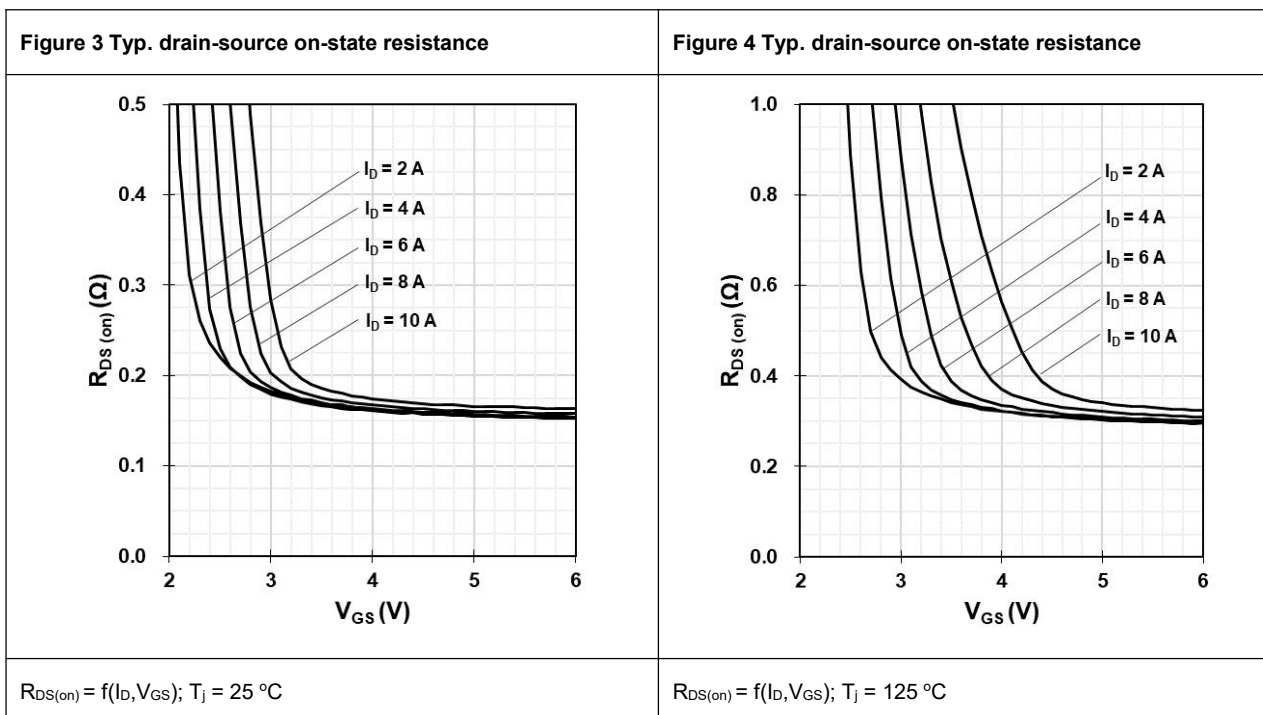
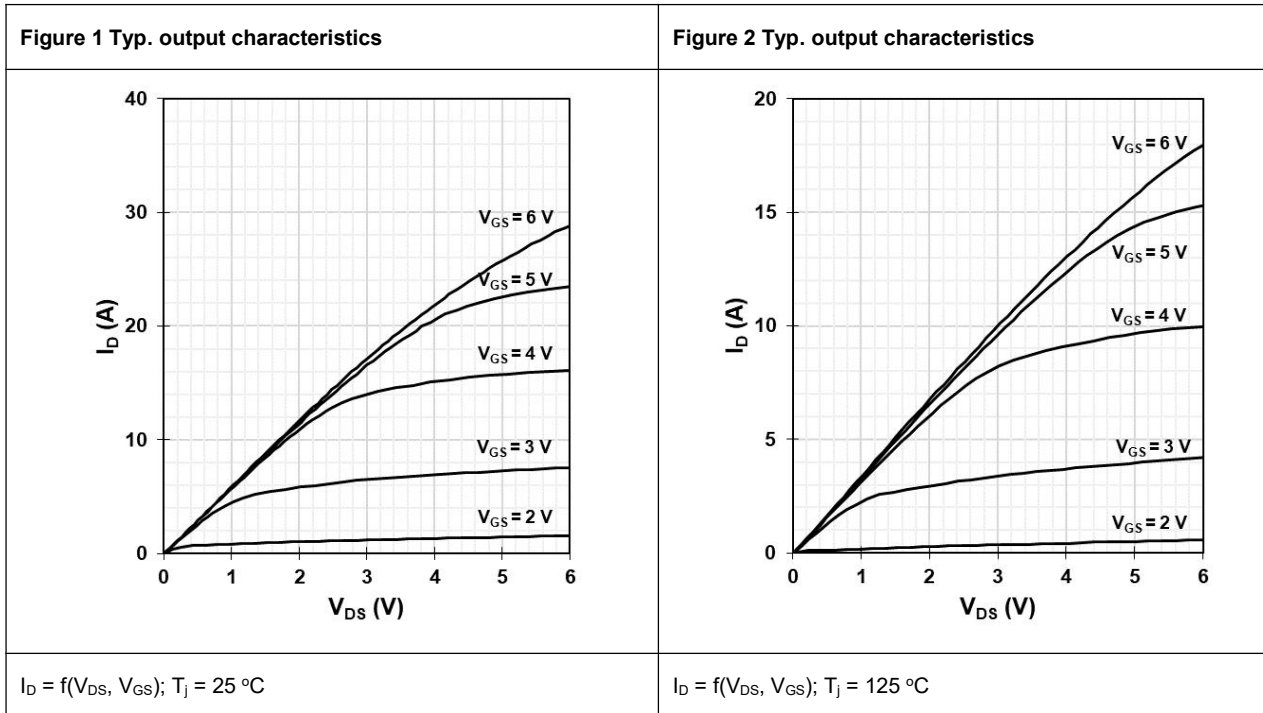
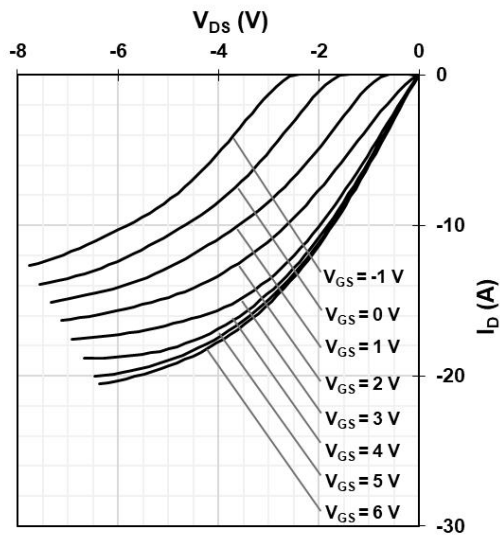
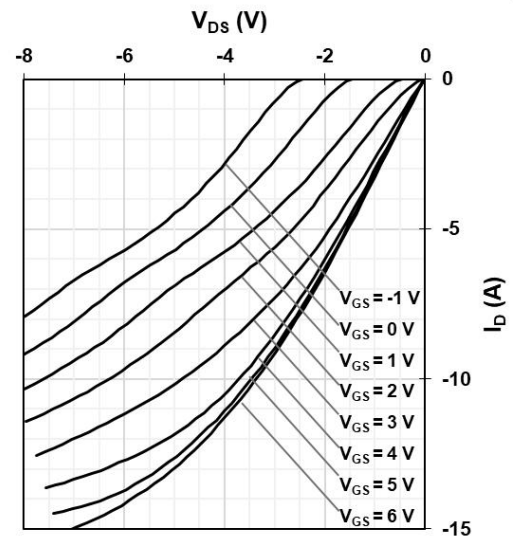


Figure 5 Typ. channel reverse characteristics



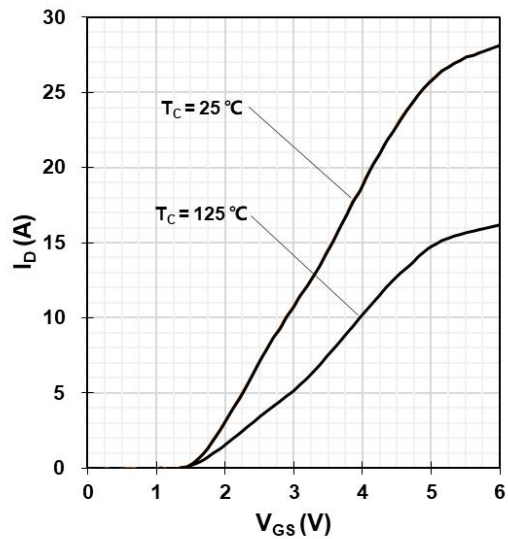
$$I_D = f(V_{DS}, V_{GS}); T_J = 25\text{ }^\circ\text{C}$$

Figure 6 Typ. channel reverse characteristics



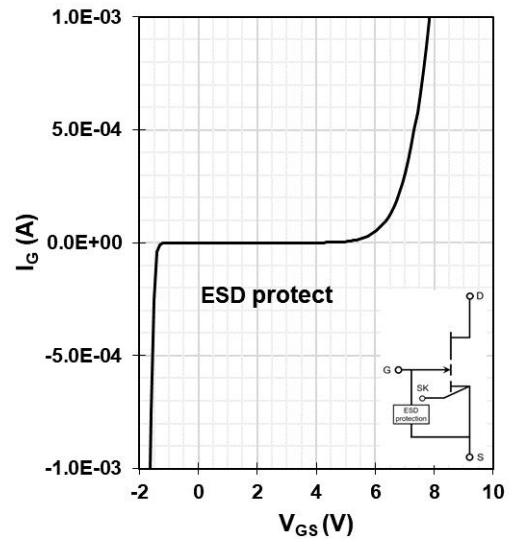
$$I_D = f(V_{DS}, V_{GS}); T_J = 125\text{ }^\circ\text{C}$$

Figure 7 Typ. transfer characteristics



$$I_D = f(V_{GS}); V_{DS} = 5\text{ V}$$

Figure 8 Typ. gate-to-source leakage



$$I_G = f(V_{GS}); I_G \text{ reverse turn on by ESD unit; } V_D = \text{open}$$

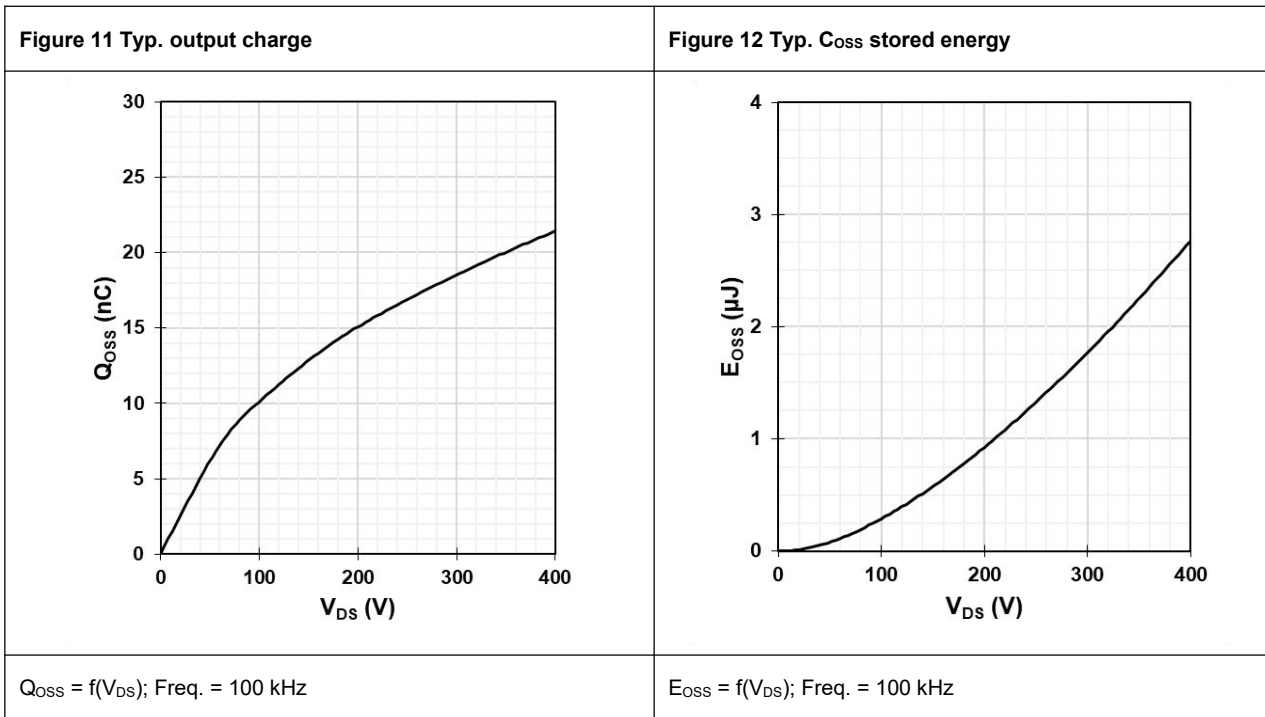
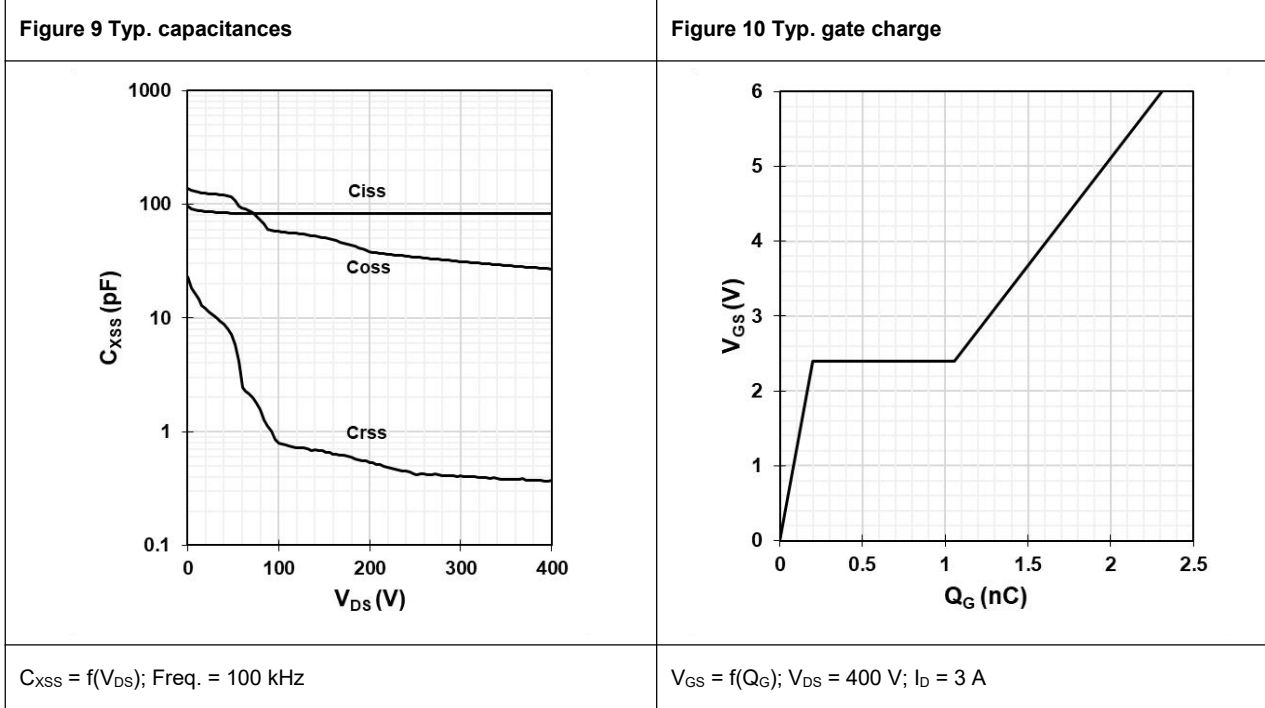
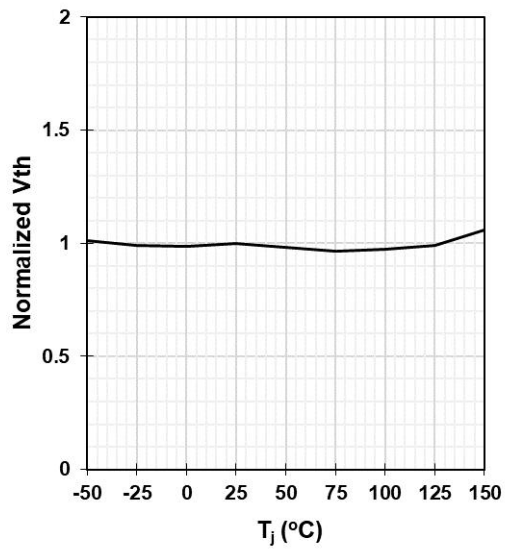
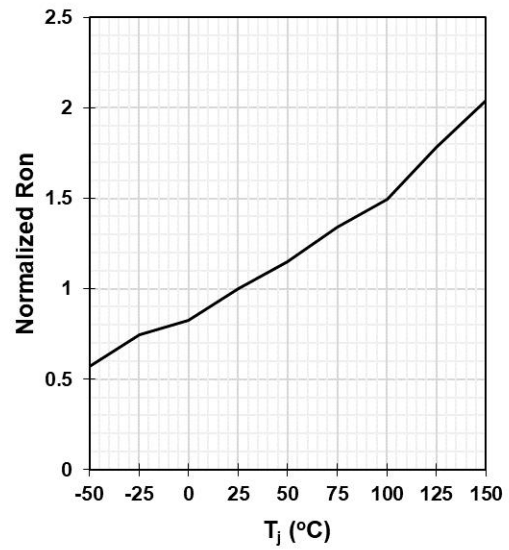


Figure 13 Gate threshold voltage



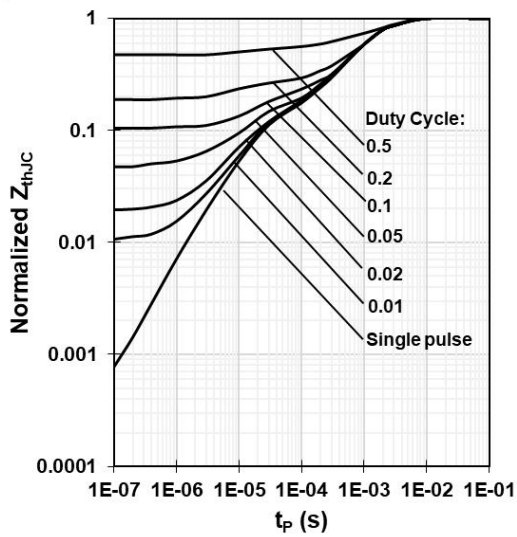
$$V_{GS(TH)} = f(T_j); V_{GS} = V_{DS}; I_D = 11 \text{ mA}$$

Figure 14 Drain-source on-state resistance



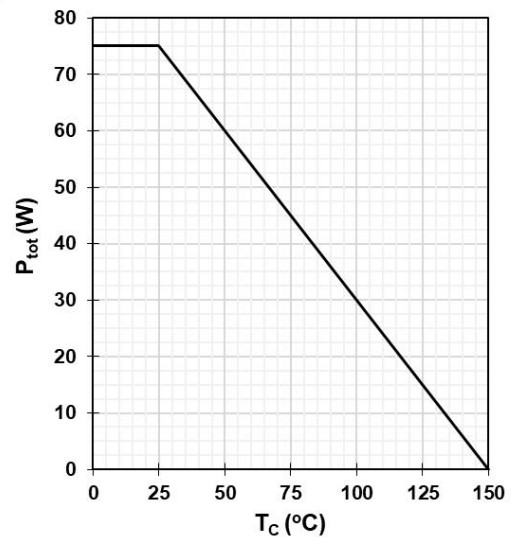
$$R_{DS(on)} = f(T_j); I_D = 3 \text{ A}; V_{GS} = 6 \text{ V}$$

Figure 15 Max. transient thermal impedance



$$Z_{thJC} = f(t_p, D)$$

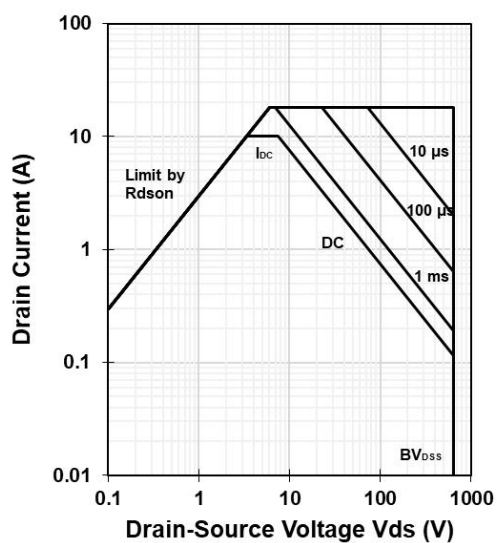
Figure 16 Power dissipation



$$P_{tot} = f(T_c)$$

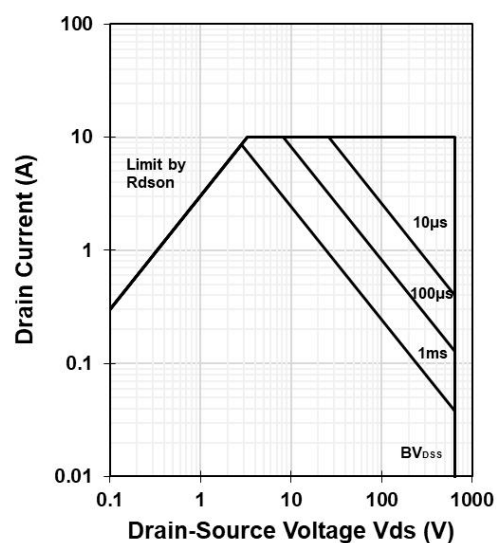


Figure 17 Safe operating area



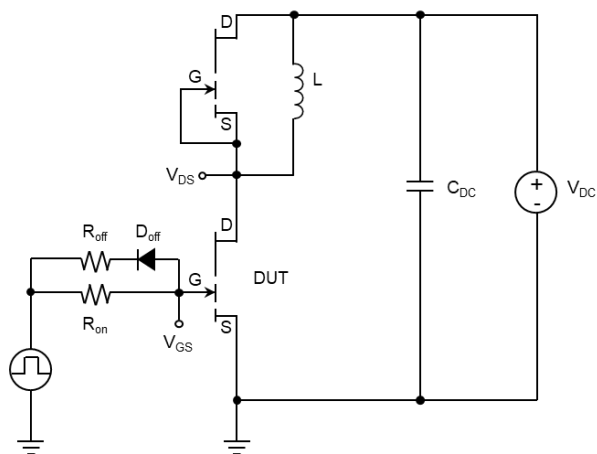
$$I_D = f(V_{DS}); T_C = 25\text{ °C}$$

Figure 18 Safe operating area



$$I_D = f(V_{DS}); T_C = 125\text{ °C}$$

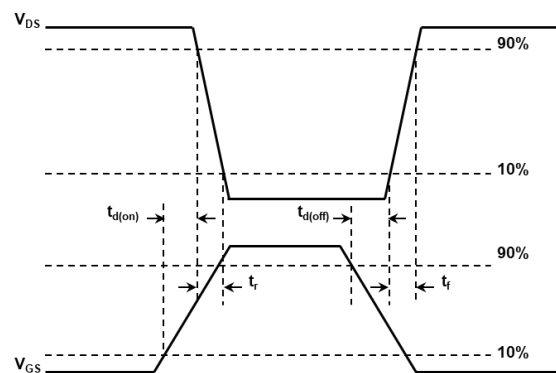
Figure 19 Switching times test circuit



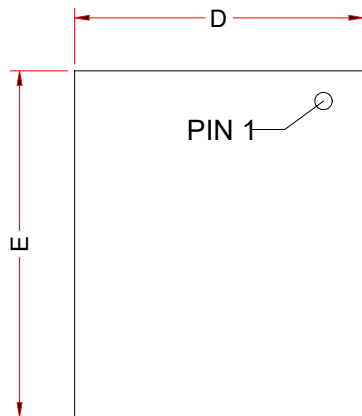
$$V_{DS} = 400\text{ V}, I_D = 6\text{ A}, L = 318\text{ }\mu\text{H}, V_{GS} = 6\text{ V},$$

$$R_{on} = 10\text{ }\Omega, R_{off} = 2\text{ }\Omega$$

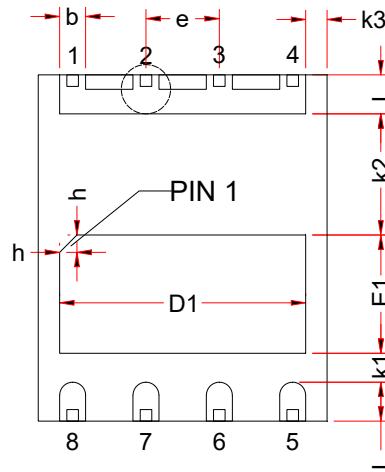
Figure 20 Typ. switching times waveform



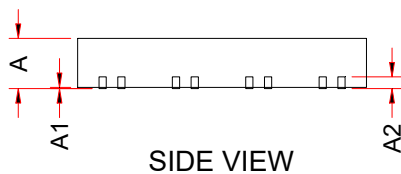
## 5 Package outlines



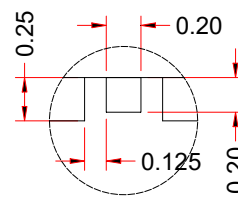
TOP VIEW



BOTTOM VIEW



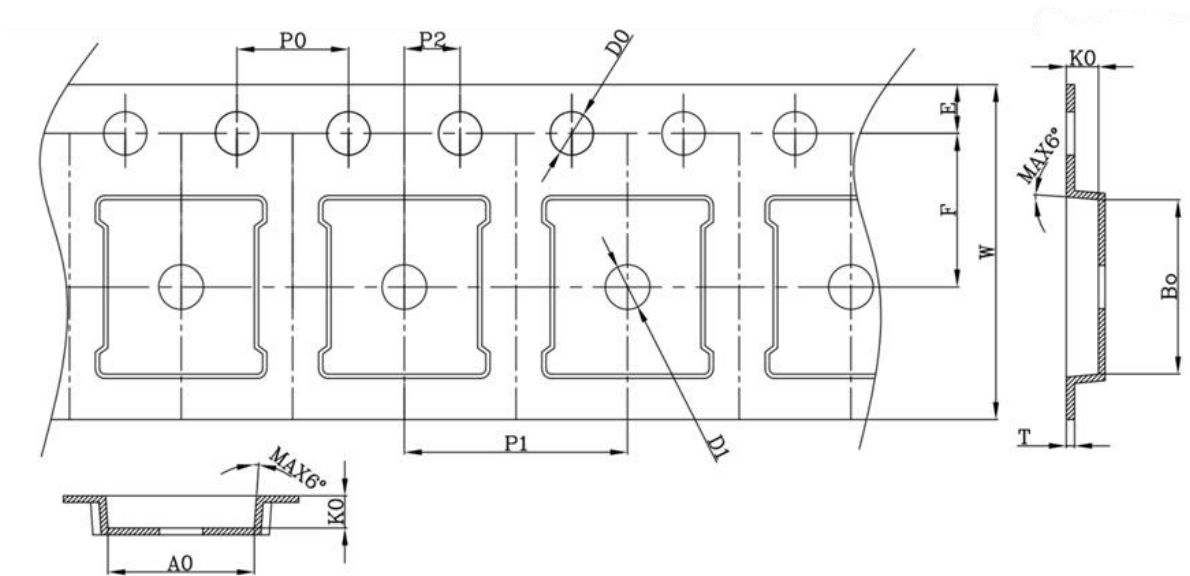
SIDE VIEW



LEAD DETAIL

	MIN	MID	MAX
A	0.75	0.85	0.95
A1	0.00	0.02	0.05
A2	0.203REF		
b	0.40	0.45	0.50
D	4.90	5.00	5.10
D1	4.16	4.26	4.36
E	5.90	6.00	6.10
E1	1.95	2.05	2.15
h	0.20	0.30	0.40
L	0.575	0.675	0.775
e	1.270BSC		
k1	0.400MIN		
k2	2.000MIN		
k3	0.270MIN		

## 6 Reel information



SYMBOL	DIMENSION	SYMBOL	DIMENSION
W	12.00±0.30	10P0	40.00±0.20
E	1.75±0.10	P1	8.00±0.10
F	5.50±0.05	A0	5.25±0.10
D0	1.55±0.05	B0	6.25±0.10
D1	1.55±0.10	K0	1.15±0.10
P0	4.00±0.10	T	0.25±0.05
P2	2.00±0.05		

