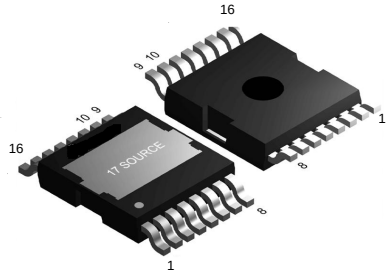
650V GaN Enhancement-mode Power Transistor

Features

- Enhancement-mode transistor - normally-OFF power switch
- Ultra-high switching frequency
- Capable of reverse conduction, no reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free



Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC, LLC
- Fast battery charging
- Industrial, telecom, datacenter SMPS
- High-density power conversion
- High-efficiency power conversion

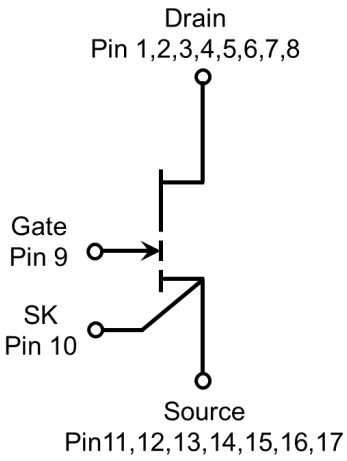


Table 1 Key Performance Parameters at T_j = 25 °C

Parameters	Values	Units
$V_{DS,\ max}$	650	V
$R_{DS(on),\ max}$	40	mΩ
$Q_{G,\ typ}$	13	nC
$I_{DS,\ Pulse}$	87	A
Q_{OSS} @ 400 V	118	nC
Q_{rr}	0	nC

Gate	9
Drain	1,2,3,4,5,6,7,8
Kelvin Source	10
Source	11,12,13,14,15,16,17

Table 2 Ordering Information

Type/Ordering Code	Package	Marking
TBA	TOLT	CID45N65

1 Maximum ratings

at T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Tokmas sales office.

Table 3 Maximum rating

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Drain-source voltage	$V_{DS, max}$	-	-	650	V	V_{GS} = 0 V, I_D = 10 µA
Drain-source voltage transient [1]	$V_{DS, transient}$	-	-	850	V	V_{GS} = 0 V, V_{DS} = 850 V
Continuous current, drain-source	I_D	-	-	45	A	T_c = 25 °C
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	-	87	A	T_c = 25 °C; V_G = 6 V
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	-	46	A	T_c = 125 °C; V_G = 6 V
Gate-source voltage, continuous [3]	V_{GS}	-7	-	+7	V	T_j = -55 °C to 150 °C
Gate-source voltage, pulsed	$V_{GS, pulse}$	-20	-	+10	V	T_j = -55 °C to 150 °C; t_{Pulse} = 50 ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	-	-	312	W	T_c = 25 °C
Operating temperature	T_j	-55	-	+150	°C	
Storage temperature	T_{stg}	-55	-	+150	°C	

1. $V_{DS, transient}$ is intended for surge rating during non-repetitive events, t_{Pulse} < 1 µs.
2. Pulse width = 10 µs.
3. The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 8.

2 Thermal characteristics

Table 4 Thermal characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-	0.4	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

3 Electrical characteristics

at T_j = 25 °C, unless specified otherwise.

Table 5 Static characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	1.2	1.7	2.5	V	I_D = 60 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	1.6	-		I_D = 60 mA; V_{DS} = V_{GS}; T_j = 125 °C
Drain-source leakage current	I_{DSS}	-	10		μA	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C
		-	26	-		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 125 °C
Gate-source leakage current	I_{GSS}	-	330		μA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	35	40	mΩ	V_{GS} = 6 V; I_D = 16 A; T_j = 25 °C
		-	63	-	mΩ	V_{GS} = 6 V; I_D = 16 A; T_j = 125 °C
Gate resistance	R_G	-	1.2	-	Ω	f = 5 MHz; open drain

Table 6 Dynamic characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	443	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Output capacitance	C_{oss}	-	135	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Reverse transfer capacitance	C_{rss}	-	0.26	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	193	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	295	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}	-	118	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Turn-on delay time	$t_{d(on)}$	-	4.0	-	ns	V_{DS} = 400 V; I_D = 12 A; L = 120 μH; V_{GS} = 6 V; R_{on} = 10 Ω; R_{off} = 1 Ω
Turn-on delay time	$t_{d(on)}$	-	8	-	ns	
Turn-off delay time	$t_{d(off)}$	-	5.5	-	ns	
Rise time	t_r	-	12.0	-	ns	

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.
2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

Table 7 Gate charge characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate charge	Q_G	-	13	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D = 16 A
Gate-source charge	Q_{GS}	-	1.0	-	nC	
Gate-drain charge	Q_{GD}	-	4.1	-	nC	
Gate plateau voltage	V_{Plat}	-	2.2	-	V	V_{DS} = 400 V; I_D = 16 A

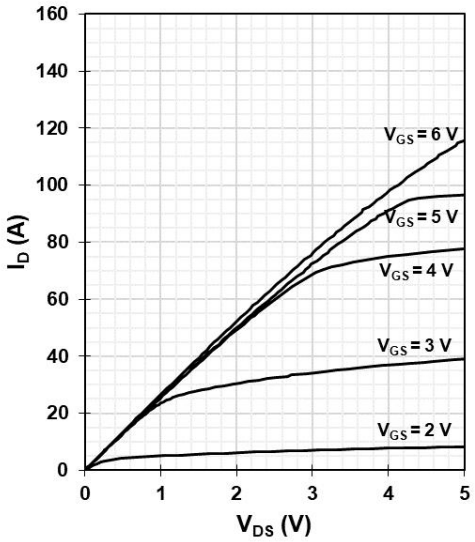
Table 8 Reverse conduction characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Source-drain reverse voltage	V_{SD}	-	2.3	-	V	V_{GS} = 0 V; I_{SD} = 16 A
Pulsed current, reverse	$I_{S,\ pulse}$	-	87	-	A	V_{GS} = 6 V
Reverse recovery charge	Q_{rr}	-	0	-	nC	I_{SD} = 16 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

4 Electrical characteristics diagrams

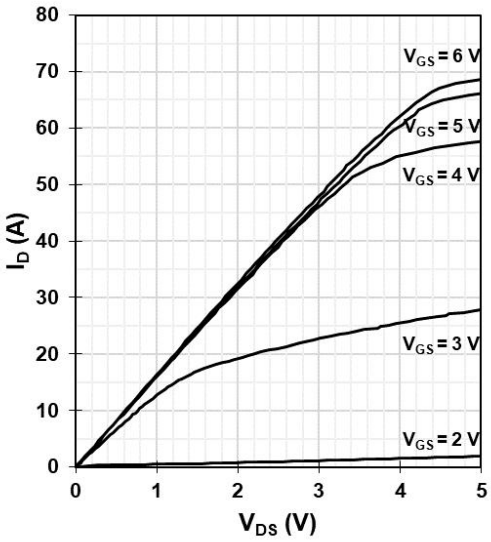
at T_j = 25 °C, unless specified otherwise.

Figure 1 Typ. output characteristics



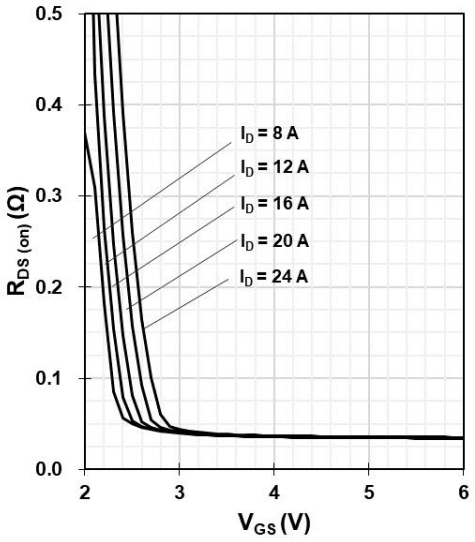
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 2 Typ. output characteristics



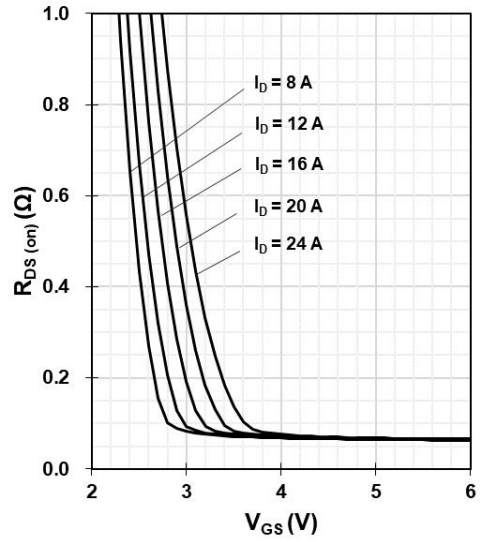
$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 3 Typ. drain-source on-state resistance



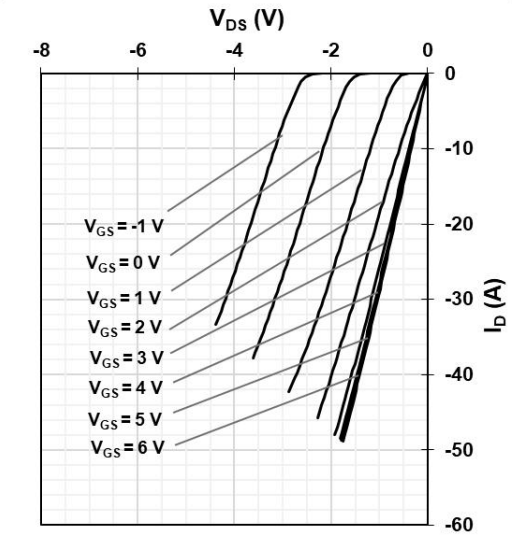
$R_{DS(on)} = f(I_{DS}, V_{GS})$; T_j = 25 °C

Figure 4 Typ. drain-source on-state resistance



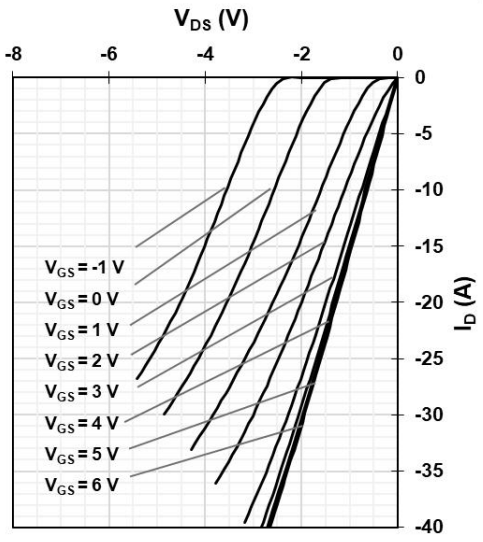
$R_{DS(on)} = f(I_{DS}, V_{GS})$; T_j = 125 °C

Figure 5 Typ. channel reverse characteristics



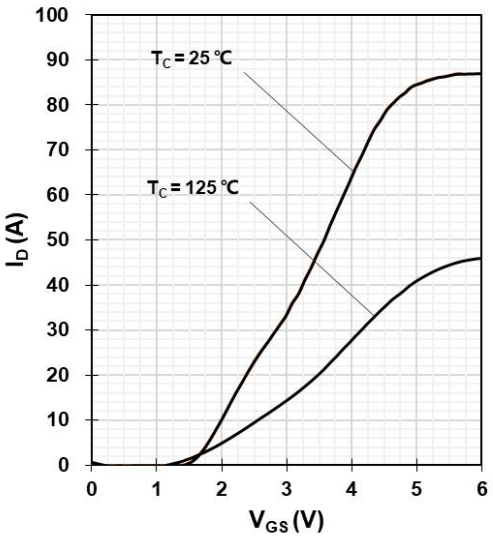
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 6 Typ. channel reverse characteristics



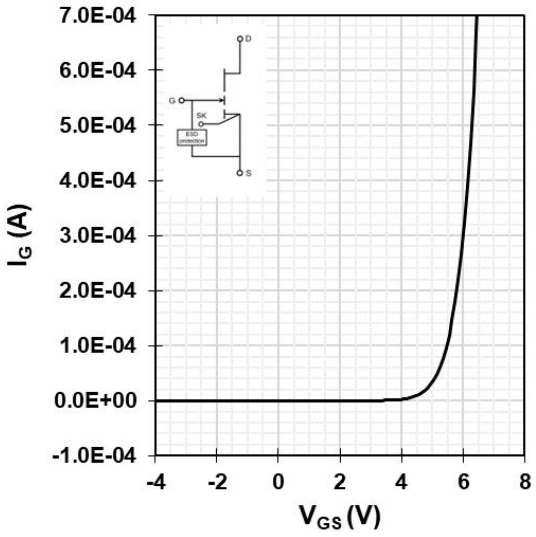
$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 7 Typ. transfer characteristics



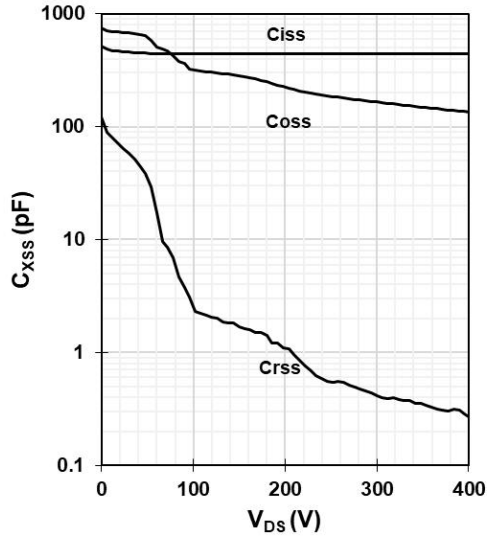
$I_D = f(V_{GS})$; V_{DS} = 5 V

Figure 8 Typ. gate-to-source leakage



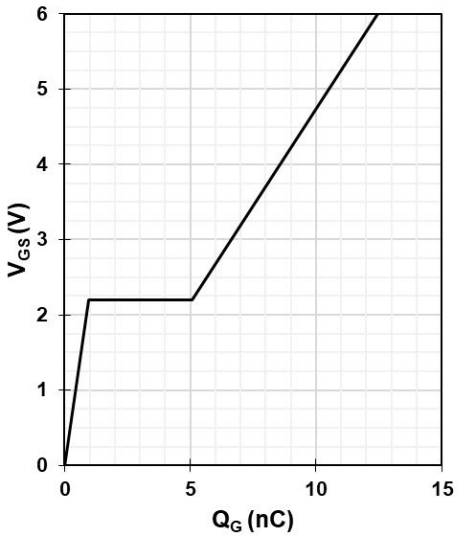
$I_G = f(V_{GS})$; V_D = open

Figure 9 Typ. capacitances



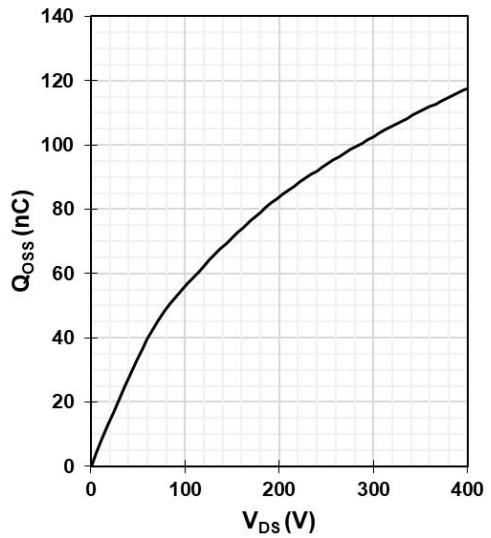
C_{XSS} = f(V_{DS}); Freq. = 100 kHz

Figure 10 Typ. gate charge



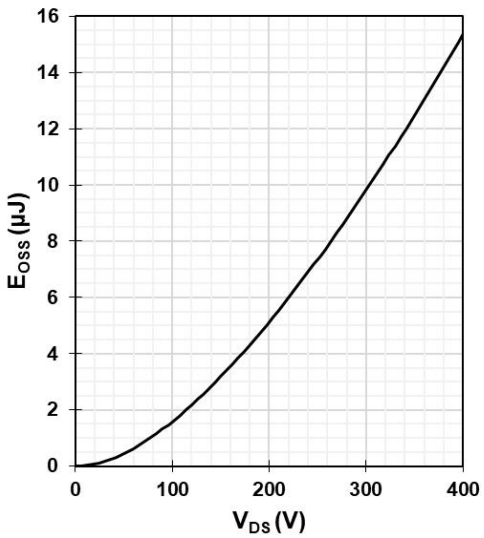
V_{GS} = f(Q_G); $V_{DC-LINK}$ = 400 V; I_D = 16 A

Figure 11 Typ. output charge

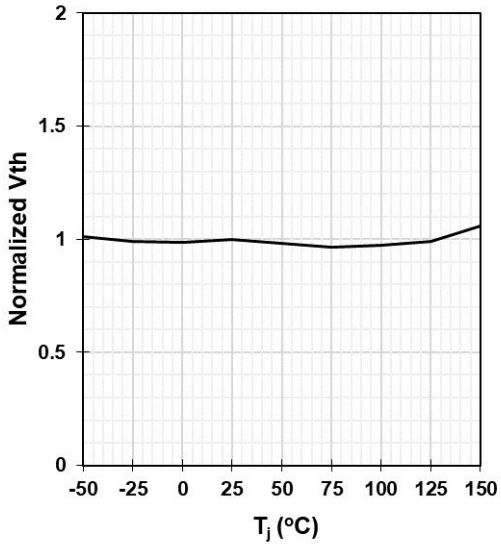
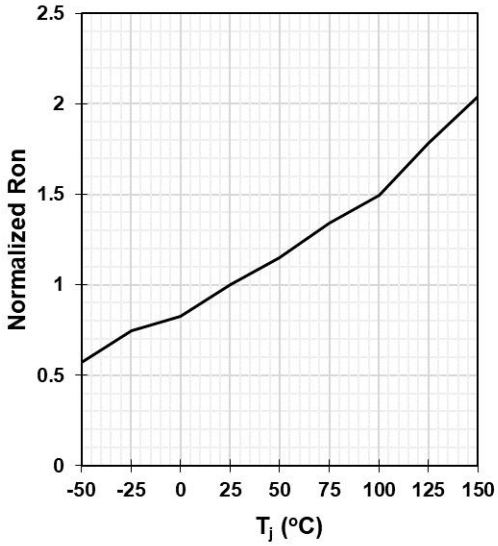


Q_{OSS} = f(V_{DS}); Freq. = 100 kHz

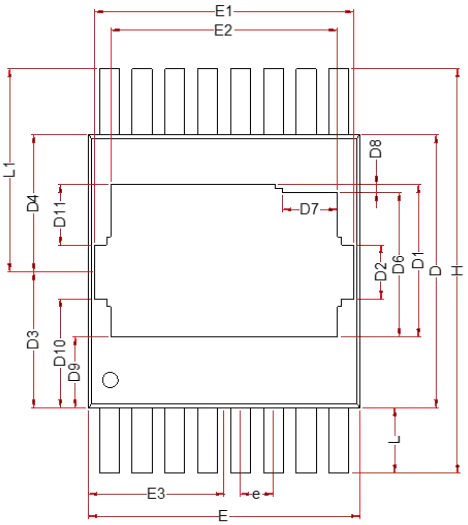
Figure 12 Typ. C_{OSS} stored energy



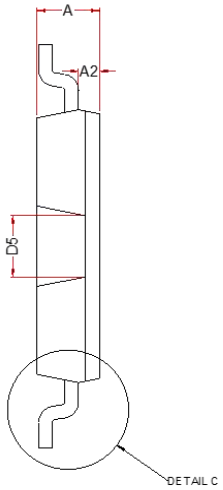
E_{OSS} = f(V_{DS}); Freq. = 100 kHz

Figure 13 Gate threshold voltage	Figure 14 Drain-source on-state resistance
	
$V_{TH} = f(T_j)$; $V_{GS} = V_{DS}$; I_D = 60 mA	$R_{DS(on)} = f(T_j)$; I_D = 16 A; V_{GS} = 6 V

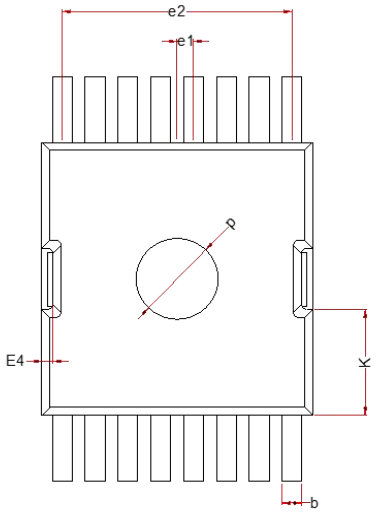
5 Package outlines



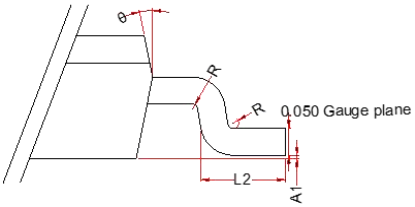
TOP VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL C

Symbol	MIN	MID	MAX
A	2.200	2.275	2.350
A1	0.010	0.060	0.110
A2	0.560	0.760	0.960
b	0.600	0.725	0.850
b1	0.600	0.700	0.800
c	0.450	0.550	0.650
c1	0.450	0.525	0.600
D	10.000	10.150	10.300
D1	5.470	5.670	5.870
D2	1.800	2.000	2.200
D3	4.850	5.050	5.250
D4	5.000	5.065	5.130
D5	2.080	2.280	2.480
D6	5.170	5.370	5.570
D7	1.800	2.000	2.200
D8	0.100	0.300	0.500
D9	2.420	2.620	2.820
D10	3.850	4.050	4.250
D11	2.040	2.240	2.440
E	9.700	9.900	10.100
E1	9.260	9.460	9.660
E2	8.100	8.300	8.500
E3	4.750	4.950	5.150
E4	0.200	0.400	0.600
e	1.200 BSC.		
e1	0.600 BSC.		
e2	8.400 BSC.		
H	14.800	15.000	15.200
K	3.710	3.910	4.110
L	2.250	2.450	2.650
L1	7.300	7.500	7.700
L2	1.300	1.500	1.700
R	0.070	-	-
P	2.900	3.000	3.100
θ	4°	7°	10°