

## SOT-363 Plastic-Encapsulate MOSFETS

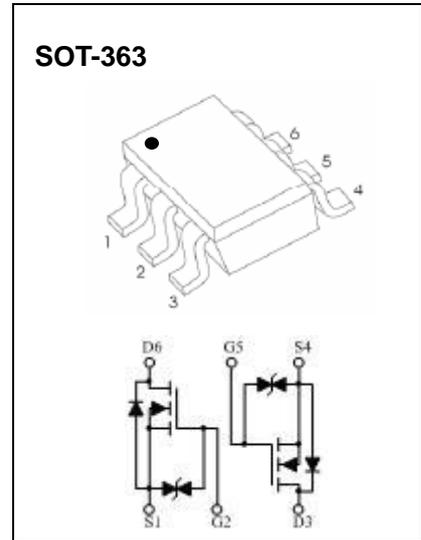
### CJ3134KDW Dual N-Channel MOSFET

#### FEATURE

- Lead Free Product is Acquired
- Surface Mount Package
- N-Channel Switch with Low  $R_{DS(on)}$
- Operated at Low Logic Level Gate Drive
- Equivalent to Two CJ3134K

#### APPLICATION

- Load/Power Switching
- Interfacing Switching
- Battery Management for Ultra Small Portable Electronics
- Logic Level Shift



#### MARKING: 34K

#### ABSOLUTE MAXIMUM RATINGS ( $T_a=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-source voltage	$V_{DS}$	20	V
Gate-source voltage	$V_{GS}$	$\pm 12$	V
Continuous drain current ( $t \leq 10\text{s}$ )	$I_D$	0.75	A
Power dissipation*	$P_D$	0.15	W
Thermal resistance from junction to ambient	$R_{\theta JA}$	833	$^{\circ}\text{C/W}$
Junction temperature	$T_J$	150	$^{\circ}\text{C}$
Storage temperature	$T_{stg}$	-55~ +150	$^{\circ}\text{C}$

\* Repetitive rating : Pulse width limited by junction temperature.

ELECTRICAL CHARACTERISTICS ( $T_a=25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>STATIC PARAMETERS</b>						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 20V, V_{GS} = 0V$			1	$\mu A$
Gate-body leakage current	$I_{GSS}$	$V_{GS} = \pm 12V, V_{DS} = 0V$			$\pm 50$	$\mu A$
Gate threshold voltage (note 1)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.35		1	V
Drain-source on-resistance (note 1)	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 0.65A$			380	$m\Omega$
		$V_{GS} = 2.5V, I_D = 0.55A$			450	$m\Omega$
		$V_{GS} = 1.8V, I_D = 0.45A$			800	$m\Omega$
Forward tranconductance (note 1)	$g_{FS}$	$V_{DS} = 10V, I_D = 0.8A$		1.6		S
Diode forward voltage(note 1)	$V_{SD}$	$I_S = 0.15A, V_{GS} = 0V$			1.2	V
<b>DYNAMIC PARAMETERS (note 2)</b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 16V, V_{GS} = 0V, f = 1MHz$		79	120	pF
Output Capacitance	$C_{oss}$			13	20	pF
Reverse Transfer Capacitance	$C_{rss}$			9	15	pF
<b>SWITCHING PARAMETERS(note 2)</b>						
Turn-on delay time	$t_{d(on)}$	$V_{GS} = 4.5V, V_{DS} = 10V, I_D = 0.5A, R_{GEN} = 10\Omega$		6.7		ns
Turn-on rise time	$t_r$			4.8		ns
Turn-off delay time	$t_{d(off)}$			17.3		ns
Turn-off fall time	$t_f$			7.4		ns
Total Gate Charge	$Q_g$	$V_{DS} = 10V, V_{GS} = 4.5V, I_D = 7A$		20		nC
Gate-Source Charge	$Q_{gs}$			1		nC
Gate-Drain Charge	$Q_{gd}$			4		nC

**Notes :**

1. Pulse Test : Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 0.5\%$ .
2. Guaranteed by design, not subject to production testing.

