13. ELECTRICAL SPECIFICATIONS

The following abbreviations, acronyms, symbols, and terms are used in the following sections:

- CFG Abbreviation for 'Configuration'
- CMD Abbreviation for Command
- CMOS Acronym for 'complementary metal-oxide semiconductor'
- High-Z A term used to indicate a high-impedance state
- MCLK An abbreviation used to indicate the CL-GD7556 internal memory clock
- T A symbol used to indicate the period for the CL-GD7556 internal MCLK
- T_A A symbol used to indicate ambient temperature
- tbd Acronym for 'to be determined'
- TYP An abbreviation used to indicate a 'typical' value
- V An abbreviation for 'volts'
- VCLK An abbreviation used to indicate the CL-GD7556 internal graphics/video clock

13.1 Absolute Maximum Ratings

Specification	Maximum Rating
Ambient temperature while operating (T_A)	0°C to 70°C
Storage temperature	–65°C to 150°C
Voltage on any I/O pin	– 0.5 V to +5.5 V
Operating power dissipation	2.75 Watts
Power supply voltage (V_{DD})	3.5 V
Injection current (latch-up testing)	100 mA

NOTES:

1) System components must be operated within the limits of the absolute maximum ratings. If system components are run at ratings at or outside these limits, the system components can be permanently damaged.
2) Functional operation at, or outside, any of the conditions indicated in the absolute maximum ratings is not implied.
3) Exposure to absolute maximum rating conditions for extended periods can affect system reliability.
4) All voltages are referenced to V_{SS}, which is tied to system ground.
5) 'Positive' currents are currents going into the CL-GD7556. 'Negative' currents are currents coming out of the CL-GD7556.

13.2 DC Specifications

13.2.1 DC Specifications — Digital Values

In the table below, V_{DD} = 3.3 ± 0.15 V and T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Units	Conditions	Note
V_{DD}	Power Supply Voltage	3.15	3.45	Volts	Normal operation	
V_{IH}	Input High Voltage	$0.7V_{DD}$	V_{DD} + 0.5	Volts	3.15 V < V_{DD} < 3.45 V	1
V_{IL}	Input Low Voltage	–0.5	$0.3V_{DD}$	Volts	3.15 V < V_{DD} < 3.45 V	1
V_{OH}	Output High Voltage	2.8	V_{DD}	Volts	I_{OH} = (see Table 13-1), V_{DD} = 3.15 V	
V_{OH}	MD[63:0] Output High Voltage	2.0	V_{DD}	Volts	I_{OH} = –12 mA, V_{DD} = 3.3 V	2
V_{OL}	Output Low Voltage		0.33	Volts	I_{OL} = (see Table 13-1), V_{DD} = 3.15 V	
V_{OL}	MD[63:0] Output Low Voltage		0.6	Volts	I_{OL} = 12 mA, V_{DD} = 3.3 V	3
I_{DD1}	Power Supply Current		345	mA	CRT-only operation: 1280 × 1024, 8 bpp, 60-Hz vertical refresh. Video window, V-Port, and BitBLT running simultaneously.	4
I_{DD2}	Power Supply Current		475	mA	Flat panel-only operation: XGA DSTN panel. Video window, V-Port, and BitBLT running simultaneously.	4
I_{DD3}	Power Supply Current		2	mA	Hardware-controlled Suspend mode	4
I_{IL}	Input Low Current		–10	µA	V_{IN} = 0.0 V	
I_{IH}	Input High Current		10	µA	V_{IN} = 5.25 V	5
I_{OZ}	Output Leakage Current	–10	10	µA	0 < V_{OUT} < 5.25 V	5,6
C_{IN}	Input Capacitance		10	pF		7
C_{OUT}	Output Capacitance		10	pF		7

NOTES:

1) All CL-GD7556 inputs are CMOS compatible, which means the threshold is approximately in the center of the voltage swing from V_{SS} (that is, ground) to V_{DD}.
2) When V_{DD} = 3.3 V, outputs MD[63:0] rated at V_{OH} = 2.4 V at I_{OH} = –3 mA can source I_{OH} = –12 mA at V_{OH} = 2.0 V.
3) When V_{DD} = 3.3 V, outputs MD[63:0] rated at V_{OL} = 0.4 V at I_{OL} = 4 mA can sink I_{OL} = 12 mA at V_{OL} = 0.6 V.
4) These power supply current values occur when V_{DD} = 3.3 V and MCLK = 80 MHz.
5) The I/O inputs of the CL-GD7556 are 5.0-V tolerant.
6) This current is a measure of tristate output leakage current when in high-impedance mode.
7) This capacitance is periodically sampled and tested.

Table 13-1. Loading Values for Digital Output Pins

PQFP Pin Number[a]	Pin Name	I_{OH} (mA)	I_{OL} (mA)	Load (pF)
26–35, 37–42, 67–76, 78–81, 83–84	AD[31:0]	–3	2	240
43	INTR#	–4	6	200
45	STOP#	–4	10	200
46	PAR	–4	10	200
47	DEVSEL#	–6	10	200
48	TRDY#	–6	10	200
57	SUSPST#	–4	6	35
98	DDCC / VCLKO	—	6	35
104	DDCD	—	4	50
112	HSYNC	–4	6	50
114	VSYNC	–4	6	50
115	VREF	Analog Output		
118	CSYNC	–4	6	50
119	PROG1	–3	6	50
120	BLUE	Analog Output		
121	GREEN	Analog Output		
122	RED	Analog Output		
123	FPVEE	–3	6	35
124	FPDECTL	–4	6	50
125	FPVCC	–3	6	35
127	PROG0 / TV-ON	–3	6	50
129	PROG2 / NTSC/PAL	–3	6	50
150:143, 141:135, 133:131, 176:172, 170:166, 164:157	FP[35:0]	–3	6	50
152	FPDE	–3	6	50
153	LLCLK[b]	–4	6	50
155	FPVDCLK[a]	–4	6	50
156	LFS	–3	6	50
178–187, 195–199, 201–206, 209–219, 234–238, 240–242, 245–249, 3–7, 9–14, 17–24	MD[63:0]	–3	4	50
188–189, 207–208, 243–244, 15–16	CAS[7:0]#	–3	4	50
	WE[7:0]#	–3	4	50
193, 221–225, 229–232	MA[9:0]	–3	4	50
194, 228	RAS[1:0]#	–3	4	50
226	CAS# / WE#	–3	4	50
245–249, 3–7, 9–14	ROMA[15:0]	–3	4	50
253	EROM#	–3	4	50
255	OE#	–3	4	50

[a] See Table 1-1 for the equivalent PBGA ball-position numbers.

[b] The LLCLK and FPVDCLK I_{OH} and I_{OL} values depend on the setting of Extension register bit SR2B[7]. The default is SR2B[7] = 0. When this bit = 1, the values for these pins are: I_{OH} = –8 mA, I_{OL} = 12 mA, and the load remains 50 pF.

13.2.2 DC Specifications — Palette DAC

In the table below, V_{DD} = 3.3 ± 0.15 V and T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Units	Conditions
DACVDD	DAC Supply Voltage	3.15	3.45	Volts	Normal Operation
$AI_{DD2,3}$	Analog Supply Current		60	mA	$AV_{DD2,3}$ = 3.45 V
I_{REF} [a] (Externally Generated)	DAC Reference Current (Nominal)	6.20	7.14	mA	Refer to note a.

[a] The standard IREF current is generated internally. However, if the internal IREF current is not used, an external source can be supplied by clearing Extension register SR32[5] to 0 and following the directions in the application note "IREF Current Source" in the *CL-GD7556 Application Book*, using the values in this table.

13.2.3 DC Specifications — Frequency Synthesizer

In the table below, V_{DD} = 3.3 ± 0.15 V and T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Units	Conditions
MAVDD VAVDD	Synthesizer Supply Voltage	3.15	3.45	Volts	V_{DD} = 3.3 ± 0.15 V

13.3 DAC Characteristics

In the table below, V_{DD} = 3.3 ± 0.15 V and T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Units	Notes
	Resolution		8	bits	
I_O	Output Current		30	mA	1
t_D	Analog Output Delay		tbd	ns	2, 3
t_r, t_f	Analog Output Rise/Fall Time		5	ns	3, 4
t_s	Analog Output Settling Time		15	ns	3, 5
t_{SK}	Analog Output Skew		tbd	ns	3, 6
FT	Clock and Data Feed-Through		tbd	MHz	3, 6
DT	DAC-to-DAC Correlation		tbd		6, 7
GI	Glitch Impulse		tbd		3, 6
CT	DAC-to-DAC Crosstalk		tbd		3, 4

NOTES:

1) I_O, the output current measure, occurs under the condition V_O < 1 volt.
2) t_D is measured from the 50% point of VCLK to 50% point of full-scale transition.
3) Per analog output, the load is 50 Ω and 30 pF.
4) t_r and t_f are measured from 10% to 90% full-scale.
5) t_s is measured from 50% of full-scale transition to output remaining within 2% of final value.
6) Outputs are loaded identically.
7) About the mid-point of the distribution of the three DACs, measured at full-scale output.

13.4 AC Parameters — List of Timing Relationships

13.5 Chip Configuration — System Reset Timing

The timing diagram in this section is for the CL-GD7556 configuration, which takes place during system reset. Table 13-2 and Figure 13-1 refer to information from the MD[40:24] and SW0 pins, which are read by Extension register bits SR22[7:0] and SR24[7,2:0] and used by the memory data lines to configure the CL-GD7556.

Table 13-2. Chip Configuration — System Reset Timing

Symbol	Parameter	MIN	MAX	Units
t_1	System reset pulse width	12	–	MCLKs
t_2	Memory data setup time to system reset rising edge	2	–	ns
t_3	Memory data hold time from system reset rising edge	5	–	ns
t_4	System reset high to first PCI bus command	12	–	MCLKs

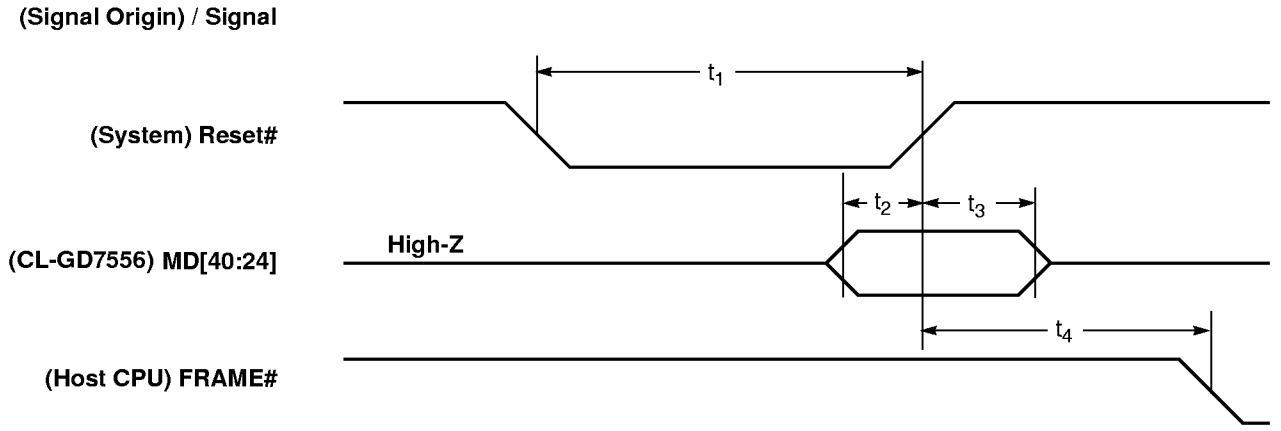


Figure 13-1. Bus Configuration — System Reset Timing

13.6 Timing Diagrams — CL-GD7556 to PCI Bus

The timing diagrams in this section apply to the interface from the CL-GD7556 to the PCI bus.

Table 13-3. PCI Bus — Clock Timing

Symbol	Parameter	MIN	MAX	Units
t_1	Rise time (10% to 90%)	0.5	4.0	ns
t_2	Fall time (90% to 10%)	0.5	4.0	ns
t_3	High pulse width	40%	60%	T_{PCI}
t_4	Low pulse width	40%	60%	T_{PCI}
T_{PCI}	Period	30	tbd	ns

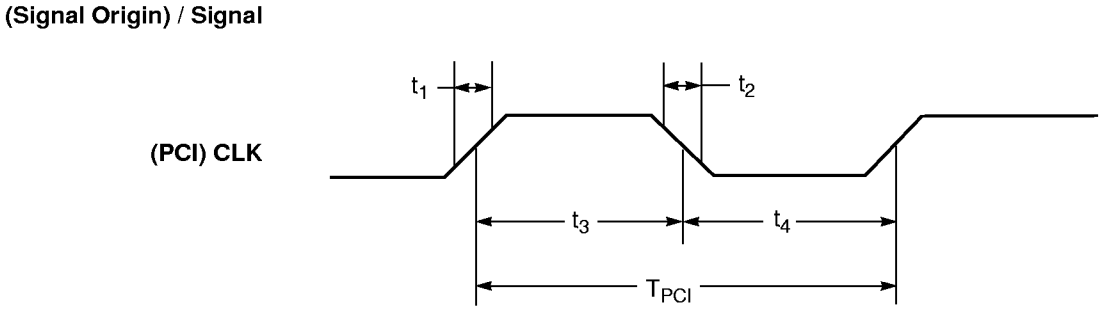


Figure 13-2. PCI Bus — Clock Timing

Table 13-4. PCI Bus — FRAME#, AD[31:0], C/BE[3:0]#, DEVSEL#, and TRDY# Timing

Symbol	Parameter	MIN	MAX	Units
t_1	FRAME# setup to CLK	7	–	ns
t_2	AD[31:0] (Address) setup to CLK	7	–	ns
t_3	AD[31:0] (Address) hold from CLK	0	–	ns
t_4	AD[31:0] (Data) setup to CLK (write)	7	–	ns
t_5	AD[31:0] (Data) hold from CLK (write)	0	–	ns
t_6	C/BE[3:0]# (Bus Command) or (Byte Enable) setup to CLK	7	–	ns
t_7	C/BE[3:0]# (Bus Command) hold from CLK	0	–	ns
t_8	AD[31:0] (Data) delay from CLK (read)	2	11	ns
t_9	AD[31:0] or C/BE[3:0]# to high-impedance delay from CLK (read)	0	28	ns
t_{10}	DEVSEL# delay from CLK	2	15	ns
t_{11}	DEVSEL# and TRDY# high before high-Z	1	–	T_{PCI}
t_{12}	TRDY# delay from CLK	2	18	ns

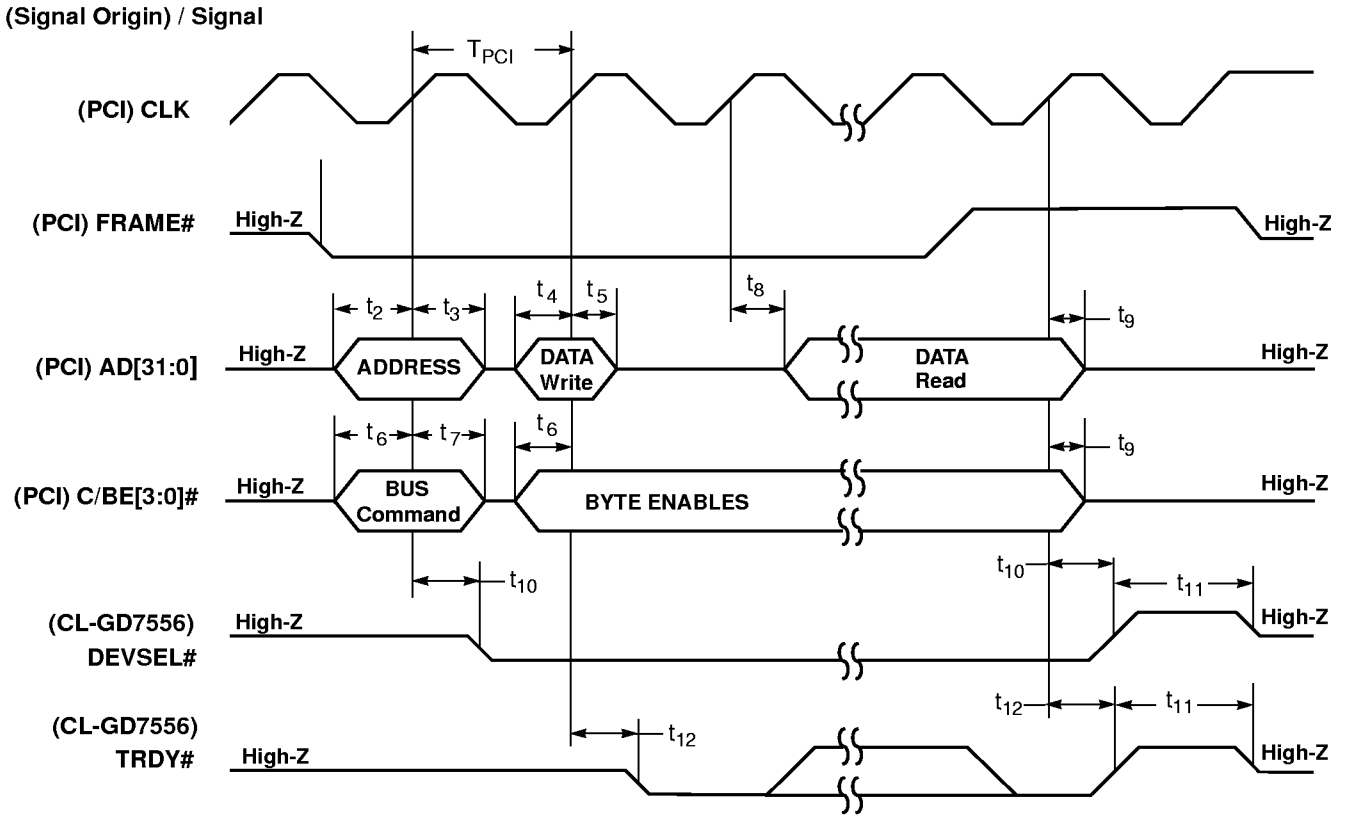


Figure 13-3. PCI Bus — FRAME#, AD[31:0], C/BE[3:0]#, DEVSEL#, and TRDY# Timing

Table 13-5. PCI Bus — STOP# Delay Timing

Symbol	Parameter	MIN	MAX	Units
t_1	STOP# low delay from CLK	2	15	ns
t_2	STOP# high delay from CLK	2	15	ns
t_3	STOP# high pulse before high-Z	1	–	T_{PCI}

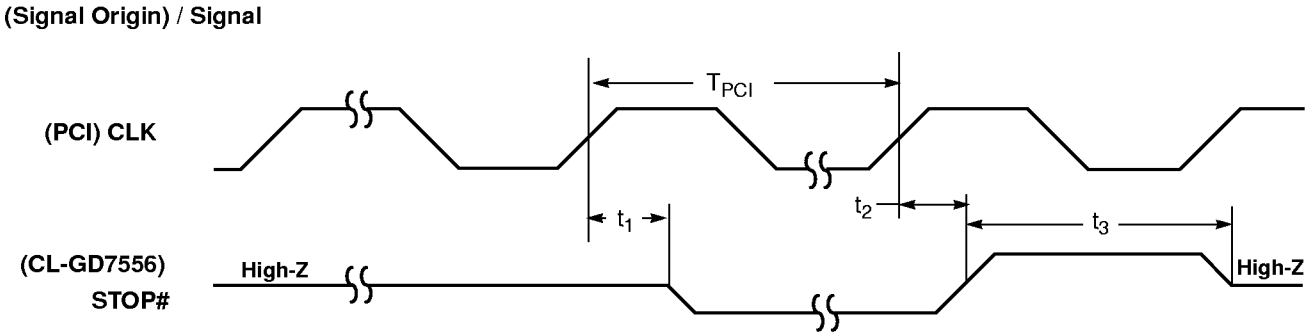


Figure 13-4. PCI Bus — STOP# Delay and Read Data / IRDY# Timing

Table 13-6. PCI Bus — Read Data / TRDY# and IRDY# Timing

Symbol	Parameter	MIN	MAX	Units
t_1	Read Data setup to TRDY# active	7	–	ns
t_2	Read Data hold from TRDY# inactive	0	–	ns
t_3	IRDY# setup to CLK	7	–	ns
t_4	IRDY# hold from CLK	0	–	ns

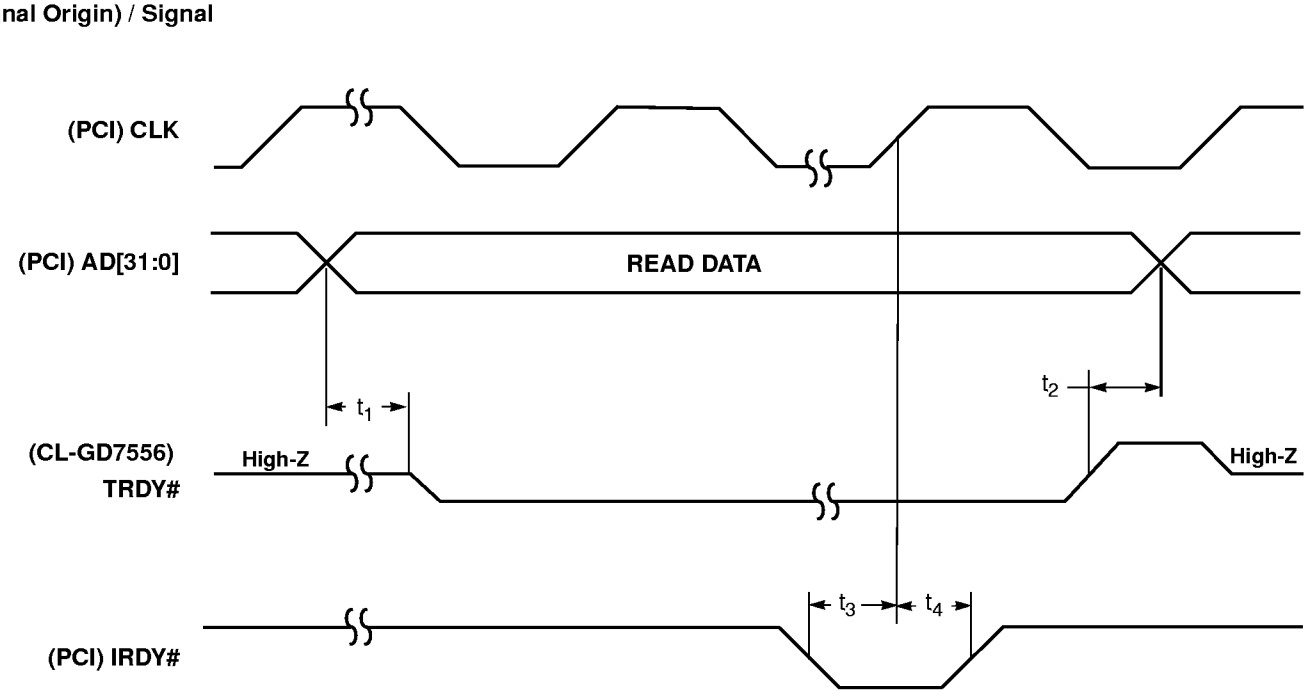


Figure 13-5. PCI Bus — TRDY# Delay and Read Data / IRDY# Timing

Table 13-7. PCI Bus — IDSEL Timing

Symbol	Parameter	MIN	MAX
t_1	IDSEL setup to CLK	7 ns	–
t_2	IDSEL hold from CLK	0 ns	–

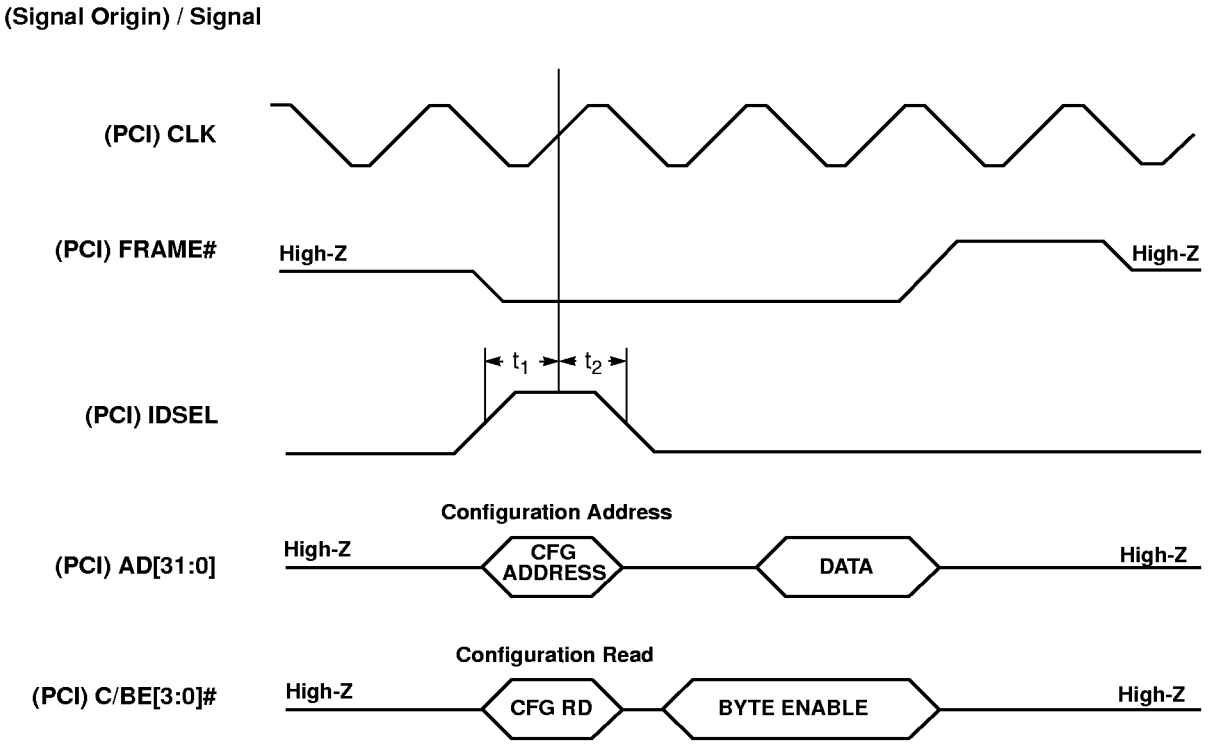


Figure 13-6. PCI Bus — IDSEL Timing

Table 13-8. PCI Bus — Parity Timing

Symbol	Parameter	MIN	MAX	Units
t_1	Address and Command PAR setup from CLK (input to CL-GD7556)	7	–	ns
t_2	Address and Command PAR hold from CLK (input to CL-GD7556)	0	–	ns
t_3	Data In and Byte Enable PAR setup from CLK (input to CL-GD7556)	7	–	ns
t_4	Data In and Byte Enable PAR hold from CLK (input to CL-GD7556)	0	–	ns
t_5	Data output PAR delay from CLK (output from CL-GD7556)	2	12	ns
t_6	Data output PAR 'off' delay from CLK (output from CL-GD7556)	–	28	ns

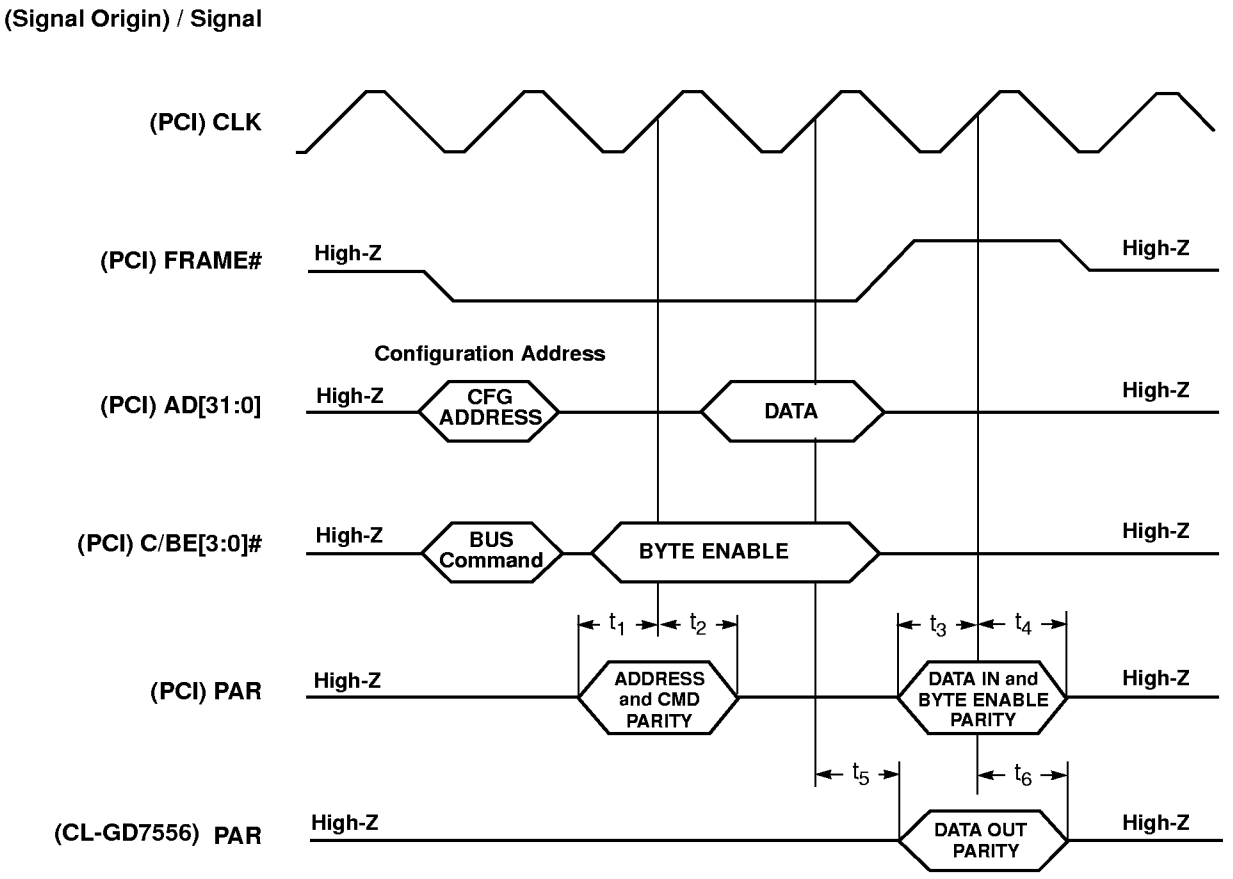


Figure 13-7. PCI Bus — Parity Timing

13.7 Timing Diagrams — CL-GD7556 to Display Memory Bus

The timing diagrams in this section apply to the interface from the CL-GD7556 to a display memory bus. Table 13-9 and Figure 13-8 apply to the interface from the CL-GD7556 to a display memory bus for EDO (extended data out) DRAMs. For the display memory bus interface for EDO DRAMs, the data bus does not go to high-impedance between paged read or write cycles.

Table 13-9. Display Memory Bus — EDO (Hyper-page-mode) DRAM Read and Write Timing

Symbol	Parameter	MIN	MAX
T	MCLK period		
t_1	RAS# pulse width low	5 T	–
t_2	RAS# precharge (t_8 = 8 MCLKs)	3 T – 1 ns	–
	RAS# precharge (t_8 = 9 MCLKs)	4 T – 1 ns	–
t_3	CAS# precharge to RAS# low	1 T – 2 ns	–
t_4	RAS# low to CAS# low delay	4 T – 2 ns	–
t_5	CAS# pulse width low	1 T	–
t_6	CAS# precharge (CAS# pulse width high)	1 T	–
t_7	CAS# (EDO Hyper-page mode) cycle time	2 T	–
t_8	Random read cycle time. (Extension register bits SR20[6] = 0 and GR18[2] = 1.)	8 T	–
	Random read cycle time. (Extension register bits SR20[6] = 1 and GR18[2] = 1.)	9 T	–
t_9	Row address setup to RAS# low	2 T	–
t_{10}	Row address hold from RAS# low	3 T – 3 ns	–
t_{11}	Column address setup to CAS# low	1 T – 3 ns	–
t_{12}	Column address hold from CAS# low	1 T – 2 ns	–
t_{13}	CAS# pulse width low for last cycle of paged read	3 T	–
EDO DRAM Read Timing			
t_{14}	WE# read command setup time	3 T – 2 ns	–
t_{15}	WE# read command hold time	1 T – 2 ns	–
t_{16}	Read data hold CAS# low	5 ns	–
t_{17}	CAS# access time	2 T – 3 ns	–
EDO DRAM Write Timing			
t_{18}	WE# write command setup time	2 T – 4 ns	–
t_{19}	WE# write command hold time	2 T – 4 ns	–
t_{20}	Write data setup time to CAS# low	1 T – 2 ns	–
t_{21}	Write data hold from CAS# low	1 T – 2 ns	–

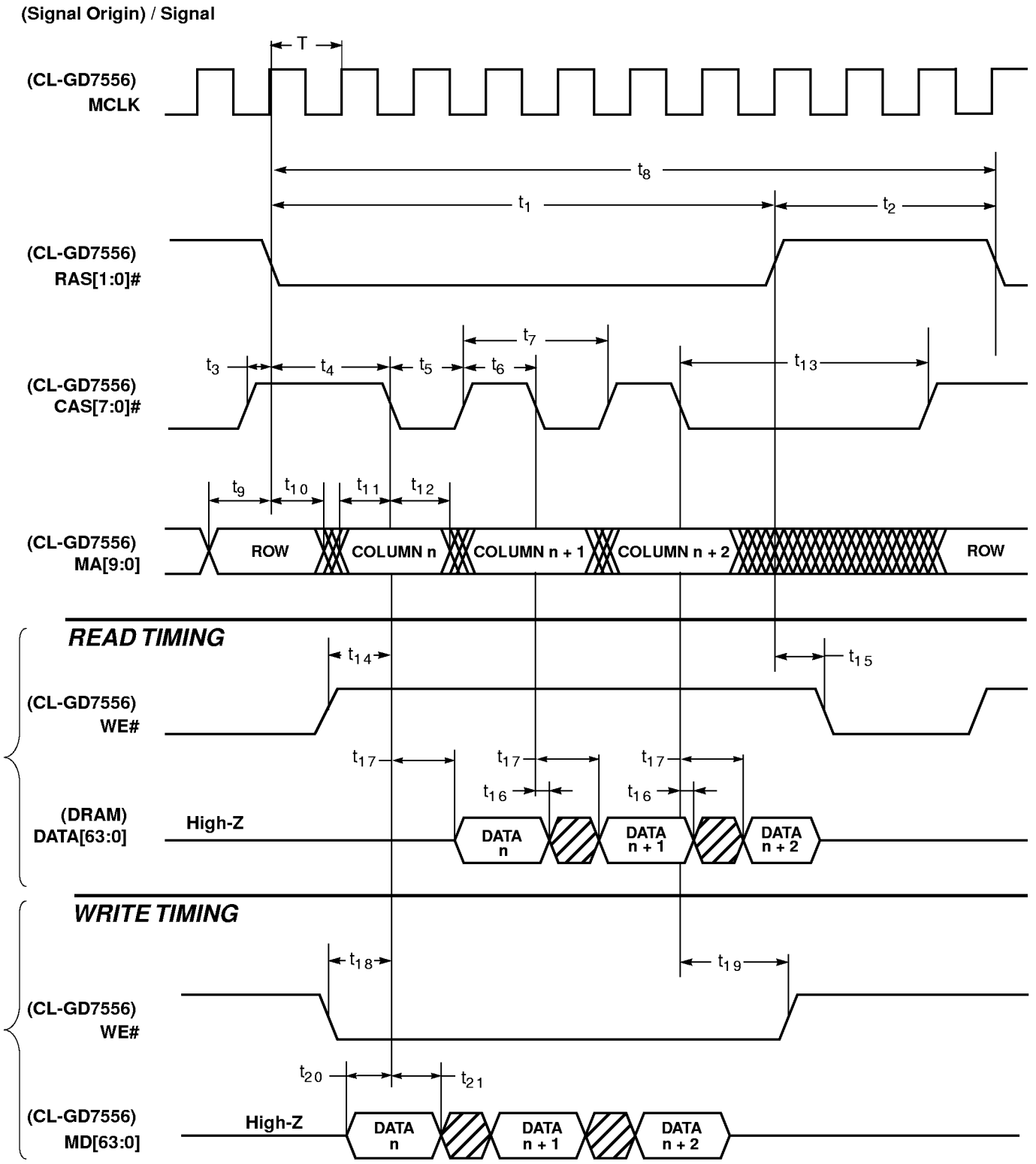


Figure 13-8. Display Memory Bus — Read and Write Timing for EDO DRAMs

Table 13-10. Display Memory Bus — Typical BitBLT Read/Write Cycle Timing

Symbol	Parameter		Nominal Cycle When Extension Register GR18[2] = 1 (EDO DRAM)
T	MCLK period		
t_1	WE# low delay from CAS# high	GR18[0] = 0	3 T
		GR18[0] =1	2 T
t_2	Read CAS# to Write CAS# delay	GR18[1] = 0	4 T
		GR18[1] = 1	3 T
t_3	WE# low setup time to CAS# low		1 T

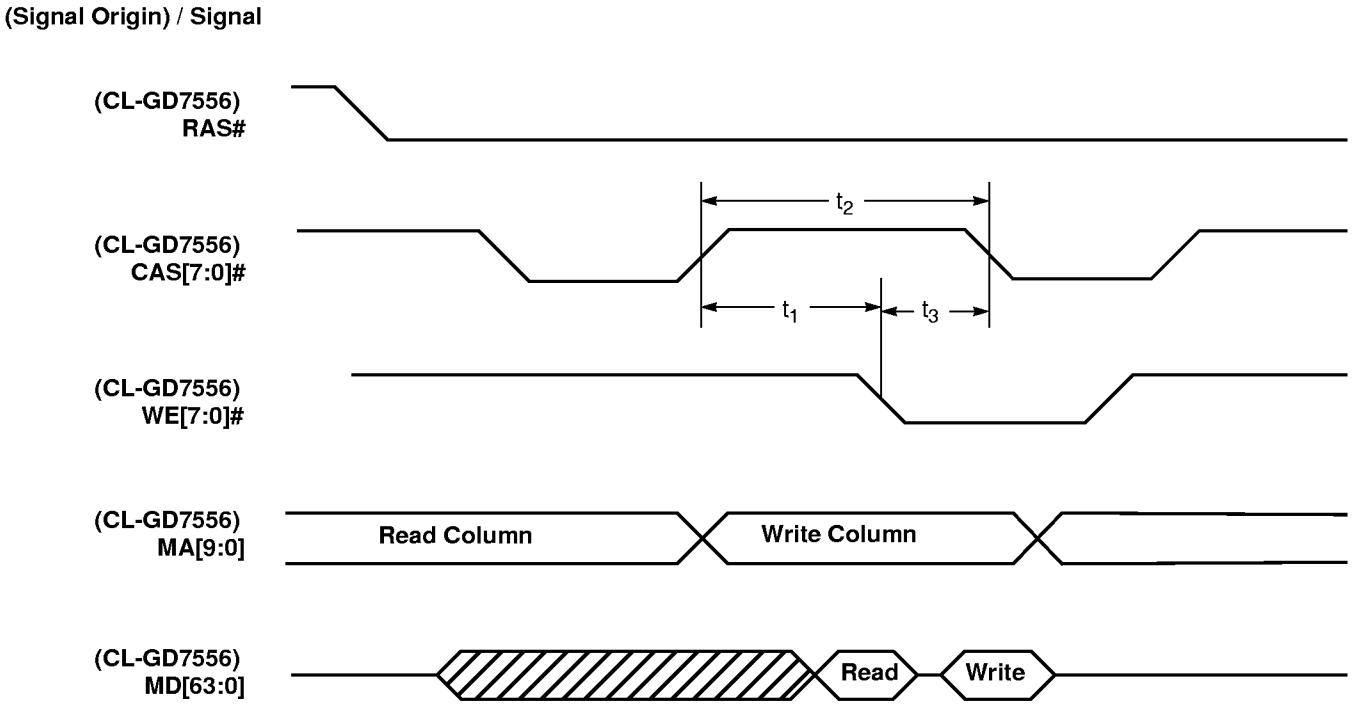


Figure 13-9. Display Memory Bus — Typical BitBLT Read/Write Cycle Timing

Table 13-11. Display Memory Bus — CAS#-before-RAS# Refresh Timing

Symbol	Parameter	MIN	MAX
T	MCLK period		
t_1	RAS# Precharge (RAS# Pulse Width High)	3 T – 1 ns	–
t_2	RAS# Pulse Width Low	5 T	–
t_3	RAS# to CAS# Precharge Time	1 T – 2 ns	–
t_4	CAS# Precharge Time	1 T – 2 ns	–
t_5	CAS# Setup Time	1 T – 2 ns	–
t_6	CAS# Hold Time	1 T – 2 ns	–

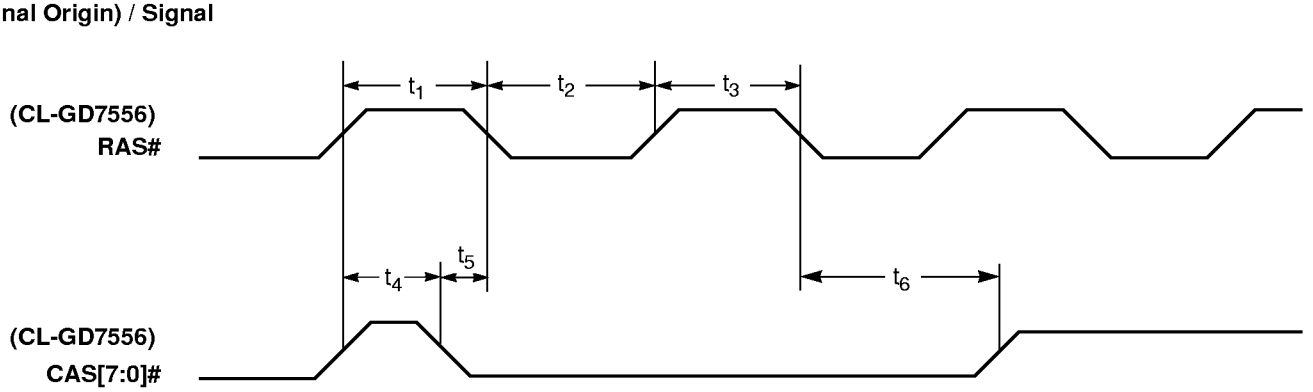


Figure 13-10. Display Memory Bus — CAS#-before-RAS# Refresh Timing

13.8 Timing Diagrams — CL-GD7556 to Flat Panel

The timing diagrams in this section apply to the interface from the CL-GD7556 to flat panels.

Typical Flat Panels Supported by the CL-GD7556

Flat Panel Code	Flat Panel Type	Flat Panel Maximum Resolution	Number of Colors Supported	Data Interface	Timing Diagram Reference
C8DD-16	Dual-Scan STN	800 × 600	8	16-bit	Figure 13-11
C8DD-8	Dual-Scan STN	800 × 600	8	8-bit	Figure 13-11
C512SS-9	1-Pixel/Clock TFT	1024 × 768	512	9-bit	Figure 13-12
C4KSS-12	1-Pixel/Clock TFT	1024 × 768	4K	12-bit	Figure 13-12
C256KSS-18	1-Pixel/Clock TFT	1024 × 768	256K	18-bit	Figure 13-12
C16MSS-24	1-Pixel/Clock TFT	1024 × 768	64K	24-bit	Figure 13-12
C4KSS-24	2-Pixel/Clock TFT	1024 × 768	4K	24-bit	Figure 13-12
C256KSS-36	2-Pixel/Clock TFT	1024 × 768	256K	36-bit	Figure 13-12

Table 13-12. Flat Panels — High-Resolution Color Dual-scan STN Timing

Symbol	Parameter	C8DD-16		C8DD-8	
		MIN	MAX	MIN	MAX
T_D	Dot Clock Period for DSTN Panel				
t_1	FPVDCLK period	$2.5T_D - 6$ ns		$T_D - 6$ ns	
t_2	FPVDCLK high time	$T_D - 6$ ns		$0.5T_D - 6$ ns	
t_3	FPVDCLK low time	$T_D - 6$ ns		$0.5T_D - 6$ ns	
t_4	FPVDCLK rise and fall time		6 ns		6 ns
t_5	Pixel Data setup time	$T_D - 6$ ns		$0.5T_D - 6$ ns	
t_6	Pixel Data hold time	$T_D - 6$ ns		$0.5T_D - 6$ ns	
t_7	FPVDCLK low to LLCLK low	$T_D - 6$ ns		$2T_D - 10$ ns	
t_8	FPVDCLK low from LLCLK low	$T_D - 6$ ns		$2T_D - 10$ ns	
t_9	LLCLK high time	$4T_D - 6$ ns		$4T_D - 6$ ns	
t_{10}	LFS high setup to LLCLK low (typical)	$2T_D$ (TYP)		$2T_D$ (TYP)	
t_{11}	LFS high hold time from LLCLK low (typical)	$2T_D$ (TYP)		$2T_D$ (TYP)	

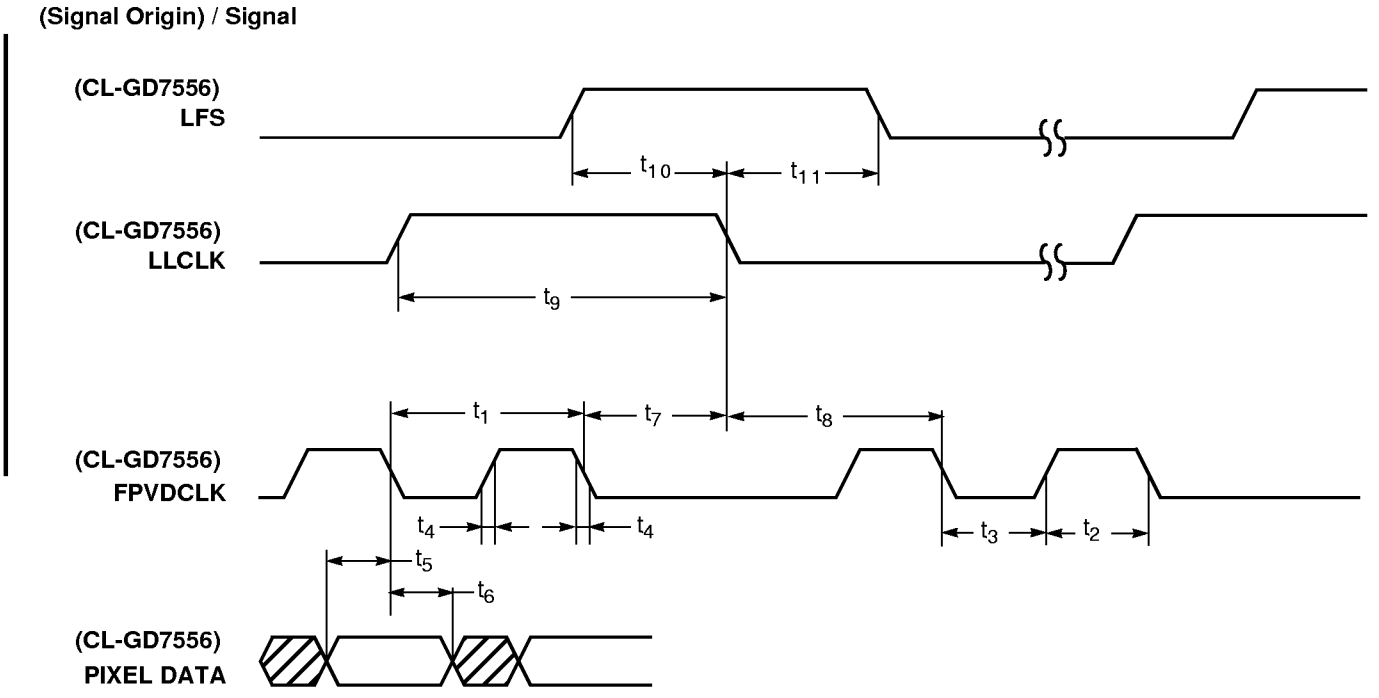


Figure 13-11. Timing Diagram for High-Resolution Color Dual-Scan STN Panels

Table 13-13. Flat Panels — High-Resolution Color TFT Timing

Symbol	Parameter	TFT C512SS / C4KSS / C256KSS / C16MSS		TFT 2-Pixel/Clock C4KSS / C256KSS	
		MIN	MAX	MIN	MAX
T_D	Dot Clock Period for TFT Panel				
t_1	FPVDCLK period	T_D – 6 ns		$2T_D$ – 6 ns	
t_2	FPVDCLK high pulse width	$0.5T_D$ – 6 ns		T_D – 6 ns	
t_3	FPVDCLK low pulse width	$0.5T_D$ – 6 ns		T_D – 6 ns	
t_4	FPVDCLK rise and fall time		6 ns		6 ns
t_5	Pixel Data setup time	$0.5T_D$ – 6 ns		T_D – 6 ns	
t_6	Pixel Data hold time	$0.5T_D$ – 6 ns		T_D – 6 ns	
t_7	FPDE setup to FPVDCLK	$0.5T_D$ – 6 ns		T_D – 6 ns	
t_8	FPDE hold to FPVDCLK	$0.5T_D$ – 6 ns		T_D – 6 ns	
t_9	LLCLK pulse width	$4T_D$ – 6 ns		$4T_D$ – 6 ns	
t_{10}	Horizontal front porch	0 ns	FPDE low period	0 ns	FPDE low period
t_{11}	Horizontal back porch	0 ns	256T	0 ns	256T
t_{12}	LFS pulse width	1 scanline	16 scanlines	1 scanline	16 scanlines
t_{13}	Vertical back porch	1 scanline		1 scanline	

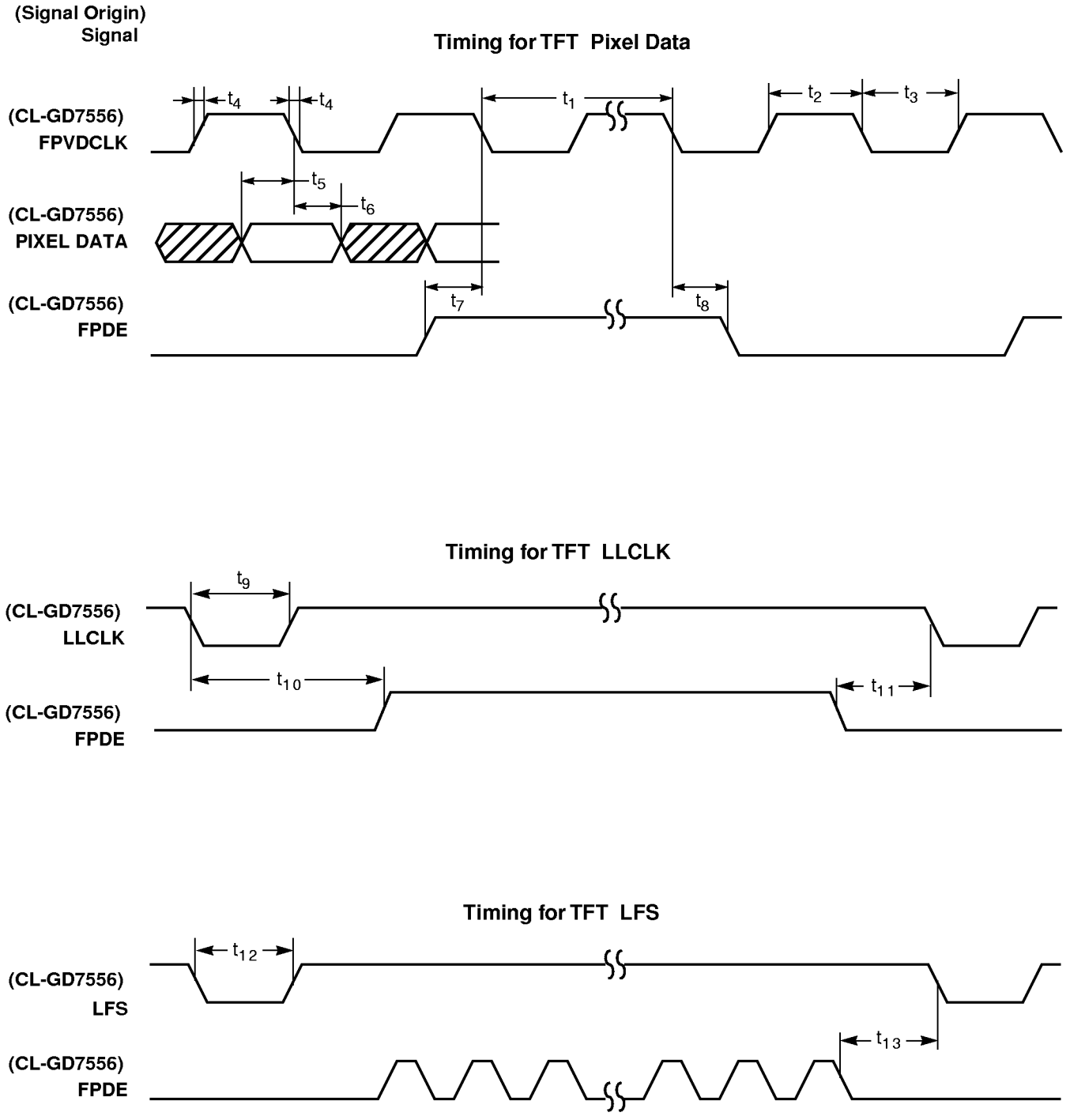


Figure 13-12. Timing Diagrams for High-Resolution Color TFT Flat Panels

Table 13-14. V-Port Timing

Symbol	Parameter	MIN	MAX	Units
t1	HREFI setup time for odd field	50		ns
t2	HREFI hold time for odd field	50		ns
t3	HREFI setup time for even field	50		ns
t4	HREFI hold time for even field	50		ns
t5	VPCLKI rise time	5	8	ns
t6	VPCLKI fall time	5	8	ns
t7	VPCLKI high pulse width	20		ns
t8	VPCLKI low pulse width	20		ns
t9	Data, VACTI setup time to VSI and VPCLKI	30		ns
t10	Data, VACTI hold time to VSI and VPCLKI	10		ns

NOTE: At 20 MHz, the maximum time for the VPCLKI period is 50 ns.

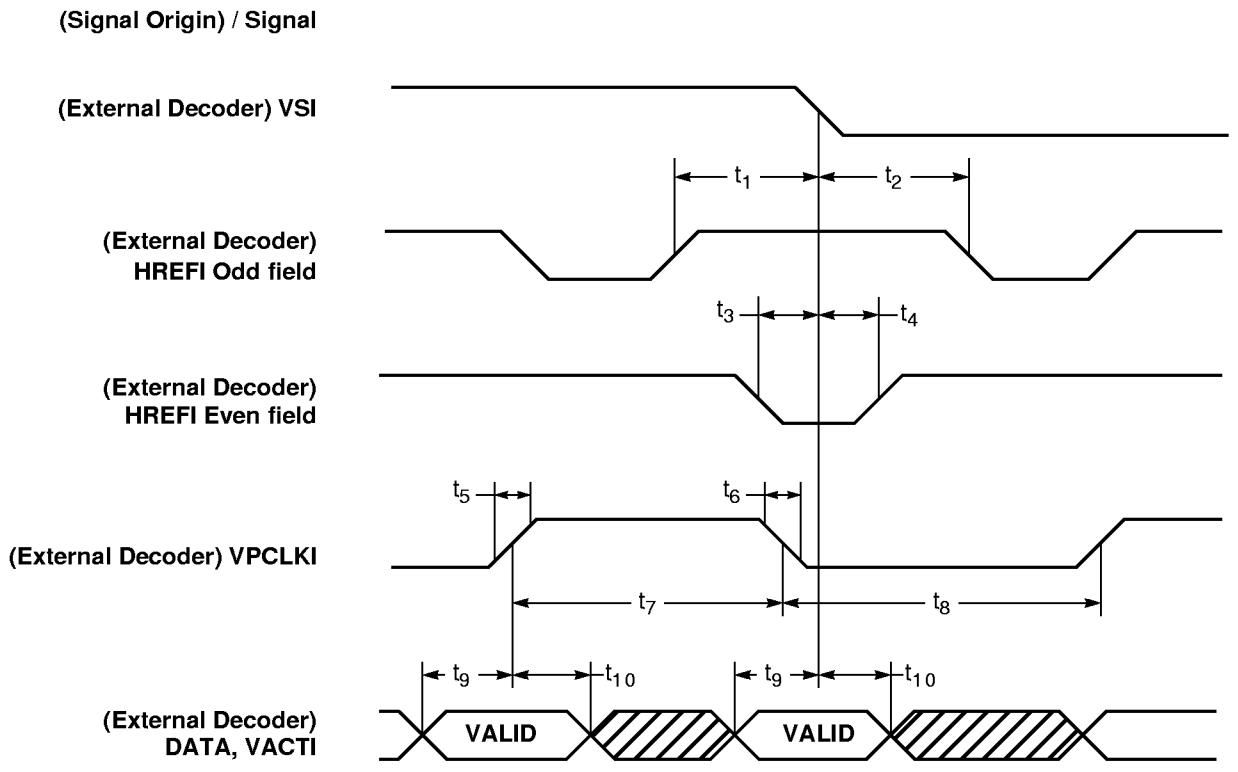


Figure 13-13. V-Port Timing Diagram

13.9 Timing Diagrams — Frequency Synthesizer Inputs

The timing diagram in this section applies to the inputs to the frequency synthesizer. The nominal frequency of the frequency synthesizer is 14.318 MHz, and the nominal period is 69.84 ns.

Table 13-15. Frequency Synthesizer (14.318 MHz) Input Timing

Symbol	Parameter	3.3 V	
		MIN	MAX
t_1	Input clock rise time	1 ns	7 ns
t_2	Input clock fall time	1 ns	7 ns
t_3	Input clock low period	$[T_{OS} / 2] - 10\% T_{OS}$	$[T_{OS} / 2] + 10\% T_{OS}$
t_4	Input clock high period	$[T_{OS} / 2] - 10\% T_{OS}$	$[T_{OS} / 2] + 10\% T_{OS}$
T_{OS}	Input clock period	69.84 ns – [0.1% of 69.84 ns] = 69.77 ns	69.84 ns +[0.1% of 69.84 ns] = 69.91 ns
V_{IH}	Input high voltage	$0.7V_{DD}$	V_{DD}
V_{IL}	Input low voltage	GND	$0.3V_{DD}$

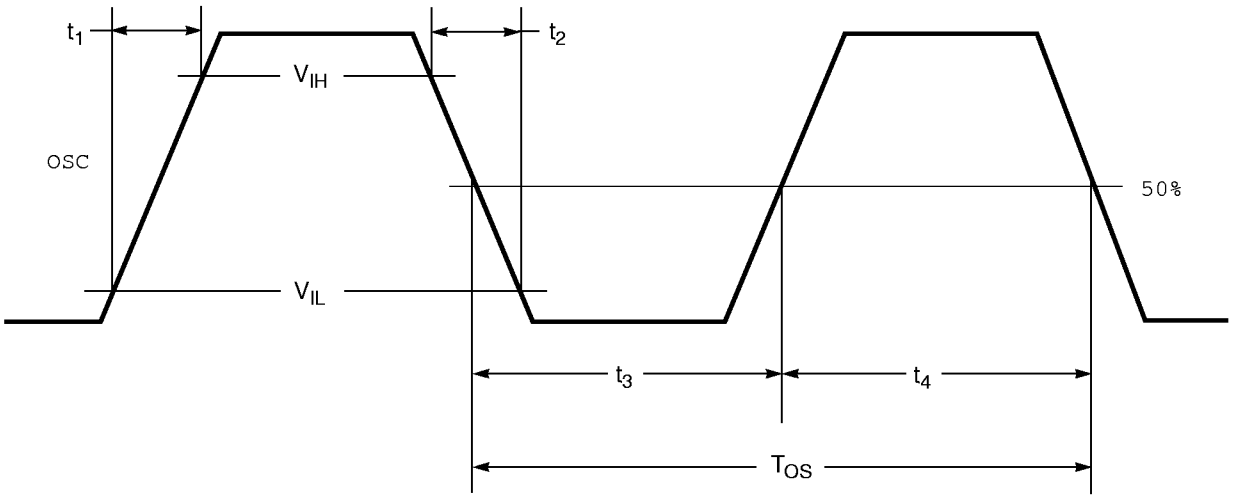
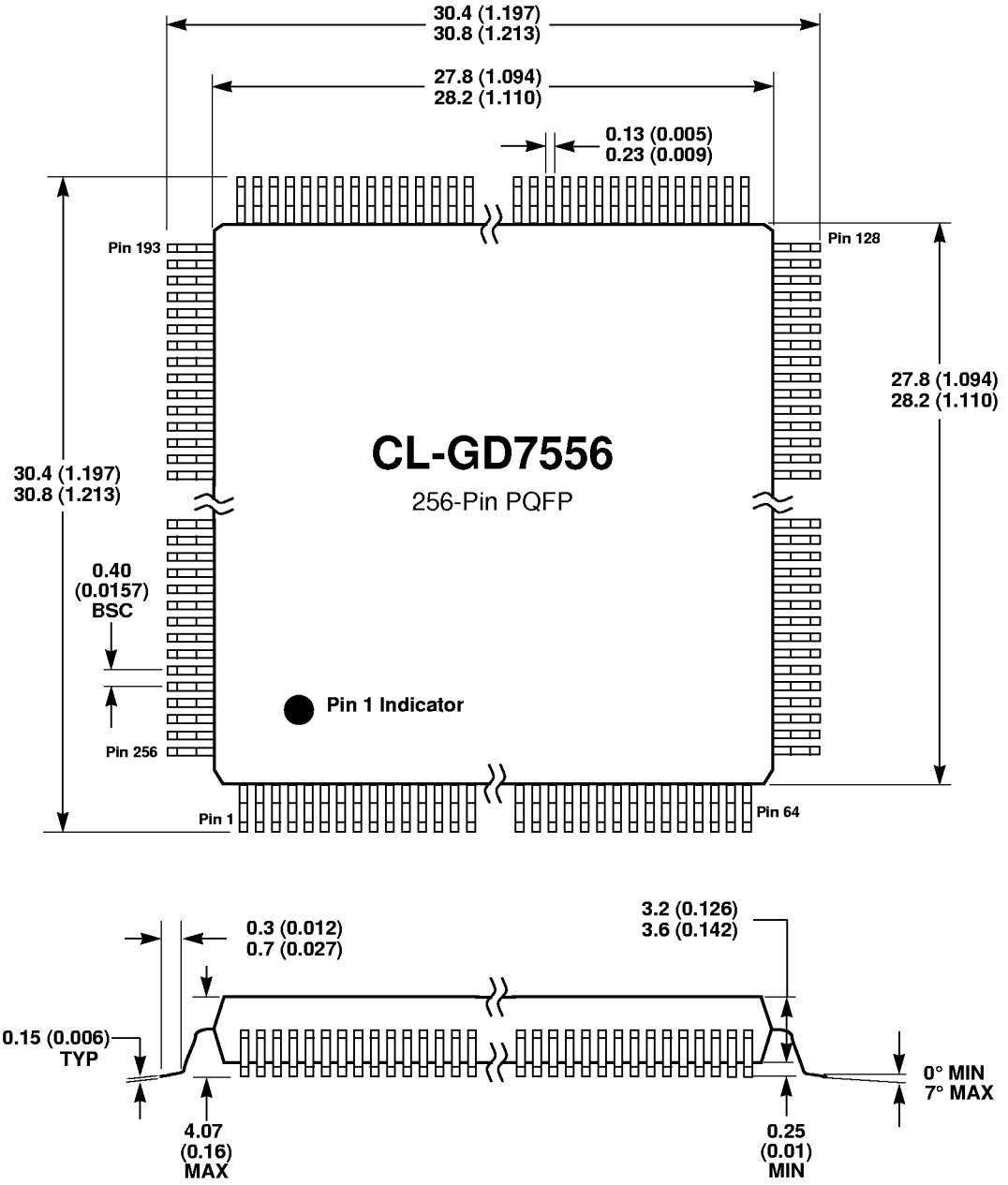


Figure 13-14. Frequency Synthesizer — Input Timing Diagram

14. PACKAGE SPECIFICATIONS

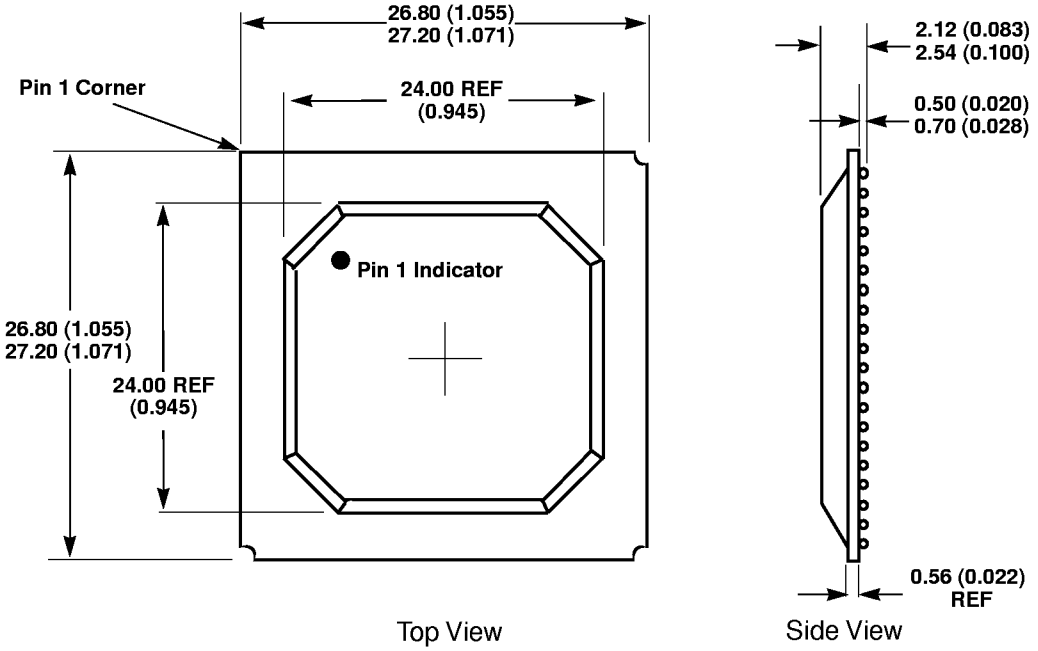
14.1 256-Pin PQFP Package Outline Drawing



NOTES:

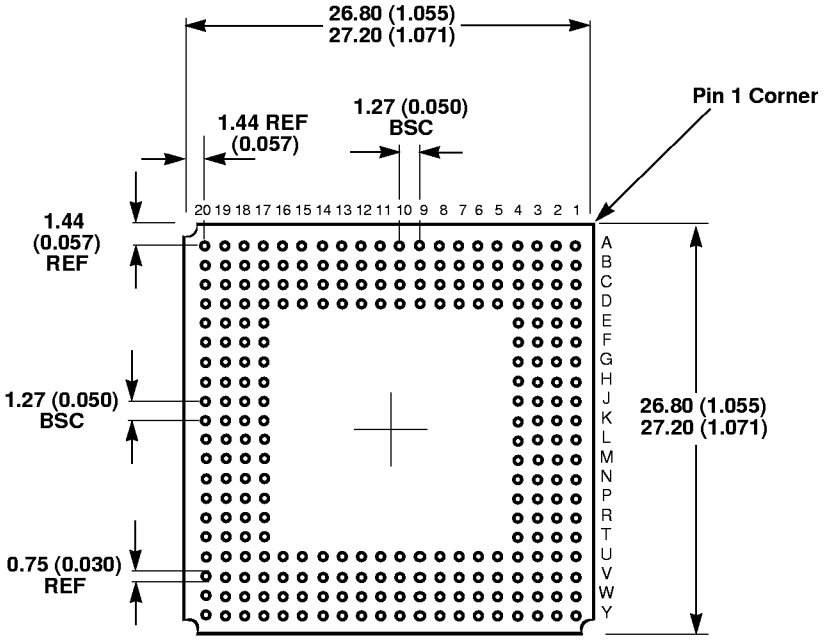
1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

14.2 256-Pin PBGA (Plastic Ball Grid Array) Package Outline Drawing



Top View

Side View



Bottom View

NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.

2) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.