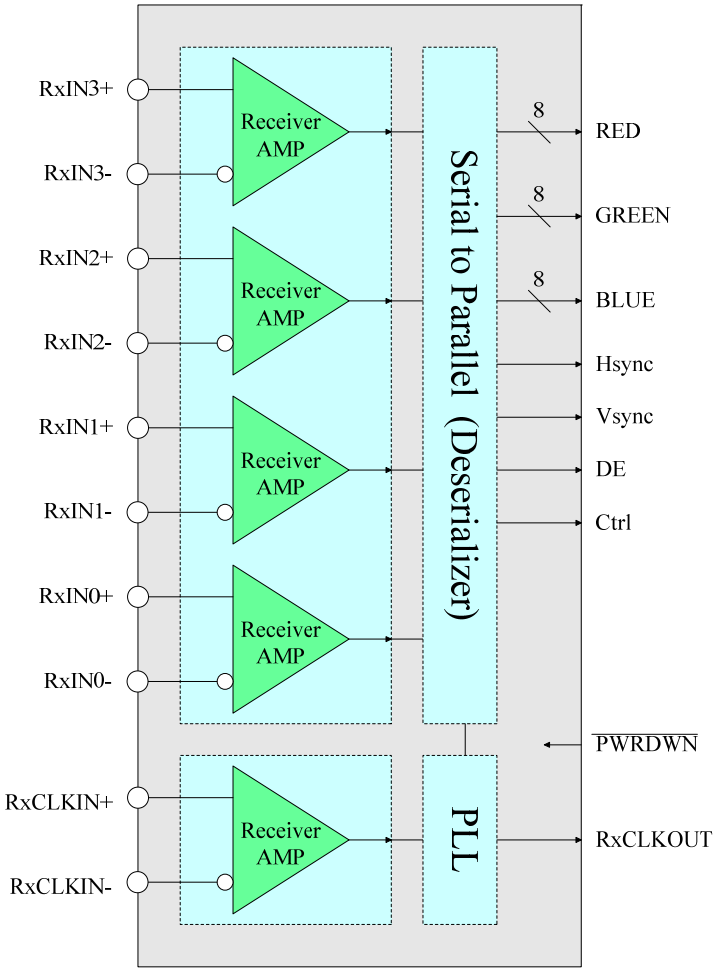
Introduction

The CL12464FF receiver converts serial four LVDS data streams data back into parallel 28bits (24bits of RGB data and 4bits of HSYNC, VSYNC, DE and Control1) of LVCMOS parallel. The CL12464FF receiver' outputs are Falling edge clock. The CL12464FF receiver is an ideal means to solve EMI and cable size problems associated with wide, high-speed LVCMOS interfaces.

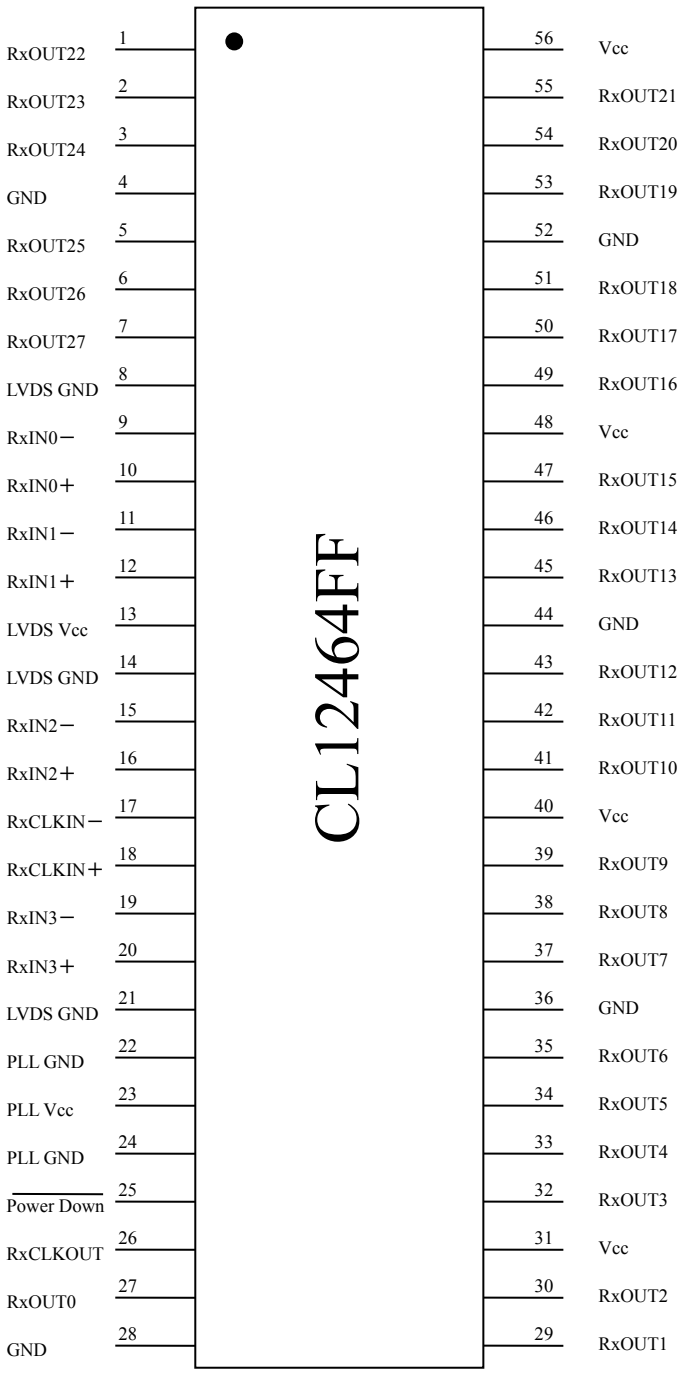
Feature

- Input Clock: 20MHz~85MHz Input Data Rate: 140Mbps~595Mbps
- Output Clock: 20MHz to 85MHz shift clock support
- Low power single 3.3V
- A falling edge strobe
- Supports VGA, SVGA, XGA, SXGA, SXGA+
- Narrow bus reduces cable size
- PLL requires no external components
- Power down mode
- Low Profile 56 Lead TSSOP Package
- 345mV swing LVDS devices for low EMI
- Supports Fail-Safe function to all input channels
- Pin Compatible with DS90C384/386, THC63LVDM84B

Block Diagram



Pin Configuration



Pin Description

Pin Name	No of Pin	I/O	Pin Description
RxOUT	28	OUT	LVCMOS Data Outputs
RxIN+	4	IN	Positive LVDS Differential Data Inputs
RxIN-	4	IN	Negative LVDS Differential Data Inputs
RxCLKOUT	1	OUT	LVCMOS Level Clock Output
RxCLKIN+	1	IN	Positive LVDS Differential Clock Input
RxCLKIN-	1	IN	Negative LVDS Differential Clock Input
$\overline{\text{Power Down}}$	1	IN	H:Normal Operation L:Power Down (all Outputs are Hi-Z)
Vcc / GND	3/5	IN	Power Supply/Ground Pins for LVCMOS Outputs
PLL Vcc / PLL GND	1/2	IN	Power Supply/Ground Pins for PLL
LVDS Vcc / LVDS GND	2/4	IN	Power Supply/Ground Pins for LVDS Inputs

Control Signal Truth Table

$\overline{\text{Power Down}}$	$\overline{\text{R\_F}}$	OE	RxOUT	RxCLKOUT
0	0	0	All Outputs Hi-Z	Output Hi-Z
0	0	1	All ”0” Outputs	”0” Output
0	1	0	All Outputs Hi-Z	Output Hi-Z
0	1	1	All ”0” Outputs	”0” Output
1	0	0	All Outputs Hi-Z	Output Hi-Z
1	0	1	All Data Outputs	Falling Edge
1	1	0	All Outputs Hi-Z	Output Hi-Z
1	1	1	All Data Outputs	Rising Edge

Absolute Maximum Ratings

Supply Voltages	-0.3V to +4V
LVCMOS Input Voltage	-0.3V to (Vcc+0.3V)
LVCMOS Output Voltage	-0.3V to (Vcc+0.3V)
LVDS Receiver Input Voltage	-0.3V to (Vcc+0.3V)
Junction Temperature	+150 ℃
Storage Temperature	-65 ℃ to +150 ℃
Lead Temperature (Soldering, 4sec)	+260 ℃
Maximum Power Dissipation Capacity at 25℃	1.4 W

Electrical Characteristics

1. LVCMOS DC Specification — Vcc=3.0V to 3.6V Ta=-10℃ to 70℃

Symbol	Parameter	Conditions	min	typ	max	unit
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	
I_{IN}	Input Current	$V_{IN}=V_{CC}$,GND,2.5V or 0.4V		±5.1	±10	μA
V_{OH}	High Level Output Voltage	I_{OH}=-0.4mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL}=12mA			0.8	

2. LVDS DC Specification — Vcc=3.0V to 3.6V Ta=-10℃ to 70℃

Symbol	Parameter	Conditions	min	typ	max	unit
V_{TH}	Differential Input High Threshold	V_{CM}=+1.2V			100	mV
V_{TL}	Differential Input Low Threshold		-100			
I_{IN}	Input Current	$0V \leqq V_{IN} \leqq V_{CC}$			±10	μA

3. Receiver Supply Current — Vcc=3.0V to 3.6V Ta=-10℃ to 70℃

Symbol	Parameter	Conditions		min	typ	max	unit
ICCRW	Receiver Supply Current	C_L=8pF Worst Case Pattern	f=65MHz		73	94	mA
			f=85MHz		83	96	
ICCRG		C_L=5pF 16Gray Scale Pattern	f=65MHz		40	54	
			f=85MHz		52	64	
ICCRZ		$\overline{\text{Power Down}}$=Low				10	μA

4. Switching Characteristics Vcc=3.0V to 3.6V Ta=-10℃ to 70℃

Symbol	Parameter	min	typ	max	unit
RCOP	RxCLK OUT Period	7.41	T	50	ns
RCOH	RxCLK OUT High Time		T/2		
RCOL	RxCLK OUT Low Time		T/2		
CLHT	LVCMOS Low to High Transition Time		1	3	
CHLT	LVCMOS High to Low Transition Time		1	3	
$RSP_{OS}0$	Receiver Input Strobe Position for Bit 0	-0.5	0	+0.5	ns
$RSP_{OS}1$	Receiver Input Strobe Position for Bit 1	T/7-0.5	T/7	T/7+0.5	
$RSP_{OS}2$	Receiver Input Strobe Position for Bit 2	2T/7-0.5	2T/7	2T/7+0.5	
$RSP_{OS}3$	Receiver Input Strobe Position for Bit 3	3T/7-0.5	3T/7	3T/7+0.5	
$RSP_{OS}4$	Receiver Input Strobe Position for Bit 4	4T/7-0.5	4T/7	4T/7+0.5	
$RSP_{OS}5$	Receiver Input Strobe Position for Bit 5	5T/7-0.5	5T/7	5T/7+0.5	
$RSP_{OS}6$	Receiver Input Strobe Position for Bit 6	6T/7-0.5	6T/7	6T/7+0.5	
RSRC	RxOUT Setup to RxCLK OUT		T/2-2.5		ns
RHRC	RxOUT Hold to RxCLK OUT		T/2-2.5		
RCCD	RxCLK IN to RxCLK OUT Delay		4T/7		
RPLLS	Receiver Phase Lock Loop Set			10	ms
RPDD	Receiver Power Down Delay			1	us

Fail-Safe Function

The CL12464FF receiver output ”high” when the differential inputs is :

1) Open
2) Undriven and Shorted
3) Undriven and Terminated

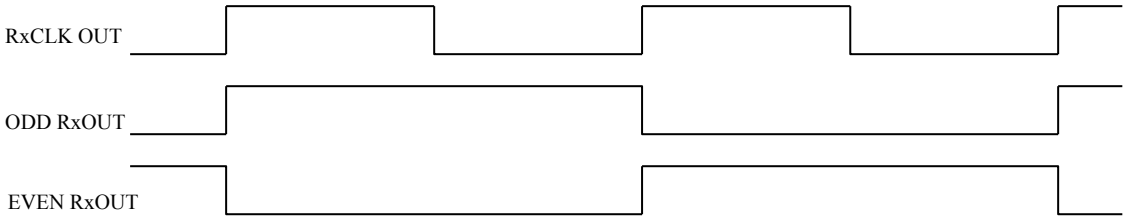


Fig.1 Worst Case Test Pattern

PIN Name	Signal	Signal Pattern	Signal Frequency
RxCLK OUT	DOT CLK		f
RxOUT0	R0		f/16
RxOUT1	R1		f/8
RxOUT2	R2		f/4
RxOUT3	R3		f/2
RxOUT4	R4		Steady State, Low
RxOUT6	R5		Steady State, Low
RxOUT27	R6		Steady State, Low
RxOUT6	R7		Steady State, Low
RxOUT7	G0		f/16
RxOUT8	G1		f/8
RxOUT9	G2		f/4
RxOUT12	G3		f/2
RxOUT13	G4		Steady State, Low
RxOUT14	G5		Steady State, Low
RxOUT10	G6		Steady State, Low
RxOUT11	G7		Steady State, Low
RxOUT15	B0		f/16
RxOUT18	B1		f/8
RxOUT19	B2		f/4
RxOUT20	B3		f/2
RxOUT21	B4		Steady State, Low
RxOUT22	B5		Steady State, Low
RxOUT16	B5		Steady State, Low
RxOUT17	B7		Steady State, Low
RxOUT23	CNTL		Steady State, Low
RxOUT24	HSYNC		Steady State, High
RxOUT25	VSYNC		Steady State, High
RxOUT26	DE		Steady State, High

Fig.2 16 Grayscale Test Pattern

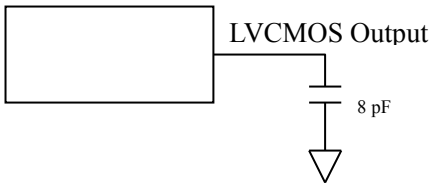


Fig.3: LVCMOS Output Load

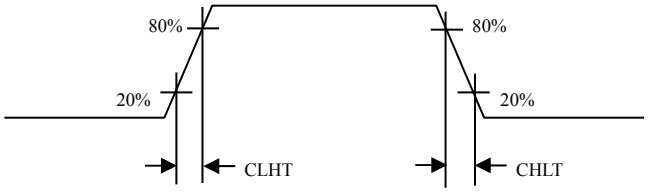


Fig.4: LVCMOS Output Transition Times

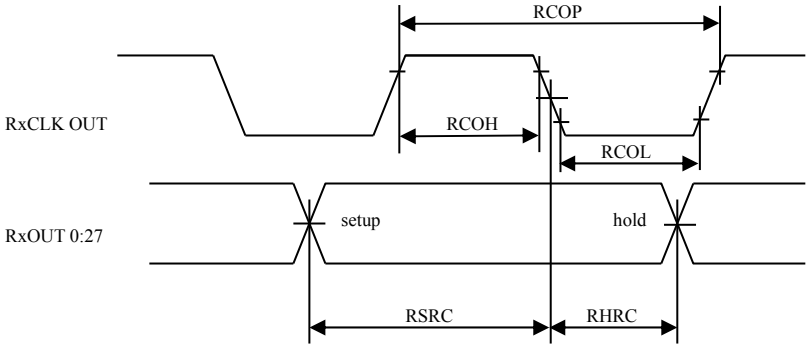


Fig.5: Receiver Setup/hold and Low/High Times

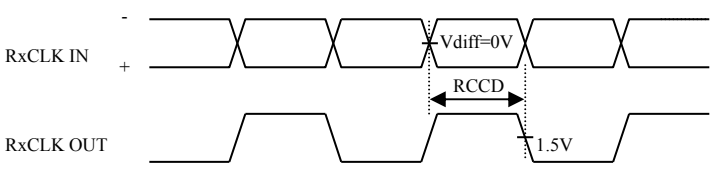


Fig.6: Receiver Clock in to Clock out Delay

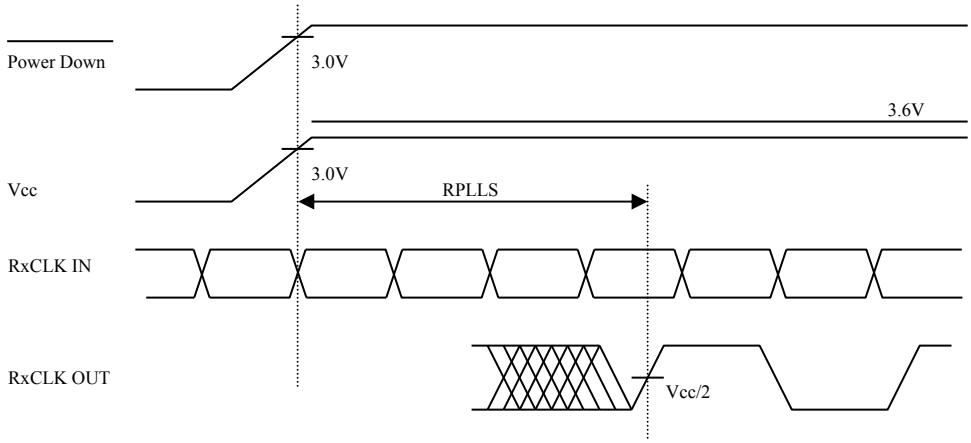


Fig.7: Receiver Phase Lock Loop Set Time

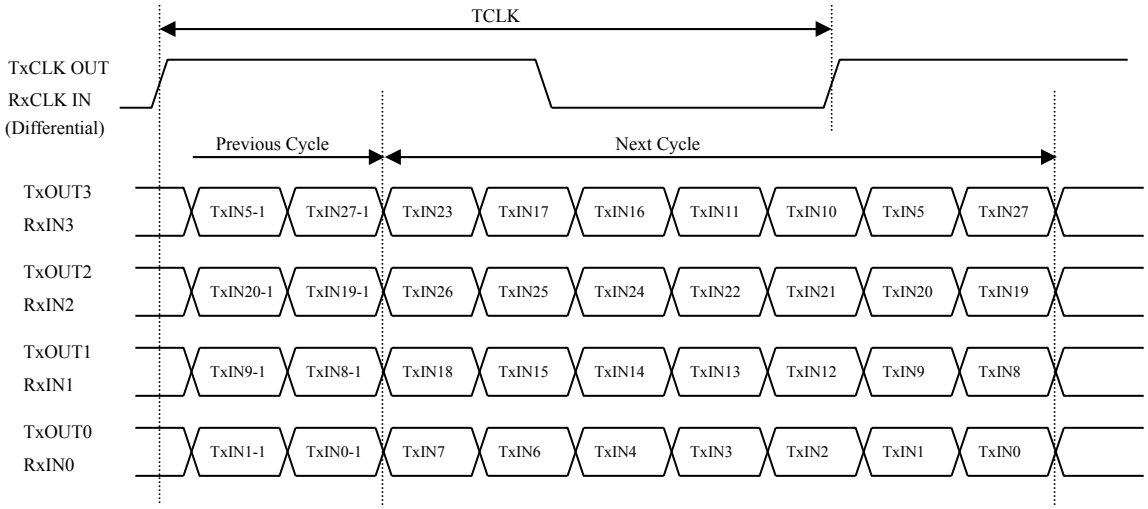


Fig.8: Parallel LVCMOS Data(TxIN) Inputs Mapped to LVDS(TxOUT) Outputs

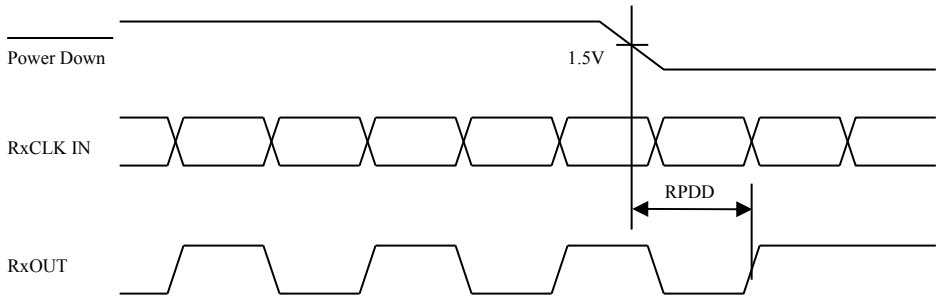


Fig.9: Receiver Power Down Delay

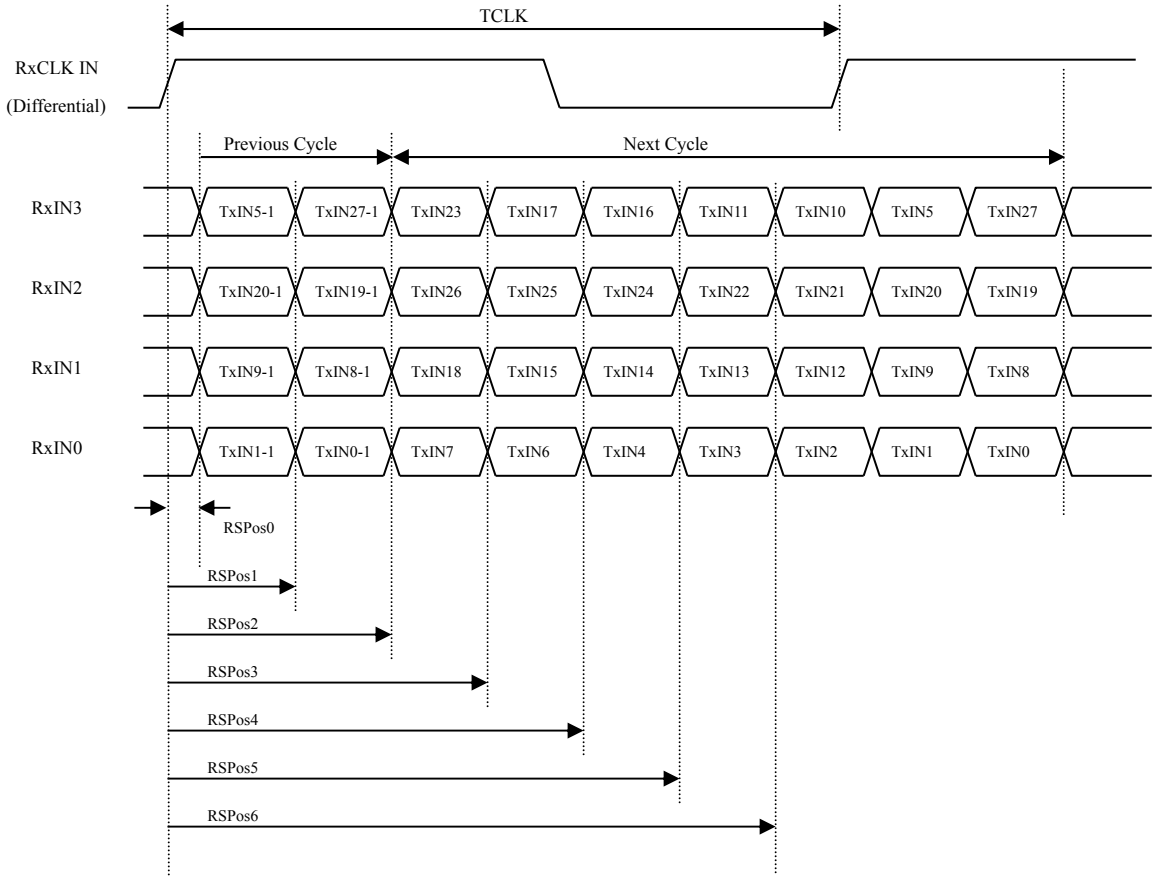
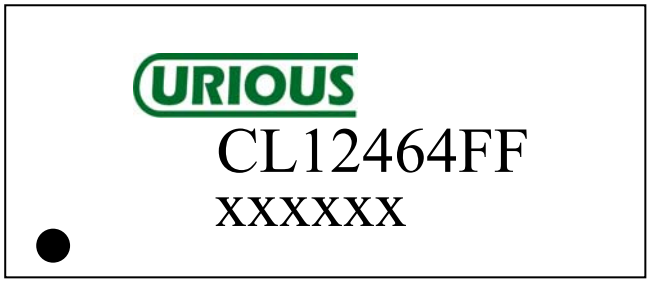


Fig.10: Receiver LVDS Input Strobe Position


CL12464FF
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Modification History

Version	Date	Contents
1.00	2010 / 1 / 12	1) Block Diagram changed
0.30	2007 / 7 / 18	1) Input Clock frequency & Data rate added
0.20	2006 / 5 / 23	1) From CL12464AF to CL12464FF changed 2) Fail-Safe Function added 3) Package LOGO changed 4) Supply Current value changed 5) Maximum Dot Clock Frequency cjanged 6) I_{OL} value changed for Changing Frequency 7) The output Rising/Falling Time value changed 8) RxCLK OUT Cycle Time Changed
0.10	2005 / 5 / 10	Fig.2 Modified turn of Pin Name and Signal
0.00	2003 / 5 / 15	First Version