Comlent Technology Inc.	Doc. Version	Date	
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CL5767 Datasheet

(For Strategic Customers)

COMLENT

Product Description

The CL5767 is a single-chip FM stereo radio for portable application with fully integrated digital low-IF selectivity and demodulation. The radio is completely adjustment-free and only requires a minimum of small and low-cost external components. The radio can tune to worldwide FM bands.

Application

MP3/MP4 players

Portable radios

PDAs

Notebook PCs

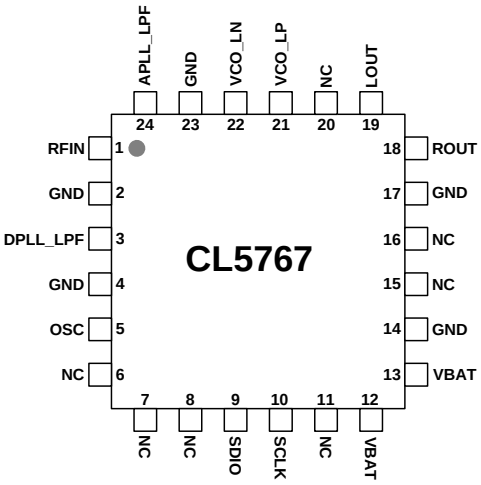
Technology

- RF CMOS Process
- 4X4 QFN24 Package

Features

- Worldwide FM Bands (70 MHz to 108 MHz)
- Digital Low-IF Receiver
- 32.768kHz/13MHz Reference Clock
- Frequency Synthesizer With Integrated VCO
- Automatic Frequency Control (AFC)
- Automatic Gain Control (AGC)
- DSP MPX Stereo Decoder
- DSP FM Demodulator
- Adaptive Noise Cancellation
- MONO/Stereo Blend
- High Cut
- Software Mute
- Programmable De-emphasis
- Bass Boost
- Integrated LDO Regulator
- Supply Voltage Ranges from 2.4 V to 5.0 V

Pin Assignment



CONTENTS

1 Electrical Specifications

1.1 Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Supply Voltage	V	- 0.5 to 5.8	V
Input Current	I_{IN}	+/-10	mA
Operating Temperature	TOP	- 40 to 85	°C
Storage Temperature	TSTG	- 55 to 150	°C
RF Input Level		0.8	V_{PP}

1.2 Specifications

Parameter	Condition	Min.	Typ.	Max.	Unit
Basic Parameters					
Power Supply	VBAT	2.4	3.0	5.0	V
Low Level Input Voltage	SCLK,SDIO			0.3*VBAT	V
High Level Input Voltage	SCLK,SDIO	0.7* VBAT			V
Low Level Output Voltage	SDIO			0.2*VBAT	V
High Level Output Voltage	SDIO	0.8* VBAT			V
Ambient Temperature		-20	25	85	°C
Power Consumption					
Work Current Consumption	Maximum Volume Output		24		mA
Idle Current Consumption	Only I2C Work，VBAT = 3V			45	uA
Receiver Characteristics					
Frequency Range (f_{FM})		70		108	MHz
LNA Input Impedance (R_{IN})	Z_{IN_LNA} = 0		50		Ω
	Z_{IN_LNA} = 1 (Default)		120		Ω
LNA Input Capacitance (C_{IN})			4		pF
Sensitivity	f_{TUNE}=76~108MHz f_{DEV}=22.5kHz; f_{MOD}=1kHz; SINAD=26dB;L=R; BAF=200Hz ~15kHz; MONO=ON		2.2		uV EMF
In-band Input IP3 ($IIP3_{INBAND}$)	Δf1=200kHz; Δf2=400kHz; f_{TUNE} =76~108MHz		66		dBuV EMF
Out-band Input IP3	Δf1=2MHz; Δf2=4MHz;		88		dBuV

($IIP3_{OUTBAND}$)	f_{TUNE} =76~108MHz				EMF
AM Suppression(AM_{SP})	V_{RF}=60dBuV FM： f_{DEV}=22.5kHz; f_{MOD}=1kHz; AM： m=0.3; f_{MOD}=1kHz; BAF=200Hz ~15kHz;MONO=ON		50		dB
Adjacent Channel Selectivity (ACS_{200})	Δf=±200kHz; f_{TUNE} =76~108MHz SINAD>26dB		40		dB
Alternate Channel Selectivity (ACS_{400})	Δf=±400kHz; f_{TUNE} =76~108MHz SINAD>26dB		45		dB
Spurious Response Rejection	Δf>±1MHz； f_{TUNE} =76~108MHz SINAD>26dB	60			dB
Audio Output Voltage	V_{RF}=60dBuV; f_{TUNE}=76~108MHz f_{DEV} =22.5kHz; f_{MOD} =1kHz; BAF=200Hz ~15kHz; MONO=ON; MAX. Volume		80		mV RMS
Audio Output L/R Imbalance	V_{RF}=60dBuV; f_{TUNE}=76~108MHz;f_{DEV} =22.5kHz; f_{MOD}=1kHz;BAF=200Hz ~15kHz;		0.1		dB
Audio Stereo Separation	V_{RF}=60dBuV; f_{TUNE} = 76~108MHz; f_{DEV} =100%; f_{MOD}=1kHz; L=1;R=0; Pilot 10% BAF=200Hz ~15kHz;	29	32	33	dB
Signal to Noise and Distortion Ratio(SINAD)	V_{RF}=60dBuV; f_{TUNE} = 76~108MHz; f_{DEV} =75kHz; f_{MOD} =1kHz; BAF=200Hz ~15kHz; MONO=ON	53	55	58	dB
Audio THD	V_{RF}=60dBuV; f_{TUNE} = 76~108MHz; f_{DEV} =75kHz; f_{MOD} =1kHz; BAF=200Hz ~15kHz; MONO=ON		0.07	0.1	%
De-emphasis Time Constant	DE=0		75		us
	DE=1		50		
Seek Time			50		ms/C
Power-up Time				1	s
External Reference Clock Mode（In Addition to 32.768kHz Crystal Mode）					
Reference Clock Frequency	Support Two Clock Frequency	32.768kHz or 13MHz			
Jitter	For Audio SNR > 40dB			1	ns

MIN. Voltage of Reference Clock	Support Both Square-wave and Sine-wave	-200		400	mV
MAX. Voltage of Reference Clock	Support Both Square-wave and Sine-wave	1200		1800	mV
32.768kHz Crystal Characteristics					
Series Oscillating Impedance				100	KΩ
Reference Frequency Tolerance		-50		50	ppm

1.3 Control Interface Timing

Control bus supports standard I2C protocol with a maximum frequency of 400 kHz.

Parameter	Symbol	Condition	Standard-Mode			Fast-Mode			Units
			MIN	TYP	MAX	MIN	TYP	MAX	
SCLK Period	Tclk			10.0			2.5		us
SCLK High Time	Thigh			4.0			1.0		us
SCLK Low Time	Tlow			4.7			1.4		us
SDIO Input, SEN to SCLK ↑ Setup	Ts			50			50		ns
SDIO Input, SEN to SCLK ↑ Hold	Th			5			1.2		us
Start Condition Hold	Tsh			4.7			1.4		us
Stop Condition Setup	Tsu			4.0			1.0		us
SCLK ↑ to SDIO Output Valid	Tcdv	Read		2			2		ns
SCLK ↑ to SDIO Output High Z	Tcdz	Read		2			2		ns

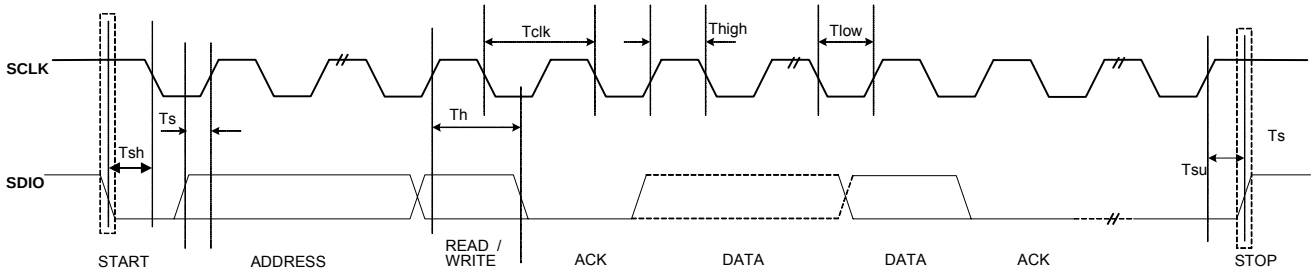


Figure 1. I^{2}C Control Interface Write Timing

2 Application Schematic

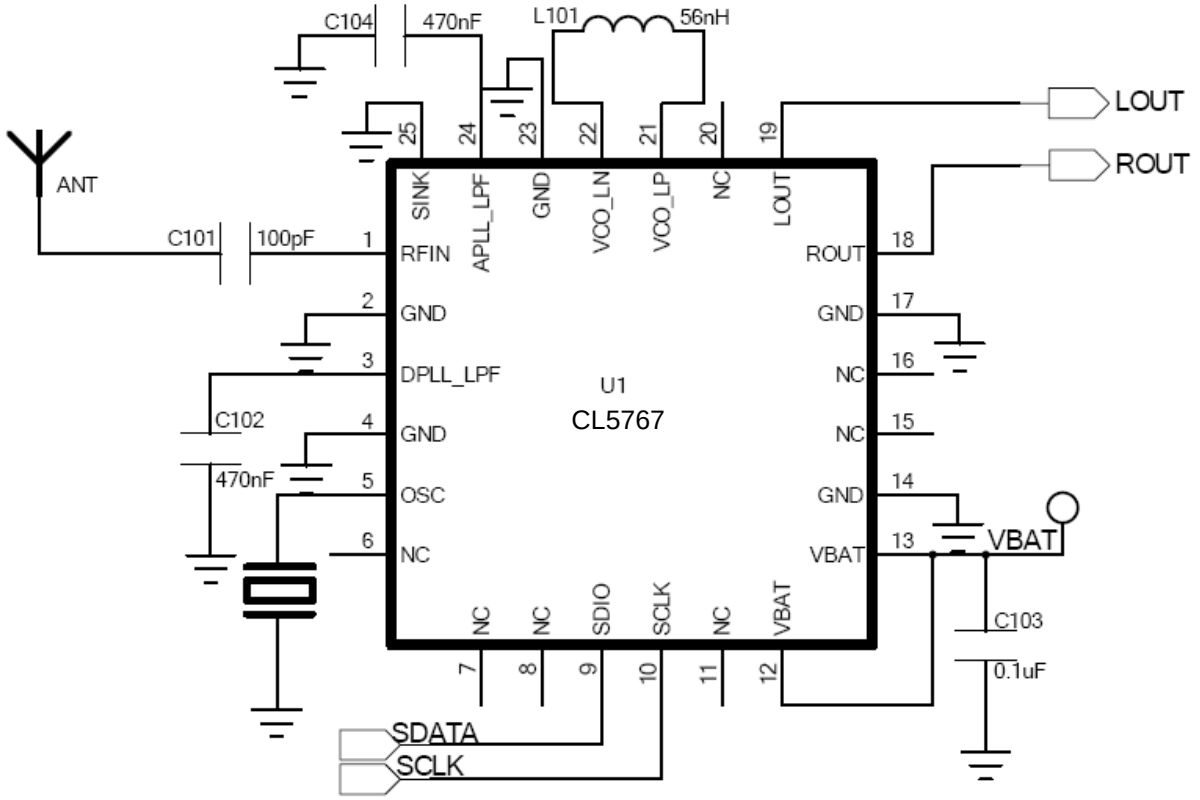


Figure 2. Application Schematic

3 BOM

Component Type	Value (Description)	Number
Capacitance	100pF (C101)	1
	470nF (C102,C104)	2
	0.1uF (C103)	1
Inductor	56nH (L101, Tolerance < 5%)	1
Crystal	32.768kHz (PPM < 50ppm)	1

4 Functional Description

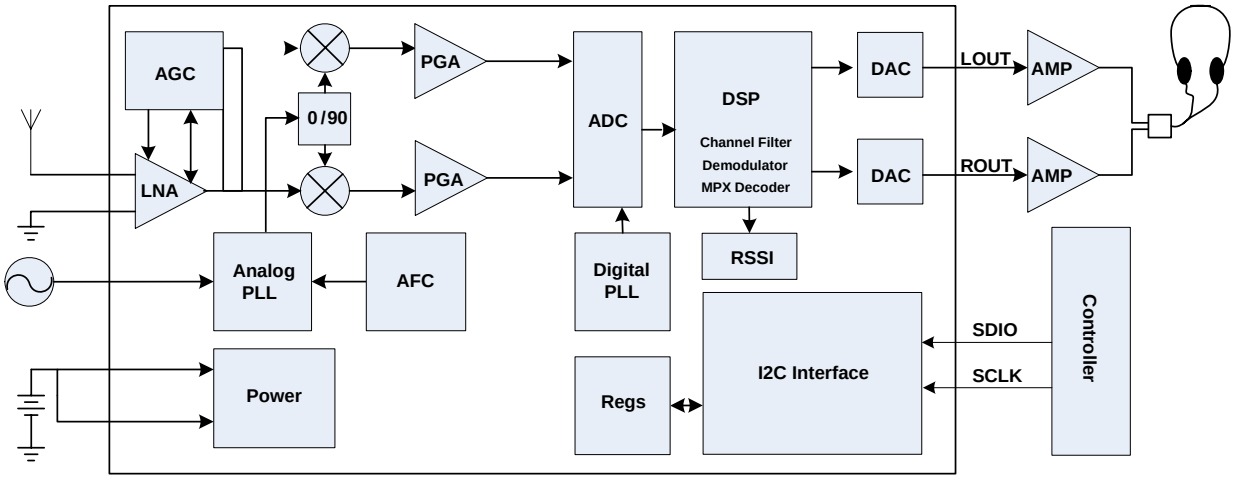


Figure 3. Block Diagram

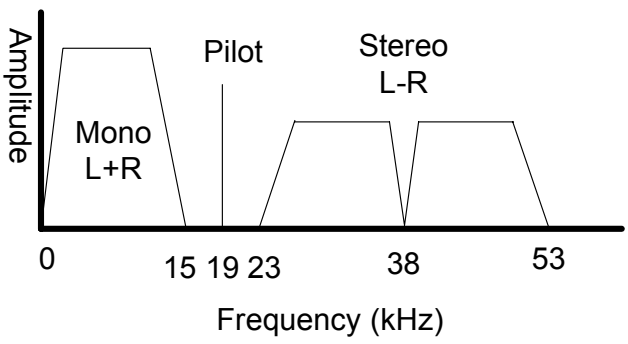
4.1 Overview

The CL5767 is a single-chip FM stereo radio for portable application with fully integrated digital low-IF selectivity and demodulation. The radio is completely adjustment-free and only requires a minimum of small, low-cost external components. The radio can tune to worldwide FM bands.

With digital low intermediate frequency (low-IF) architecture and frequency synthesizer technology, CL5767 delivers superior RF performance and can be utilized to provide optimum sound quality. The improved digital processing and power management assure the low power consumption with a supply voltage range from 2.4 V to 5.5 V. The highly integrated single-chip solution makes CL5767 easier to its applications in handset, MP3 and other portable products.

4.2 Stereo Decoder

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX standard was developed in 1961, and is used worldwide. Today's MPX signal format consists of Left + Right (L + R) audio, Left - Right (L - R) audio and a 19 kHz pilot tone as shown in figure.



The CL5767 integrated stereo decoder

automatically decodes the MPX signal using DSP techniques. The 0 to 15 kHz (L + R) signal is the mono output of the FM tuner. Stereo is generated from the (L + R), (L - R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L - R) signal. Output left and right channels are obtained by adding and subtracting the (L + R) and (L - R) signals respectively.

4.3 Audio Processing

Pre-emphasis and De-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. All FM receivers incorporate a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The de-emphasis compensation effect is shown in below figure.

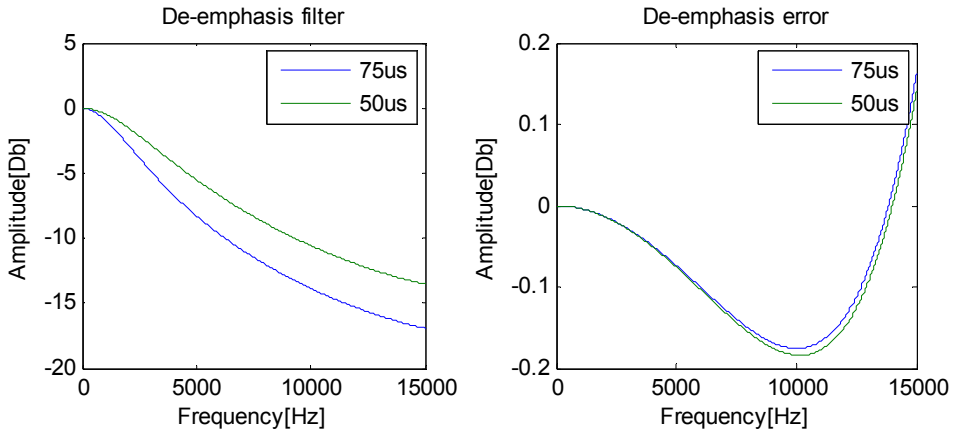


Figure 4. De-emphasis Filter

CL5767 has a bass boost filter to enhance low frequency.

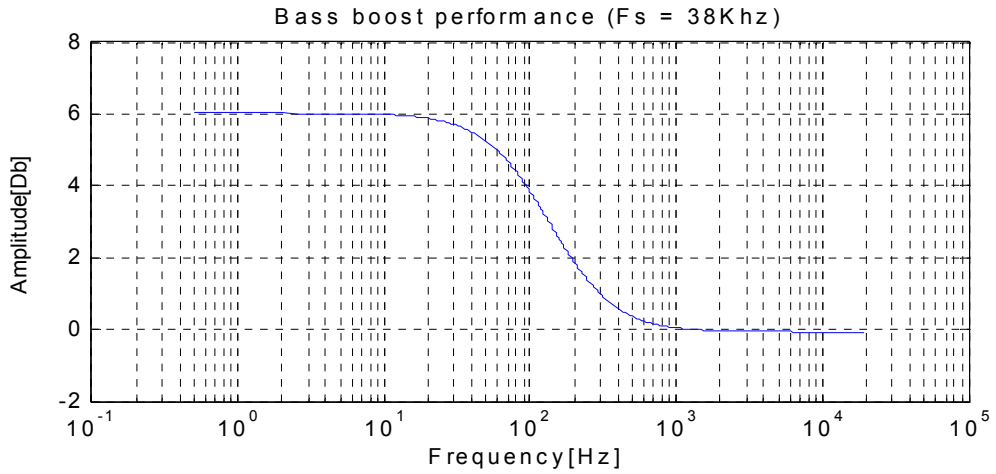


Figure 5. Bass Boost Filter

4.4 Tuning and Seeking under C-Mode

Tuning under C-Mode needs only to update bits CHAN[9:0], then trigger it by bit Tune rising edge (from 0 to 1). The whole process requires approximately 50mS. After tuning process is completed, three values are given in read-only registers: 8-bit RSSI for signal strength, 6-bit ENVELOP_NUM for signal-to-noise ratio and 8-bit FD_NUM for frequency deviation. These values are in format of two's complement. The suggested criteria of radio station are (RSSI≥176)&(ENVELOP_NUM≤38)&(Abs(FD_NUM)≤14).

Hardware seeking function is integrated within CL5767 with less than 10 second to find a radio station. The trigger condition is control bit SEEK rising edge, i.e. bit SEEK from 0 to 1. When seeking is completed, bit STC will be sent to as 1, and the chip is tuned to new radio station frequency, if there is no station, it returns to starting frequency. STC value can be tracked to read the register through I2C. Control bit SF is the indicator of radio station, if SF=0, the current stop is a radio station, if SF=1, STC=1, it means there is no station across FM radio frequency band. Radio station frequency can be acquired from control bit READCHAN[9:0] and the tuning frequency is defined as

Frequency (MHz) = 50 kHz * READCHAN[9:0] + 70MHz

READCHAN[9:0] is 0 for 70MHz.

Seeking can be triggered again with bit SEEK rising edge to find the next radio station after it is completed.

4.5 Tuning and Seeking under P-Mode

Tuning under P-Mode is triggered by changing control bit PLL[13:0]. If the chip read the same PLL[13:0] number, it will keep current working status and there is no PLL locking process, if the chip read in a different PLL[13:0] number, PLL relocks and the chip is tuned to new frequency. When tuning is completed, it provides two control bits: 7-bit IF and 4-bit Lev. The suggested criteria of radio station are(48≤IF≤62)&(Lev≥5).

Seeking function under P-Mode is triggered by control bit SM rising edge, i.e. SM from 0 to 1. When seeking is completed, it sends out two control bits: RF and BLF. RF = 1 means that seeking is completed, if BLF =0, there is a radio station, if BLF=1, there is no radio station across FM band. Radio station frequency can be acquired from control bit PLL[13:0] in read-only registers.

4.6 Reference Clock

The CL5767 can be used with 32.768 kHz crystal, the required frequency stability is less than +/-50ppm in the working temperature range. Also it accepts a 32.768 kHz or 13MHz reference clock, the required jitter is less than 1ns.

4.7 Control Interface

Two-wire slave-transceiver (I2C interface) is provided for the controller IC to read and write the control registers. Registers may be written and read when the VIO supply is applied regardless of the state of the VBAT supplies.
For two-wire operation, a transfer begins with the START condition. The control word is latched internally on rising SCLK edges. The device acknowledges the address by setting SDIO low on the next falling SCLK edge.

For write operations, the device acknowledge is followed by an eight bit data word latched internally on rising edges of SCLK. The device always acknowledges the data by setting SDIO low on the next falling SCLK edge.

For read operations, the device acknowledge is followed by an eight bit data word shifted out on falling SCLK edges. The controller IC returns an acknowledge if additional data will be transferred. The transfer ends with the STOP conditions regardless of the state of the acknowledge.

4.8 RESET, Power-up and Power-down

First of all, power supply to the CL5767, with 100ns (minimum) delay, digital part circuit reset automatically.

Then, IC can be powered on with set bit “Disable”, analog part circuit will be powered on with this bit control.

With action bit “Disable” was toggled to “0”, 5ms latter, DSP power on reset will be active and clock will be output 0.8s latter than POR.

4.9 Power Sequence

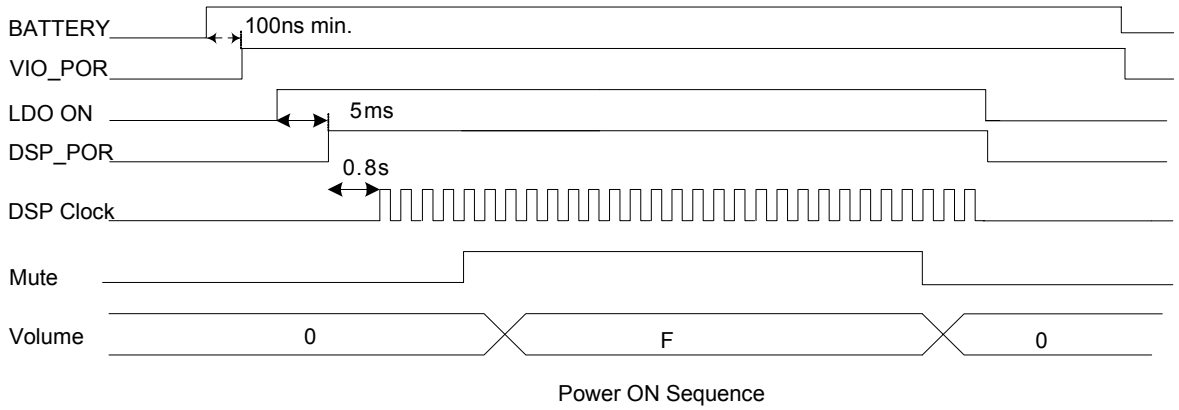


Figure 6. Power Sequence

Power-up Sequence:

1. Power supply the IC with battery;
2. POR of I2C startup at least 100ns later after power on;
3. Toggle the bit “Disable=0” come to work mode and enable the LDO for both digital and analog;
4. Last action will trigger the DSP part power on rest action, and this action will be done in 5ms;
5. Refer to “Disable=0”, crystal oscillator will start to oscillate and DSP clock should be ready in 800ms;
6. Set the MUTE and volume bit by I^2C to enable audio output.

Power-down Sequence:

1. Set the MUTE bit low to disable the audio output
2. Set the bit “Disable” to 1 to power down the device
3. Remove power supply

5 Registers Definition

5.1 Register Overall Description

The IC address is 0010 000b for C-Mode, 1100 000b for P-Mode. This means that the first byte to be transmitted to the CL6017 should be “0x20”(C-Mode) / “0xC0”(P-Mode) for a WRITE operation or “0x21”(C-Mode) / “0xC1”(P-Mode) for READ operation.

Register map

Reg.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	StatusRSSI	Mode	Reserved			HLSi _Flag	STC	SF	ST	RSSI							
01h	ReadChan	Envelop_Number						ReadCHAN									
02h	QOS	DeviceID								FD_Number							
03h	Function	Disable	DSP	Mute	LMute	RMute	SMute	Tune	Seek	Seek _up	MONO	Stereo	HCC _EN	BB _EN	---	HLSi_ CTRL	HLSi
04h	Channel Volume	Reserved		Volume				CHAN									
05h	SysConfig	Band		Space		DEEN	DE	AFC _EN	AFC _Pol	CHK	RSSI _EN	Reserved					
06h	APLLN	---	Xtal _Sel	Xtal _EN	ON _LNA	ZIN _LNA	RSSITU				NK _Sel	APLLN					
07h	APLLK	APLLK															
08h	Seek_TH	Seek_TH								PGA_RD_TH		Envelop_TH			FD_TH		
09h	Reserved																
0Ah	Reserved																
0Bh	Reserved																
0Ch	Reserved																
0Dh	Reserved																
0Eh	Reserved																

5.2 Register Word Description

Register	Default	Type	Function
00h	0x0800	R	StatusRSSI
01h	0x02F8	R	ReadChan
02h	0xA600	R	QOS, DeviceID
03h	0xE481	R/W	Function
04h	0x3EF8	R/W	Channel, Volume
05h	0x1F40	R/W	SysConfig
06h	0x385A	R/W	APLLN
07h	0xE8AC	R/W	APLLK
08h	0xB0F1	R/W	Seek Threshold
09h	0x8BAA	R/W	Reserved
0Ah	0xC604	R/W	Reserved
0Bh	0x6D25	R/W	Reserved
0Ch	0xFFFC	R/W	Reserved
0Dh	0x120F	R/W	Reserved
0Eh	0x451D	R/W	Reserved

5.3 Register Word Description

Bit	Word	Bit	Type	Default	Function Description
StatusRSSI					
Mode_SEN	00h	15	R	0	I2C Mode Indicator 0---C-Mode 1---P-Mode
HLSi_FLAG	00h	11	R	1	HLSi status indicator in auto mode 0---Low side injection

					1---High side injection
STC	00h	10	R	0	Seek/Tune Complete 0---Not complete 1---Complete STC flag is set when seek or tune operation completes. Set the SEEK or TUNE bit low (both of TUNE and SEEK are low) will clear STC.
SF	00h	9	R	0	Seek Fail 0---Seek successful 1---Seek failure The seek fail flag is set when the seek operation fails to find a channel with RSSI[7:0]>= {SEEKTH[7:0]} (before map). Setting the SEEK bit low will clear SF.
ST	00h	8	R	0	Stereo Indicator 0---Mono 1---Stereo
RSSI	00h	7:0	R	0x00	Received Signal Strength Indicator (RSSI) RSSI scale is logarithmic, 1db/step
ReadChan					
Envelop_NUM	01h	15:10	R	0	Envelop detection
ReadCHAN	01h	9:0	R	760 108MHz	Current Channel No Channel Frequency=50kHz*ReadCHAN + 70MHz ReadCHAN is updated according to CHAN in the beginning of tune operation, or updated during seek operation.
QOS					

DeviceID	02h	15:8	R	0xA7	
FD_NUM	02h	7:0	R	0x00	Frequency deviation
Function					
Disable	03h	15	R/W	1	Power Down control 0---Work mode 1---Power down mode (Only I2C supply is on for digital control access.)
Reset_DSP	03h	14	R/W	1	DSP reset software control 0---Reset DSP 1---Normal operation
Mute	03h	13	R/W	1	Mute 1---Mute L/R channel 0---Normal operation
LMute	03h	12	R/W	0	Left Mute 1---Mute 0---Normal operation
RMute	03h	11	R/W	0	Right Mute 1---Mute 0---Normal operation
SMute	03h	10	R/W	1	Soft Mute Disable 0---Mute (if RSSI<RSSI_MUTE then mute L/R) 1---Normal operation(do not mute)
Tune	03h	9	R/W	0	Tune Enable 0---Disable 1---Enable The tune operation begins when the TUNE bit is set high. The STC bit is set high when the tune operation completes. Set TUNE=0 (1->0) (by i2c), will clear STC registers.
Seek	03h	8	R/W	0	Seek Enable 0---Disable 1---Enable

SeekUp	03h	7	R/W	1	Seek process 0---Seek down 1---Seek up
MONO	03h	6	R/W	0	Mono Selection 0---Auto mode 1---Force in mono mode
Stereo	03h	5	R/W	0	Force in stereo mode 0---No force (means Stereo Noise Canceling On) 1---If detect pilot, then force to stereo (means Stereo Noise Canceling Off)
HCC_EN	03h	4	R/W	0	High Cut Enable 0---Bypass high cut filter 1---Enable high cut filter The hccen signal to other digital part is decided by HCCEN, RSSIEN, RSSI(before map), RSSI_HCC registers. If HCCEN=1, hccen=1; If HCCEN=0 and RSSIEN=0, hccen=0; If HCCEN=0 and RSSIEN=1, If RSSI<={ RSSI_HCC,00 00}, hccen=1; else hccen=0.
BB_EN	03h	3	R/W	0	Bass Boost Enable 0---Disable 1---Enable
HLSi_CTRL	03h	1	R/W	0	High-Low side injection control 0---Manually control 1---Automatically control
HLSi	03h	0	R/W	1	High/Low side injection in manual mode 0---Low side injection 1---High side injection
Channel Volume					
Volume	04h	13:10	R/W	1111	Volume 0000---Min. volume

					1111---Max. volume
CHAN	04h	9:0	R/W	760 108MHz	Channel Selection Frequency = 50kHz*CHAN + 70MHz CHAN is updated every tune
SysConfig					
Band	05h	15:14	R/W	00	Band Select 00---87.5MHz~108MHz (US/Europe, China) 10---76MHz~90MHz(Japan) 11---70MHz~108MHz
Space	05h	13:12	R/W	01	Channel Spacing 00---200kHz 01---100kHz (Europe, Japan) 10---50kHz (USA)
DEEN	05h	11	R/W	1	De-emphasis enable. 0---Disable 1---Enable
DE	05h	10	R/W	1	De-emphases 0---75 μs (USA) 1---50 μs (China)
AFC_EN	05h	9	R/W	1	AFC mode selection 0---No AFC 1---in Tune module
AFC_Polarity	05h	8	R/W	1	AFC Polarity Selection in tuning module 0---Low LO, + AFCIN; high LO, -AFCIN 1---Low LO, - AFCIN; high LO, +AFCIN
QOS_CHK	05h	7	R/W	0	Quality of Signal check method
RSSI_EN	05h	6	R/W	1	Enable RSSI result update RSSITU. 0---RSSI disable, tuning module use RSSITU written by bus as rssi value. 1---RSSI enable, tuning module use RSSI generated in FM demodulator as rssi value. It is also related to DMUTE and

					HCCEN. See DMUTE and HCCEN register definition.
APLLN					
Xtal_Sel	06h	14	R/W	0	Crystal selection 0---32.768kHz 1---13MHz
Xtal_EN	06h	13	R/W	1	Interal crystal oscillator enable signal 0---Disable oscillator circuit and enable differential pair as buffer but will not use it as buffer 1---Enable oscillator circuit, it can support XTAL, but also use it as 13.768kHz and 13MHz buffer
ON_LNA	06h	12	R/W	1	LNA ON/bypass control when AGC PD 0---Low gain (bypass LNA) 1---High gain (LNA active)
ZIN_LNA	06h	11	R/W	1	LNA input impedance 0---50ohm input impedance 1---120ohm input impedance
RSSITU	06h	10:7	R/W	0000	RSSI value written by I2C for Tuning module. RSSITU is written by bus. If RSSIEN=0, tuning module use RSSITU as rssi value. If RSSIEN=1, tuning module use the rssi generated in FM demodulator, and RSSITU is ignored.
APLL_NK_SEL	06h	6	R/W	1	APLL N/K mode selection 0---N/K value used in APLL is APLLN and APLLK (registers) set by I2C 1---N/K value used in APLL is generated in tuning module
APLLN	06h	5:0	R/W	26	N to APLL when APLL_NK_SEL=0
APLLK					

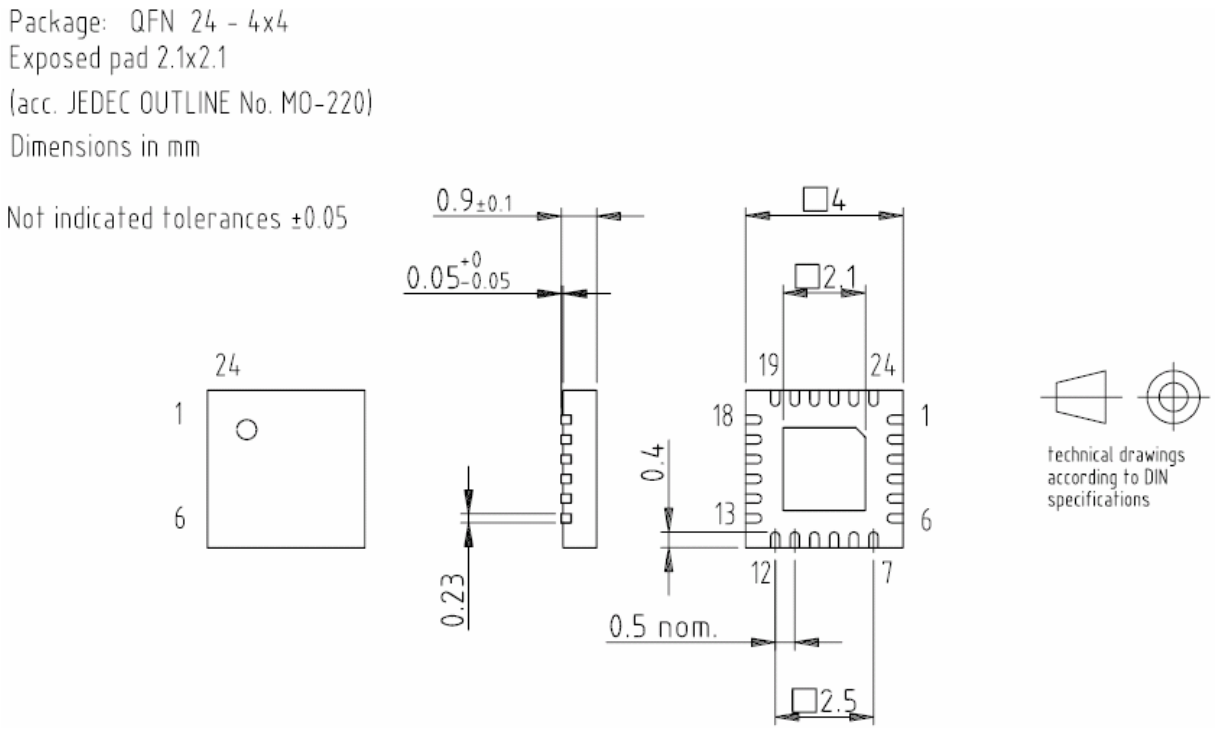
APLLK	07h	15:0	R/W	59564	K to APLL when APLL_NK_SEL=0
Seek_TH					
SeekTH	08h	15:8	R/W	176	Seek Threshold 11001001---201 11111111---Max. RSSI RSSI scale is logarithmic.
PGA_RD_TH	08h	7:6	R/W	11	PGA range detector switching threshold 00---35000 01---30000 10---25000 11---20000
Envelop_TH	08h	5:3	R/W	110	Envelop detection threshold 000---224 (14) 001---288 (18) 010---352 (22) 011---416 (26) 100---480 (30) 101---544 (34) 110---608 (38) 111---672 (42)
FD_TH	08h	2:0	R/W	001	Frequency deviation detection threshold 000---12 001---14 010---16 011---18 100---20 101---22 110---24 111---26

6 PIN Descriptions

PIN	Name	Description
1	RFIN	RF Single-end input
2	GND	Ground
3	DPLL_LPF	Digital PLL LPF
4	GND	Ground
5	OSC	Crystal Single-end Input
6	NC	Not Connect
7	NC	Not Connect
8	NC	Not Connect
9	SDIO	I2C Data
10	SCLK	I2C Clock
11	NC	Not Connect
12	VBAT	Batter Power Supply
13	VBAT	Batter Power Supply
14	GND	Ground
15	NC	Not Connect
16	NC	Not Connect
17	GND	Ground
18	ROUT	Right Audio Output
19	LOUT	Left Audio Output
20	NC	Not Connect
21	VCO_LP	Noinverting port for external inductor for Analog VCO
22	VCO_LN	Inverting port for external inductor for Analog VCO
23	GND	Ground
24	APLL_LPF	Analog PLL LPF

7 Package Outline

QFN24 pin. 4 X4 X 0.9mm



8 Convection Solder Reflow Requirements

Reflow Condition	SnPb Process	Pb-Free Process
Average ramp-up rate (TL to Peak)	3 C/second max.	3 C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	 100 C 150 C 60-120 seconds	 150 C 200 C 60-180 seconds
Tsmax to TL - Ramp-up Rate	3 C/second max.	3 C/second max.

Time maintained above: - Temperature (TL) - Time (tL)	 183 C 60-150 seconds	 217 C 60-150 seconds
Peak Temperature (Tp)	240 +0/-5oC	260 +5/-0oC
Time within 5 C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6 C/second max.	6 C/second max.
Time 25 C to Peak Temperature	180-360 seconds.	300-480 seconds

The peak temperatures shown in the tables are the target temperatures. A range of 10 C is allowed if needed due to convection oven/board loading limitations. For the SnPb process the allowable temperatures range is +5/-5 C and for the Pb-free process the allowable range is +10/-0 C.