Linear, 100mA, Constant Current LED Driver with Enable Input

Features

- 100mA ±5% constant current drive
- Built-in reverse polarity protection
- Logic level enable
- Dimmable via $\overline{EN}$ pin
- Overtemperature protection
- 90V max rating for transient immunity

Applications

- Flashlights
- Specialty lighting
- Low voltage signage
- Low voltage lighting

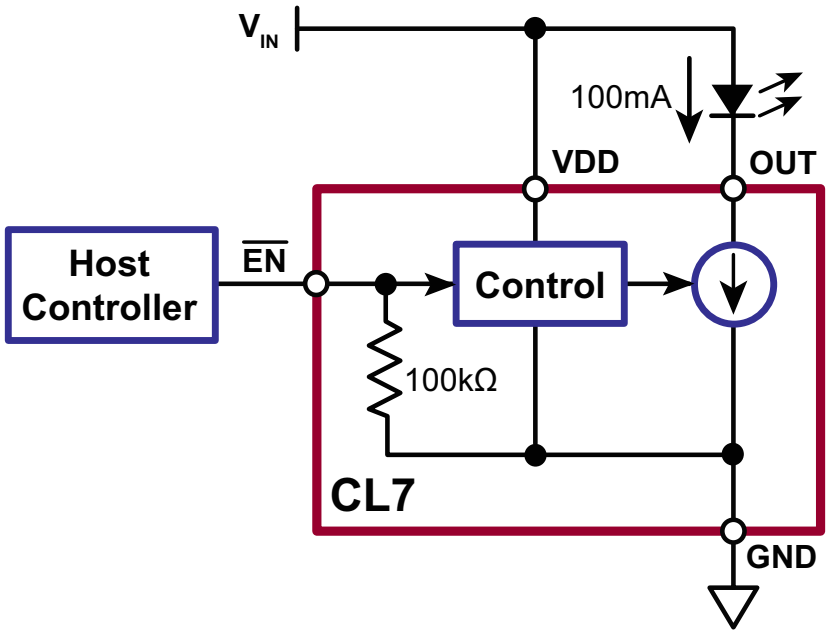
General Description

The CL7 is a linear fixed current regulator designed for driving high brightness LEDs at 100mA from nominal 12V, 24V, and 48V power supplies. With a maximum rating of 90V, it is able to withstand transients without the need for additional transient protection circuitry. The CL7 is offered in the 8-Lead SOIC package.

An active low enable input ($\overline{EN}$) allows logic level control of the LED for on/off control or PWM dimming. The enable input has 100kΩ pull-down resistance. For applications not needing an enable input, refer to the CL6 data sheet.

Over temperature protection shuts off the LED current when the die temperature rises above 135°C (nominal). Full LED current resumes when the die temperature falls below 105°C (nominal).

Typical Application Circuit



Ordering Information

Part Number	Package Options	Packing
CL7SG-G	8-Lead SOIC (w/heat slug)	2500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

Parameter	Value
Supply voltage, V_{DD}	-25V to +100V
Output voltage, V_{OUT}	-25V to +100V
Enable voltage, V_{EN}	-0.5V to +6.5V
Operating junction temperature	-40°C*
Storage temperature	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Note:

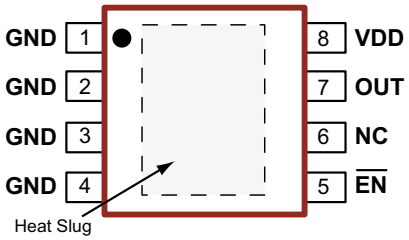
** Maximum junction temperature internally limited.*

Typical Thermal Resistance

Package	θ_{ja}
8-Lead SOIC (w/heat slug)	84°C/W*

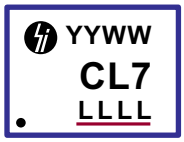
** Mounted on JEDEC test PCB (2s 2p)*

Pin Configuration



8-Lead SOIC w/heat slug
(top view)
(Heat slug potential is at ground)

Product Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC w/heat sug

Pin Designation

Pin	Name	Description
VDD	VDD	Supply voltage for the CL7
OUT	Output	Connect the LED between this pin and the supply voltage
GND	Ground	Circuit common
$\overline{EN}$	Enable	Active low enable input - this input has an internal 100kΩ pull-down resistance

Recommended Operating Conditions *(all voltages with respect to GND pin)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
V_{DD}	Supply voltage	Normal Extended	6.5 6.5	-	28 90	V	---
V_{OUT}	Voltage at OUT pin(1)	Normal Extended	4.0 4.0	-	28 90	V	---
T_J	Junction temperature(2)		-40	-	119	°C	---

Note:

1. *Continuous operation at high V_{OUT} voltages may result in activation of over temperature protection. Use appropriate heat sinking.*
2. *Maximum junction temperature internally limited.*

Thermal Characteristics *(Guaranteed by design – not production tested)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
T_{LIM}	Over-temperature limit	120	135	150	°C	---
T_{HYS}	Over-temperature hysteresis	-	30	-	°C	---

Electrical Characteristics

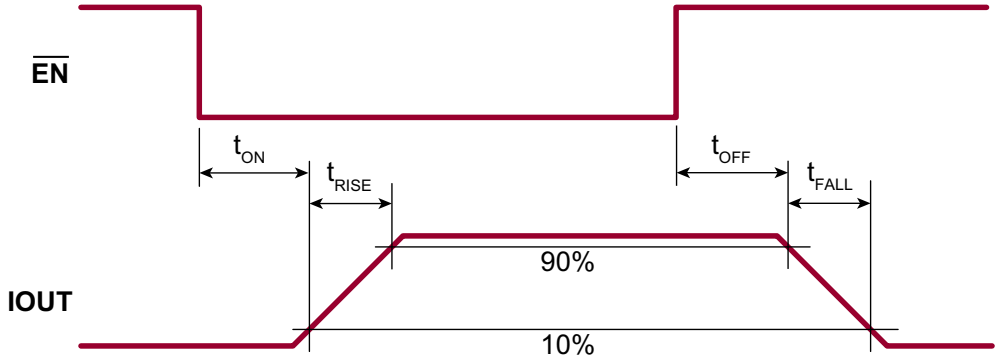
(Over normal recommended operating conditions unless otherwise specified. All voltages with respect to GND pin. Production tested @ 25°C.)

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{DD}	Current into VDD pin	3.0	5.0	10	mA	---
I_{OUT}	Current into OUT pin[1]	95 90 50	100 100 -	105 110 120	mA	Normal conditions, 25°C Normal conditions, full temp[2] Extended conditions
$I_{OUT(OFF)}$	Current into OUT pin with VDD pin open or $\overline{EN}$ = 1	-	-	10	µA	V_{DD} = open
$V_{EN(ON)}$	Enable voltage, on	-	-	0.8	V	---
$V_{EN(OFF)}$	Enable voltage, off	2.4	-	-	V	---
R_{EN}	Enable pull-down resistance	-	100	-	kΩ	---
V_{OFF}	Voltage at VDD to shut off LED current	-	-	1.0	V	I_{OUT} < 10µA
t_{ON}	On delay, $\overline{EN}$ to OUT	-	3.0	-	µs	$\overline{EN}$ = 0V
t_{OFF}	Off delay, $\overline{EN}$ to OUT	-	0.1	-	µs	$\overline{EN}$ = 5V
t_{RISE}	Current rise time, $\overline{EN}$ to OUT	-	4.0	-	µs	$\overline{EN}$ = 0V
t_{FALL}	Current fall time, $\overline{EN}$ to OUT	-	0.3	-	µs	$\overline{EN}$ = 5V

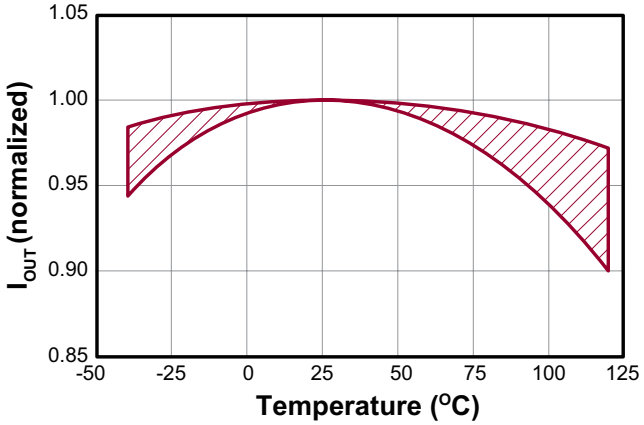
Note:

1. *Continuous operation at high V_{OUT} voltages may result in activation of over temperature protection. Use appropriate heat sinking.*
2. *Maximum junction temperature internally limited.*

Timing

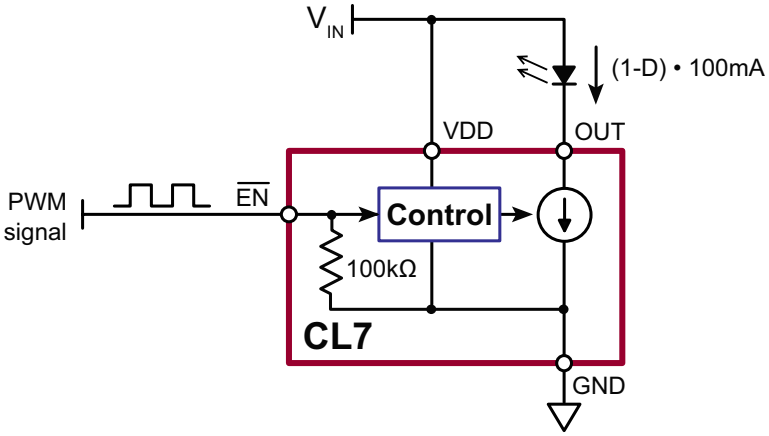


I_{OUT} vs Temperature



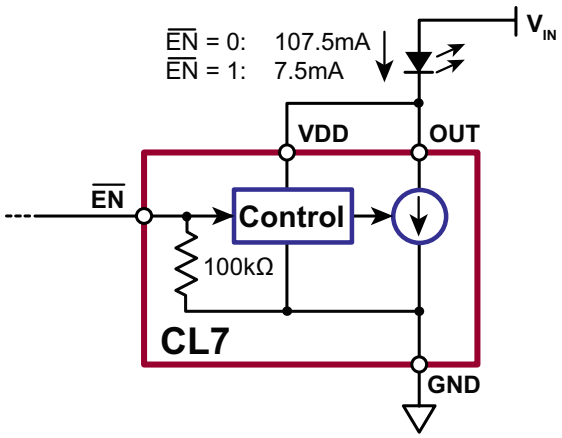
Application Circuits

PWM Dimming



D is the portion of time the PWM signal is high.

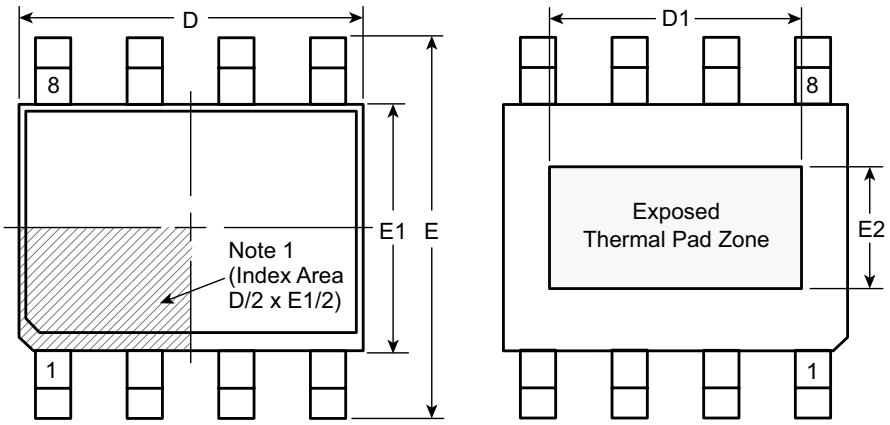
2-Level LED Circuit



Minimum V_{IN} is increased by LED drop.

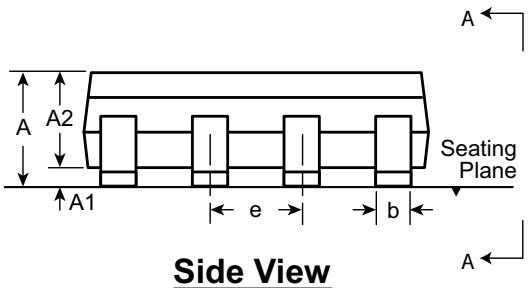
8-Lead SOIC (Narrow Body w/Heat Slug) Package Outline (SG)

4.90x3.90mm body, 1.70mm height (max), 1.27mm pitch

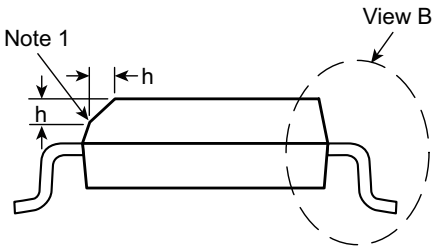


Top View

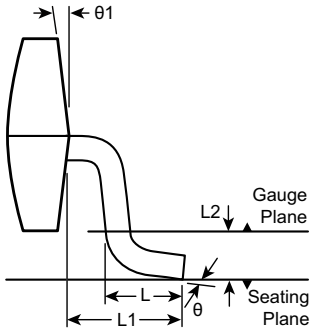
Bottom View



Side View



View A-A



View B

Notes:

1. *If optional chamfer feature is not present, a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/ identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	E2	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.25*	0.00	1.25	0.31	4.80*	3.30†	5.80*	3.80*	2.29†	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	-	6.00	3.90	-		-	-			-	-
	MAX	1.70	0.15	1.55*	0.51	5.00*	3.81†	6.20*	4.00*	2.79†		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation BA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
***Supertex Doc. #:** DSPD-8SOSG, Version D041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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