

High Efficiency Thyristor

$$V_{RRM} = 1200 \text{ V}$$

$$I_{TAV} = 5 \text{ A}$$

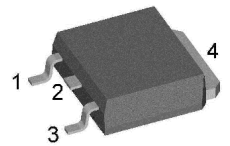
$$V_T = 1.31 \text{ V}$$

Single Thyristor

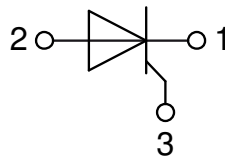
Part number

CLA5E1200UC

Marking on Product: C5TLUE



Backside: anode



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: TO-252 (DPak)

- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0

Terms Conditions of usage:

The data contained in this product data sheet is exclusively intended for technically trained staff. The user will have to evaluate the suitability of the product for the intended application and the completeness of the product data with respect to his application. The specifications of our components may not be considered as an assurance of component characteristics. The information in the valid application- and assembly notes must be considered. Should you require product information in excess of the data given in this product data sheet or which concerns the specific application of your product, please contact the sales office, which is responsible for you.

Due to technical requirements our product may contain dangerous substances. For information on the types in question please contact the sales office, which is responsible for you.

Should you intend to use the product in aviation, in health or live endangering or life support applications, please notify. For any such application we urgently recommend

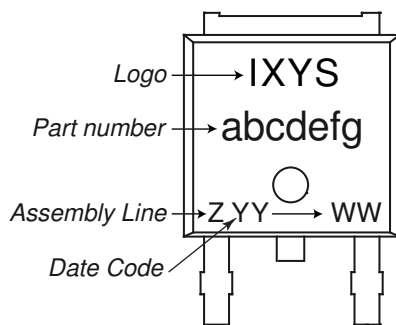
- to perform joint risk and quality assessments;

- the conclusion of quality agreements;

- to establish joint measures of an ongoing product survey, and that we may make delivery dependent on the realization of any such measures.

Thyristor			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1300	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1200	V
I_{RD}	reverse current, drain current	$V_{R/D} = 1200\text{ V}$	$T_{VJ} = 25^{\circ}C$		10	μA
		$V_{R/D} = 1200\text{ V}$	$T_{VJ} = 125^{\circ}C$		1	mA
V_T	forward voltage drop	$I_T = 5\text{ A}$	$T_{VJ} = 25^{\circ}C$		1.33	V
		$I_T = 10\text{ A}$			1.62	V
		$I_T = 5\text{ A}$	$T_{VJ} = 125^{\circ}C$		1.31	V
		$I_T = 10\text{ A}$			1.72	V
I_{TAV}	average forward current	$T_C = 135^{\circ}C$	$T_{VJ} = 150^{\circ}C$		5	A
$I_{T(RMS)}$	RMS forward current	180° sine			7.8	A
V_{T0}	threshold voltage	} for power loss calculation only	$T_{VJ} = 150^{\circ}C$		0.89	V
r_T	slope resistance				85	m Ω
R_{thJC}	thermal resistance junction to case				1.5	K/W
R_{thCH}	thermal resistance case to heatsink			0.50		K/W
P_{tot}	total power dissipation		$T_C = 25^{\circ}C$		85	W
I_{TSM}	max. forward surge current	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		70	A
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$		76	A
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}C$		60	A
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$		64	A
I^2t	value for fusing	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		25	A ² s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$		24	A ² s
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}C$		18	A ² s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$		17	A ² s
C_J	junction capacitance	$V_R = 400\text{ V } f = 1\text{ MHz}$	$T_{VJ} = 25^{\circ}C$		2	pF
P_{GM}	max. gate power dissipation	$t_p = 30\text{ }\mu s$	$T_C = 150^{\circ}C$		5	W
		$t_p = \mu s$			2.5	W
P_{GAV}	average gate power dissipation				0.25	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 150^{\circ}C; f = 50\text{ Hz}$ repetitive, $I_T = 10\text{ A}$			150	A/ μs
		$t_p = 200\text{ }\mu s; di_G/dt = 0.1\text{ A}/\mu s;$ $I_G = 0.1\text{ A}; V = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 5\text{ A}$			500	A/ μs
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^{\circ}C$		500	V/ μs
		$R_{GK} = \infty$; method 1 (linear voltage rise)				
V_{GT}	gate trigger voltage	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}C$		1.8	V
			$T_{VJ} = -40^{\circ}C$		1.9	V
I_{GT}	gate trigger current	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}C$		30	mA
			$T_{VJ} = -40^{\circ}C$		50	mA
V_{GD}	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^{\circ}C$		0.2	V
I_{GD}	gate non-trigger current				1	mA
I_L	latching current	$t_p = 10\text{ }\mu s$	$T_{VJ} = 25^{\circ}C$		45	mA
		$I_G = 0.1\text{ A}; di_G/dt = 0.1\text{ A}/\mu s$				
I_H	holding current	$V_D = 6\text{ V } R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		30	mA
t_{gd}	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}C$		2	μs
		$I_G = 0.1\text{ A}; di_G/dt = 0.1\text{ A}/\mu s$				
t_q	turn-off time	$V_R = 100\text{ V}; I_T = 5\text{ A}; V = \frac{2}{3} V_{DRM}$ $di/dt = 10\text{ A}/\mu s \quad dv/dt = 20\text{ V}/\mu s \quad t_p = 200\text{ }\mu s$	$T_{VJ} = 125^{\circ}C$		150	μs

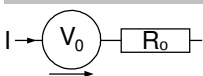
Package TO-252 (DPak)			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
I_{RMS}	RMS current	per terminal			20	A
T_{VJ}	virtual junction temperature		-40		150	°C
T_{op}	operation temperature		-40		125	°C
T_{stg}	storage temperature		-40		150	°C
Weight				0.3		g
F_C	mounting force with clip		20		60	N

Product Marking

Part description

- C = Thyristor (SCR)
- L = High Efficiency Thyristor
- A = (up to 1200V)
- 5 = Current Rating [A]
- E = Single Thyristor
- 1200 = Reverse Voltage [V]
- UC = TO-252AA (DPak)

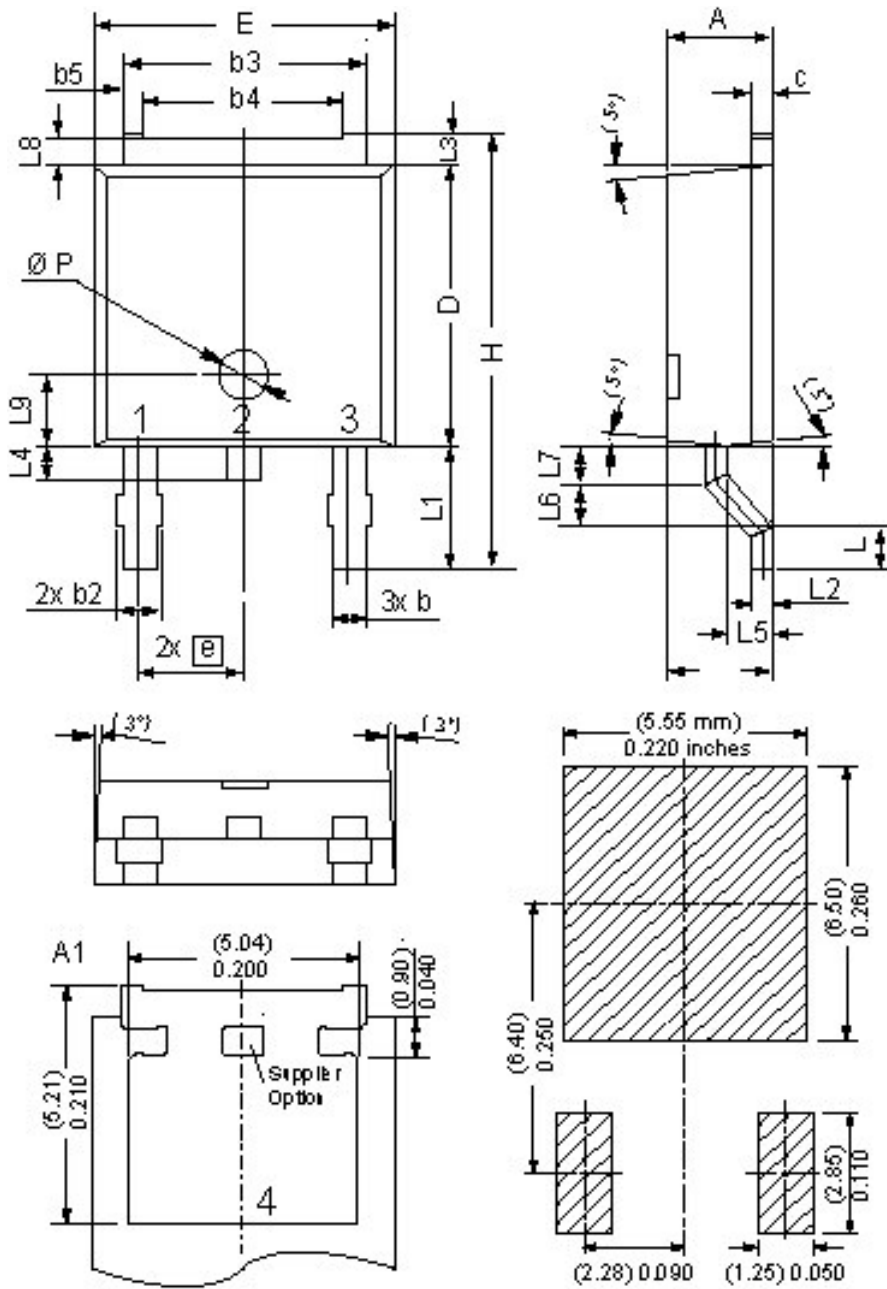
Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CLA5E1200UC	C5TLUE	Tape & Reel	2500	509799

Similar Part	Package	Voltage class
CLA5E1200PZ	TO-263AB (D2Pak) (2HV)	1200

Equivalent Circuits for Simulation
** on die level*
 $T_{VJ} = 150\text{ °C}$

Thyristor

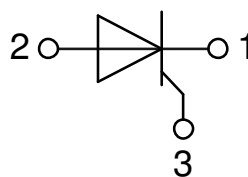
$V_{0\ max}$	threshold voltage	0.89	V
$R_{0\ max}$	slope resistance *	82	mΩ

Outlines TO-252 (DPak)



Dim	Millimeters		Inches	
	min	max	min	max
A	2.20	2.40	0.087	0.094
A1	2.10	2.50	0.083	0.098
b	0.66	0.86	0.026	0.034
b2	-	0.96	-	0.038
b3	5.04	5.64	0.198	0.222
b4	4.34 BSC		0.171 BSC	
b5	0.50 BSC		0.020 BSC	
c	0.40	0.86	0.016	0.034
D	5.90	6.30	0.232	0.248
E	6.40	6.80	0.252	0.268
e	2.10	2.50	0.083	0.098
H	9.20	10.10	0.362	0.398
L	0.55	1.28	0.022	0.050
L1	2.50	2.90	0.098	0.114
L2	0.40	0.60	0.016	0.024
L3	0.50	0.90	0.020	0.035
L4	0.60	1.00	0.024	0.039
L5	0.82	1.22	0.032	0.048
L6	0.79	0.99	0.031	0.039
L7	0.81	1.01	0.032	0.040
L8	0.40	0.80	0.016	0.031
L9	1.50 BSC		0.059 BSC	
Ø P	1.00 BSC		0.039 BSC	

Recommended min. foot print



Thyristor

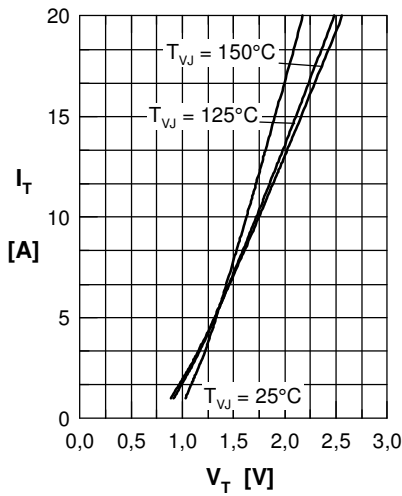


Fig. 1 Forward characteristics

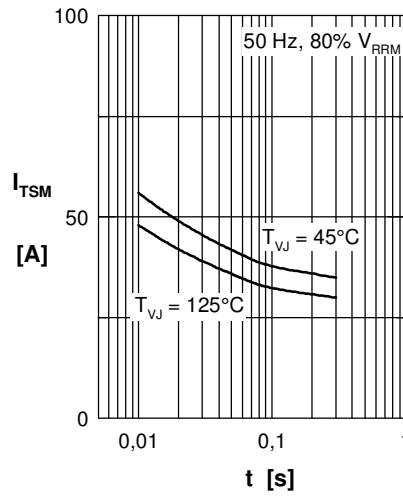


Fig. 2 Surge overload current
I_{TSM}: crest value, t: duration

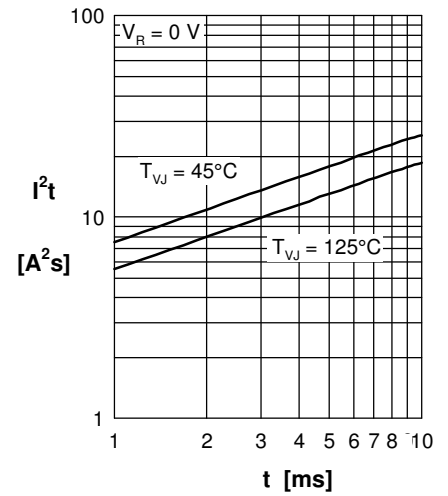


Fig. 3 I²t versus time (1-10 s)

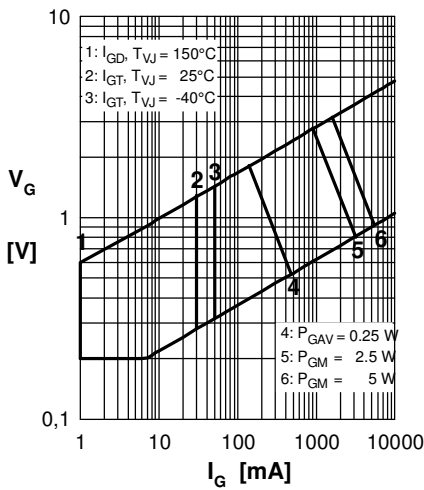


Fig. 4 Gate voltage & gate current

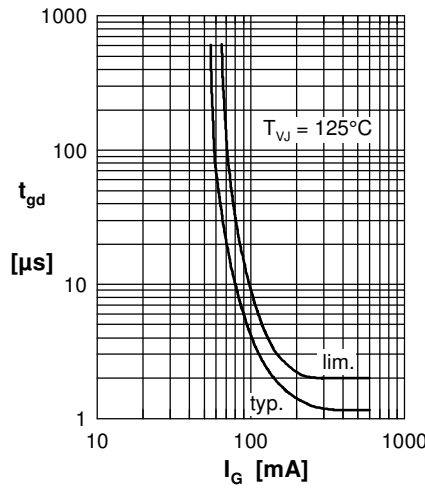


Fig. 5 Gate controlled delay time t_{gd}

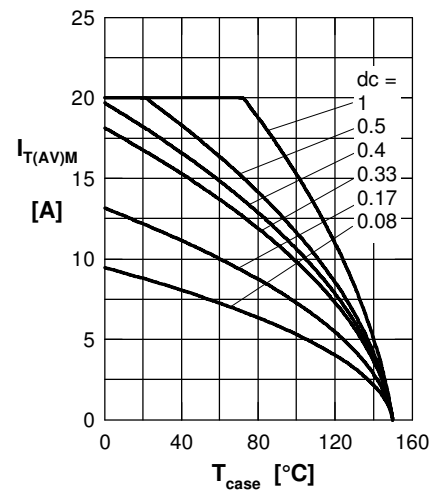


Fig. 6 Max. forward current at case temperature

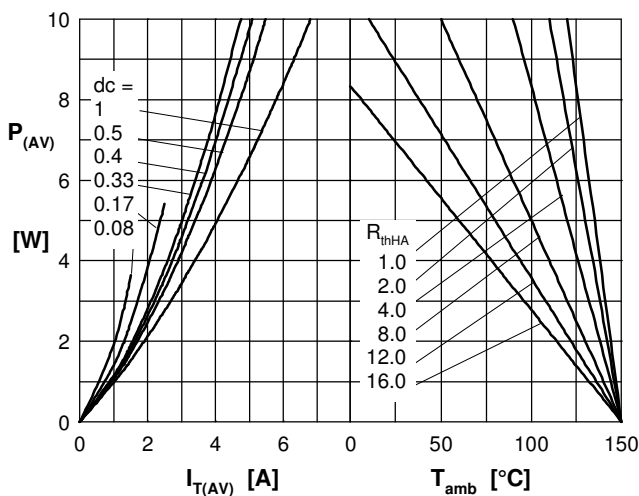


Fig. 7a Power dissipation versus direct output current
Fig. 7b and ambient temperature

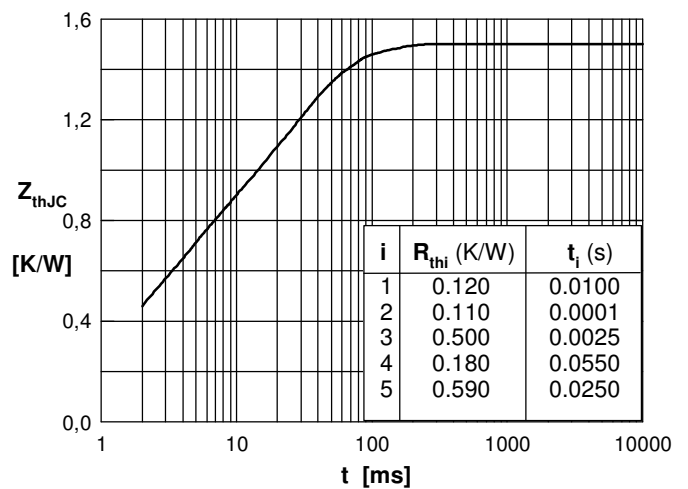


Fig. 7 Transient thermal impedance junction to case