Chunghwa Picture Tubes, Ltd.
Technical Specification

5k4T :

o

Date : **2013 / 08 / 26**

TFT-LCD

CLAA080WQ05 (tentative)

Accepted by:

APPROVED BY	CHECKED BY	PREPARED BY
		Application Division

Product Planning Management Center

CHUNGHWA PICTURE TUBES, LTD.
1127 Hopin Rd., Padeh, Taoyuan, Taiwan 334, R.O.C.
TEL: +886 3 3675151 FAX: +886 3 260 7003

Doc. No:	CLAA080WQ05 (tentative)	Issue Date:	2013 / 08 / 26

Modification Record List

NO.	Issue Date	Modification Index
1	2013 / 08/ 26	First version

Table of Content

1. OVERVIEW

CLAA080WQ05 is 8” color TFT LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, MIPI driver ICs, control circuit and backlight. By applying 8 bit digital data, 800×RGB (3) ×1280, 16.7M color images are displayed on the 8” diagonal screen. General specifications are summarized in the following table：

ITEM	SPECIFICATION
Display Area	107.64(H)x172.224(V) (mm) (8-inch diagonal)
Number of Pixels	800 ×3(H)×1280 (V)
Pixel Pitch	0.13455(H)×0.13455(V) (mm)
Color Pixel Arrangement	RGB vertical stripe
Display Mode	Normally Black
Number of Colors	16.7M(8bits)(MIPI)
Gamut	58%(Typ)
Optimum Viewing Angle	whole view
Response Time	20ms (Typ) (Black to White)
Surface Treatment	HC , Hardness：3H
Viewing Angle(CR>10)	85°、85° / 85°、85°(Typ.)
Brightness	350 cd/m^2 (5P) (Typ)
Uniformity	5point：80 %(Typ.)/ 13point：70 %(Typ.)
Consumption of Power	Logic 0.4W (W Pattern)/ BL_ 1.26W
Module Size	114.8 (H)×184.7 (V)×4.56 (D) (Max.)(mm)
Module Weight	105g (Max.)

The LCD Products listed on this document are not suitable for use of aerospace equipment, submarine cable, and nuclear reactor control system and life support systems. If customers intend to use these LCD products for applications listed above or those not included in the "Standard" list as follows, please contact our sales in advance.

Standard：Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tool, Industrial robot, Audio and Visual equipment, Other consumer products.

2. ABSOLUTE MAXIMUM RATINGS

The following are maximum value, which if exceeded, may cause faulty operation or damage to the unit.

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
LCD Power Voltage	VDDI	-0.3	4.0	V	
	VCCI	-0.3	2	V	
Operation Temperature	Top	0	50	℃	*1). 2). 3). 4)
Storage Temperature	Tstg	-20	60	℃	*1). 2). 3)

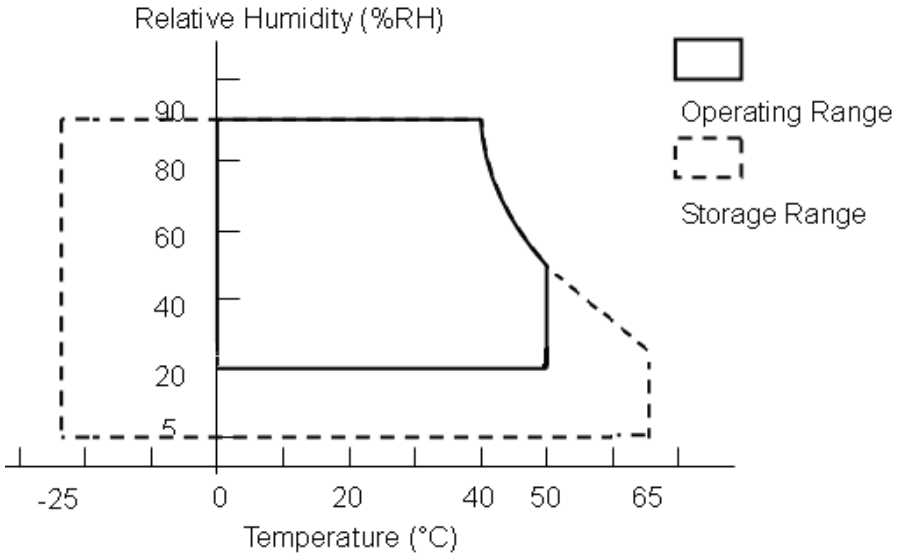
【Note】

*1) The relative temperature and humidity range are as below sketch, 90%RH Max. (Ta≦40℃)

*2) The maximum wet bulb temperature ≦39℃(Ta＞40℃) and without dewing.

*3) If product in environment which over the definition of the relative temperature and humidity out of range too long, it will affect visual of LCD.

*4) If you operate LCD in normal temperature range, the center surface of panel should be under 50℃.



3. ELECTRICAL CHARACTERISTICS

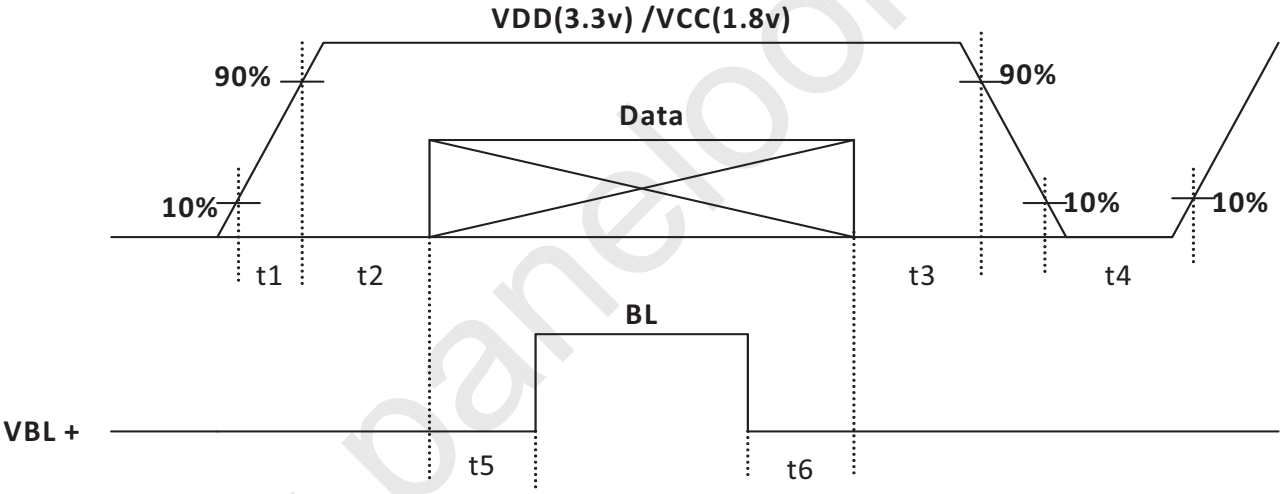
(A) TFT LCD

TEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
LCD Power Voltage	VDDI	3	3.3	3.6	V	*1)
	VCCI	1.7	1.8	1.9	V	
LCD Power Current	IDD	-	113	157	mA	*2)
	ICC	-	14	15.5	mA	
Rush Current	Irush	-	-	2	A	*4)

【Note】

*1) Power Sequence：

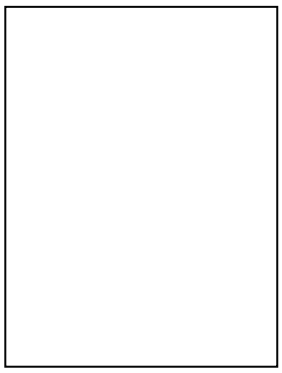
0.5 ms ≦t1≦10ms
0.01 ms＜t2≦50 ms
0.01 ms＜t3≦50 ms
500 ms≦t4
200 ms≦t5
200 ms≦t6



※Please refer to initial code

*2) Typ. value is White Pattern：1280 line mode。

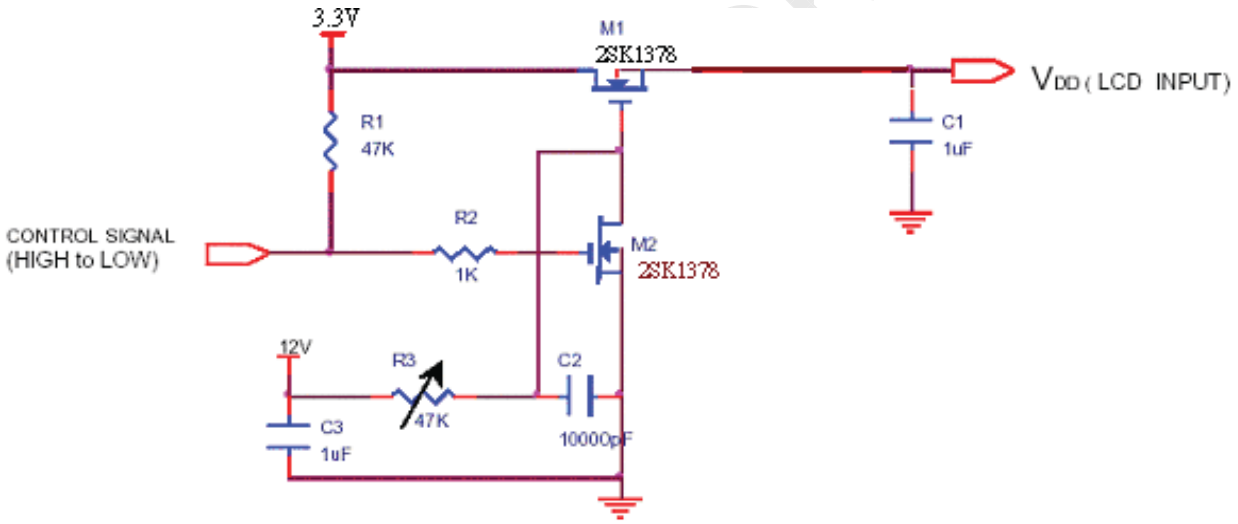
Circuit condition (Max.)：VDDI=3.3 V，f_V=60 Hz，f_H=77.76 kHz，f_{CLK}=68.43 MHz

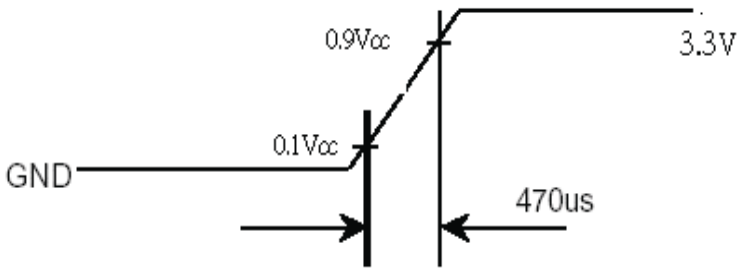


Max. value is R /G /B Pattern：1280 line mode。

Circuit condition (Max.)：VDDI=3.3 V，f_V=60 Hz，f_H=77.76 kHz，f_{CLK}=68.43 MHz

*3) Irush measure condition





(B) BACK LIGHT

(a) ELECTRICAL CHARACTERISTICS

Ta=25℃

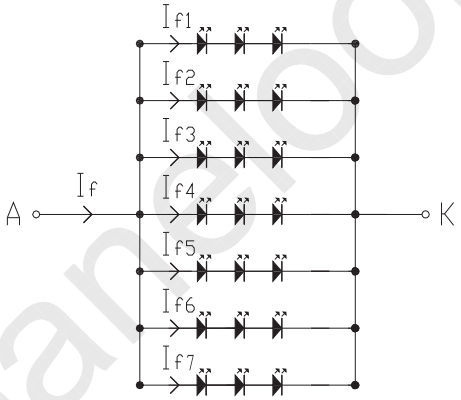
ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
LED Total Iuput Voltage	VBL+	-	8.55	9.0	V	
LED Total Input Current	IBL+	-	140	-	mA	
Forward Voltage per LED	VF	2.7	2.85	3	V	
Forward Current per LED	IF	-	20	-	mA	*1)
Power consumption	PLED	-	-	1.26	W	*3)

(b) LED LIFE – TIME

ITEM	Condition	min	typ	max	UNIT	NOTE
LIFE TIME	IF=20mA、Ta=25℃	10000	x	x	**hrs**	***4)**

【Note】

*1)LED Circuit Diagram：



*2) A：Anode(＋)，K：Cathode( )

*3) Calculator value for reference $I_F \times V_F \times N$ = PLED

*4) Life time means that estimated time to 50% degradation of initial luminous intensity.

4. Connector Interface PIN & Function

CN (Interface signal)

Outlet connector: AYF333135 (Panasonic)

Pin No.	Pin Name	Description
1	VPP	NC (reserve for CPT internal test)
2	GND	Ground
3	NC	NC
4	D2_P	MIPI Input Data Pair
5	FB1	LED Feedback1
6	D2_N	MIPI Input Data Pair
7	FB2	LED Feedback2
8	GND	Ground
9	FB3	LED Feedback3
10	D1_P	MIPI Input Data Pair
11	GND	Ground
12	D1_N	MIPI Input Data Pair
13	VLED	LED Output
14	GND	Ground
15	VLED	LED Output
16	CLK_P	MIPI Input Data Pair
17	GND	EDID > CPT GND
18	CLK_N	MIPI Input Data Pair
19	LOGIC_3V3	Power Supply, 3.3V(Typical)
20	GND	Ground
21	LOGIC_3V3	Power Supply, 3.3V(Typical)
22	D0_P	MIPI Input Data Pair
23	NC	NC
24	D0_N	MIPI Input Data Pair
25	LOGIC_1V8	Power Supply, 1.8V(Typical)
26	GND	Ground
27	LOGIC_1V8	Power Supply, 1.8V(Typical)
28	D3_P	MIPI Input Data Pair
29	LCD_RST	REST PIN (H 1.8V L 0V)
30	D3_N	MIPI Input Data Pair
31	NC	NC

5. INTERFACE TIMING CHART

(1) MIPI Interface Timing Sequence

(a) MIPI interface DC characteristic：

Item		Parameter	Min.	Typ.	Max.	Unit
LP_TW	Thevenin output high level	VOH	1.1	1.2	1.3	V
	Thevenin output low level	VOL	-50		50	mV
	Output impedance of LP transmitter	ZOLP	110			Ω
HS_RX	Common-mode voltage HS receive mode	VCMRX(DC)	70		330	mV
	Differential input high threshold	VIDTH			70	mV
	Differential input low threshold	VIDTL	-70			mV
	Single-ended input high voltage	VIHHS			460	mV
	Single-ended input low voltage	VILHS	-40			mV
	Single-ended threshold for HS termination enable	VTERM-EN			450	mV
	Differential input impedance	ZID	80	100	125	Ω
LP_RX	Logic 1 input voltage	VIH	880			mV
	Logic 0 input voltage. not in ULPState	VIL			550	mV
	Input hysteresis	VHYST	25			mV
LP_CD	Logic 1 contention threshold	VIHCD	450			mV
	Logic 1 contention threshold	VILCD			200	mV

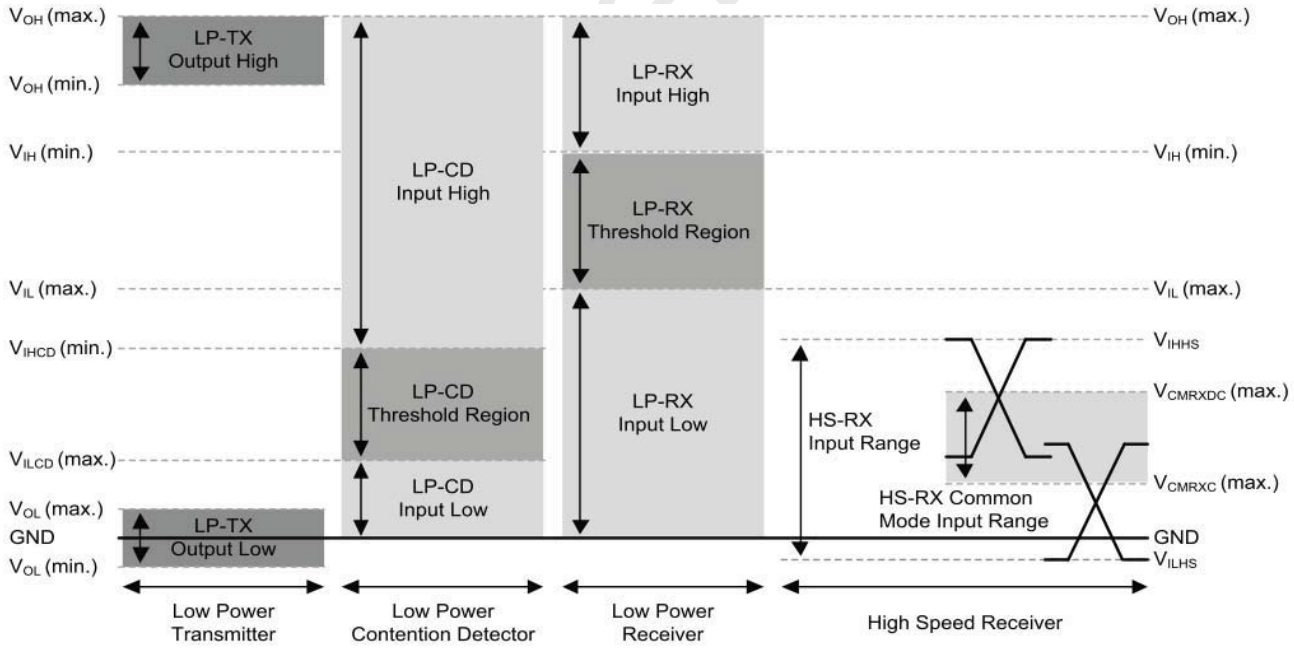


Figure1. MIPI DC Diagram

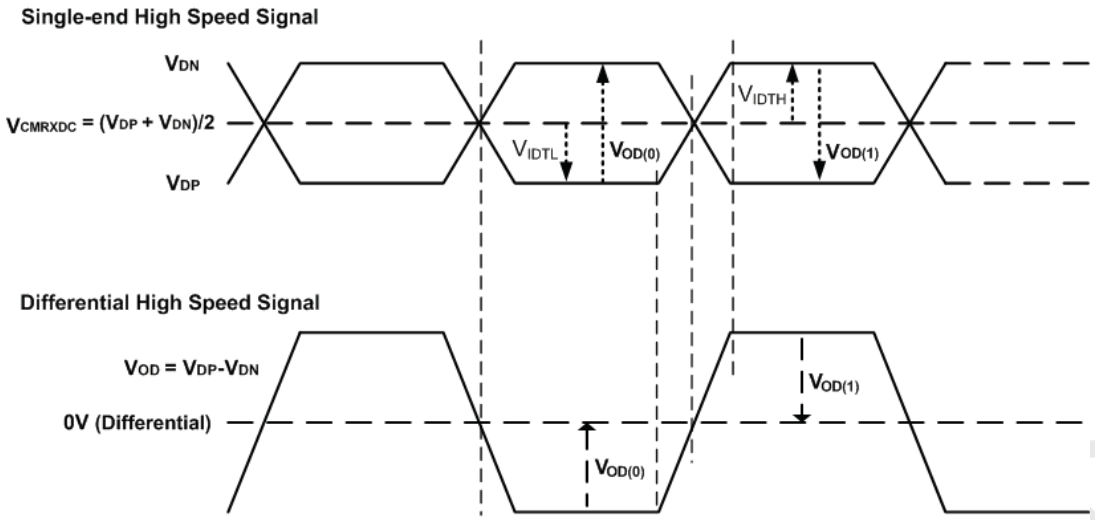


Figure2. Signal-ended and Resulting Differential HS Signals Diagram

(b) MIPI data to clock timing definitions

Clock Parameter	Symbol	Min	Typ.	Max.	Unit
UI instantaneous	UI INST	2		12.5	ns
Data to Clock Setup Time[Receiver]	T SETUP[RX]	0.15			UI INST
Clock to Data Hold Time[Receiver]	T HOLD[RX]	0.15			UI INST
Data to Clock Skew (Measured at transmitter)	T SKEW[TX]	-0.15		0.15	

【Note】

*1) This max value corresponds to a minimum 80 Mbps data rate per lane

*2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

*3) Total silicon and package delay budget of 0.3 UIINST

4) Total setup and hold window for receiver of 0.3 UIINST

*5) T SETUP[Rx] and T HOLD[RX] are only for RX without FPCB and connector and guaranteed by design.

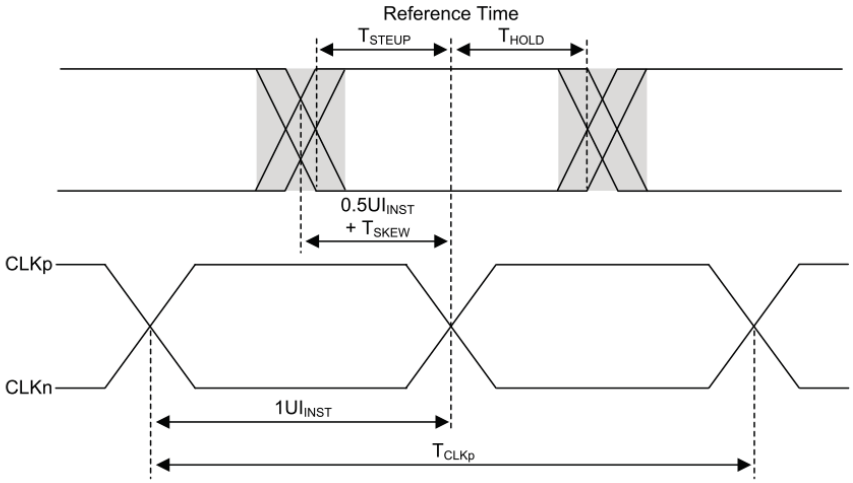
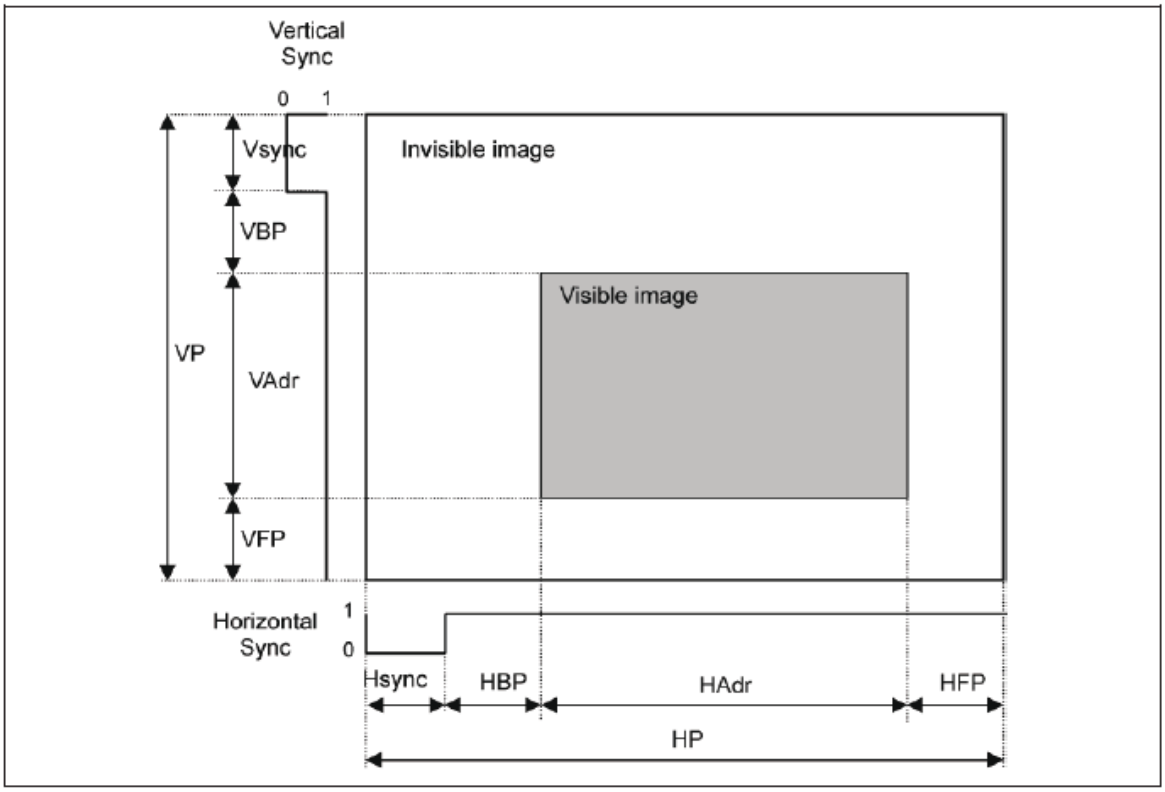


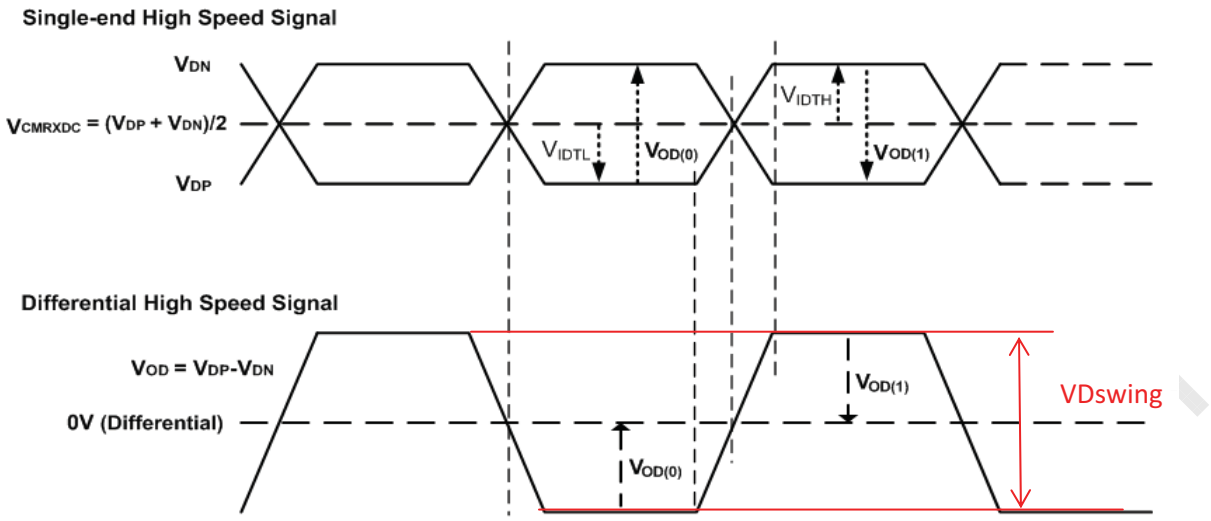
Figure3. MIPI data to clock timing definitions

(2) Timing Chart

ITEM			SYNBOL	Timing	UNIT
LCD	Frame Rate		-	60	Hz
Timing	DCLK	Frequency	fCLK	68.43	MHz
		Period	Tclk	14.61	ns
	Horizontal	Horizontal total time	tHP	880	t_{CLK}
		Horizontal Active time	tHadr	800	t_{CLK}
		Horizontal Pulse Width	tHsync	5	t_{CLK}
		Horizontal Back Porch	tHBP	59	t_{CLK}
		Horizontal Front Porch	tHFP	16	t_{CLK}
	Vertical	Vertical total time	tvp	1296	t_H
		Vertical Active time	tVadr	1280	t_H
		Vertical Pulse Width	tVsync	5	t_H
		Vertical Back Porch	tVBP	3	t_H
		Vertical Front Porch	tVFP	8	t_H
Differential Swing			VDswing	250	mV
Bit Rate			TX SPD(MBPS)	450	Mbps
Pixel Fomat				888	Data bit/pixel
Lane				4	Lane

※Please refer to initial code





(3)Reset Input Timing

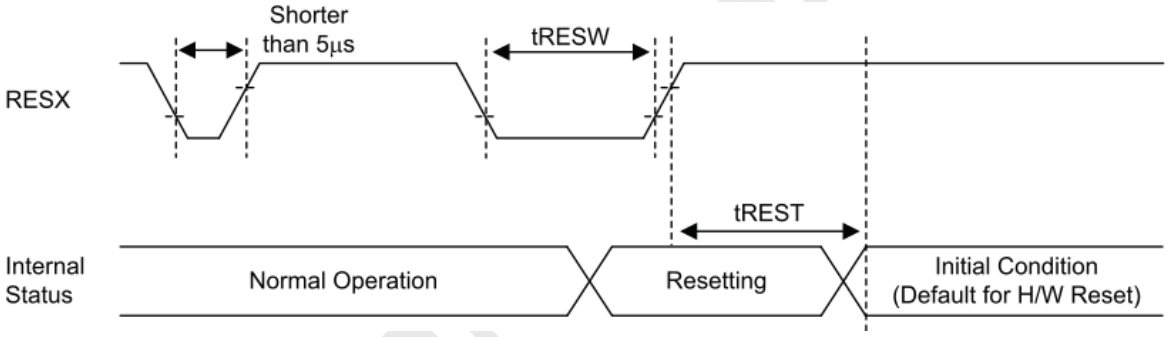


Figure4. Reset Input Timing

Symbol	Parameter	Pad	Min.	Typ.	Max.	Unit	Note
tRESW	Reset low pulse width	RESX	10			us	
tREST	Reset completion time	RESX			5	ms	Reset during Sleep In mode
		RESX			120(5)		Reset during Sleep Out mode

【Note】

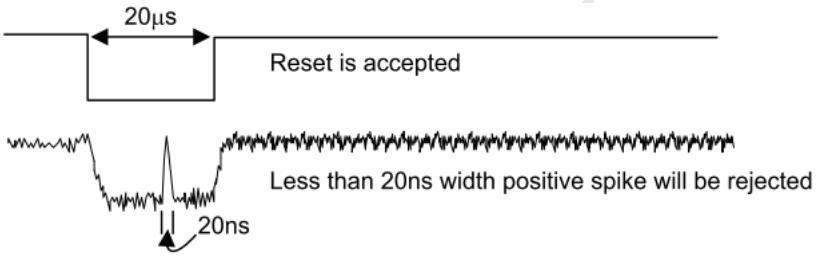
*1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset Start

*2) During the reset period, the display will be blanked. (The display is entering blanking sequence, for which the maximum time is 120ms, when Reset starts is sleep out-mode. The display remains in the blank state is Sleep In-mode) and then return to default condition for H/W reset.

*3) During Reset Completion Time, ID bytes (or similar) value in MTP block will be latched to the internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

*4) Spike Rejection also applies during a valid reset pulse as shown below:



*5) It is necessary to wait for 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(4) DATA mapping

COLOR	INPUT DATA	R DATA								G DATA								B DATA							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	CYAN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	MAGENTA	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	GREEN(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
BLUE	BLUE(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	BLUE(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

【Note】

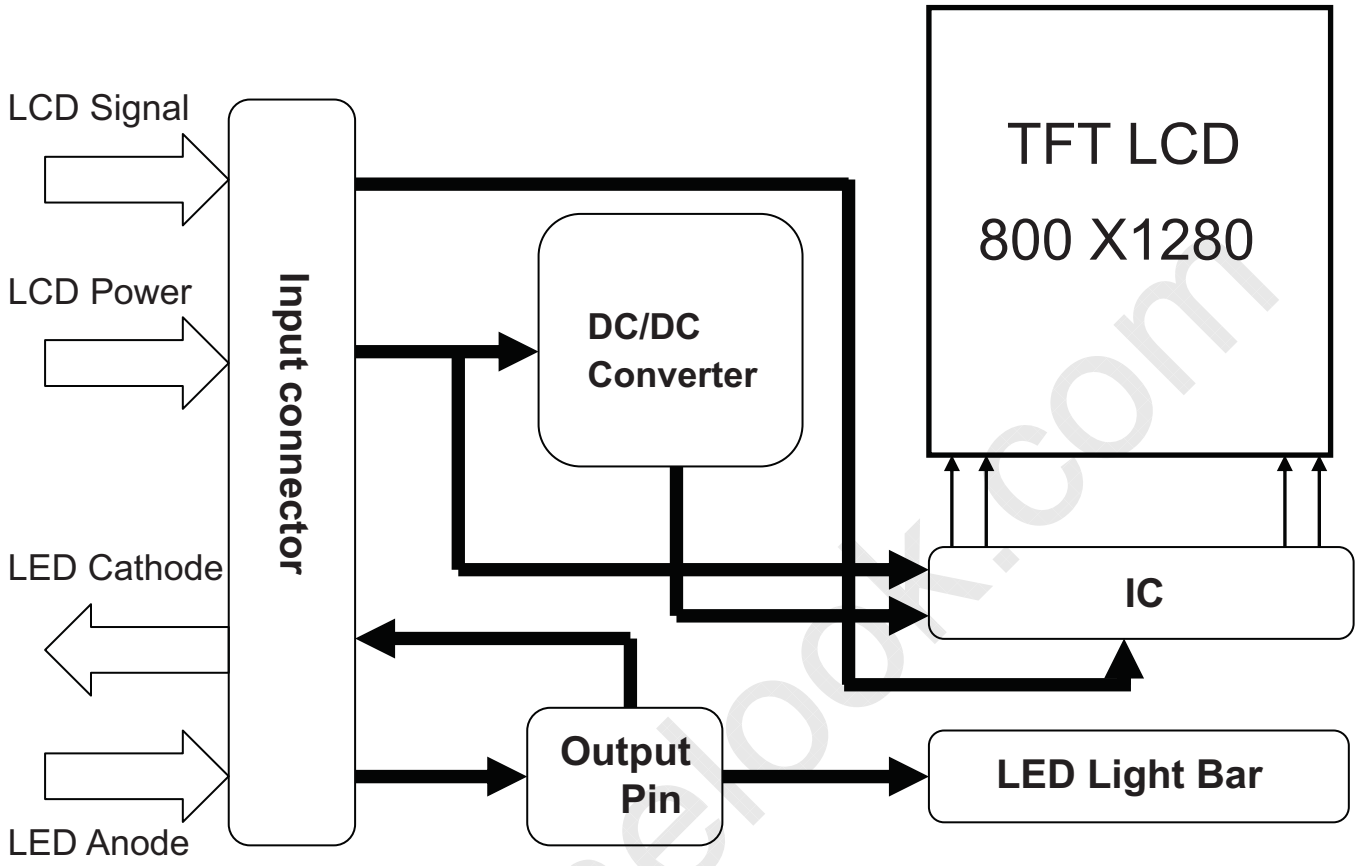
*1) Gray level:

Color(n)：n is level order; higher n means brighter level.

*2) DATA:

1: high，0: low

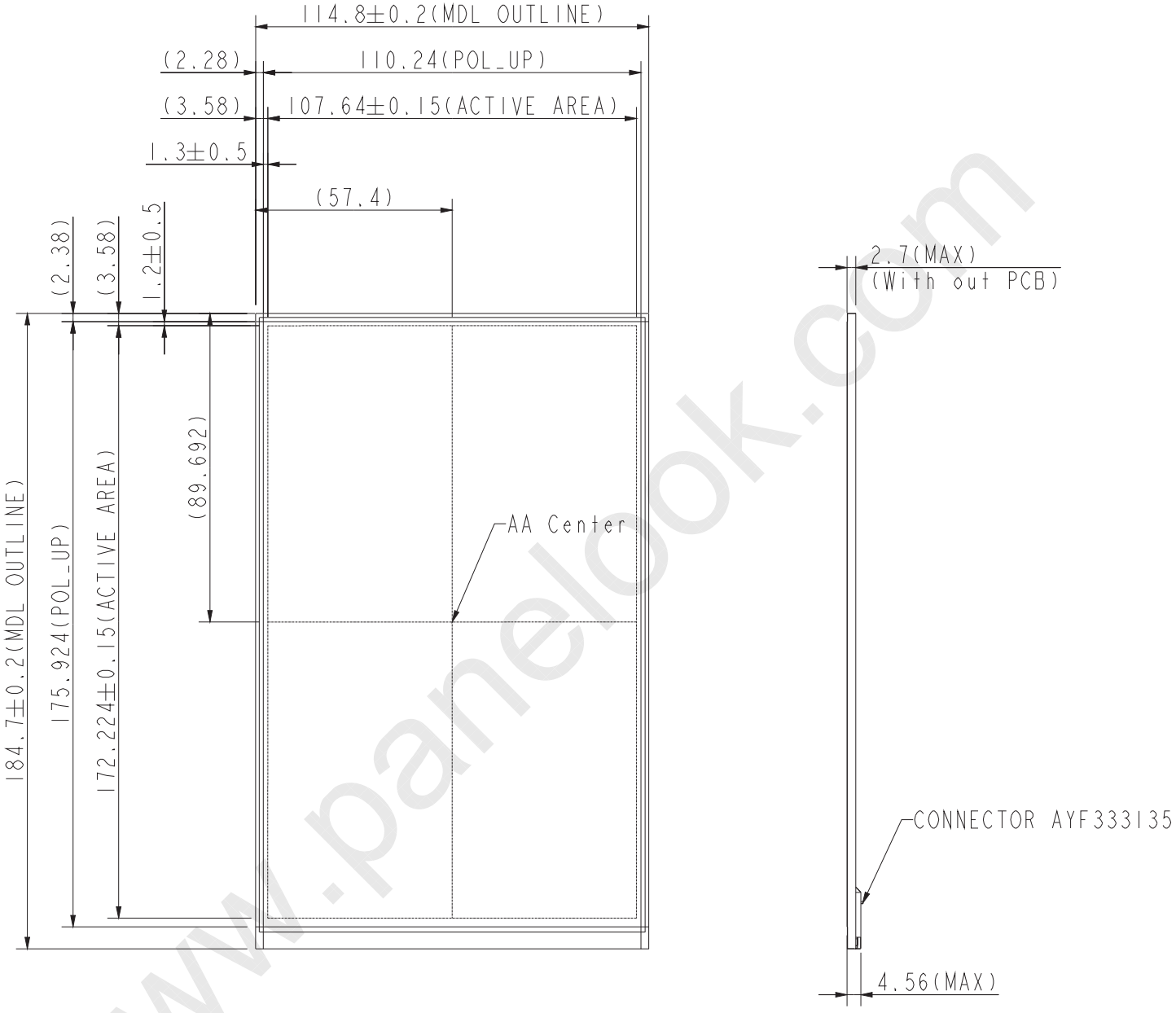
6. BLOCK DIAGRAM



7. MECHANICAL SPECIFICATION

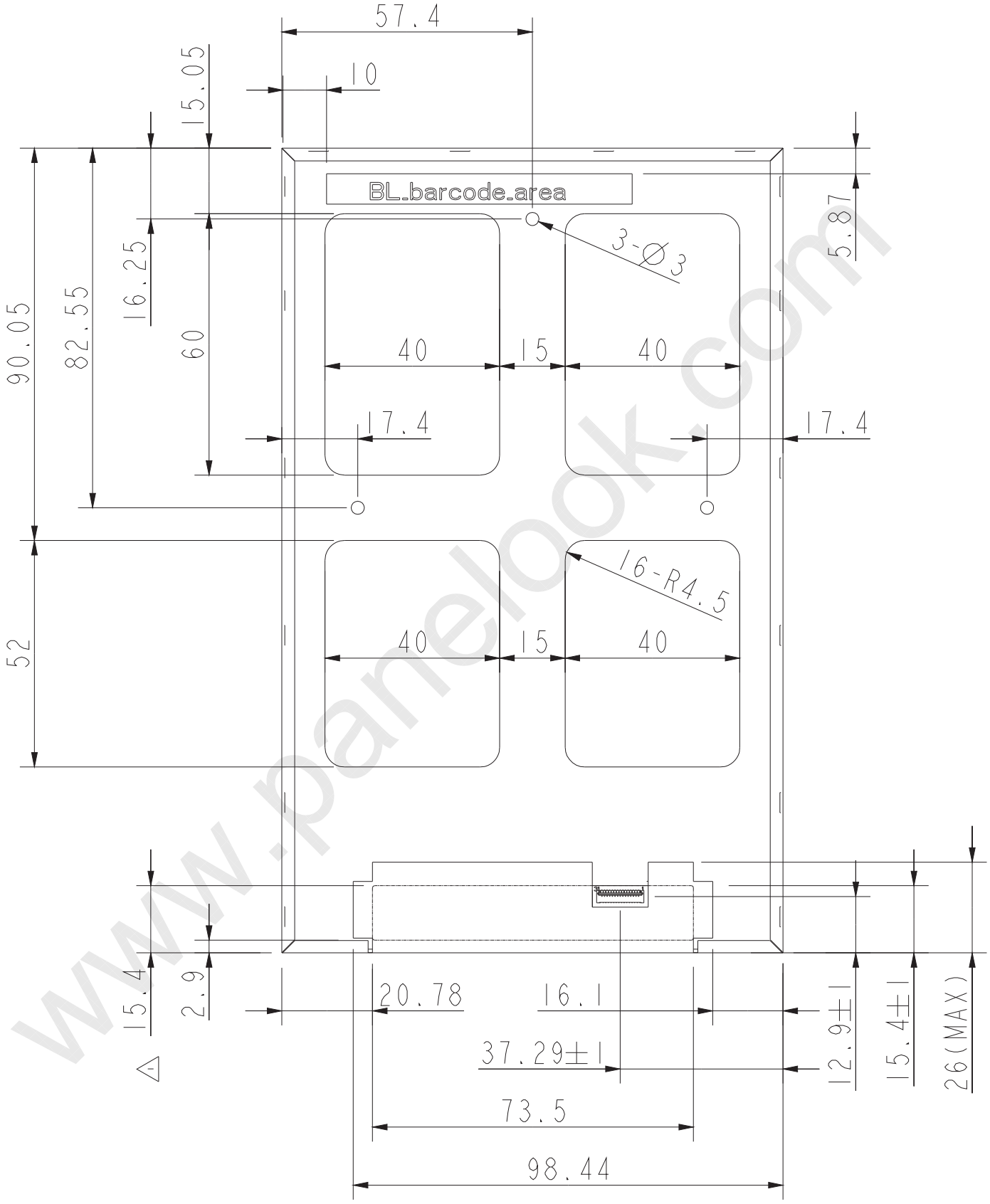
(1) Front side

The tolerance, not show in the figure, is ±0.15mm. **[Unit： mm]**



2) Rear side

The tolerance, not show in the figure, is ±0.15mm. **[Unit： mm]**



8. OPTICAL CHARACTERISTICS

Ta=25℃，VDD=3.3V

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Contrast Ratio		CR	θ=ψ= 0°	600	800	--	--	*1) 2)
Luminance (Center)		L	θ=ψ= 0°	300	350	--	cd/m^2	*1) 3)
Uniformity(5P)		ΔL	θ=ψ= 0°	--	70	--	%	*1) 3)
Uniformity(9P)		ΔL	θ=ψ= 0°	--	80	--	%	*1) 3)
Response Time		Tr+Tf	θ=ψ= 0°	--	25	30	ms	*5)
Cross talk		CT	θ=ψ= 0°	--	--	2	%	*6)
View angle	Horizontal	Ψ	CR≧10	80/-80	85/-85	--	°	View angle
	Vertical	θ		80/-80	85/-85	--	°	
Color Temperature Coordinate	W	X	θ=ψ= 0°	0.283	0.313	0.343	--	Color Temperature Coordinate
		Y		0.299	0.329	0.359		
	R	X		TBD	TBD	TBD	--	
		Y		TBD	TBD	TBD		
	G	X		TBD	TBD	TBD	--	
		Y		TBD	TBD	TBD		
	B	X		TBD	TBD	TBD	--	
		Y		TBD	TBD	TBD		
Gamut			θ=ψ= 0°	55	58	--	--	
Gamma		γ	GL	2.0	2.2	2.4	--	*7)

Color coordinate and color gamut are measured by SRUL1R, response time is measured by TRD-100,and all the other items are measured by BM-5A (TOPCON). All these items are measured under the dark room condition (no ambient light).

Measurement Condition: IL=20 mA(each LED)

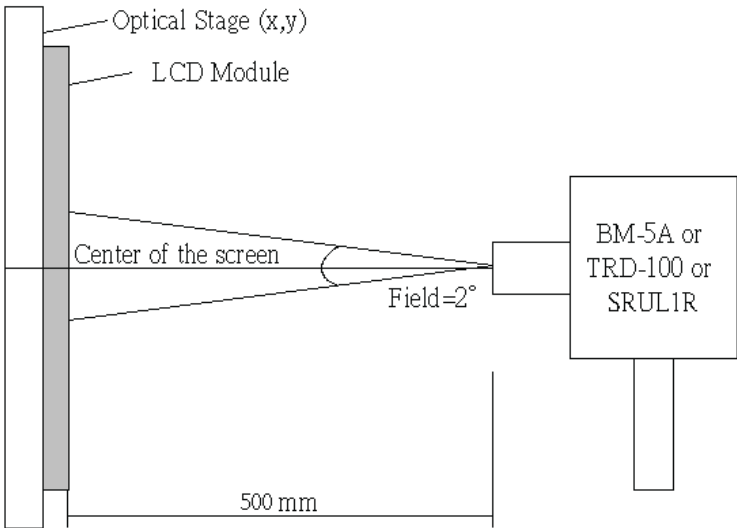
Definition of these measurement items is as follows:

***1) Setup of Measurement Equipment**

The LCD module should be turn on to a stable luminance level to be reached. The measurement should be executed after lighting Backlight for 20 minutes and in a dark room.

***2) Definition of Contrast Ratio**

CR=ON (White) Luminance/OFF (Black) Luminance

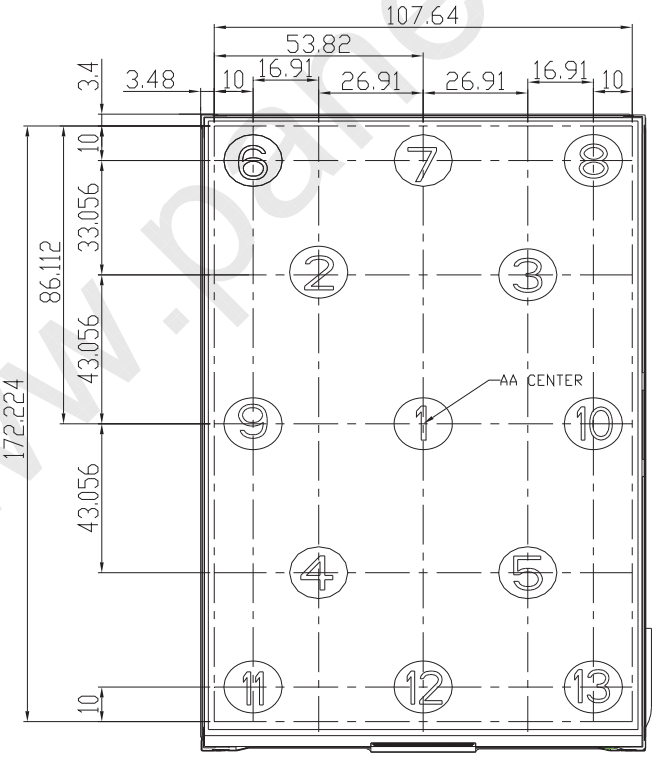


***3) Definition of Luminance and Luminance uniformity**

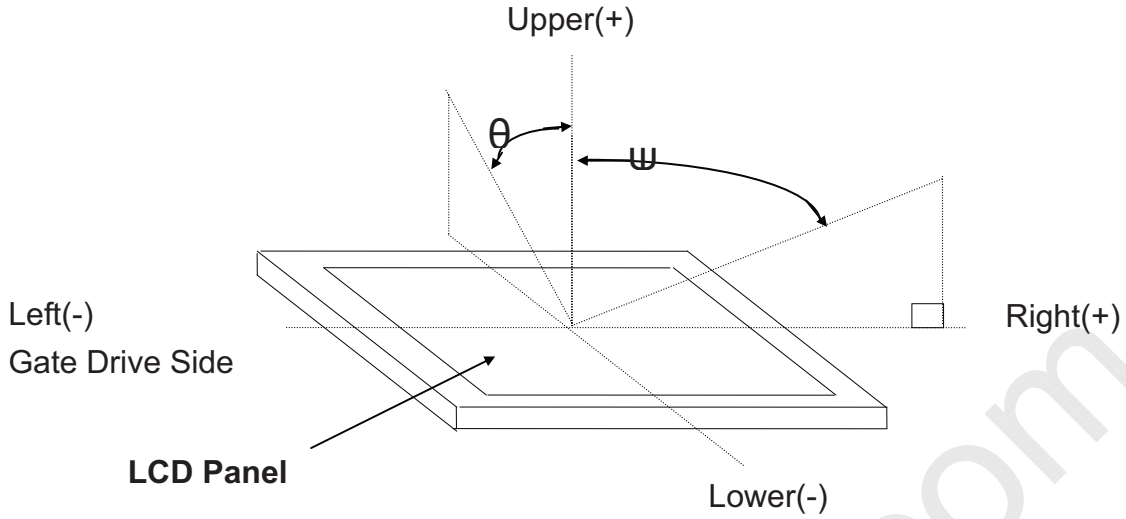
Central luminance: The white luminance is measured at the center position “1” on the screen, see Fig below.

5P Luminance (AVG): The white luminance is measured at measuring points 1~5 see Fig below.

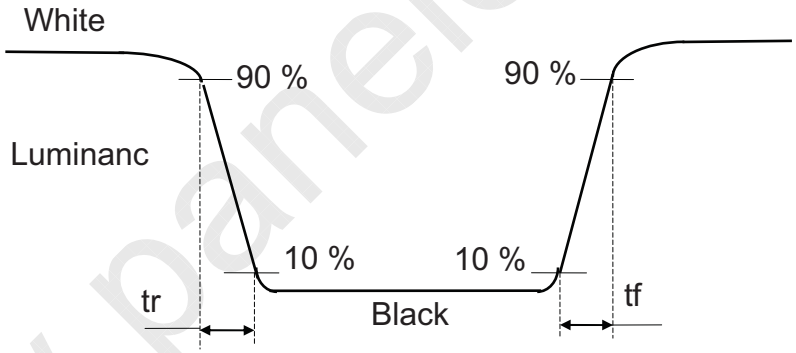
9P Uniformity: Δ L = (Lmin / Lmax) ×100% at measuring points 1 & 6~13 see fig below.



***4) Definition of view angle(θ，ψ)**



***5) Definition of response time**



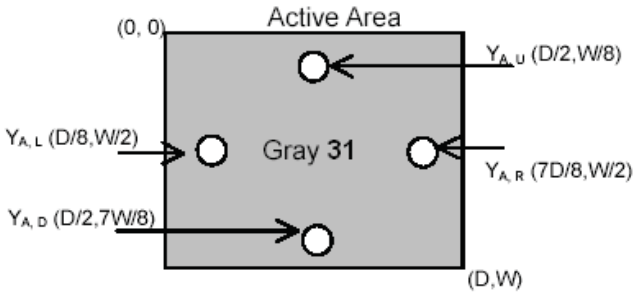
***6) Crosstalk Modulation Ratio:**

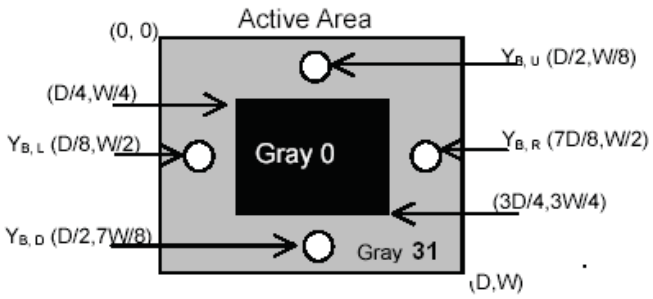
CT= $|Y_B - Y_A|$ / Y_{Ax}× 100%

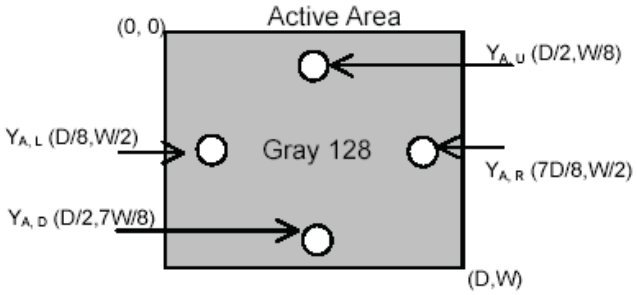
Y_A 、Y_B measure position and definition

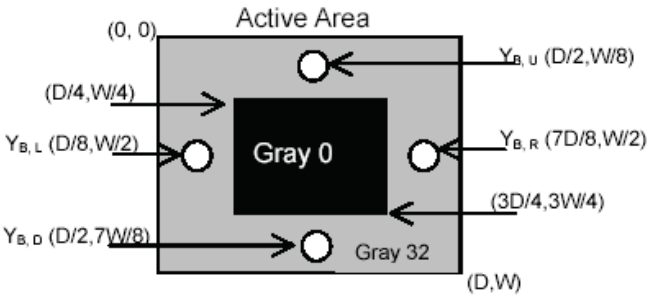
Y_A means luminance at gray level 31(exclude gray level 0 pattern)

Y_B means luminance at gray level 31(include gray level 0 pattern)



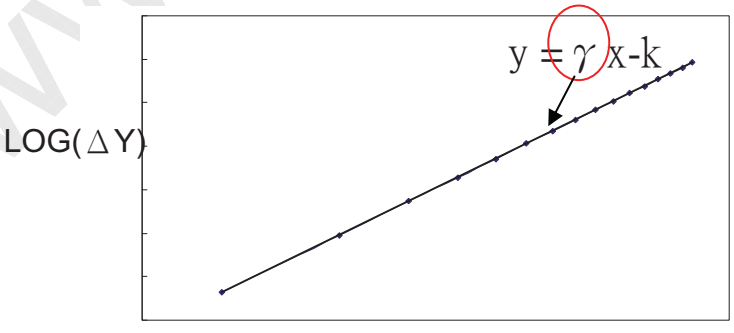






***7) Definition Gamma (VESA)**

Based on Customer Sample, take the average value as a standard center value and the variation range of gamma value caused by loop voltage error should be between +/ 0.2. the bellow figure shows how to obtain the gamma curve and γ (from gray level: 0、4、8 60、63).



9. RELIABILITY TEST CONDITIONS

Test Items	Conditions
High Temp. Operating Test	50℃, 240 Hrs
High Temp. Storage Test	65℃, 240 Hrs
High Temp/ High Humidity Operating Test	40℃, 90% RH, 240Hrs
High Temp./High Humidity Storage Test	60℃, 90% RH, 48Hrs
Low Temp. Operating Test	0℃, 240 Hrs
Low Temp. Storage Test	-20℃, 240 Hrs
Shock Test	980m/s2,Action time: 6ms, Time: 3 times for each direction, Direction:+/–X, +/–Y, +/–Z
ESD	Air +/–15KV ,contact +/–8KV , No damage, power off

【Note】

The judgment of the above test should be made as follow:

Pass：Normal display image with no obvious non-uniformity and no line defect.

Partial transformation of the module parts should be ignored.

Fail：No display image, obvious non-uniformity, or line defects.