Chunghwa Picture Tubes, Ltd.
Technical Specification

To : **Jean Co.**
Date : 2005/3/22

CPT TFT-LCD

CLAA170EA 08Q

ACCEPTED BY :

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1. OVERVIEW

CLAA170EA08Q is 17.0" color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, driver ICs, control circuit and backlight.By applying 6 bit digital data, 1280×1024, 26.2M-color images are displayed on the 17.0" diagonal screen. Input power voltage is 12.0V for LCD driving.Inverter for backlight is not included in this module. General specification are summarized in the following table:

ITEM	SPECIFICATION
Display Area (mm)	337.920(H) x 270.336(V)(17.0- inch diagonal)
Number of Pixels	1280(H) x 1024(V)
Pixel Pitch (mm)	0.264(H) x 0.264(V)
Color Pixel Arrangement	RGB vertical stripe (Stripe)
Display Mode	normally white，TN
Number of Colors	262K (6Bits)
Optimum Viewing Angle	6 o'clock
Brightness(cd/m^2)	300cd/m^2 (Typ.)(Center point,lamp current，7.0 mA)
Viewing Angle	140/130 (Typ.)
Wide Viewing Angle Technology	Optical Compensation Film
Surface Treatment	Anti-glare
Total Module Power (W)	21.4 (Typ.)
Module Size (mm)	358.5(W) x 296.5(H) x 17.5(D)(max)
Module Weight (g)	2000 (Typ.)
Backlight Unit	CCFL, 4 tables, (Top*2/Bottom*2)，Edge light

2. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT	Remark
Power Supply Voltage for LCD	VCC	-0.5	15	V	--
Logic Input Voltage	VDDD	-0.5	4.0	V	--
Lamp Voltage	VL	625	832	Vrms	
Lamp Current	IL	3	7.5	mArms	**4)** • 6)
Lamp Frequency	FL	40	80	kHz	
static electricity	$VESD_t$	-200	200	V	*5)
	$VESD_C$	-8000	8000	V	
Operation Temperature	T_{op}	0	50	℃	*1), 2), 3)
Storage Temperature	T_{stg}	-20	60	℃	*1), 2), 3)
Delayed Discharge Time	TD	--	1	Sec	*7)

*1)If you operate the product in normal temperature range, the surface of panel should be under 60℃.

*2) The relative temperature and humidity range are as below sketch, 90%RHMax.(Ta≦40℃) . The maximum wet bulb temperature ≦39℃(Ta＞40℃) and without dewing.。

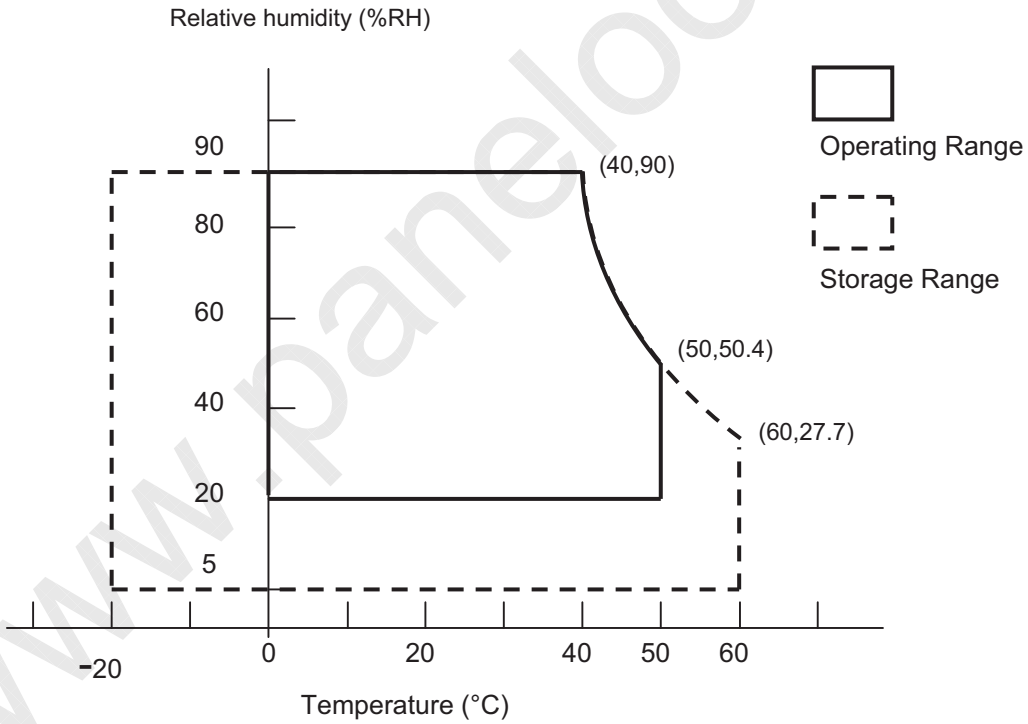
*3) If you use the product in a environment which over the definition of temperature and humidity too long to effect the result of eye-atching.。

*4) The life time of the lamp is relate to the current of the lamp, so please accronding to the description of the “(b) backlight” on page 5.

*5) Test Condition: IEC 1000-4-2 ,
VESDt：Contact discharge to input connector；$VESD_C$：Contact discharge to module

*6) When lamp current is out of the absolute maximum range，the life will fall rapidly or shown unusual sign.
IL min 2~3mA only for test only, but we can’t guarantee the lifetime and performance

*7) Delay lighting testing needs the volt above start volagte Vrms.Before the procedure，tube needs typical lighting for 1 minute and stay in the temperature 25±2℃ for 24 hours and then testing in the same condition in dark room .



3. ELECTRICAL CHARACTERISTICS

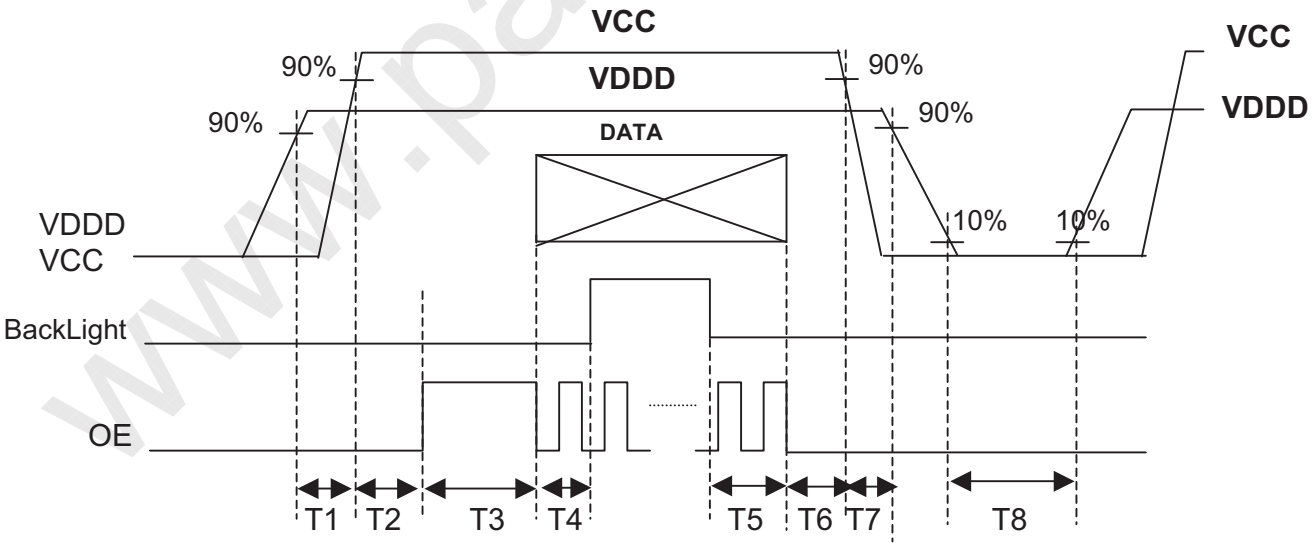
(a) **TFT-LCD** Ta=25℃

ITEM		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
Power Supply Voltage for LCD		VCC	10.8	12.0	13.2	V	*1) *2)
Power Supply Current for LCD		ICC	--	(200)	(350)	mA	*3)
Logic Input Voltage		VCRP	--	--	100	mVp-p	V=+12.0V
Logic Input Current		VDDD	3.0	3.3	3.6	V	*1) *2)
Power Supply Current for Logic		IDDD	--	(40)	(100)	mA	*3)
Permissive Ripple Voltage		VDRP	--	--	30	mVp-p	V=+3.3V
Differential impendence		Zm	90	100	110	Ω	--
Logic Input Voltage	High	VIH	2.5	3.3	3.6	V	--
	Low	VIL	0	--	0.8	V	--
LCD Inrush Current		Irush	--	--	3	A	*4)
Power consumption		P		2.6	4.6	W	*3)

*1) power source sequence
When the power on，OE needs time called “H”，and the correlation of OE and Vcc(12V) is shown as following.

0<T1、T5、T6、T7≦10ms
(6≦T2≦11ms);
(31≦T3≦36ms)
200ms≦T4
1 sec≦T8

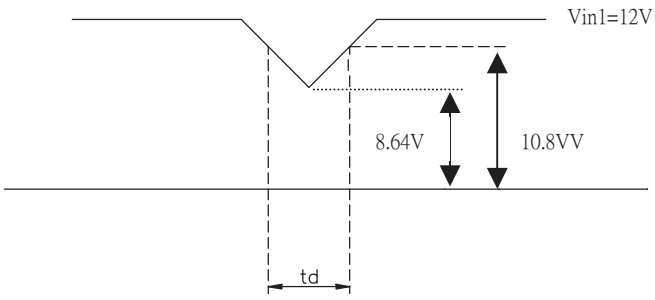
T1 propose value：1ms
T2 propose value：(7)ms
T3 propose value：(32)ms



*2) VCC VCC-dip conditions

(1) When 8.64 V＜VCC(min)＜10.8V，td≦10 ms

(2) When VCC＜10.8V，VCC-dip conditions should also follow the VCC-turn-on conditions.

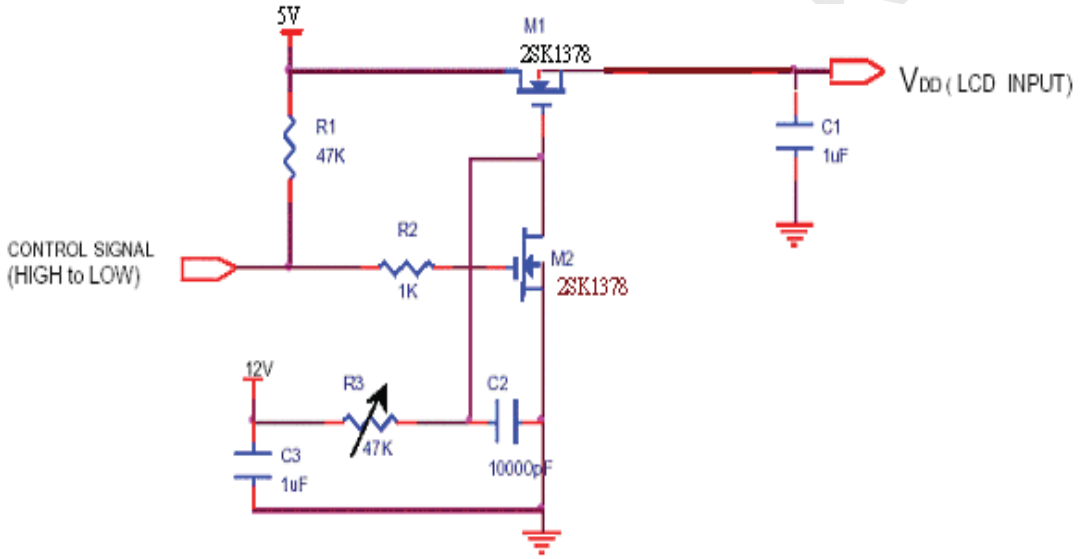


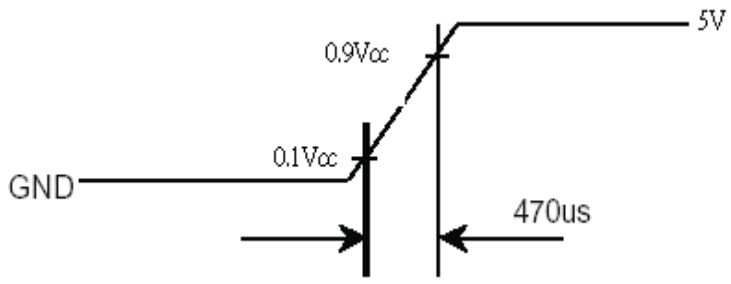
*3) Typical current situation (Typ.) 64 gray-bar pattern，1280 line mode，

VCC=12.0V，f_H=64kHz，fv=60Hz，f_{CLK}=54 MHz

VDDD=3.3V，f_H=64kHz，fv=60Hz，f_{CLK}=54 MHz

*4) Irush Measurement Condition





(b) **Backlight**

a. Electrical Characteristics

Ta=25℃

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	REMARK
Lamp Voltage	VL	603	670	737	Vrms	IL=7mA Ta=25℃
Lamp Current-standard	IL	6.5	7.0	7.5	mArms	*1) Ta=25℃
Lamp Current-operation	ILO	3.0	7.0	7.5	mArms	
Inverter Frequency	FI	45	50	65	kHz	*2)
Starting Lamp Voltage	VS			1710	Vrms	*3) Ta=0℃
				1490	Vrms	*3)Ta=25℃
Power consumtion	WL	—	18.8	20.7	W	*4) IL=7.0mA Ta=25℃

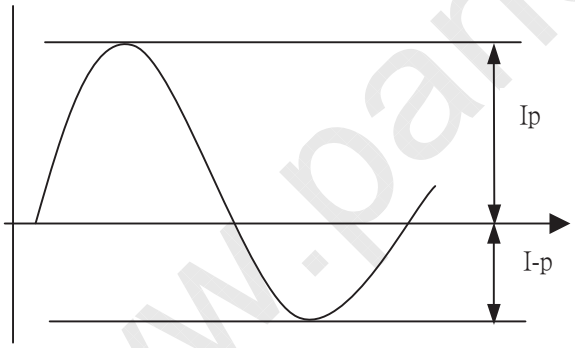
b. Lamp Life Time

ITEM	IL at 3.0 mA	IL at 7.0 mA	IL at 80.0 mA	UNIT	REMARK
Lamp Life Time (LT)	Min50，000	Min.40，000	Min.30，000	hr	Continuous Operation *5)
Turn-on and Turn-off Operation	--	Min.100，000	--	time	Test condition *6)

[Note] Measuring inverter Type：M063-4

If the waveform of light up-driving is asymmetric, the distribution of mercury inside the lamp tube will become unequally or will deplete the Ar gas in it. Then it may cause the abnormal phenomenon of lighting-up. Therefore, designers have to try their best to forfill the conditions under the inverter designing-stage as below:

- The degrees of unbalance： ＜10%
- The ratio of wave height：＜$\sqrt{2}$ ±10%



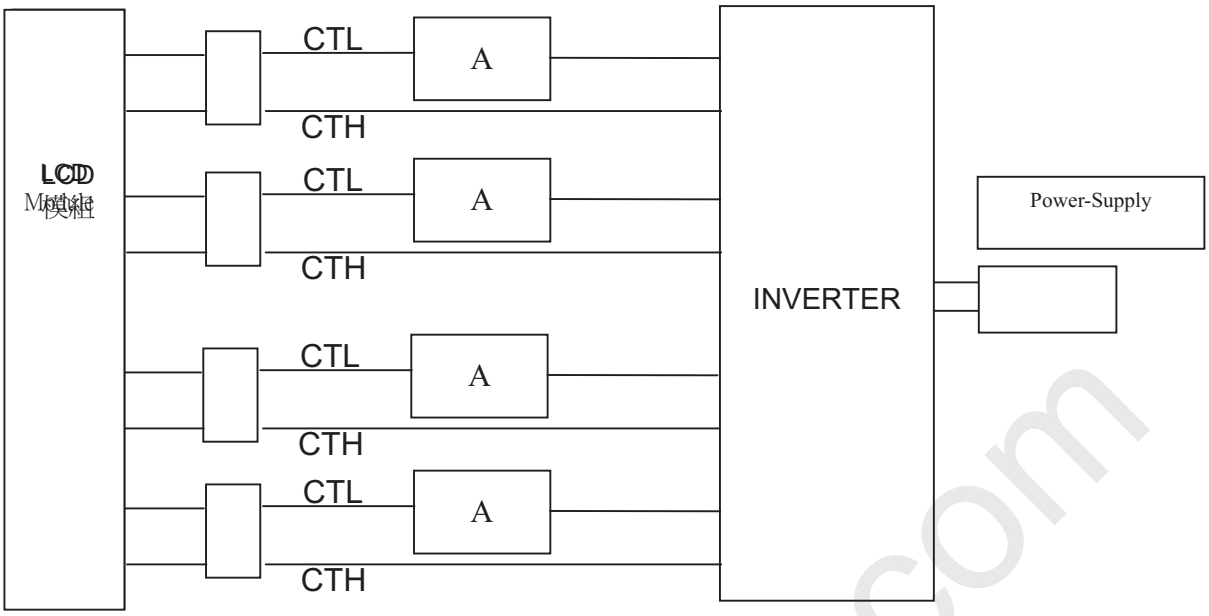
Ip：high side peak

I-p：low side peak

A：The degrees of unbalance = | Ip – I-p | / Irms ×100 (%)

B：The ratio of wave height = Ip (or I-p) / Irms

*1) Lamp Current measurement method (The current meter is inserted in cold line)



*2) 1.Frequency in this range can mala the characterisitics of electric and optics maintain in +/- 10% except hue.
2.If the lamp frequency can be maintain in 50~60KHz, the better charactristics of the electrical and the optical can be presented.
3.If the operating frequency is 40~80 KHz, the life time and the reliability of the lamp will not be affect.
4.Lamp frequency of inverter may produce interference with horizontal synchronous frequency,and this may cause horizontal beat on the display.Therefore, please adjust lamp frequency, and keep inverter as far from module as possible or use electronic shielding between inverter and module to avoid the interference.

*3) WL=IL x VL x 4

*4) It is necessary to consider the maximal value when design inverter，in order to asure lighting.

*5) Definition of the lamp life time： Luminance (L) under 50% of specification starting lamp voltage or starting lamp voltage is more than 130% of the initial value

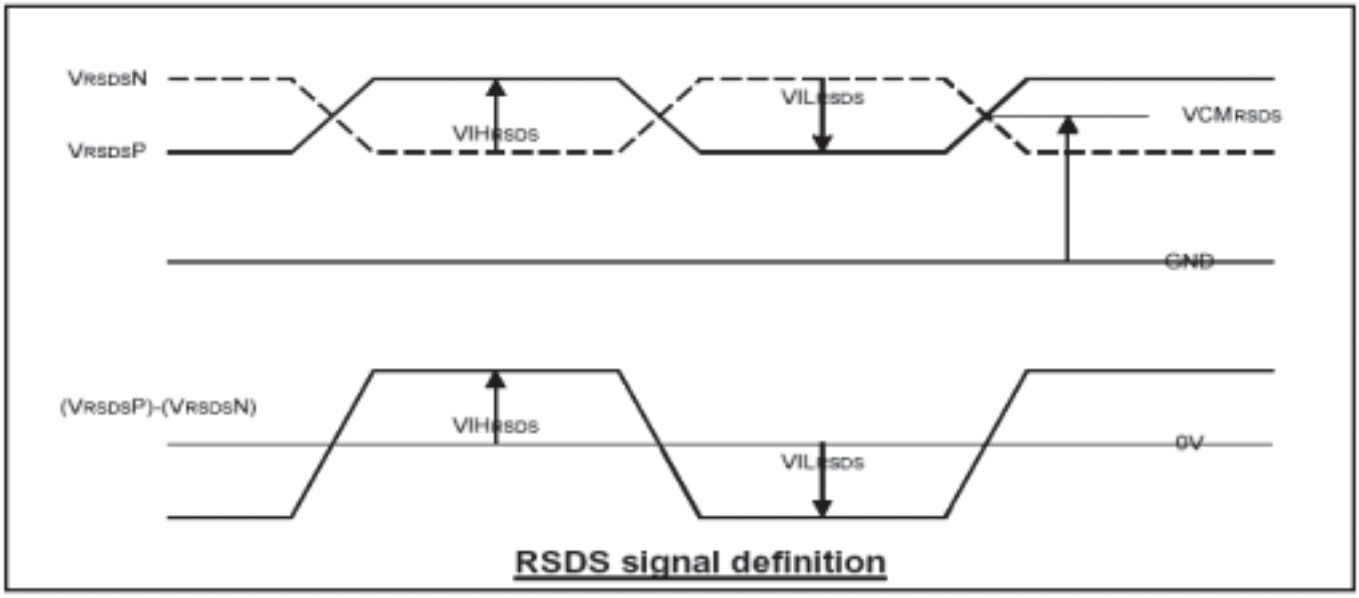
*6) The condition of Turn-on and Turn-off operation is as below:
a. Lamp current is 7.0mA
b. Frequency is 10 sec.(on)/10 sec.(off)
c. Repeat it for 10 thousand times
d. The result of eye-atching of the lamp hue is normal, and can switch the lamp.
It should not have motion fail when starting lamp voltage is lower than 130% of the initial value

(c) RSDS Characteristics

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
RSDS high input voltage	VIH_{RSDS}	100	200	--	mV	VCM_{RSDS}=+1.2V
RSDS Low input voltage	VIL_{RSDS}	--	-200	-100	mV	VCM_{RSDS}=+1.2V
RSDS Common mode input voltage range	VCM_{RSDS}(1)	0.5	--	1.4	V	$VDIFF_{RSDS}$(2)=200mV (minimum value)
RSDS Input leakage current	IDL	-10	--	10	uA	$D_{XX}P$, $D_{XX}N$, CLKP, CLKN

[Note]
(1) VCM_{RSDS}=(VCLKP+VCLKN)/2 or VCM_{RSDS}=($VD_{XX}P$ +$VD_{XX}N$)/2
(2) $VDIFF_{RSDS}$= VCLKP-VCLKN or $VDIFF_{RSDS}$= $VD_{XX}P$ -$VD_{XX}N$

Standard peak-to-peak voltage differential for RSDS is 400mV, from –200mV to +200mV.



RSDS signal definition

4. INTERFACE PIN CONNECTION

(1) CN1(Data signl and supply power)

Outlet connector：AF7301-N2G1Z(P-two) or equivalent

PIN NO.	Function	Function
1	GND	Ground
2	B2P_B	Blue differential data output pin
3	B2N_B	Blue differential data output pin
4	GND	Ground
5	B1P_B	Blue differential data output pin
6	B1N_B	Blue differential data output pin
7	GND	Ground
8	B0P_B	Blue differential data output pin
9	B0N_B	Blue differential data output pin
10	GND	Ground
11	G2P_B	green differential data output pin
12	G2N_B	green differential data output pin
13	GND	Ground
14	G1P_B	green differential data output pin
15	G1N_B	green differential data output pin
16	GND	Ground
17	G0P_B	green differential data output pin
18	G0N_B	green differential data output pin
19	GND	Ground
20	CLKP_B	Gate driver IC Clock output pin
21	CLKN_B	Gate driver IC Clock output pin
22	GND	Ground
23	R2P_B	red differential data output pin
24	R2N_B	red differential data output pin
25	GND	Ground
26	R1P_B	red differential data output pin
27	R1N_B	red differential data output pin
28	GND	Ground
29	R0P_B	red differential data output pin
30	R0N_B	red differential data output pin

(2) CN2

use connector：AF7301-N2G1Z (P-two) or equivalent

PIN NO.	symbol	function
1	GND	Ground
2	B2P_F	Blue differential data output pin
3	B2N_F	Blue differential data output pin
4	GND	Ground
5	B1P_F	Blue differential data output pin
6	B1N_F	Blue differential data output pin
7	GND	Ground
8	B0P_F	Blue differential data output pin
9	B0N_F	Blue differential data output pin
10	GND	Ground
11	G2P_F	green differential data output pin

12	G2N_F	green differential data output pin
13	GND	Ground
14	G1P_F	green differential data output pin
15	G1N_F	green differential data output pin
16	GND	Ground
17	G0P_F	green differential data output pin
18	G0N_F	green differential data output pin
19	GND	Ground
20	CLKP_F	Source Driver IC Clock output pin
21	CLKN_F	Source Driver IC Clock output pin
22	GND	Ground
23	R2P_F	red differential data output pin
24	R2N_F	red differential data output pin
25	GND	Ground
26	R1P_F	red differential data output pin
27	R1N_F	red differential data output pin
28	GND	Ground
29	R0P_F	red differential data output pin
30	R0N_F	red differential data output pin
31	GND	Ground
32	STH_F	Source Driver IC start pulse wave input pin
33	LP	Source Driver IC output pin
34	POL	Source Driver output polar data output pin
35	STH_B	Source Driver IC start pulse wave input pin
36	GND	Ground
37	CLKV	Gate Driver IC Clock output pin
38	STV	Gate Driver IC start pulse wave input pin
39	OE	Gate Driver enable output pin
40	VCOM(test)	Common voltage (test use)
41	GND	Ground
42	3.3V	Logic power voltage
43	3.3V	Logic power voltage
44	12V	LCD power voltage
45	GND	Ground
46	12V	LCD power voltage
47	12V	LCD power voltage
48	12V	LCD power voltage
49	NC	NC
50	NC	NC

(3)CN3，4，5，6(Backlight)
Backlight-side connecto:BHSR-02VS-1(JST)
Inverter-side connecto:SM02(4.0)B-BHS-1-TB(JST)

Pin NO.	symbol	function
1	CTH	Power for CCFL
2	CTL	Power return for CCFL

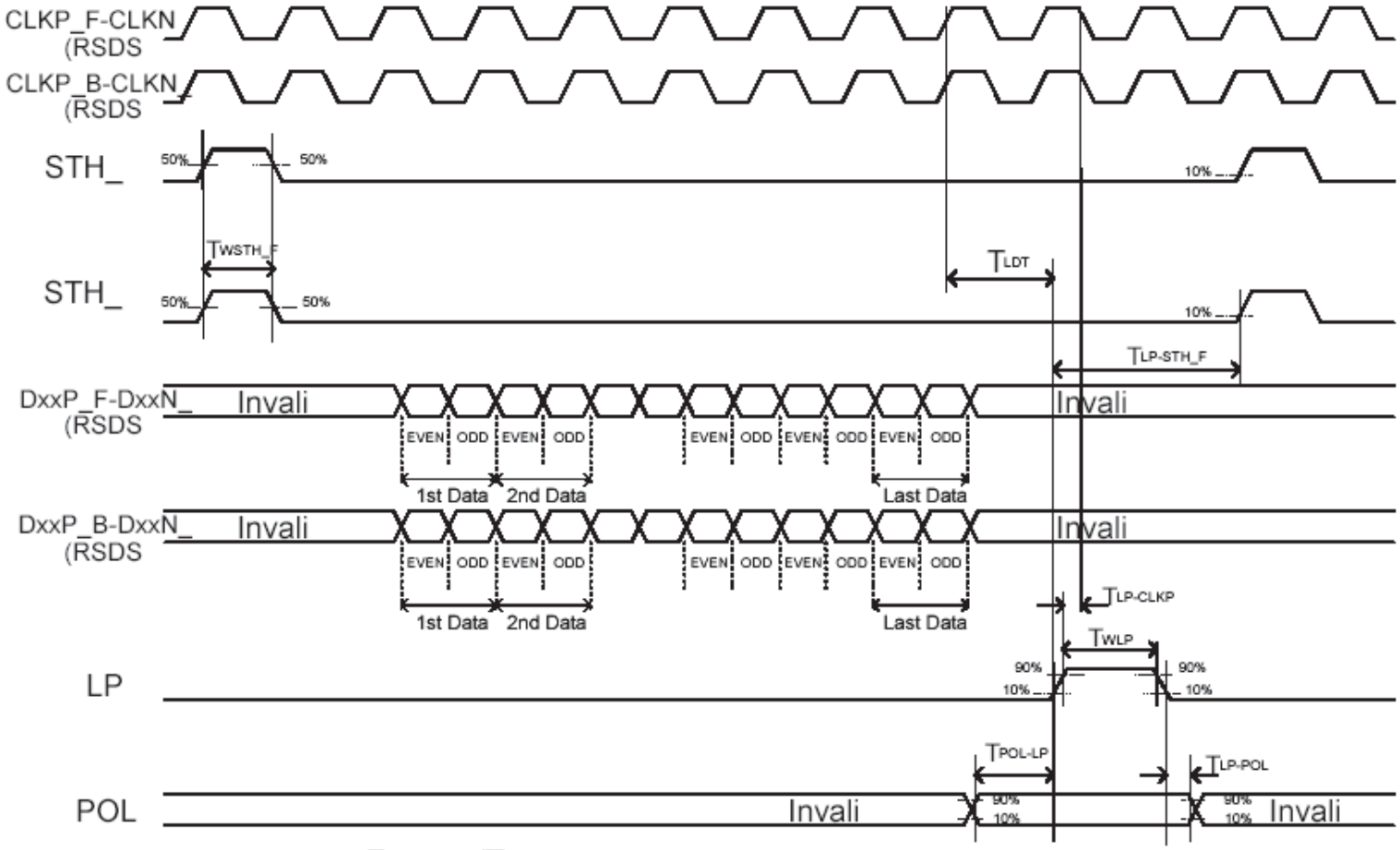
5. INPUT TIMING SIGNAL

(1)Timing specifications

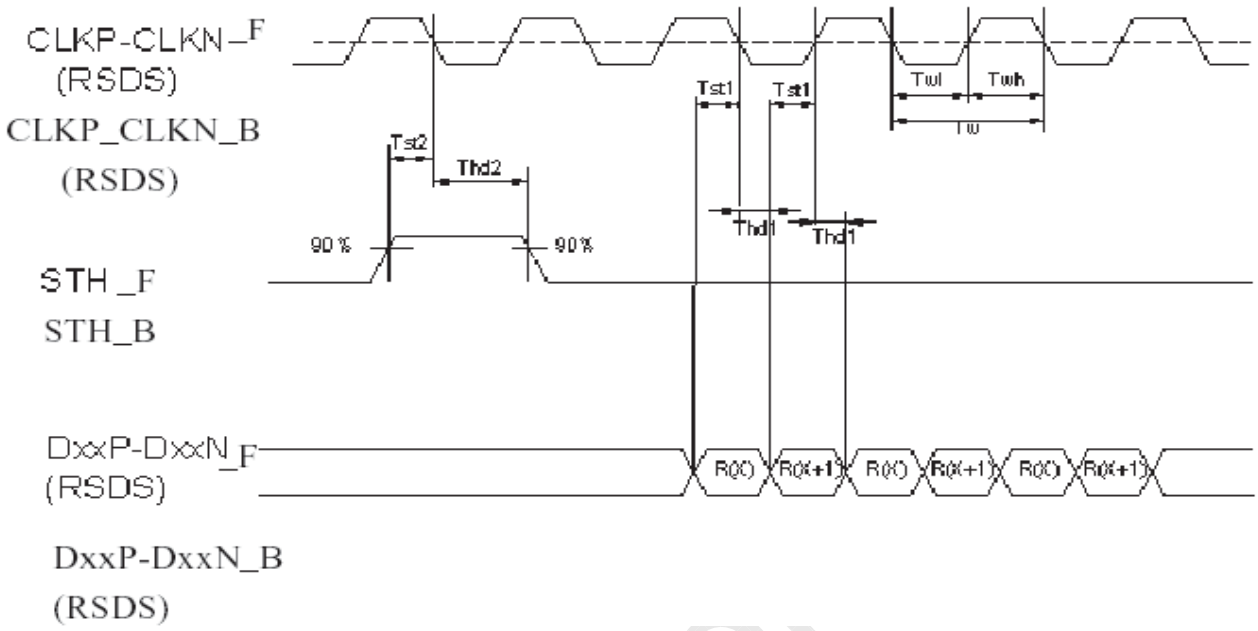
ITEM			SYMBOL	MIN	TYP	MAX	UNIT
LCD Timing	DCLK	Frequency	f_{CLK}	41.6	54	67.5	MHz
		Period	t_{CLK}	14.8	18.5	24	ns

(2) Horizontal timing

(a)Timing Diagram 1



(b) Timing Diagram 2



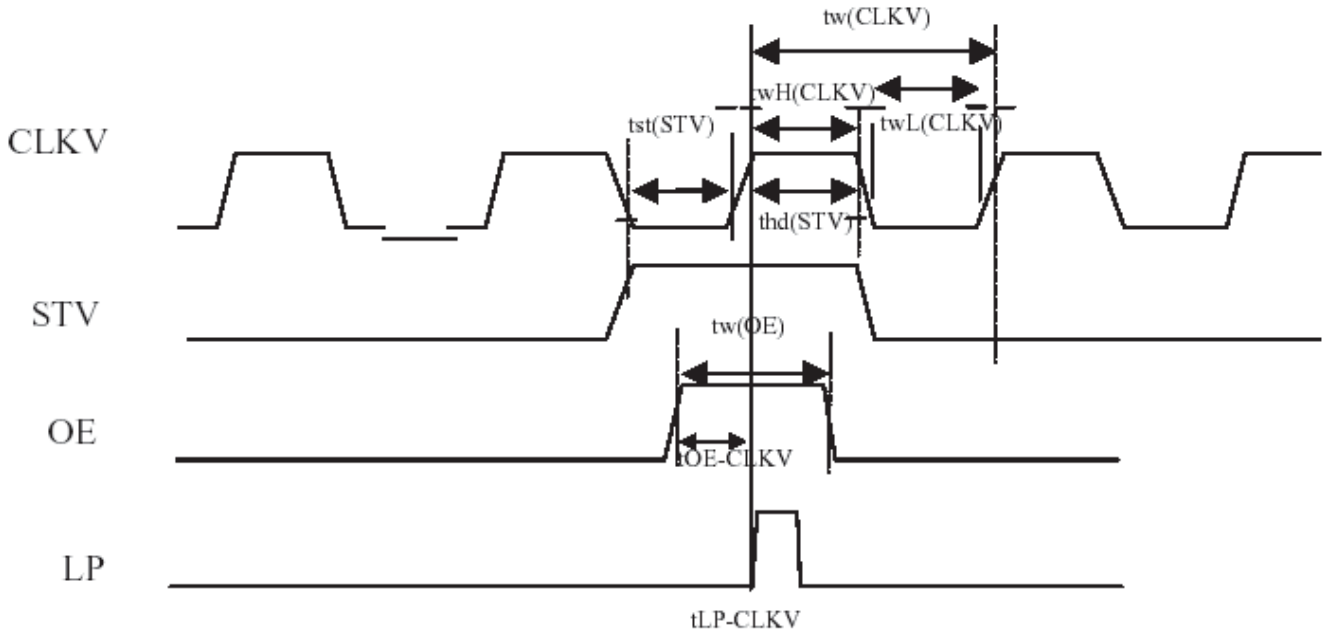
(c) Timing characteristic

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
CLK pulse width	Tw	14	18.5	24	ns
CLK pulse width (H)	Twh	6	--	--	ns
CLK pulse width (L)	Twl	6	--	--	ns
STV set-up time	tst (STV)	1	--	--	μs
STH set-up time	Tst2	4	--	--	ns
STH hold time	Thd2	4	--	--	ns
STH pulse width	Twsth	1	1	2	CLKP period
LP pulse width (H)	Twlp	(48)	--	(53)	CLKP period
LP to STH setup time	Tlp-sth1	7	--	--	CLKP period
Last data time	Tldt	1	--	--	CLKP period
CLK-LP time	Tclk-lp	4	--	--	ns
POL-LP time	Ypol-lp	(7)	--	(30)	CLKP period
LP-POL time	Tlp-pol	(640)	--	(784)	CLKP period

[note] After CPT testing，the hypothetical number did not show any unusual value；however，customers，usage will possibally change the value.

(3) Vertical timing

(a) Vertical timing diagram



[Note]：The start signal of STV and CLKV are $V_{OL(MAX)}$＝80% and $V_{OH(MIN)}$＝20%

(b) Vertical Timing characteristic

ITEM	SYMBOL	SPECIFICATIONS			UNIT
		MIN	TYP	MAX	
STV set-up time	tst (STV)	1	--	--	μs
STV hold time	thd (STV)	1	--	--	μs
CLKV periodc	tw (CLKV)	8	--	--	μs
CLKV High width	twH (CLKV)	3.5	--	--	μs
CLKV Low width	twL (CLKV)	3.5	--	--	μs
OE width	Tw (OE)	2.4	2.9	3.4	μs
OE-CLKV time	tOE-CLKV	1.5	2	3	μs
LP rise-CLKV time	tLP-CLKV	0	0	0	ns

(4) CLKV, LP and POL signal are alternate:

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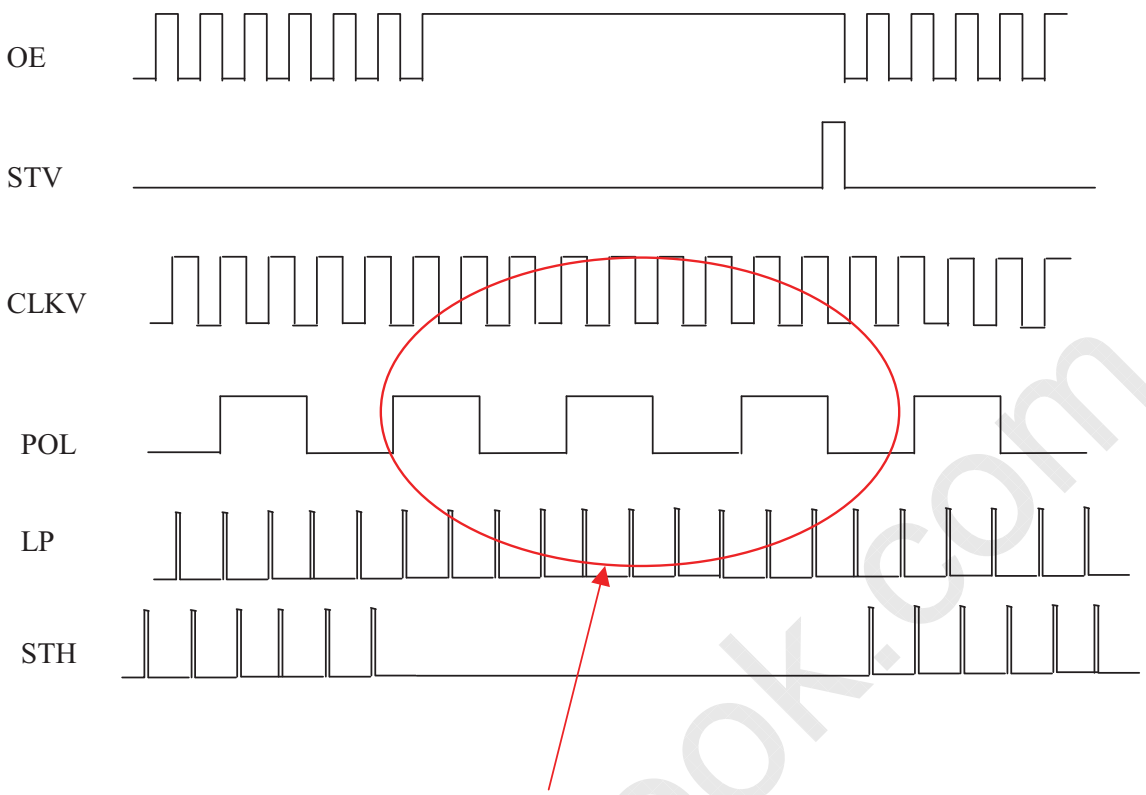


STH toggle 1024 times. LP, POL and CLKV in V-blank time have to continued toggle.
OE signal inV-blank time don't toggle

(4) Color Data Assignment

Color	Input Data	R DATA						G DATA						B DATA					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
		MSB					LSB	MSB					LSB	MSB					LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green (0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Green (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Blue (0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

[Note]

(1) Definition of gray scale:

Color (n): n indicates gray scale level; higher n means brighter level.

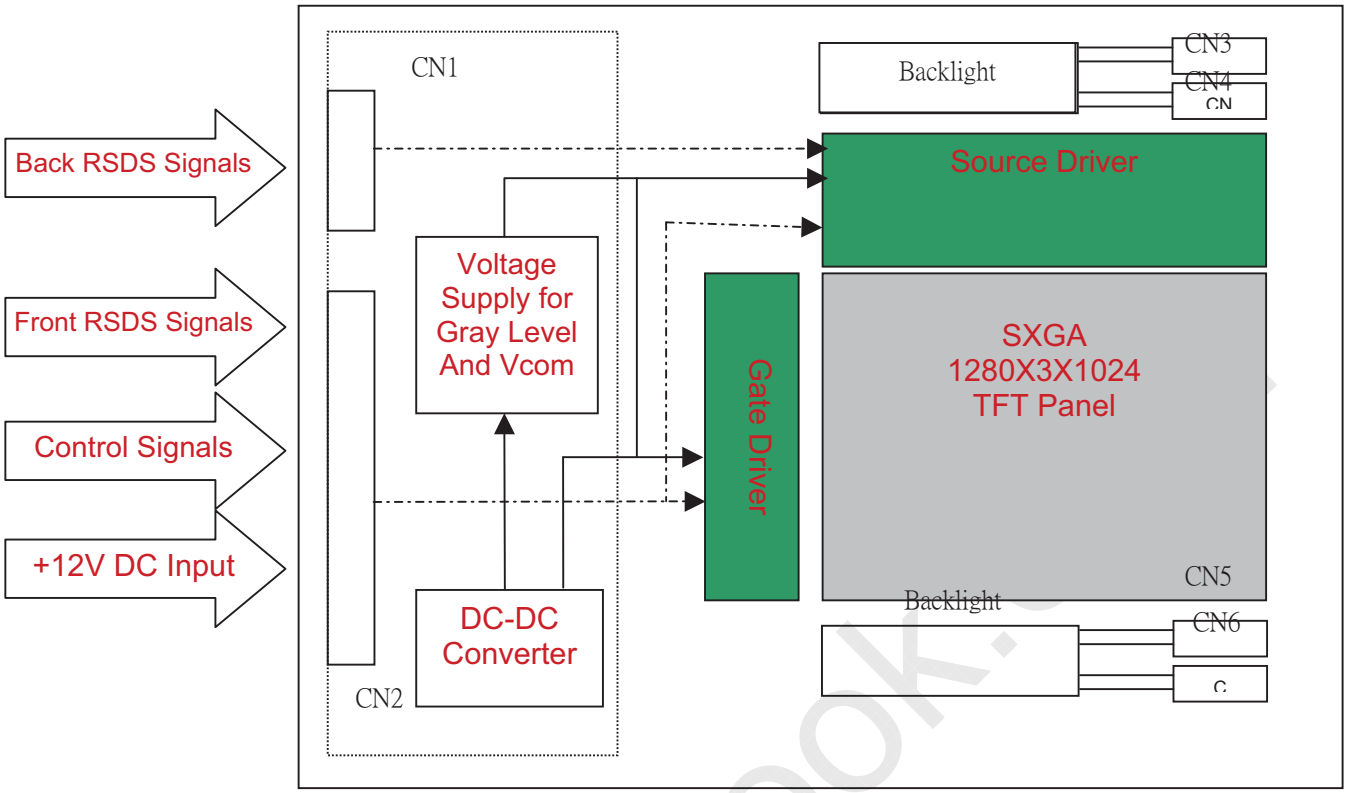
(2) Data: 1-High, 0-Low.

(5) Color Data Assignment

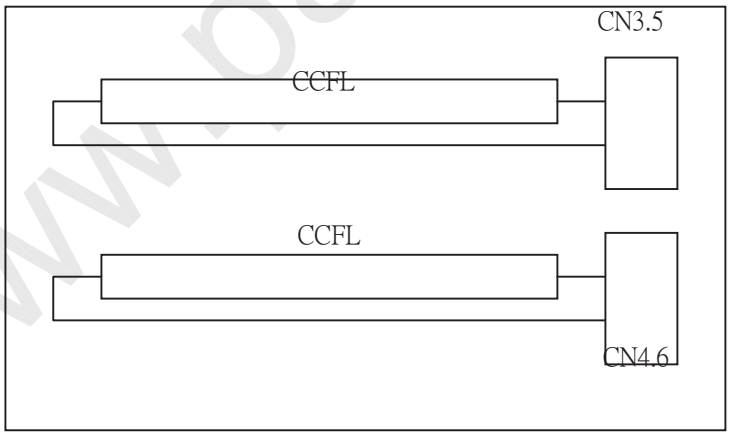
D(1,1)	D(2,1)	--	D(X,1)	--	D(1279,1)	D(1280,1)
D(1,2)	D(2,2)	--	D(X,2)	--	D(1279,2)	D(1280,2)
|--	|--	+	..	+	|--	|--
D(1,Y)	D(2,Y)	--	D(X,Y)	--	D(1279,Y)	D(1280,Y)
--|	|--	+	..	+	--|	|--
D(1,1023)	D(2, 1023)	--	D(X, 1023)	--	D(1279,1023)	D(1280,1023)
D(1,1024)	D(2, 1024)	--	D(X, 1024)	--	D(1279,1024)	D(1280,1024)

TFT-LCD Module

6. BLOCK DIAGRAM

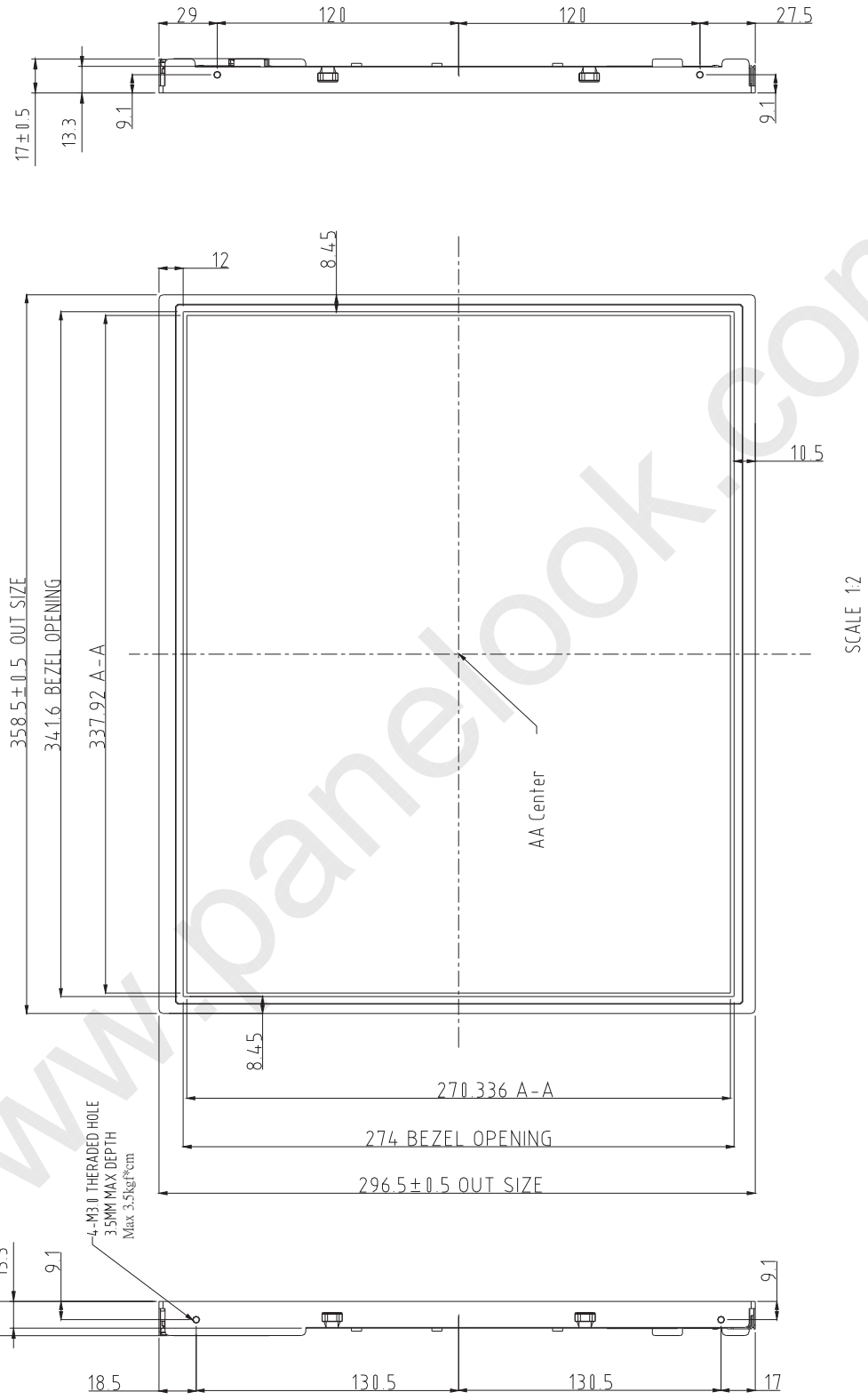


Lamp Unit in Backlight

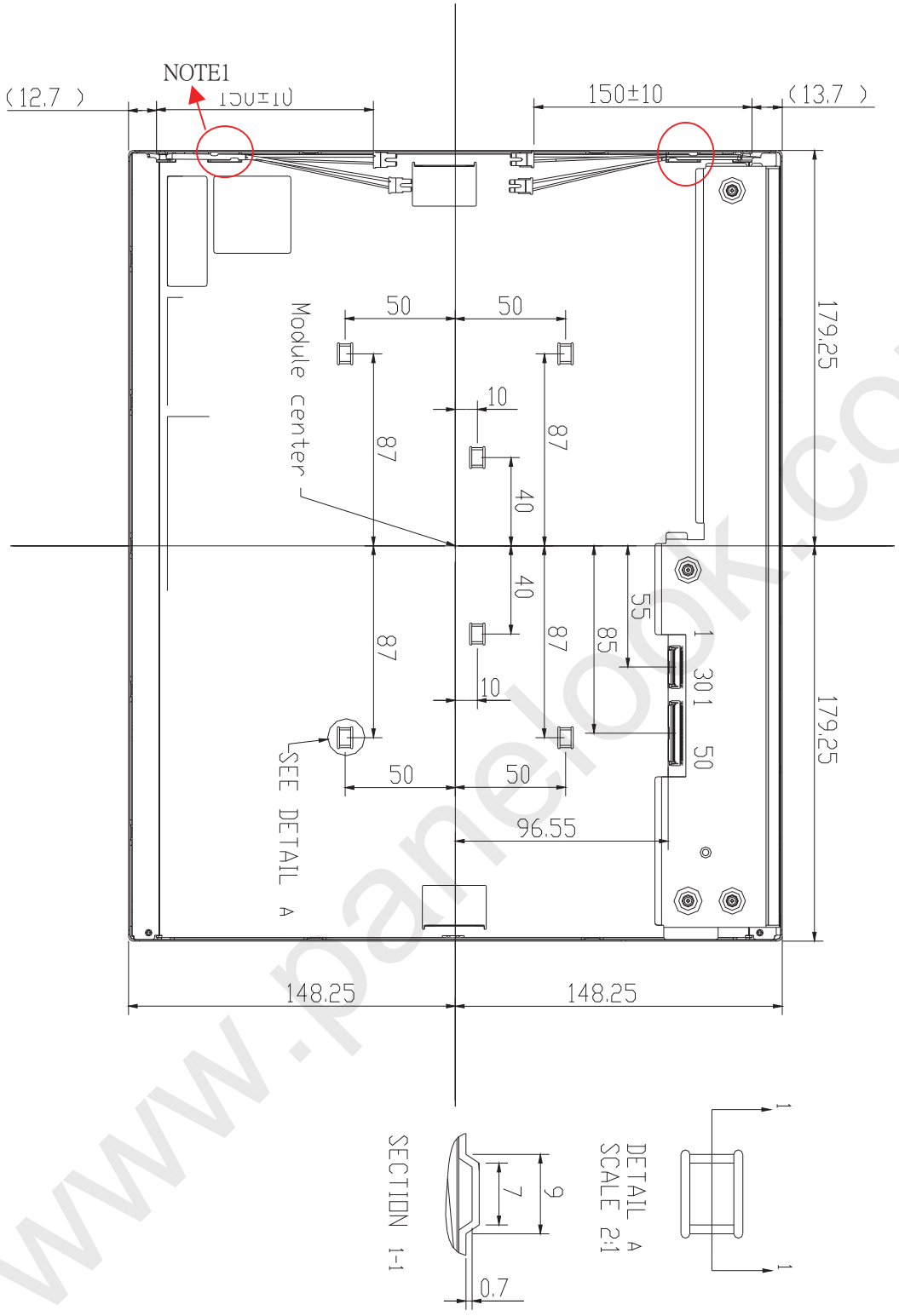


7. MECHANICAL SPECIFICATION

(1) Front side (Tolerance is ± 0.5mm unless noted) [Unit: mm]



(2) Rear side (Tolerance is ±0.5mm unless noted) [Unit: mm]



Note1: Suggestion: don' release the lamp wire hook for protect lamp solder and lamp wire

8.OPTICAL CHARACTERISTICS

Ta=25℃，VCC=5.0V

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Contrast Ratio		CR	θ= ϕ= 0°	450	500	--	--
Luminance	Center	L	θ= ϕ= 0°	250	300	--	cd/m^2
	Uniformity	ΔL	θ= ϕ= 0°	75%	--	--	
Response Time		Tr	θ= ϕ= 0°	--	(2)	(4)	ms
		Tf	θ= ϕ= 0°	--	(6)	(10)	ms
Viewing Angle	Horizontal	ϕ	CR≧5	80/80	85/85	--	°
	Vertical	θ		75/75	85/85	--	°
	Horizontal	ϕ	CR≧10	65/65	70/70	--	°
	Vertical	θ		60/50	67/63	--	°
Color Coordinates	White	Wx Wy	θ= ϕ= 0°	0.283 0.299	0.313 0.329	0.343 0.359	--
	Red	Rx Ry		0.625 0.297	0.655 0.327	0.685 0.357	
	Green	Gx Gy		0.243 0.587	0.273 0.617	0.303 0.647	
	Blue	Bx By		0.114 0.049	0.144 0.079	0.174 0.109	
Image sticking		Tis	2 hour			2	sec
Crosstalk		CT				1.5 %	
Gamut		CS		70%	72%		
Gamma		y	VESA	2.0	2.2	2.4	

All optical specification condition:

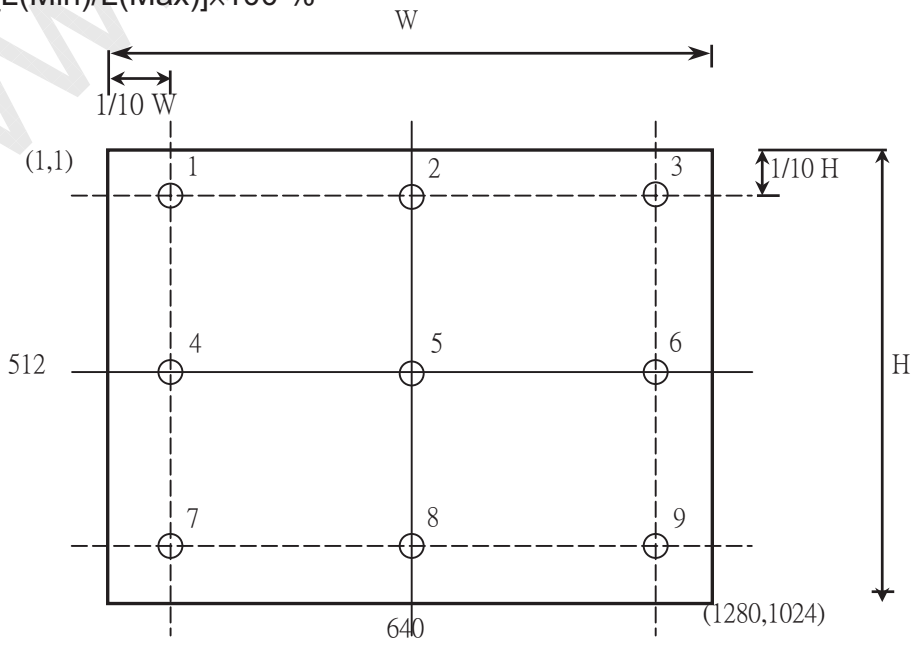
(1) Equipment: CS-1000 (MINOLUTA) OR BM-5A(TOPCON) under the dark room condition(no ambient light) after more than 30 minutes turning on the lamp

(2) Condition: IL=7.0(each lamp) mA, Inverter: Multipal (M063-4), Frequency=50kHz.

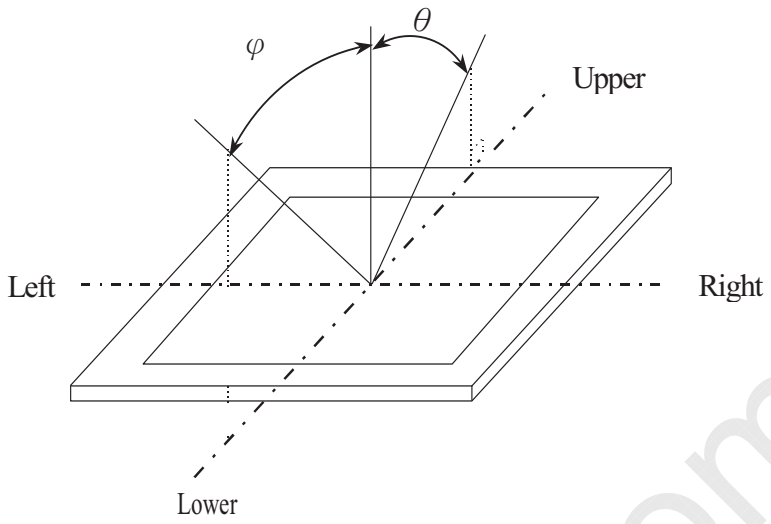
[Note 1] Defination of Contrast Ratio： CR=ON(White)Luminance/OFF(Black)Luminance

[Note 2] Defination of Luminance and Luminance uniformity

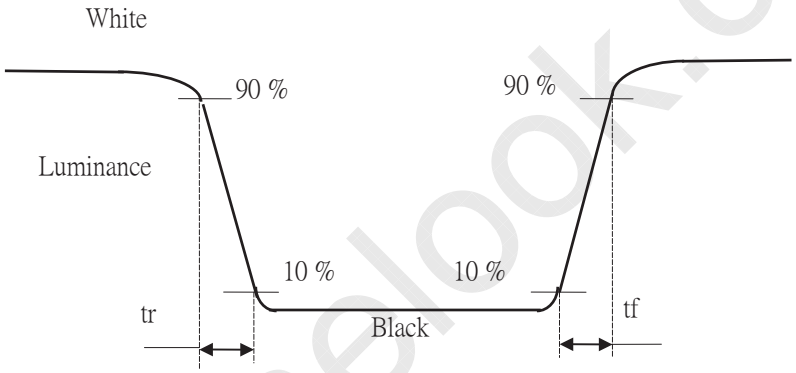
ΔL=[L(Min)/L(Max)]×100 %



[Note 3] Definition of Viewing Angle(θ , ϕ)

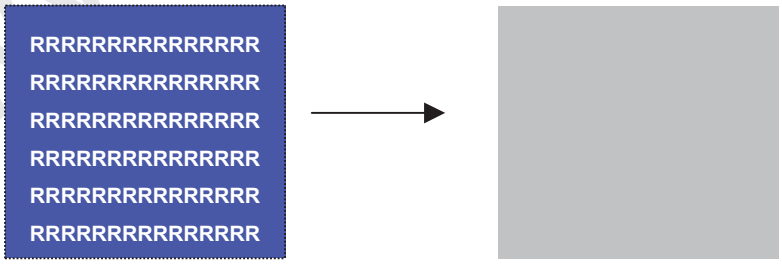


[Note 4] Definition of Response Time



[Note 5] Definition of image sticking:

From Continuous display pattern (white “R” with blue background) 2hours change to 128 gray level pattern .The previous image shall not persist more then 2 second at 25 C.

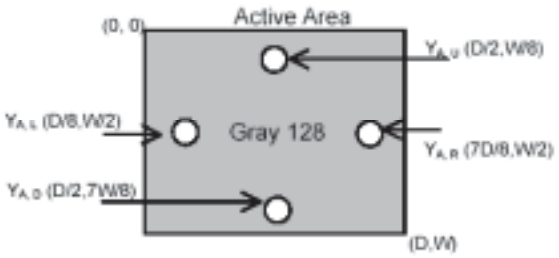


[Note 6] Defination of crosstalk

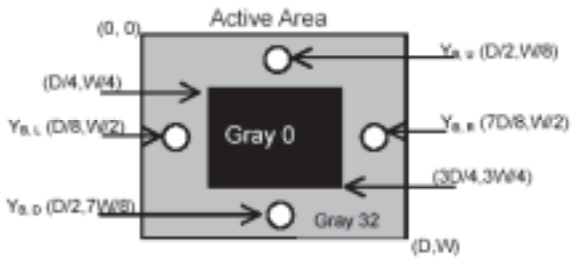
$CT = |Y_B - Y_A| / Y_A \times 100\ (\%)$

Y_A: The luminance of measured position at pattern A

Y_B: The luminance of measured position at pattern B with gary level 0

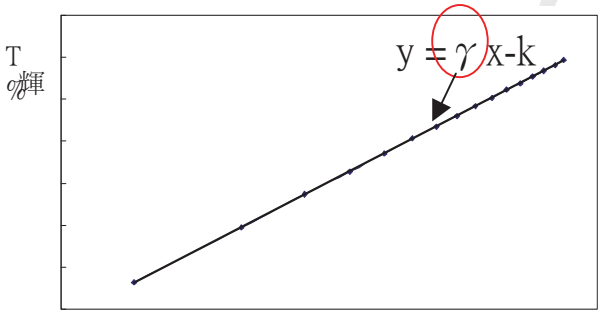


Pattern A



Pattern B

[Note7] Defination of Gamma (γ) , follow VESA standard sampling evary 16 gray level(0,16,32,…..224,240,255)



9. RELIABILITY TEST CONDITIONS

(1) Temperature and Humidity

TEST ITEMS	CONDITIONS
High Temperature Operation	50℃; 240 hour
High Temperature Storage	60℃; 240h
High Temperature High Humidity Operation	50℃; 95%RH; 240 hour(No condensation)
High Temperature High Humidity Storage	60℃; 90%RH;48 hour(No condensation)
Low Temperature Operation	0℃; 240h
Low Temperature Storage	-20℃; 240 hour
Thermal Shock	-20℃(1hr)~ 60℃(1hr); 100 CYCLES

(2) Shock & Vibration

ITEMS	CONDITIONS
Shock (Non-Operation)	Shock level:1470m/s^2(150G) Waveform: half sinusoidal wave, 2ms Number of shocks: one shock input in each direction of three mutually perpendicular axes for a total of six shock inputs
Vibration (Non-Operation)	Vibration level: 9.8m/s^2(1.0G) zero to peak Waveform: sinusoidal Frequency range: 5 to 500 Hz Frequency sweep rate: 0.5 octave/min Duration: one sweep from 5 to 500Hz in each of three mutually perpendicular axis(each x,y,z axis: 1 hour, total 3 hours)

(3) ESD test

TEST ITEM	TEST STATEMENTS
Connector	Test condition:200 pF，0 Ω，±250 V By using contact-mode to discharge each pin one time and then check the module frame.
Module	Test condition:150 pF，330 Ω，±15KV 1.Under test conditions, by using air-mode to discharge each test point 25 times continueously and then check the module frame. 2. Under test conditions, by using contact-mode to discharge each test point of panel frame 25 times continueously and then check the module frame.

(4) **Low Presure test**

TEST ITEM	CONDITION
Low Presure test(storage)	260HPa (30000 ft.)；24 Hr

(5) Judgment standard

The judgment of the above test should be made as follow:

Pass: Normal display image with no obvious non-uniformity and no line defect.
Partial transformation of the module parts should be ignored.

Fail: No display image, obvious non-uniformity, or line defects.

10. HANDLING PRECAUTIONS FOR TFT-LCD MODULE

Please pay attention to the followings in handling- TFT-LCD products;

10.1 ASSEMBLY PRECAUTION

(1) Please use the mounting hole on the module side in installing and do not beading or wrenching LCD in assembling. And please do not drop, bend or twist LCD module in handling.

(2) Please design display housing in accordance with the following guide lines.

- Housing case must be destined carefully so as not to put stresses on LCD all sides and not to wrench module. The stresses may cause non-uniformity even if there is no non-uniformity statically.
- Keep sufficient clearance between LCD module back surface and housing when the LCD module is mounted. Approximately 1.0 mm of the clearance in the design is recommended taking into account the tolerance of LCD module thickness and mounting structure height on the housing.
- When some parts, such as, FPC cable and ferrite plate, are installed underneath the LCD module, still sufficient clearance is required, such as 0.5mm. This clearance is, especially, to be reconsidered when the additional parts are implemented for EMI countermeasure.
- Design the inverter location and connector position carefully so as not to give stress to lamp cable, or not to interface the LCD module by the lamp cable.
- Keep sufficient clearance between LCD module and the others parts, such as inverter and speaker so as not to interface the LCD module. Approximately 1.0mm of the clearance in the design is recommended.

(3) Please do not push or scratch LCD panel surface with any-thing hard. And do not soil LCD panel surface by touching with bare hands. (Polarizer film, surface of LCD panel is easy to be flawed.)

(4) Please do not press any parts on the rear side such as source TCP, gate TCP, control circuit board and FPCs during handling LCD module. If pressing rear part is unavoidable, handle the LCD module with care not to damage them.

(5) Please wipe out LCD panel surface with absorbent cotton or soft cloth in case of it being soiled.

(6) Please wipe out drops of adhesives like saliva and water on LCD panel surface immediately. They might damage to cause panel surface variation and color change.

(7) Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.

(8) Please do not touch metal frames with bare hands and soiled gloves. A color change of the metal frames can happen during a long preservation of soiled LCD modules.

(9) Please pay attention to handling lead wire of backlight so that it is not tugged in connecting with inverter.

2. OPERATING PRECAUTIONS

(1) Please be sure to turn off the power supply before connecting and disconnecting signal input cable.

(2) Please do not change variable resistance settings in LCD module. They are adjusted to the most suitable value. If they are changed, it might happen LCD does not satisfy the characteristics specification.

(3) Please consider that LCD backlight takes longer time to become stable of radiation characteristics in low temperature than in room temperature.

(4) A condensation might happen on the surface and inside of LCD module in case of sudden change of ambient temperature.

(5) Please pay attention to displaying the same pattern for very long time. Image might stick on LCD. If then, time going on can make LCD work well.

(6) Please obey the same caution descriptions as ones that need to pay attention to ordinary electronic parts.

3. PRECAUTIONS WITH ELECTROSTATICS

(1) This LCD module use CMOS-IC on circuit board and TFT-LCD panel, and so it is easy to be affected by electrostatics. Please be careful with electrostatics by the way of your body connecting to the ground and so on.

(1)Please remove protection film very slowly on the surface of LCD module to prevent from electrostatics occurrence.

4. STORAGE PRECAUTIONS

(1) When you store LCDs for a long time, it is recommended to keep the temperature between 0℃ ~40℃ without the exposure of sunlight and to keep the humidity less than 90%RH.

(2) Please do not leave the LCDs in the environment of high humidity and high temperature such as 60℃ 90%RH.

(3) Please do not leave the LCDs in the environment of low temperature; below -20℃.

5. SAFETY PRECAUTIONS

(1) When you waste LCDs, it is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.

(2)If any liquid leaks out of a damaged-glass cell and comes in contact with the hands, wash off throughly with soap and water.

6. OTHERS

(1) A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight Land strong UV rays.

(2) Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.

(3) For the packaging box, please pay attention to the followings:

- Packaging box and inner case for LCD are designed to protect the LCDs from the damage or scratching during transportation. Please do not open except picking LCDs up from the box.
- Please do not pile them up more than 3 boxes. (They are not designed so.) And please do not turn over.
- Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
- Packing box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)