Chunghwa Picture Tubes, Ltd.
Product Tentative Specification

To :
Date :

TFT LCD

CLAF050LG41 TXX

ACCEPTED BY :

Tentative V2.0

APPROVED BY	CHECKED BY	PREPARED BY

Prepared by :

Small &Medium Product Planning Management Department

Small &Medium Product General Division

CHUNGHWA PICTUER TUBES, LTD.

1127 Hopin Rd., Padeh, Taoyuan, Taiwan 334, R.O.C.
TEL: +886-3-3675151 FAX: +886-3-377-3001

REVISION STATUS

Revision Notice	Description	Page	Rev. Date
0.0	First revision (Tentative)	---	2013.04.02
0.0	FPC Pin Assignment	12	2013.04.02
1.0	Modify Outline Dimension	6	2013.06.05
1.0	Remove Polarizer Information	26	2013.06.05
2.0	Add IC-> ILI9807		2014.02.19

Contents

1. OVERVIEW

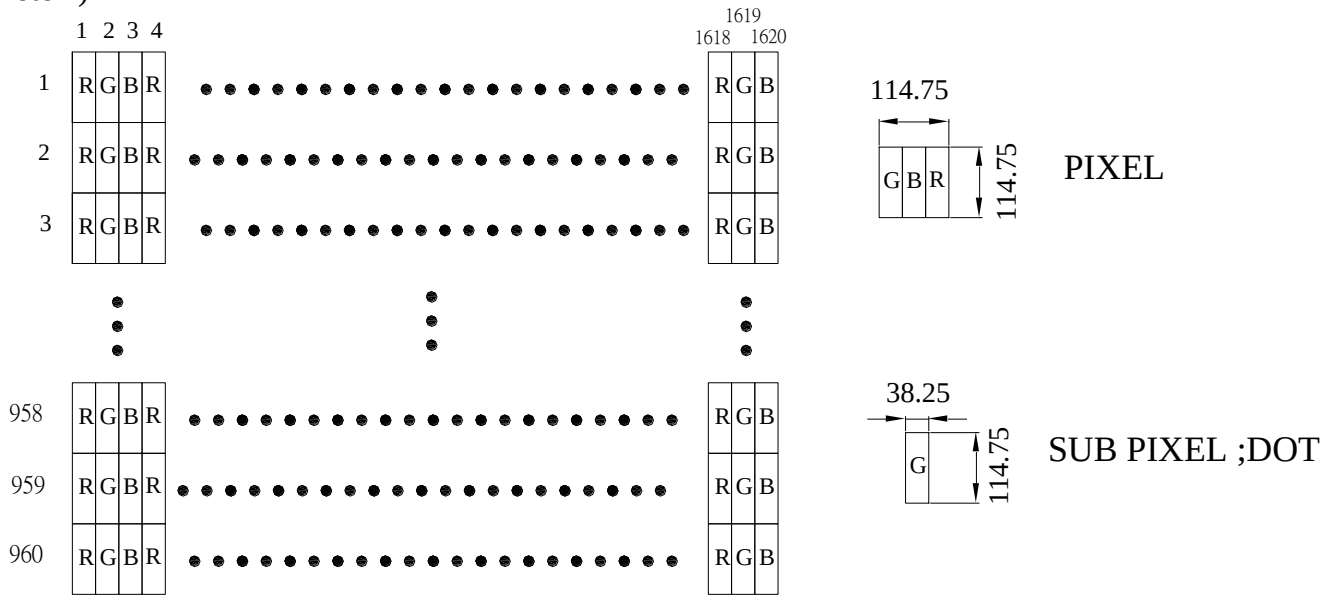
CPT CLAF050LG41 is a full cell (or ODF Full cell) product of TFT-LCD substrate with optimum arrangement provides up to 70 pieces of 9:16 aspect ratio panels for the high end PND or PDVD application.

The 5” screen produces a high resolution image that is composed of 518,400 (540×960) pixel elements in a delta arrangement.

General specifications are summarized in the following table:

ITEM	SPECIFICATION
Panel Size	5" inch
Display Area (mm)	61.965 (H) x 110.16 (V)
CF glass dimension	64.87 (H) x 114.31 (V) x 0.2(Thickness)
TFT glass dimension	64.87 (H) x 118.31 (V) x 0.2(Thickness)
Number of Pixels	540x3(H) x 960(V)
Pixel Pitch (mm)	0.11475(H) x 0.11475(V)
Color Pixel Arrangement	RGB stripe type
Display Mode	normally black
NTSC	70%
Driving Method	TFT active matrix
Viewing Direction	85/85/85/85

LCD Cell Drawing
(Note 1)



The LCD Products listed on this document are not suitable for use of aerospace equipment, submarine cables, nuclear reactor control system and life support systems. If customers intend to use these LCD products for above application or not listed in "Standard" as follows, please contact our sales people in advance.

2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remark
Operating Ambient Temperature	T_{OP}	-20	+70	˚C	
Operating Ambient Humidity	H_{OP}	10	90	% (RH)	
Storage Temperature	T_{STG}	-30	+80	˚C	
Storage Humidity	H_{STG}	10	90	% (RH)	

Note 1. The absolute maximum ratings are the values that must not be exceeded at any time for this product. It is not allowed for any of these ratings to be exceeded. Should a product be used with any of the absolute maximum ratings exceeded, the characteristics of the product may not be recovered, or in an extreme case, the product may be permanently destroyed.

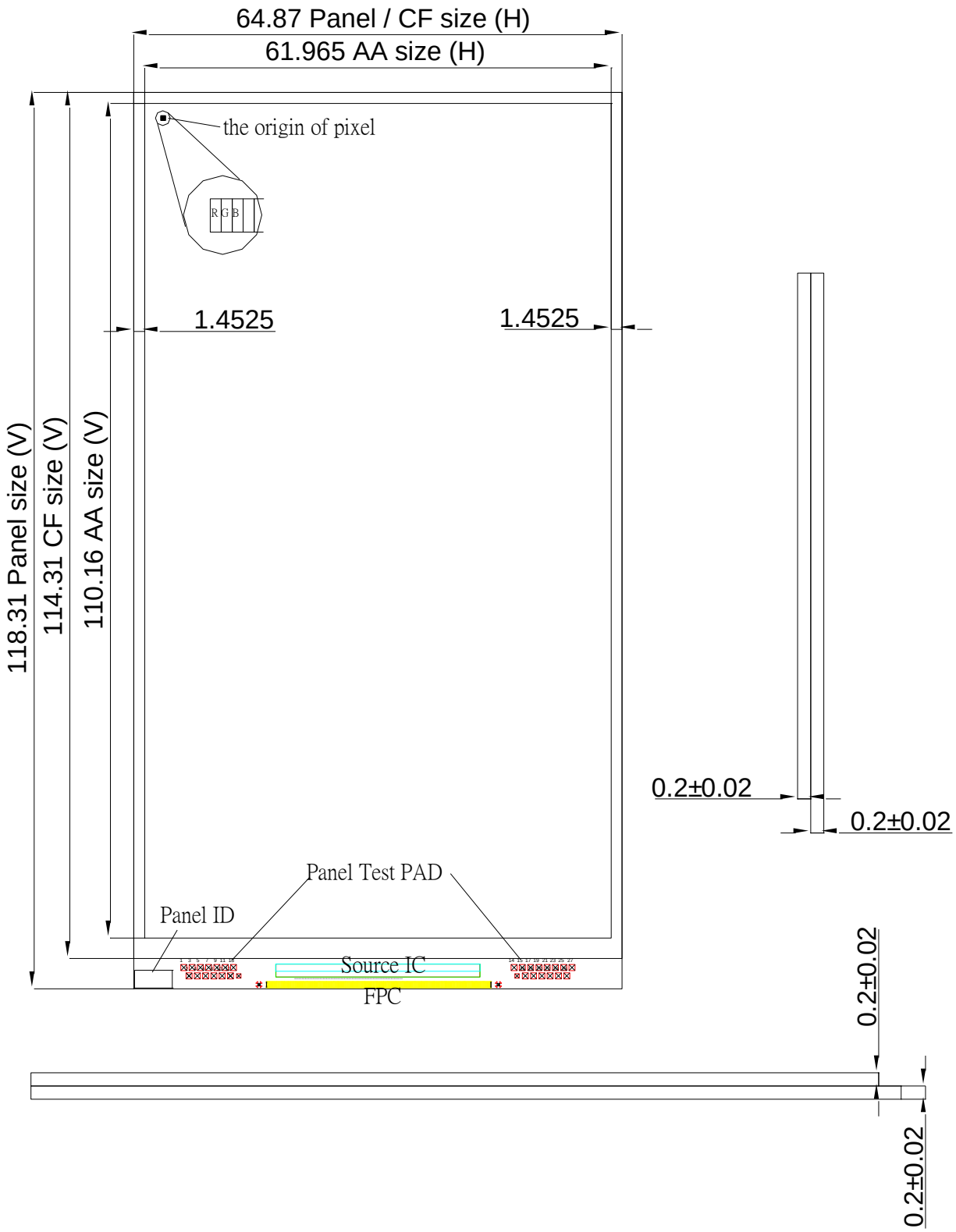
Therefore, when desigining a system incorporating the product, make sure that adequate attentions be paid to the variations in the supply voltages, the characteristics of parts that are connected, surges in the input and output lines, and the ambient temperatures.

Note 2. This specification applys after the driver IC mounting and the FPC mounting. (This specification isn't applicable at time of driver IC un-mounting and FPC un-mounting.)

LCD should keep the condition that dew dosen't storage in case of driver IC un-mounting and FPC un-mounting. Dew may break the LCD. Especially part is very weak for dew.

3. MECHANICAL SPECIFICATIONS

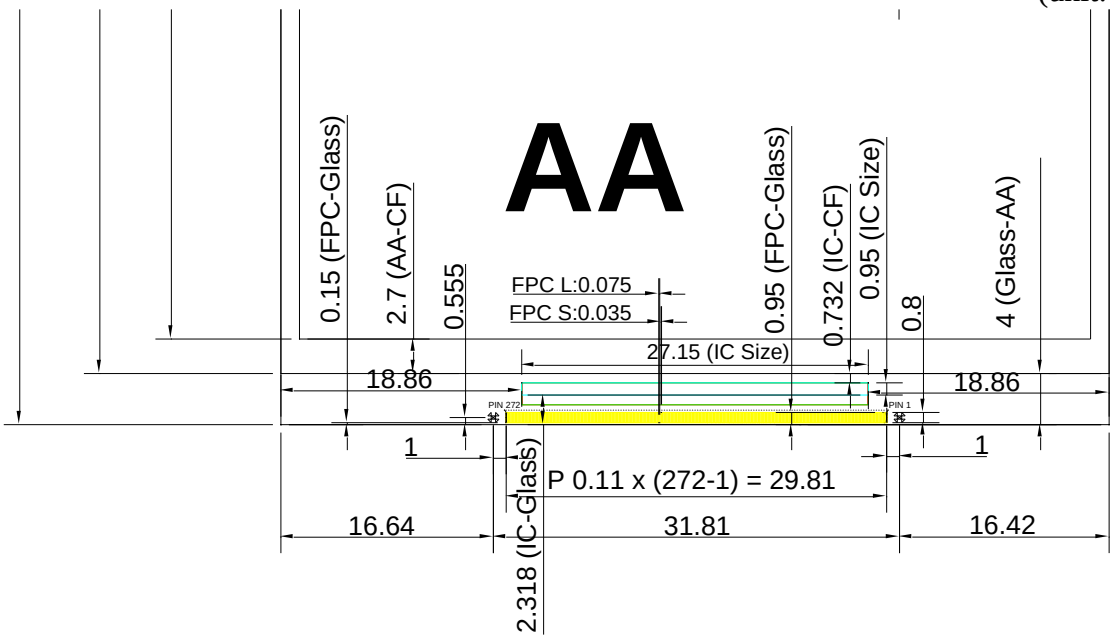
3.1 Outline Dimension



(unit: mm)

3.2 IC & FPC Pads

(unit: mm)

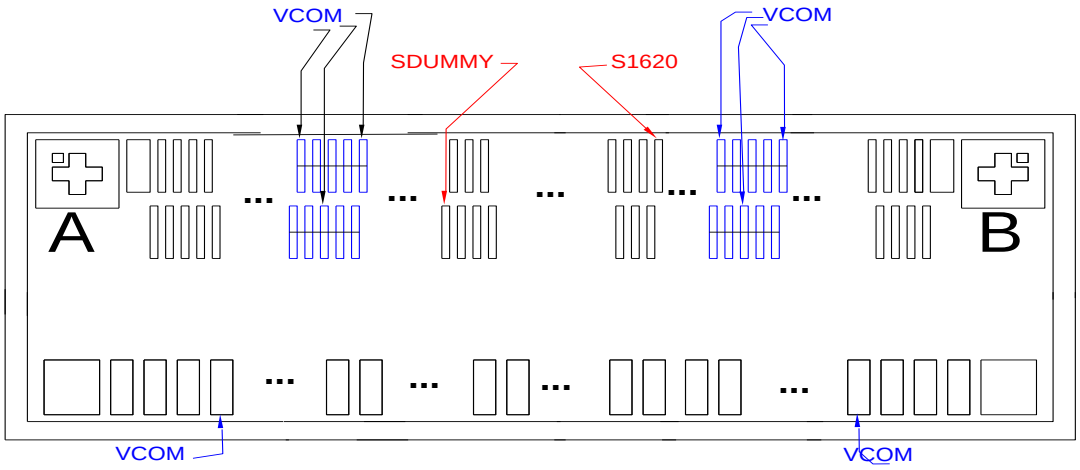


Note1. Color Filter is at the side , TFT is at bottom side

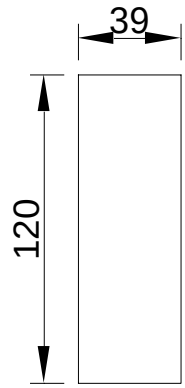
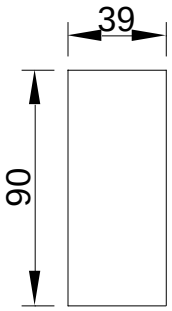
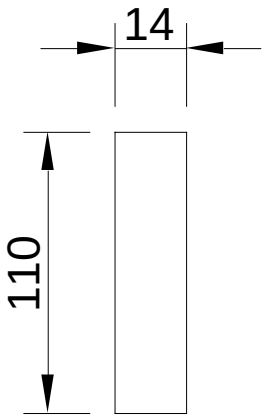
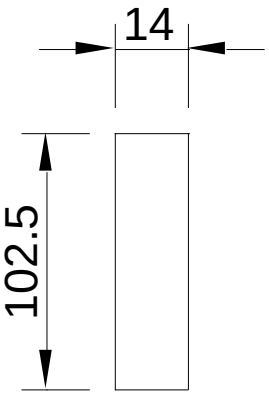
Note2. This Source IC size is of NT35516/OTM9608/OTM9605/ILI9807

3.2.1 IC Pads

Source IC （NT35516/OTM9608/OTM9605/ILI9807）



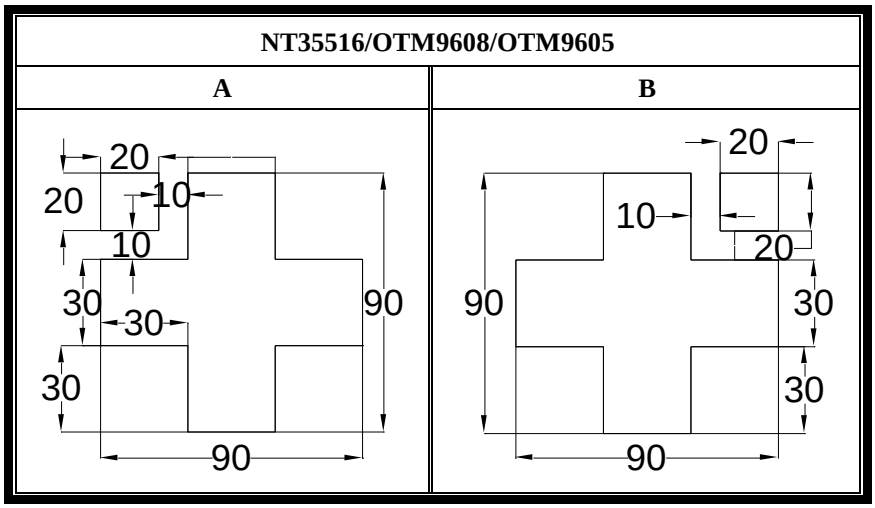
1. Gold Bump Size(unit：um)：

	Source IC (NT35516/OTM9608/OTM9605)	**Source IC (ILI9807)**
Input Bump		
Output Bump		

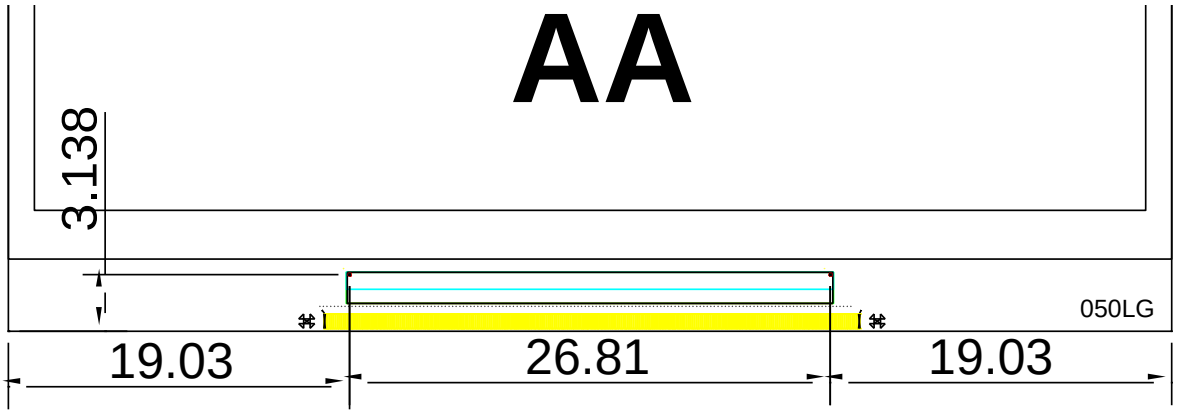
2. Chip Size：

IC	Chip Size
NT35516	27.07 mm x 1.72 mm
OTM9608	27.15 mm x 1.72 mm
OTM9605	27.15 mm x 0.95 mm
ILI9807	27.15 mm x 0.8 mm

3. Alignment Mark Size (unit：um)：

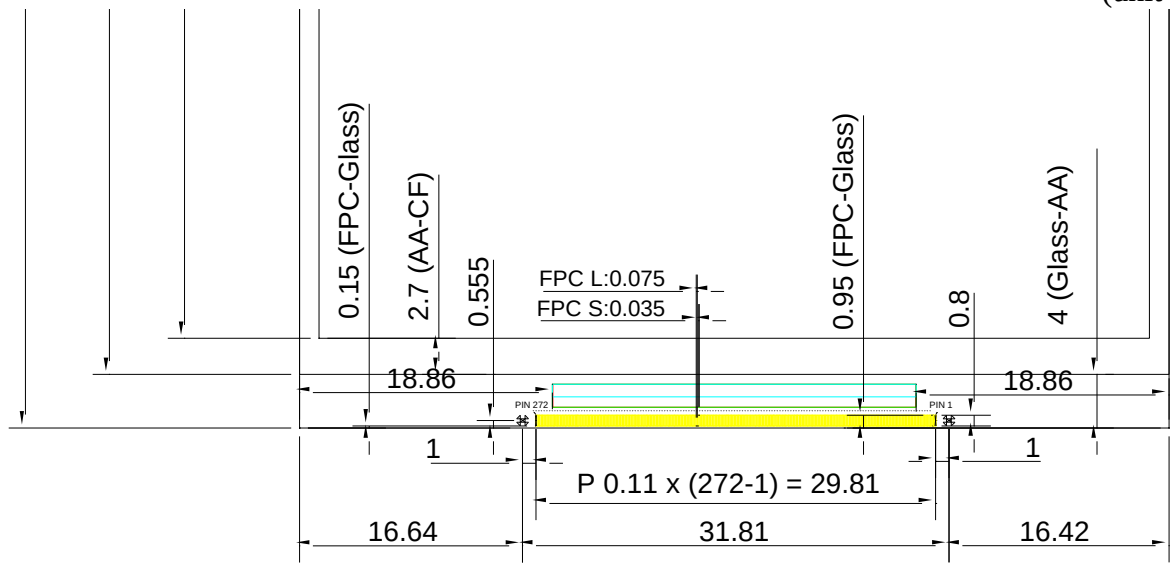


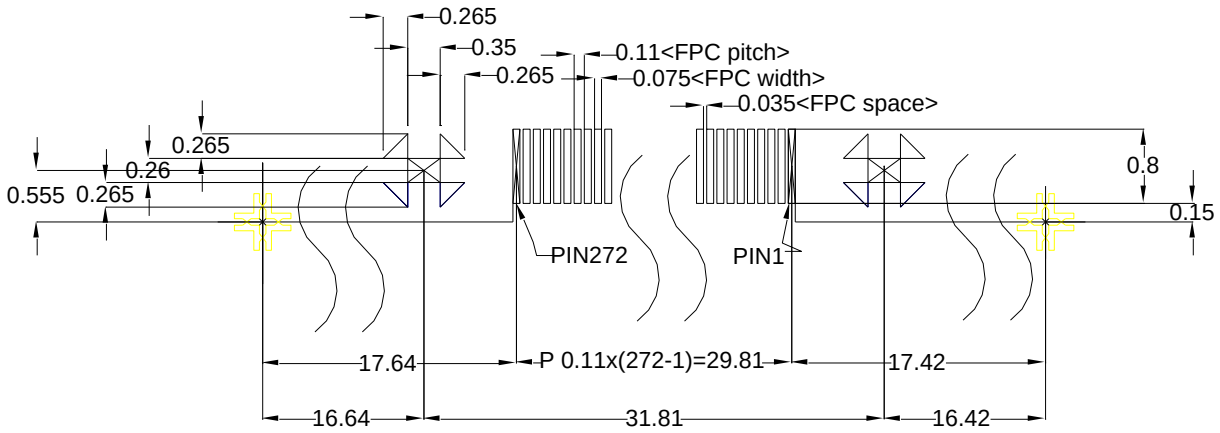
(unit = mm)



3.2.2 FPC Pads

(unit = mm)





3.2.3 FPC Pin Assignment (ILI9807)

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	DUMMY	71	CSX	141	D0P	211	C21N
2	DUMMY	72	RESX	142	D0N	212	C21N
3	Ground	73	DGND	143	D0N	213	C21N
4	Ground	74	IOVCC	144	DGND	214	C22P
5	VCOM	75	NBWSEL	145	DUMMY	215	C22P
6	DUMMY	76	D23	146	DUMMY	216	C22P
7	DUMMY	77	D22	147	DUMMY	217	C22N
8	DUMMY	78	D21	148	DUMMY	218	C22N
9	DUMMY	79	D20	149	DGND	219	C22N
10	VCOM	80	D19	150	VCI	220	C23N
11	VCOM	81	D18	151	TE_R	221	C23N
12	DUMMY	82	D17	152	VSS	222	C23N
13	DUMMY	83	D16	153	DUMMY	223	C23P
14	DUMMY	84	D15	154	DUMMY	224	C23P
15	DUMMY	85	D14	155	EXTP	225	C23P
16	DUMMY	86	D13	156	DUMMY	226	DDVDL
17	DUMMY	87	D12	157	EXTN	227	DDVDL
18	DUMMY	88	D11	158	DUMMY	228	DDVDL
19	DUMMY	89	D10	159	AGND	229	VCI
20	DUMMY	90	D9	160	AGND	230	VCI
21	DUMMY	91	D8	161	AGND	231	VCI
22	VPP	92	D7	162	C11P	232	AGND
23	VGL	93	D6	163	C11P	233	AGND
24	VGL_REG_L	94	D5	164	C11P	234	AGND
25	VRGH_REG_L	95	D4	165	C11N	235	C41P
26	VCL	96	D3	166	C11N	236	C41P
27	VCL	97	D2	167	C11N	237	C41N
28	VCL	98	D1	168	C12P	238	C41N
29	VREF15	99	D0	169	C12P	239	C51N
30	AGND	100	DE	170	C12P	240	C51N
31	AGND	101	PCLK	171	C12N	241	C51P
32	VCI	102	HS	172	C12N	242	C51P
33	VCI	103	VS	173	C12N	243	VGH
34	VCI	104	LEDPWM	174	C13N	244	VGH
35	AGND	105	LEDON	175	C13N	245	VGH
36	VCI	106	ERR	176	C13N	246	VGH
37	TESTDIN	107	IOVCC	177	C13P	247	VRGH
38	DUMMY	108	DGND	178	C13P	248	VRGH
39	DUMMY	109	VCI	179	C13P	249	VGL_REG_R
40	VGMN	110	VCI	180	DDVDH	250	VGL_REG_R
41	VGMP	111	VCC	181	DDVDH	251	VGL
42	DGND	112	DDVDH	182	DDVDH	252	VGL
43	DGND	113	DDVDH	183	VCI	253	VGL
44	IOVCC	114	DDVDL	184	VCI	254	VGL
45	IOVCC	115	DDVDL	185	VCI	255	AGND
46	AGND	116	AGND	186	VCI	256	AGND
47	AGND	117	AGND	187	VCI	257	VCI
48	LANSEL	118	IOVCC	188	AGND	258	VCI
49	DSWAP0	119	IOVCC	189	AGND	259	IOVCC
50	DUMMY	120	VCORE_MIPI	190	AGND	260	IOVCC
51	PSWAP	121	VCI	191	AGND	261	AGND
52	TESTDIN6	122	V12_MIPI	192	AGND	262	AGND
53	TESTDIN7	123	DGND	193	C31P	263	VCOM
54	TESTOUT0	124	DGND	194	C31P	264	VCOM
55	IM3	125	DUMMY	195	C31P	265	DUMMY
56	IM2	126	DUMMY	196	C31N	266	DUMMY
57	IM1	127	DUMMY	197	C31N	267	DUMMY
58	IM0	128	DUMMY	198	C31N	268	DUMMY
59	GPO3	129	DGND	199	C32P	269	VGL
60	GPO2	130	D1P	200	C32P	270	VCOM
61	GPO1	131	D1P	201	C32P	271	DUMMY
62	GPO0	132	D1N	202	C32N	272	DUMMY
63	TESTOUT1	133	D1N	203	C32N		
64	TE_L	134	DGND	204	C32N		
65	TESTOUT2	135	CLKP	205	VCL		
66	SDO	136	CLKP	206	VCL		
67	SDI	137	CLKN	207	VCL		
68	TESTOUT3	138	CLKN	208	C21P		
69	WRX	139	DGND	209	C21P		
70	TESTD_EN	140	D0P	210	C21P		

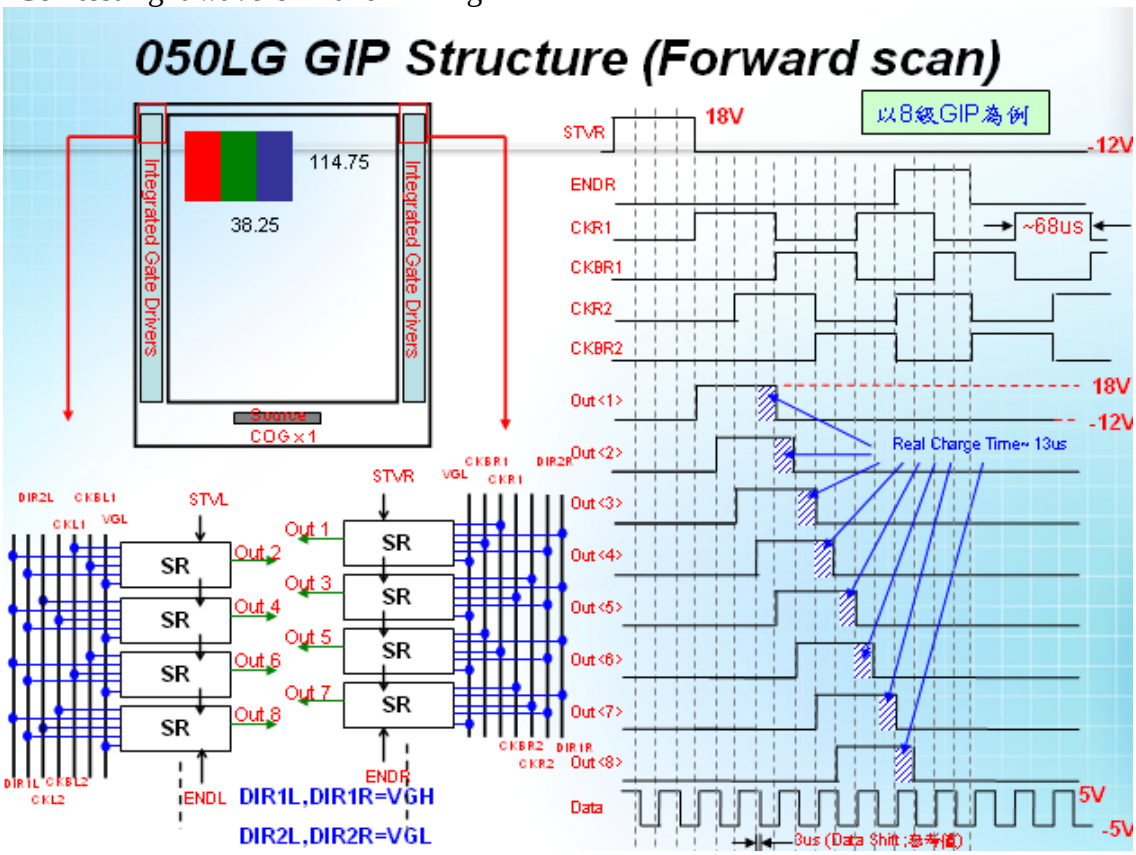
FPC Pin Assignment (NT35516)

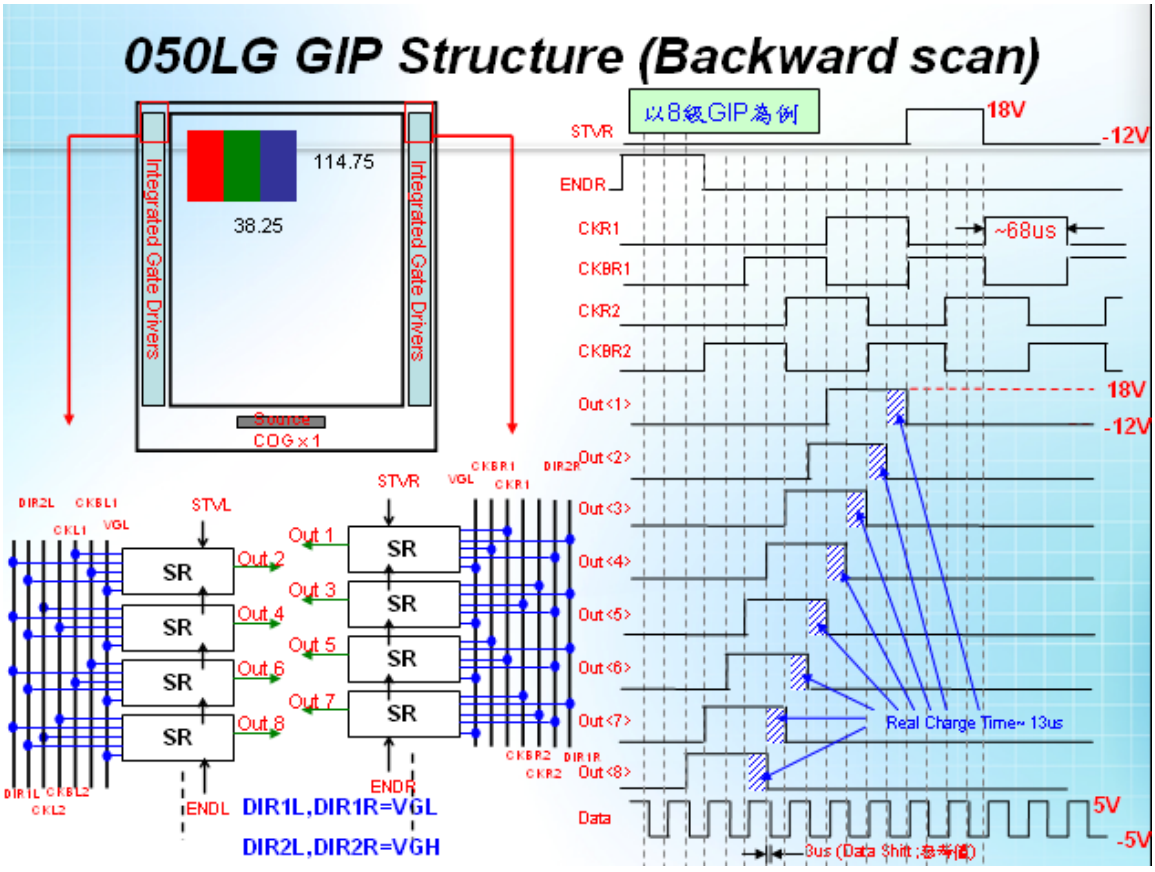
Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	DUMMY	71	CSX	141	HSSI_D0_P	211	C21N
2	DUMMY	72	RESX	142	HSSI_D0_N	212	C21N
3	Ground	73	VSSI	143	HSSI_D0_N	213	C21N
4	Ground	74	VDDI	144	VSSAM	214	C22P
5	VCOM	75	NBWSEL	145	HSSI_D21_P	215	C22P
6	DUMMY	76	D23	146	HSSI_D21_P	216	C22P
7	DUMMY	77	D22	147	HSSI_D21_N	217	C22N
8	DUMMY	78	D21	148	HSSI_D21_N	218	C22N
9	DUMMY	79	D20	149	VSSAM	219	C22N
10	VCOM	80	D19	150	VDDR	220	C23N
11	VCOM	81	D18	151	TE_R	221	C23N
12	OUT3D1)	82	D17	152	VSSR	222	C23N
13	OUT3D1)	83	D16	153	VREFCP	223	C23P
14	OUT3D2)	84	D15	154	VRGH	224	C23P
15	OUT3D2	85	D14	155	EXTP	225	C23P
16	OUT3D3	86	D13	156	CSP	226	AVEE
17	OUT3D3	87	D12	157	EXTN	227	AVEE
18	OUT3D4	88	D11	158	CSN	228	AVEE
19	OUT3D4	89	D10	159	AVSS	229	VDDB
20	BVP3D	90	D9	160	AVSS	230	VDDB
21	BVN3D	91	D8	161	AVSS	231	VDDB
22	MTP_PWR	92	D7	162	C11P	232	VSSB
23	VGLX	93	D6	163	C11P	233	VSSB
24	VGL_REG	94	D5	164	C11P	234	VSSB
25	VRGH	95	D4	165	C11N	235	C41P
26	VCL	96	D3	166	C11N	236	C41P
27	VCL	97	D2	167	C11N	237	C41N
28	VCL	98	D1	168	C12P	238	C41N
29	VREF	99	D0	169	C12P	239	C51N
30	VSSA	100	DE	170	C12P	240	C51N
31	VSSA	101	PCLK	171	C12N	241	C51P
32	VDDA	102	HS	172	C12N	242	C51P
33	VDDA	103	VS	173	C12N	243	VGH
34	VDDR	104	LEDPWM	174	C13N	244	VGH
35	VSSR	105	LEDON	175	C13N	245	VGH
36	VDD_DET	106	ERR	176	C13N	246	VGH
37	DIOPWR	107	VDDI	177	C13P	247	VRGH
38	VGSN	108	VSSI	178	C13P	248	VRGH
39	VGSP	109	VDDA	179	C13P	249	VGL_REG
40	VGMN	110	VDDA	180	AVDD	250	VGL_REG
41	VGMP	111	VDDA	181	AVDD	251	VGL
42	DVSS	112	AVDD	182	AVDD	252	VGL
43	DVSS	113	AVDD	183	VDDB	253	VGL
44	DVDD	114	AVEE	184	VDDB	254	VGL
45	DVDD	115	AVEE	185	VDDB	255	AVSS
46	AVSS	116	DVSS	186	VDDB	256	AVSS
47	AVSS	117	DVSS	187	VDDB	257	VDDA
48	LANSEL	118	DVDD	188	VSSB	258	VDDA
49	DSWAP0	119	DVDD	189	VSSB	259	DVDD
50	DSWAP1	120	MVDDA	190	VSSB	260	DVDD
51	PSWAP	121	VDDAM	191	VSSB	261	DVSS
52	DSTB_SEL	122	MVDDL	192	VSSB	262	DVSS
53	RGBBP	123	VSSAM	193	C31P	263	VCOM
54	I2C_SA0	124	VSSAM	194	C31P	264	VCOM
55	IM3	125	HSSI_D22_P	195	C31P	265	DUMMY
56	IM2	126	HSSI_D22_P	196	C31N	266	DUMMY
57	IM1	127	HSSI_D22_N	197	C31N	267	DUMMY
58	IM0	128	HSSI_D22_N	198	C31N	268	DUMMY
59	GPO3	129	VSSAM	199	C32P	269	VGL
60	GPO2	130	HSSI_D1_P	200	C32P	270	VCOM
61	GPO1	131	HSSI_D1_P	201	C32P	271	DUMMY
62	GPO0	132	HSSI_D1_N	202	C32N	272	DUMMY
63	EXB1T	133	HSSI_D1_N	203	C32N		
64	TE_L	134	VSSAM	204	C32N		
65	VSEL	135	HSSI_CLK_P	205	VCL		
66	SDO	136	HSSI_CLK_P	206	VCL		
67	SDI	137	HSSI_CLK_N	207	VCL		
68	DCX	138	HSSI_CLK_N	208	C21P		
69	WRX	139	VSSAM	209	C21P		
70	RDX	140	HSSI_D0_P	210	C21P		

FPC Pin Assignment (OTM9605A)

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	DUMMY	71	CSX	141	D0P	211	C21N
2	DUMMY	72	RESX	142	D0N	212	C21N
3	Ground	73	VSSI	143	D0N	213	C21N
4	Ground	74	VDDIO	144	LVDSVSS	214	C22P
5	VCOM	75	NBWSEL	145	D2P	215	C22P
6	DUMMY	76	D23	146	D2P	216	C22P
7	DUMMY	77	D22	147	D2N	217	C22N
8	DUMMY	78	D21	148	D2N	218	C22N
9	DUMMY	79	D20	149	LVDSVSS	219	C22N
10	VCOM	80	D19	150	VDD	220	C23N
11	VCOM	81	D18	151	TE_R	221	C23N
12	3D_CLK_0	82	D17	152	VSS	222	C23N
13	3D_CLK_0	83	D16	153	VREFCP	223	C23P
14	3D_CLK_1	84	D15	154	VRGH	224	C23P
15	3D_CLK_1	85	D14	155	EXTP	225	C23P
16	3D_CLK_2	86	D13	156	CSP	226	NVDDA
17	3D_CLK_2	87	D12	157	EXTN	227	NVDDA
18	3D_CLK_3	88	D11	158	CSN	228	NVDDA
19	3D_CLK_3	89	D10	159	VSSA	229	VDD
20	BVP3D	90	D9	160	VSSA	230	VDD
21	BVN3D	91	D8	161	VSSA	231	VDD
22	MTP_PWR	92	D7	162	C11P	232	VSS
23	VGL	93	D6	163	C11P	233	VSS
24	VGL_REG	94	D5	164	C11P	234	VSS
25	VRGH	95	D4	165	C11N	235	C41P
26	VCL	96	D3	166	C11N	236	C41P
27	VCL	97	D2	167	C11N	237	C41N
28	VCL	98	D1	168	C12P	238	C41N
29	VREF	99	D0	169	C12P	239	C51N
30	VSSA	100	DE	170	C12P	240	C51N
31	VSSA	101	PCLK	171	C12N	241	C51P
32	VDD	102	HS	172	C12N	242	C51P
33	VDD	103	VS	173	C12N	243	VGH
34	VDD	104	LEDPWM	174	C13N	244	VGH
35	VSS	105	LEDON	175	C13N	245	VGH
36	VDD	106	ERR	176	C13N	246	VGH
37	DIOPWR	107	VDDIO	177	C13P	247	VRGH
38	VGSN	108	VSS	178	C13P	248	VRGH
39	VGSP	109	VCC	179	C13P	249	VGL_REG
40	VGMN	110	VCC	180	VDDA	250	VGL_REG
41	VGMP	111	VCC	181	VDDA	251	VGL
42	VSS	112	VDDA	182	VDDA	252	VGL
43	VSS	113	VDDA	183	VDD	253	VGL
44	VDD_1.8V	114	NVDDA	184	VDD	254	VGL
45	VDD_1.8V	115	NVDDA	185	VDD	255	VSSA
46	VSSA	116	VSS	186	VDD	256	VSSA
47	VSSA	117	VSS	187	VDD	257	VDD
48	LANSEL	118	VDD_1.8V	188	VSS	258	VDD
49	DSWAP0	119	VDD_1.8V	189	VSS	259	VDD_1.8V
50	DSWAP1	120	LVDSVDD	190	VSS	260	VDD_1.8V
51	PSWAP	121	VDDAM	191	VSS	261	VSS
52	DSTB_SEL	122	VDDP	192	VSS	262	VSS
53	RGBBP	123	LVDSVSS	193	C31P	263	VCOM
54	I2C_SA0	124	LVDSVSS	194	C31P	264	VCOM
55	IM3	125	D22P	195	C31P	265	DUMMY
56	IM2	126	D22P	196	C31N	266	DUMMY
57	IM1	127	D22N	197	C31N	267	DUMMY
58	IM0	128	D22N	198	C31N	268	DUMMY
59	GPO3	129	LVDSVSS	199	C32P	269	VGL
60	GPO2	130	D1P	200	C32P	270	VCOM
61	GPO1	131	D1P	201	C32P	271	DUMMY
62	GPO0	132	D1N	202	C32N	272	DUMMY
63	EXB1T	133	D1N	203	C32N		
64	TE_L	134	LVDSVSS	204	C32N		
65	VSEL	135	CLKP	205	VCL		
66	SDO	136	CLKP	206	VCL		
67	SDI	137	CLKN	207	VCL		
68	DCX	138	CLKN	208	C21P		
69	WRX	139	LVDSVSS	209	C21P		
70	RDX	140	D0P	210	C21P		

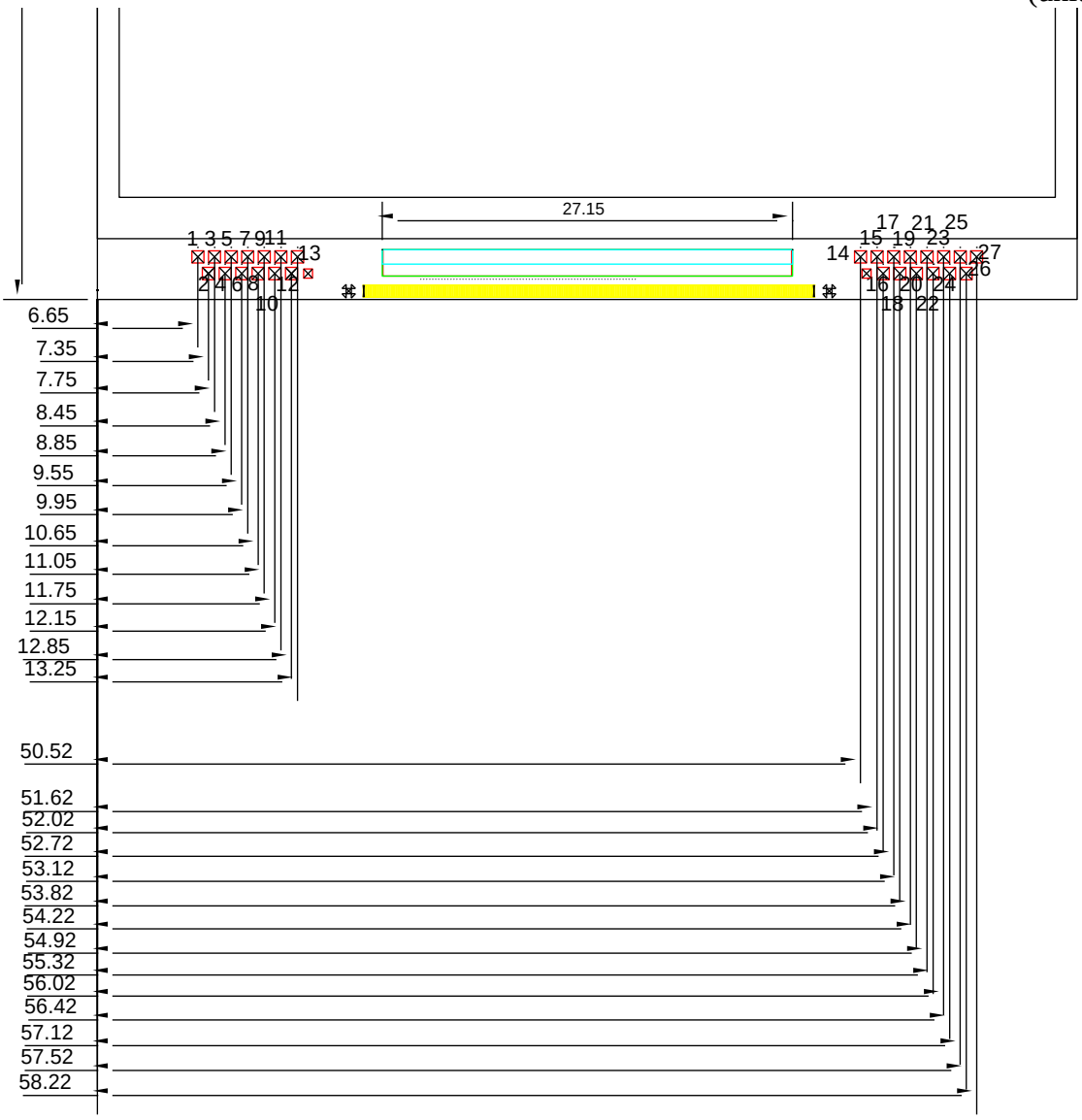
3.2.4 Cell test light waveform and Timing





3.3 Panel Testing pads in panel

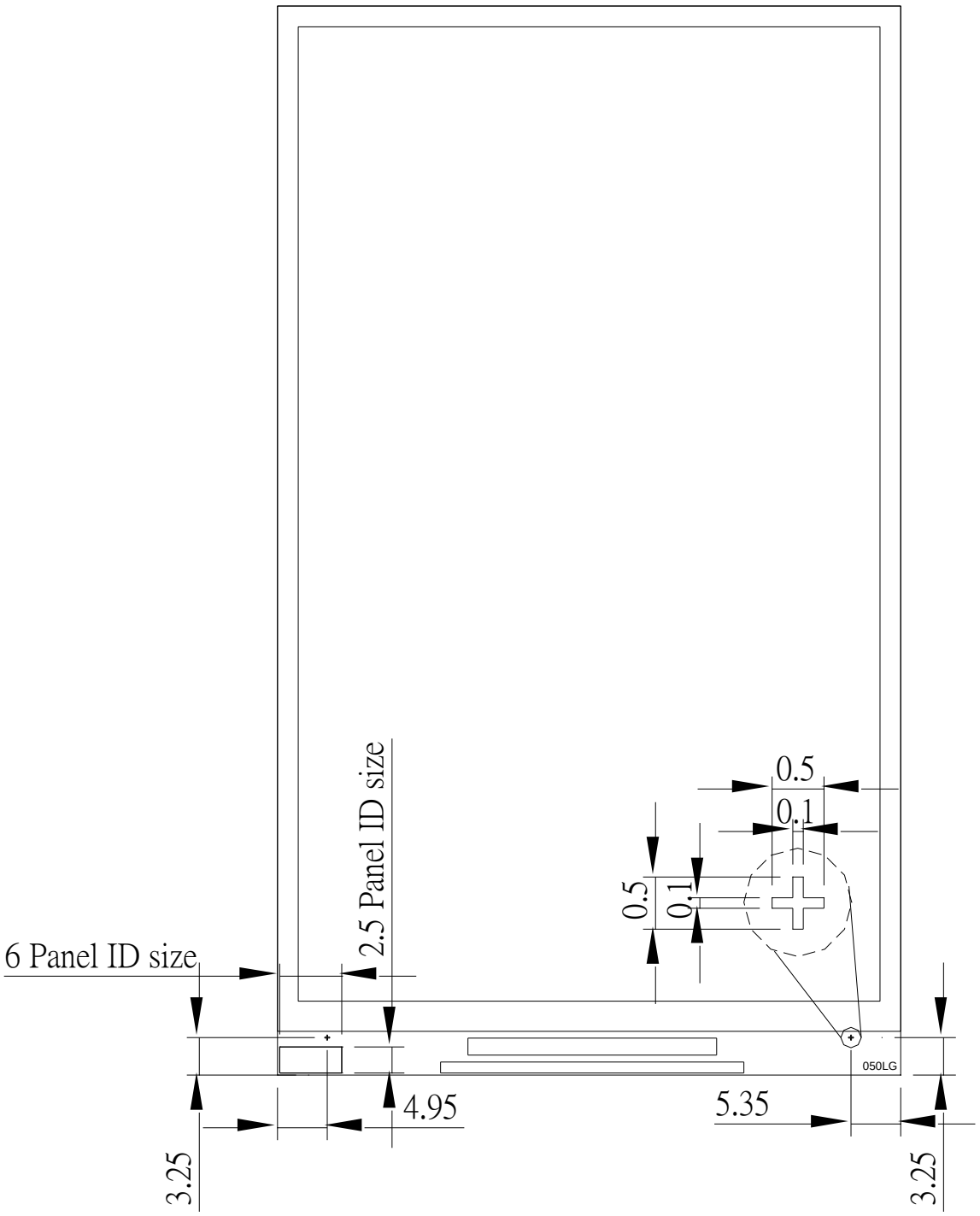
(unit = mm)



No.	TEST PAD NAME	Note	No.	TEST PAD NAME	Note
1	VCOM	-	14	VCOM	-
2	D_R	P TEST	15	VGLTEST	GIP signal
3	SW	P TEST	16	RSTO	GIP signal
4	STVE	GIP signal	17	CK2BO	GIP signal
5	VGLE	GIP signal	18	CK2O	GIP signal
6	DIR1E	GIP signal	19	CK1BO	GIP signal
7	DIR2E	GIP signal	20	CK1O	GIP signal
8	CK1E	GIP signal	21	DIR2O	GIP signal
9	CK1BE	GIP signal	22	DIR1O	GIP signal
10	CK2E	GIP signal	23	VGLE	GIP signal
11	CK2BE	GIP signal	24	STVO	GIP signal
12	RSTE	GIP signal	25	D_B	P TEST
13	VCOM	-	26	D_G	P TEST
			27	VCOM	-

3.4 Panel ID pad

(unit = mm)



4. ELECTRICAL CHARACTERISTICS

4.1 TFT LCD Power Supply Voltage

(GND=AVSS=0V)

Ta = 25℃

Parameter	SYMBOL	Min	Typ	Max	Unit	Remarks
Analog Power Voltage1	VCI	2.5	2.8	3.6	V	
I/Oand Digital Power Voltage	IOVCC	1.65	1.8	3.6	V	
Highspeed Power Voltage	HS_VCC	1.65	2.8	3.3	V	
Current For Driving	IDD		TBD	TBD	mA	Note 1
Input Signal Voltage	VIH	0.7*IOVCC	-	IOVCC	V	Note 2
	VIL	0	-	0.3*IOVCC	V	

Note 1：Typ. specification：Gray-256 test Pattern
Max. specification：White test Pattern
Note 2：IOVCC = 1.8V

4.2 TFT-LCD consumption Current

(GND=AVSS=0V)

Ta = 25℃

MODE	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
Total Power Consumption	Pc		-	TBD	TBD	mW	Note1

Note1：Typ. specification：Gray-256 test Pattern
Max. specification：White test Pattern

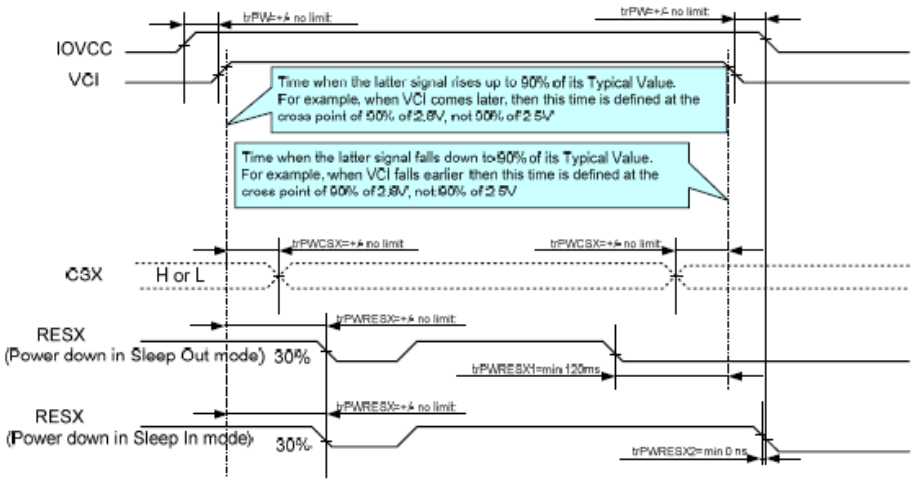
(a)Gray-256 Pattern

(b)White Pattern

4.3 Power on/off sequence

Case 1 – RESX Line is Held High or Unstable by Host at Power ON

If RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



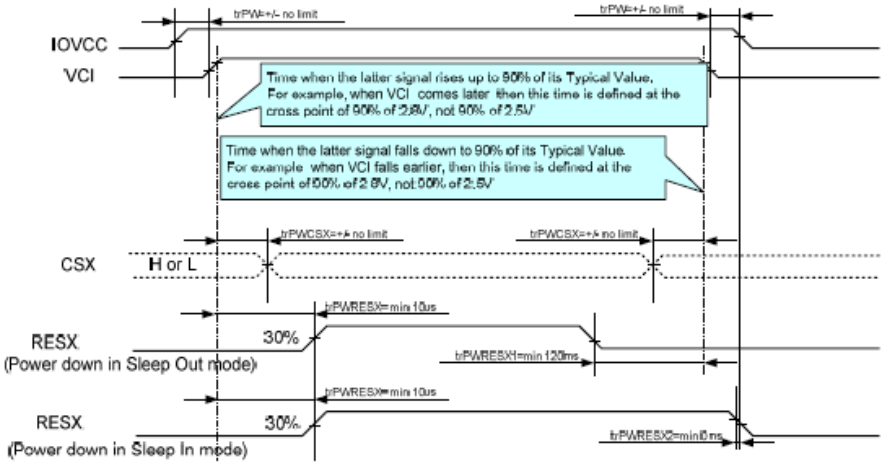
trPWRESX1 is applied to RESX falling in the Sleep Out Mode

trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note: Unless otherwise specified, timings herein show the cross point at 50% of the signal power level.

Case 2 – RESX Line is Held Low by Host at Power ON

If RESX line is held Low (and stable) by the host during Power On, then RESX must be held low for minimum 10µsec after both VCI and IOVCC have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode

trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note: Unless otherwise specified, timings herein show the cross point at 50% of the signal power level.

5. INPUT SIGNAL TIMING

5.1. MIPI Timing DC Characteristics

DSI is using different state codes which are depending on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined on the following table.

State Code	Line DC Voltage Levels	
	HS_CP or HS_D0P/HS_D1P	HS_CN or HS_D0N/HS_D1N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	Low (LP)

Note: Ta = -30℃ to 70℃ (to 85℃ no damage)

DC Characteristics for Power Lines

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Analog power supply voltage	V_{CI}	Operating voltage	2.5	2.8	3.3	V
Digital power supply voltage	V_{IOVCC}	I/O supply voltage	1.65	1.8	3.3	V
Analog power supply voltage noise	V_{VCI_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV
		Noise Range, 0 to 30kHz, Pulse Wave with Duty Cycle (50%/50%)	-	-	500	mV
I/O power supply voltage noise	V_{IOVCC_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV

Note:

1. Ta = -30℃ to 70℃ (to 85℃ no damage)
2. These values are not symmetric amplitude, which center points are IOVCC or VCI. See examples as reference purposes, when V_{VCI_NOISE} and V_{IOVCC_NOISE} are maximums, below.

DC Characteristics for DSI LP Mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined on table below: DC Characteristics for DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned on the condition column. Other logical levels of the table are for MPU interface.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic High level output voltage	V_{OH}	I_{OUT}=-1mA Note 2	0.8 V_{IOVCC}	-	V_{IOVCC}	V
Logic Low level output voltage	V_{OL}	I_{OUT}=-1mA Note 2	0.0	-	0.2V_{IOVCC}	V
Logic High level input voltage	V_{IHLPCD}	LP-CD Note 3	450	-	1350	mV
Logic Low level input voltage	V_{ILLPCD}	LP-CD Note 3	0.0	-	200	mV
Logic High level input voltage	V_{IHLPRX}	LP-RX (HS_CP/N, HS_D0P/N, HS_D1P/N) Note 3	880	-	1350	mV
Logic Low level input voltage	V_{ILLPRX}	LP-RX (HS_CP/N, HS_D0P/N, HS_D1P/N) Note 3	0.0	-	550	mV
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX (HS_CP/N ULP mode) Note 3	0.0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (HS_D0P/N) Note 3	1.1	-	1.3	V
Logic Low level output voltage	V_{OLLPTX}	LP-TX (HS_D0P/N) Note 3	-50	-	50	mV
Logic High level input current	I_{IH}	LP-CD, LP-RX Note 3	-	-	10	uA
Logic Low level input current	I_{IL}	LP-CD, LP-RX Note 3	-10	-	-	uA

Note:

1. Ta = -30℃ to 70℃ (to 85℃ no damage)
2. LEDPWM signals
3. DSI High Speed mode is Off.

DC Characteristics for DSI HS Mode

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Input Common Mode Voltage for Clock	V_{CMCLK}	HS_CP/N Note 2,3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	HS_D0P/N, HS_D1P/N Note 2,3	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	HS_CP/N Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	HS_D0P/N, HS_D1P/N Note 4	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	HS_CP/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	HS_D0P/N, HS_D1P/N	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	HS_CP/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	HS_D0P/N, HS_D1P/N	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	HS_CP/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	HS_D0P/N, HS_D1P/N	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	HS_CP/N, HS_D0P/N, HS_D1P/N Note 3	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	HS_CP/N, HS_D0P/N, HS_D1P/N Note 3	-	-	460	mV
Differential Termination Resistor	R_{TERM}	HS_CP/N, HS_D0P/N, HS_D1P/N	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	HS_CP/N, HS_D0P/N, HS_D1P/N	-	-	450	mV
Termination Capacitor	C_{TERM}	HS_CP/N, HS_D0P/N, HS_D1P/N Note 5	-	-	60	pF

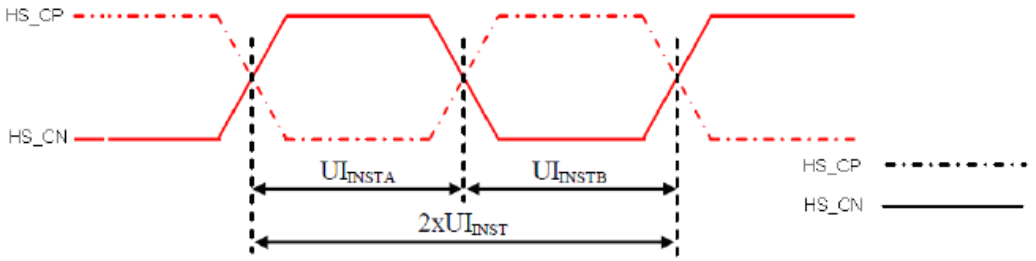
Note:

1. Ta = -30 to 70 ℃ (to 85℃ no damage), IOVCC = 1.65 to 3.3V.
2. Includes 50mV (-50mV to 50mV) ground difference.
3. Without $V_{CMRCLKM450}$/$V_{CMRDATAM450}$.
4. Without 50mV (-50mV to 50mV) ground difference
5. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

5.2 MIPI Timing Characteristics for DSI

5.2.1. High Speed Mode

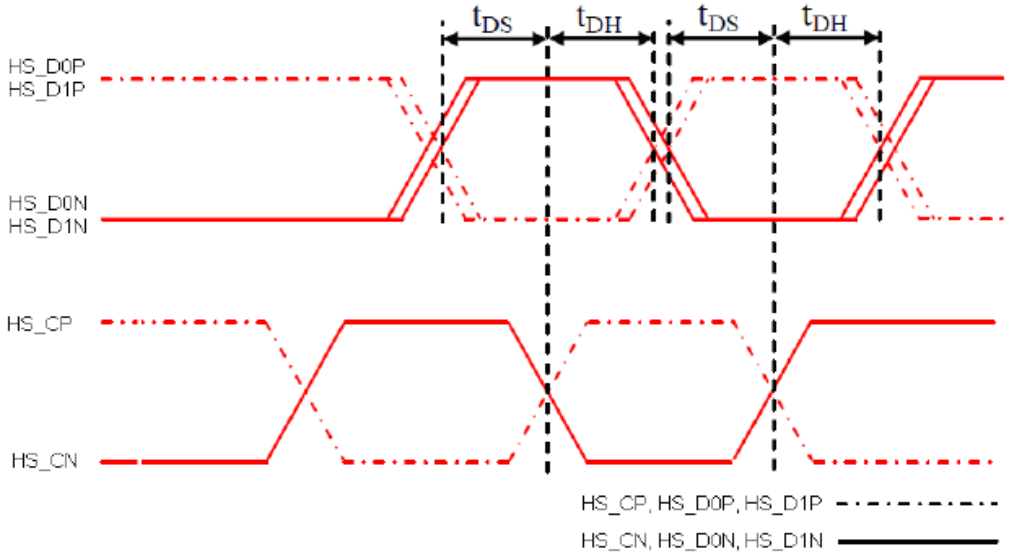
High Speed Mode – Clock Channel Timing



Signal	Symbol	Parameter	Min	Max	Unit
HS_P/N	$2xUI_{INST}$	Double UI instantaneous	3.08	25	ns
HS_P/N	UI_{INSTA}, UI_{INSTB}	UI instantaneous Half	1.54	12.5	ns

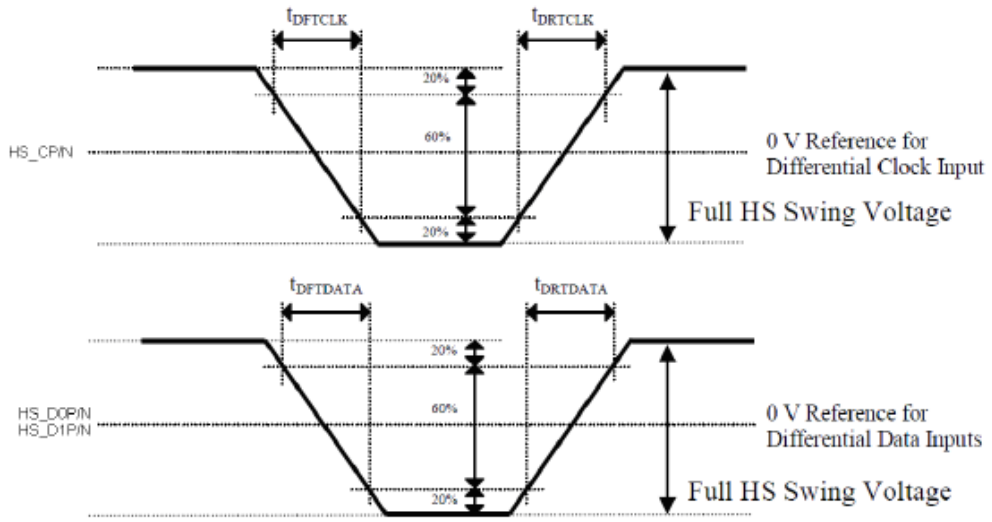
Note: UI = UIINSTA = UIINSTB

High Speed Mode – Data Clock Channel Timing



Signal	Symbol	Parameter	Min	Max	Unit
HS_D0P/N HS_D1P/N	t_{DS}	Data to Clock Setup time	0.15xUI	-	ps
	t_{DH}	Clock to Data Hold Time	0.15xUI	-	ps

High Speed Mode – Rise and Fall Timings

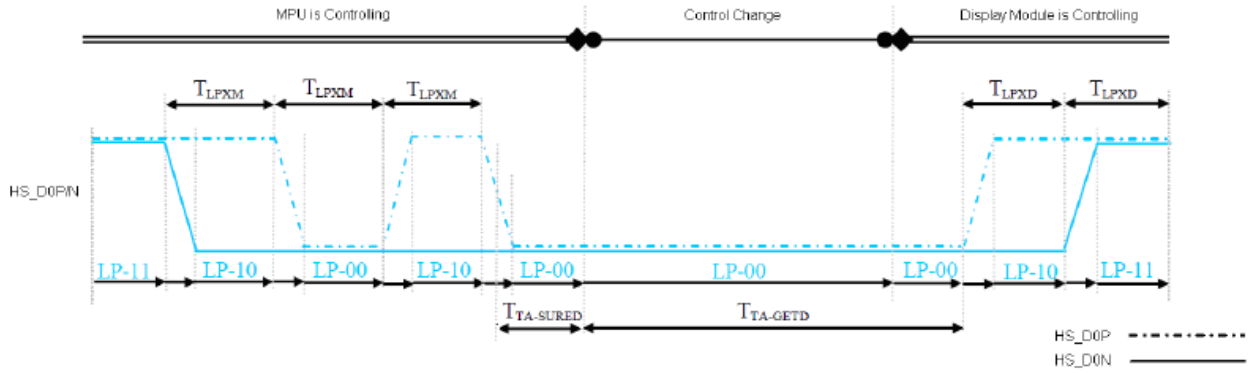


Parameter	Symbol	Condition	Specification			
			Min	Typ	Max	Unit
Differential Rise Time for Clock	t_{DRTCLK}	HS_CP/N	-	-	150 (Note)	ps
Differential Rise Time for Data	$t_{DRTDATA}$	HS_D0P/N, HS_D1P/N	-	-	150 (Note)	ps
Differential Fall Time for Clock	t_{DFTCLK}	HS_CP/N	-	-	150 (Note)	ps
Differential Fall Time for Data	$t_{DFTDATA}$	HS_D0P/N, HS_D1P/N	-	-	150 (Note)	ps

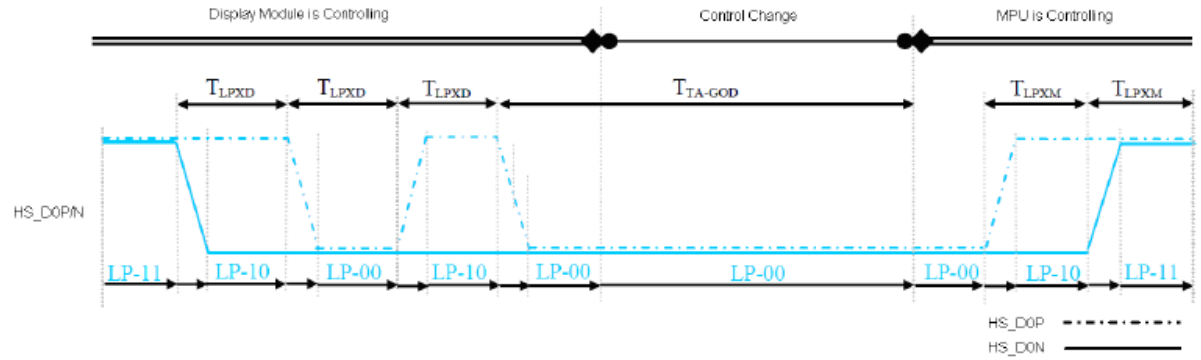
Note: The display module has to meet timing requirements, whah are defined for the transmitter (MPU) on MIPI D-PHY standard.

5.2.2. Low Power Mode

Low Power Mode and its State Periods are illustrated for refrence purposes on the Bus Turnaround (BTA) from the MPU to the display module (ILI9807) sequence below.



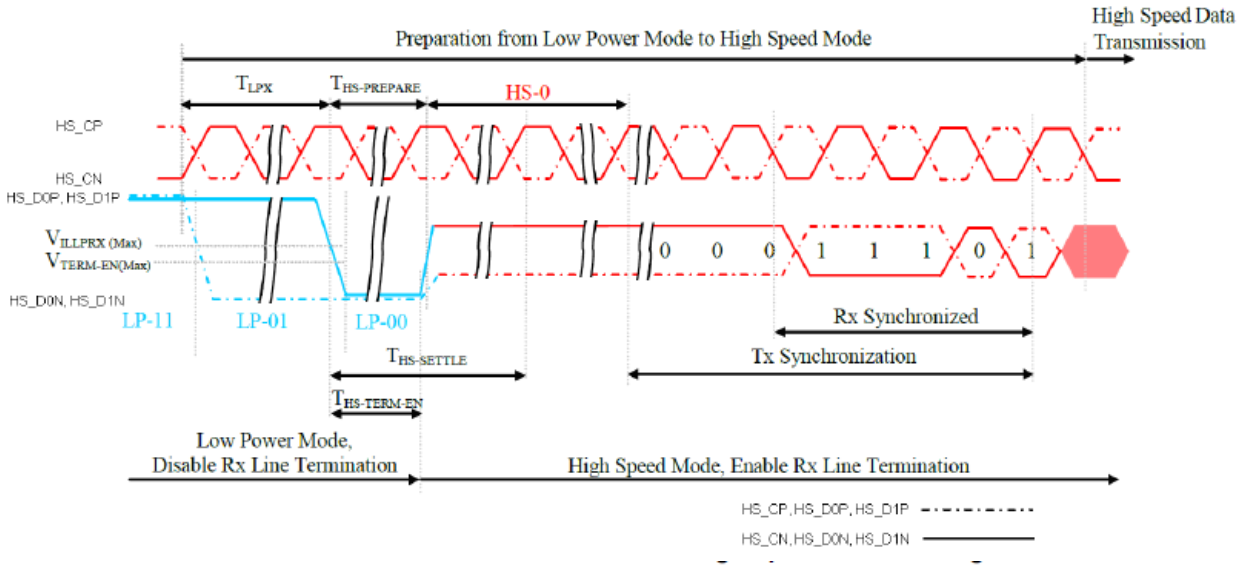
Low Power Mode and its State Periods are illustrated for reference purpose on the Bus Turnaround (BTA) from the display module (ILI9807) to the MPU sequence below.



Signal	Symbol	Description	Min	Max	Unit
HS_D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU ➔ Display Module (ILI9807)	50	75	ns
HS_D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9807 ➔ MPU)	50	75	ns
HS_D0P/N	$T_{TA-SURED}$	Time-out before the Display Module(ILI9807) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

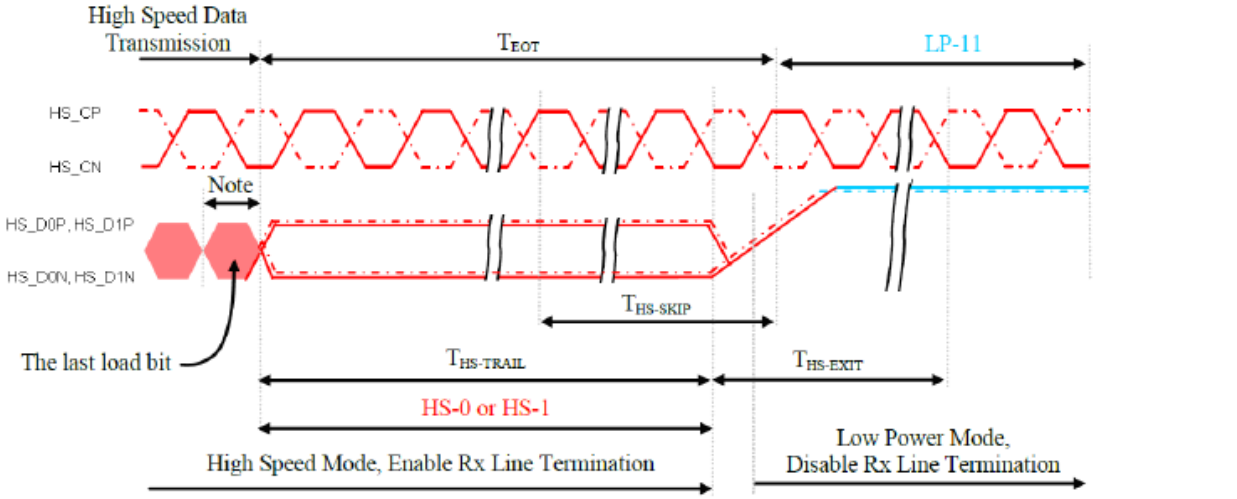
Signal	Symbol	Description	Time	Unit
HS_D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by the Display Module (ILI9807)	$5xT_{LPXD}$	ns
HS_D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MPU	$4xT_{LPXD}$	ns

5.2.3. DSI Bursts



Signal	Symbol	Description	Min	Max	Unit
HS_D0P/N, HS_D1P/N	T_{LPX}	Length of any Low Power State Period	50	-	ns
	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses V_{ILMAX}	-	35+4xUI	ns

Note: $UI = UI_{INSTA} = UI_{INSTB}$

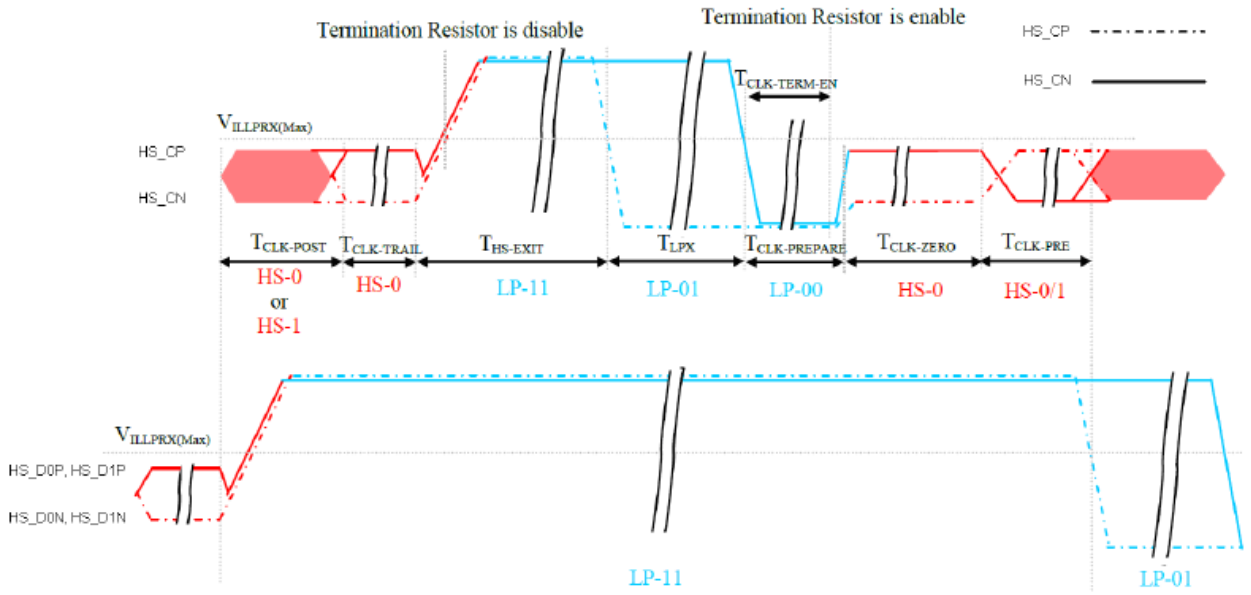


Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

Signal	Symbol	Description	Min	Max	Unit
HS_D0P/N, HS_D1P/N	$T_{HS-SKIP}$	Time-out at the Display Module (ILI9807) to Ignore Transition Period of EoT	40	50+4xUI	ns
	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

Note: $UI = UI_{INSTA} = UI_{INSTB}$

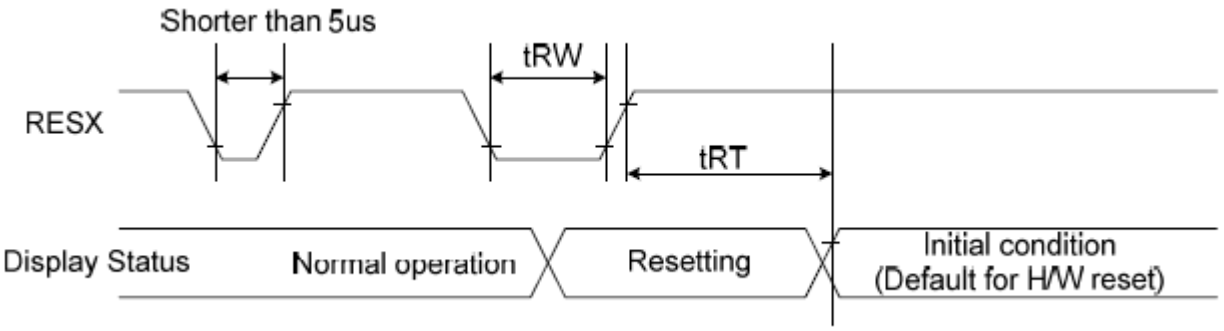
DSI Clock Burst – High Speed Mode to/from Low Power Mode



Signal	Symbol	Description	Min	Max	Unit
HS_CP/N	$T_{CLK-POST}$	Time that the MPU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

Note: $UI = UI_{INSTA} = UI_{INSTB}$

5.2.4. Reset Input Timing



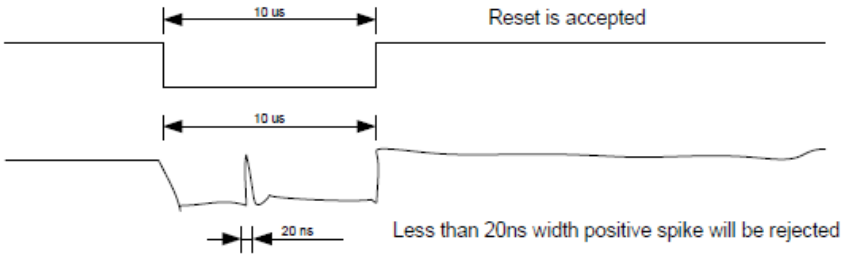
Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from OTP to registers. This loading is done every time when there is H/W reset cancel (tRT) within 5ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 35.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

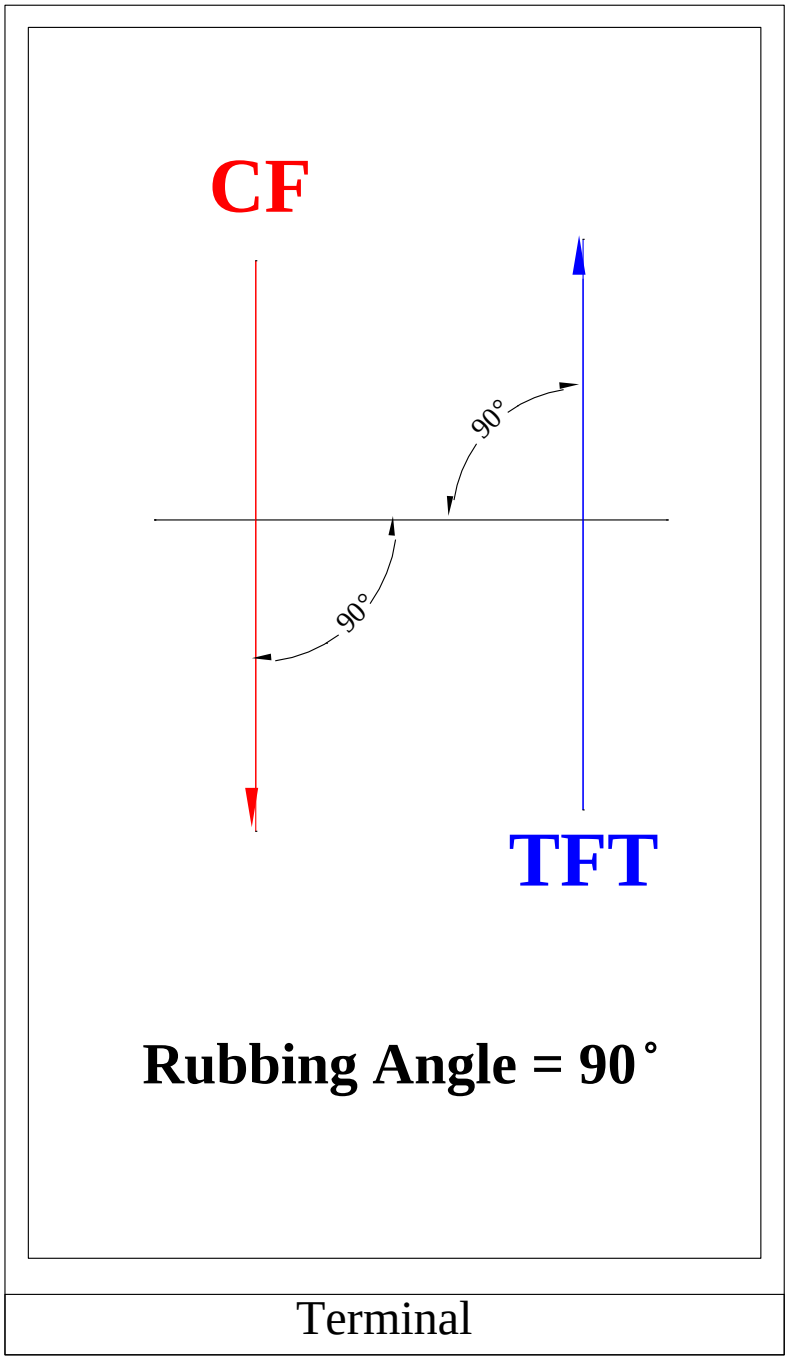
3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset starts in the Sleep Out mode. The display remains the blank state in Sleep In mode.) and then return to default condition for Hardware Reset.
4. Spike Rejection can applies during a valid reset pulse as shown below:



6. CELL PROCESS RULES

Item	Specification
Cell gap	3.6±0.2um
Assembly precision	±4um

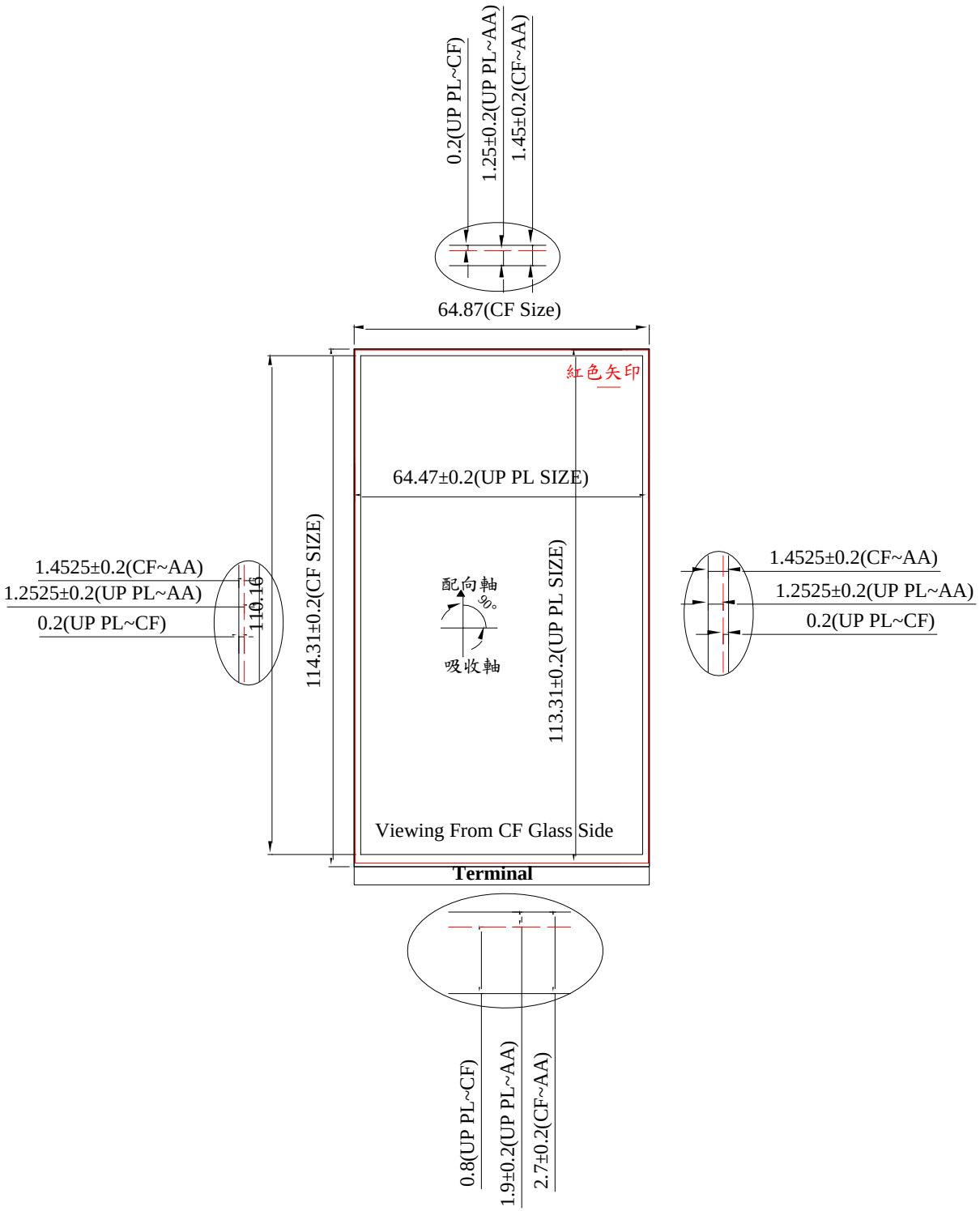
6.1 Rubbing Direction



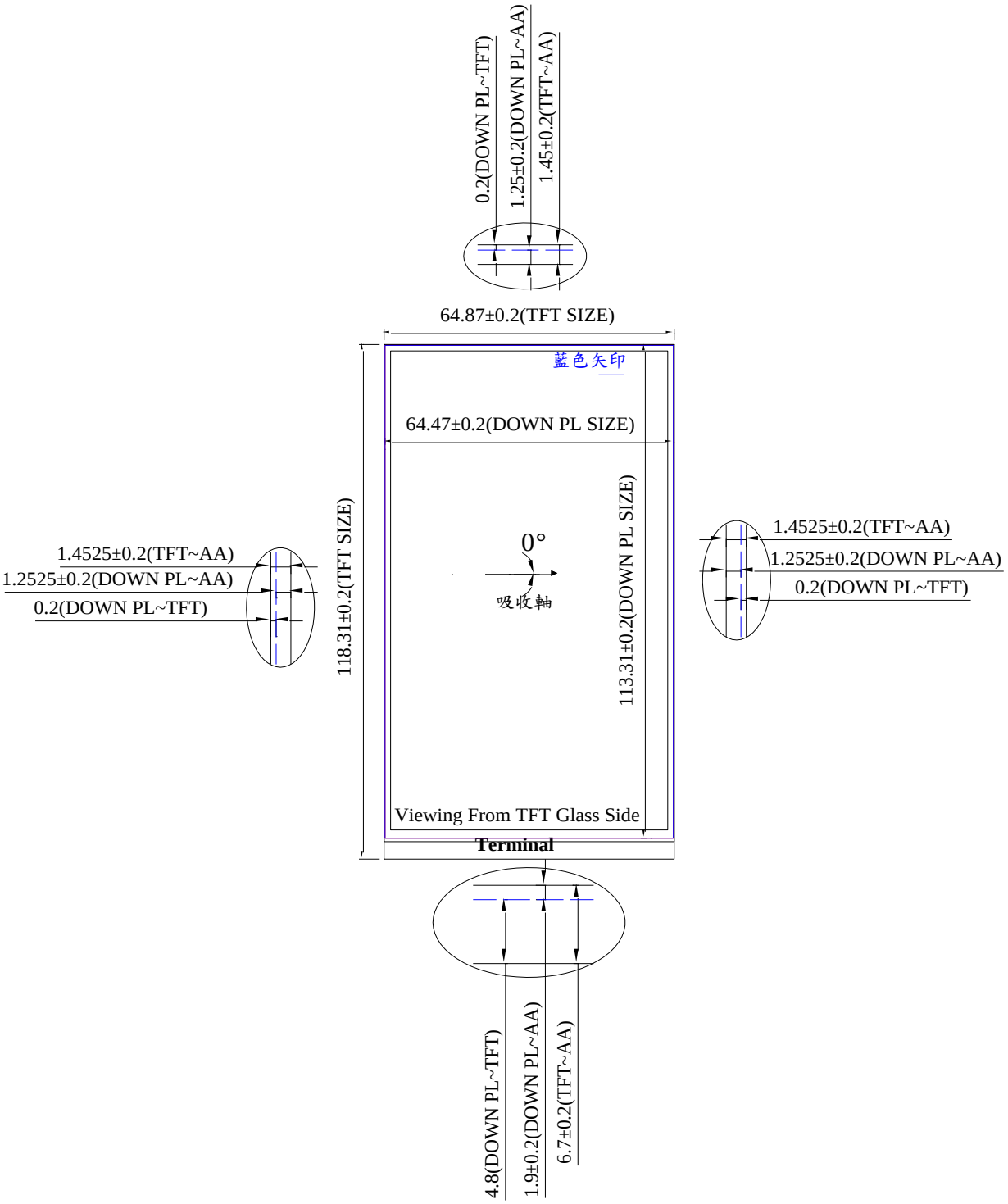
6.2 Polarizer Information

<HC/APCF>

a. CF Side



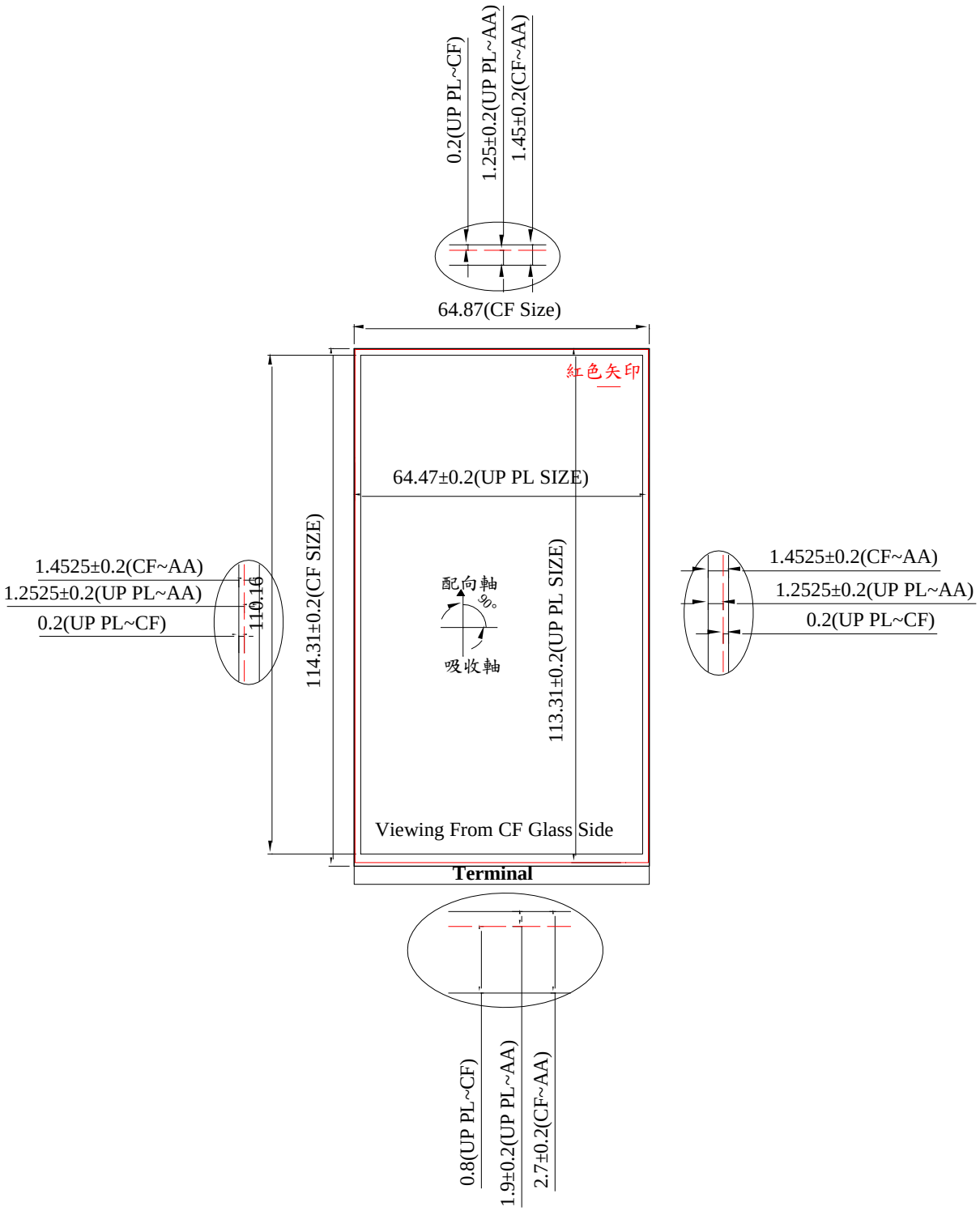
b. TFT Side



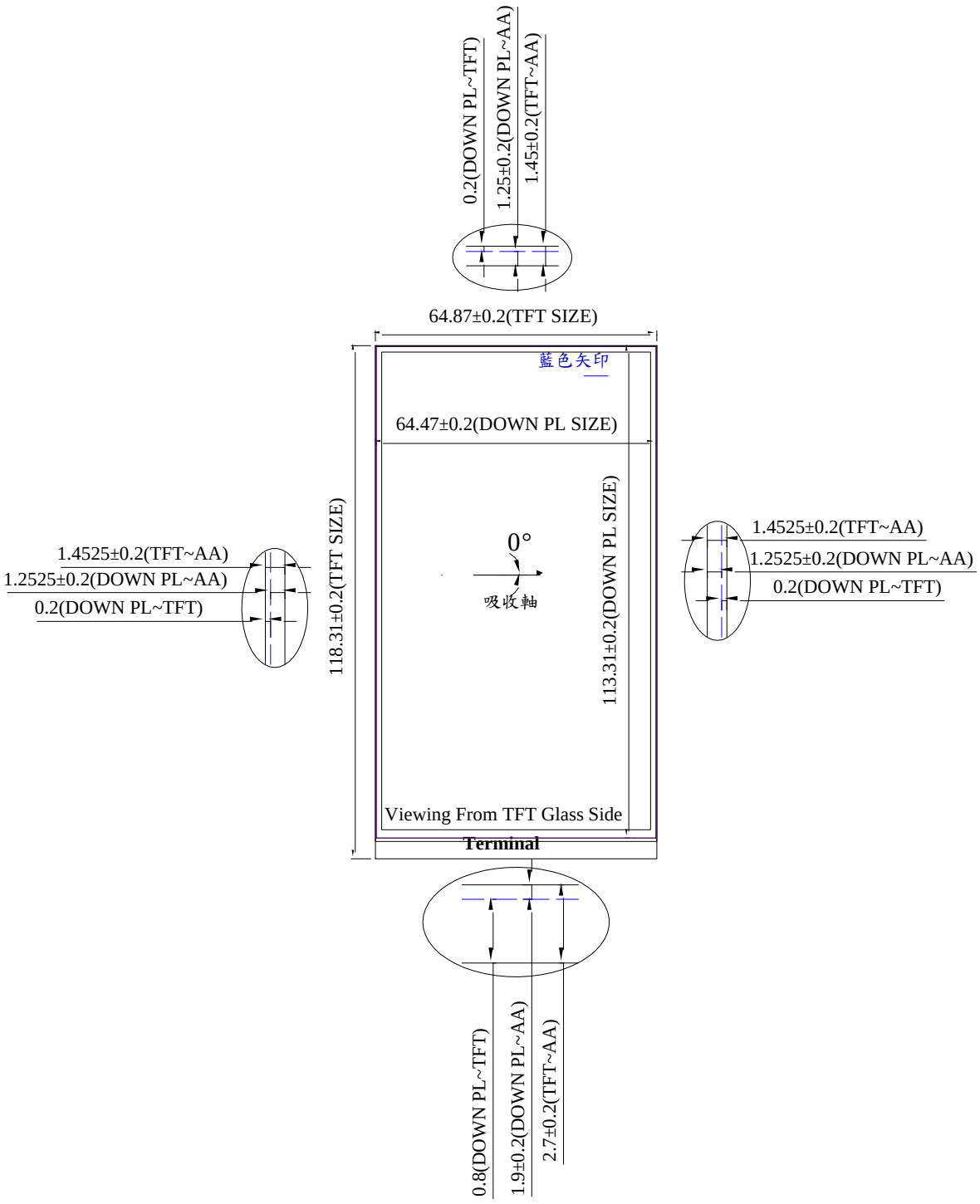
Up PL : HC **64.47 x 113.31 x 0.116mm**
Down PL : APCF **64.47 x 113.31x 0.136mm**
Up PL Thickness& Surface Treatment : 116um±20um HC
Down PL Thickness& Surface Treatment : 136um±20um APCF

<HC/AG40%>

a. CF Side

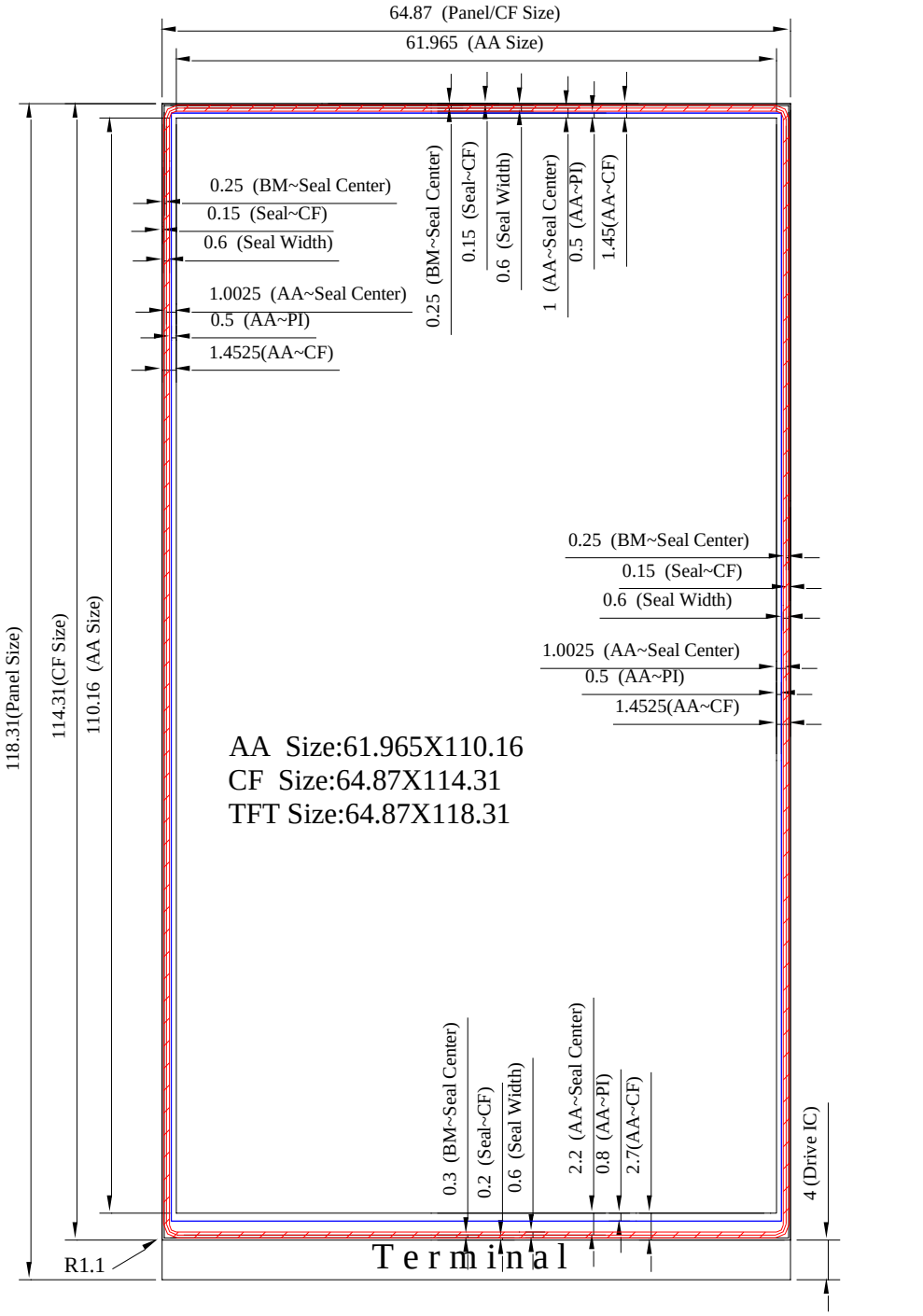


b. TFT Side



Up PL : HC **64.47 x 113.31 x 0.116mm**
Down PL : AG42% **64.47 x 113.31x 0.116mm**
Up PL Thickness& Surface Treatment : 116um±20um HC
Down PL Thickness& Surface Treatment : 116um±20um AG40%

6.3 PI & Seal pattern

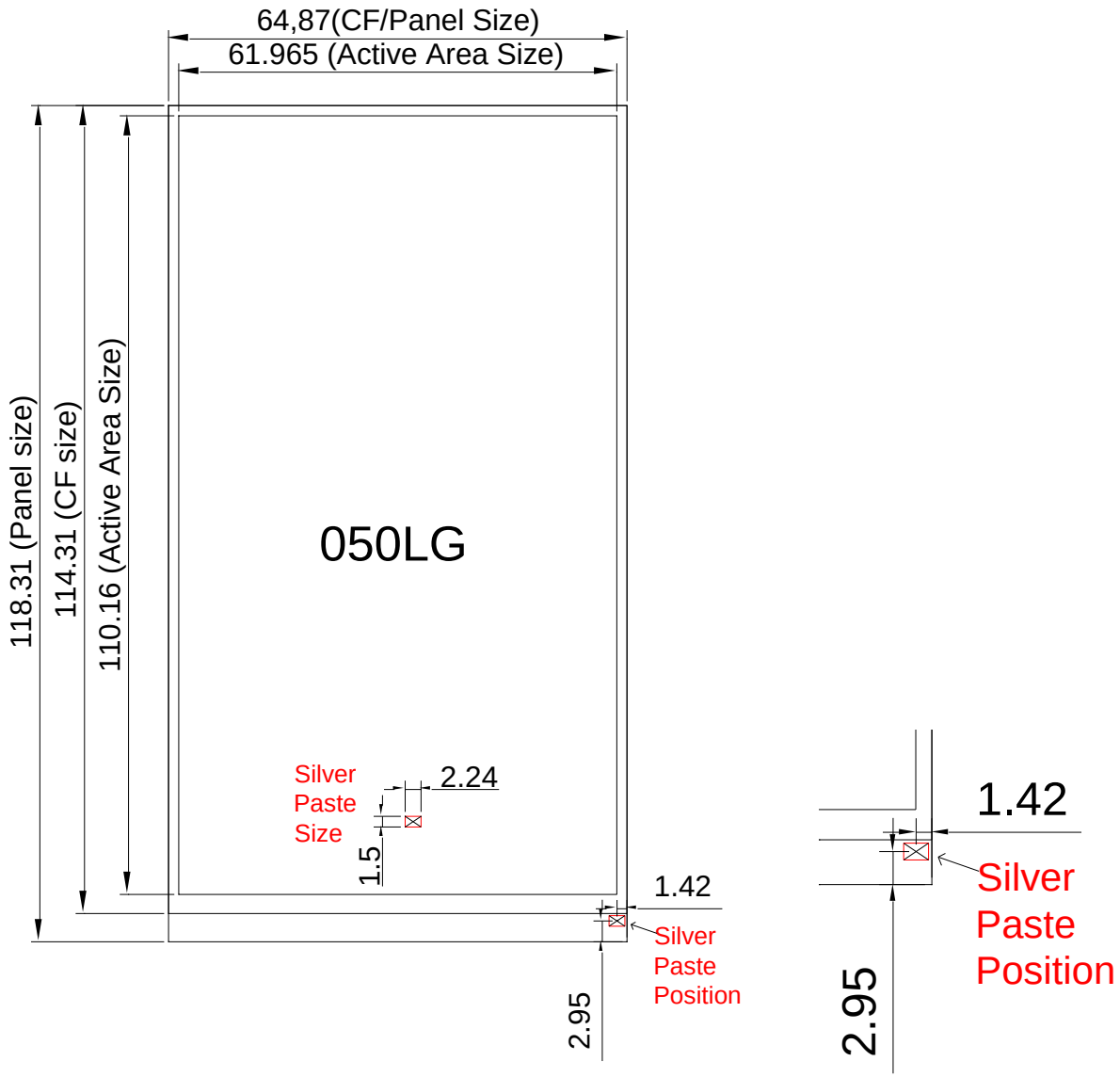


(unit = mm)

Notes:

1. Seal width (Typ.) = 0.6±0.2mm
2. Seal center to CF edge = 0.45±0.2mm (面板左、右側)
   Seal center to CF edge = 0.45±0.2mm (面板上側)
   Seal center to CF edge = 0.5±0.2mm (面板下側)

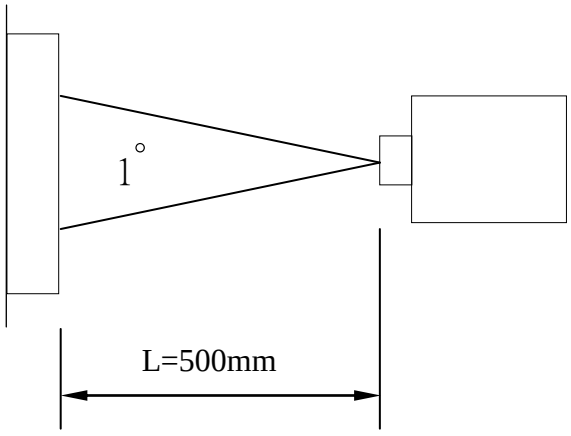
6.4 Silver Paste Position



7. OPTICAL SPECIFICATION

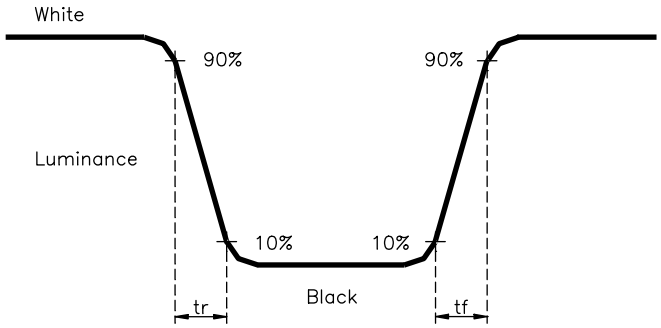
ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
Transmittance		T		4.6 (W/ APCF) 3.3 (W/O APCF)	4.97 (W/ APCF) 3.74 (W/O APCF))		%	
Contrast Ratio		CR	*1)		500	800	-	--
Response Time		Tr+ Tf	*3)		-	30ms	40ms	ms
Viewing Angle	U	θ*2)	- - - -	-	85	-		Note 5
	D			-	85	-		
	L	ψ*2)		-	85	-		
	R			-	85	-		
Color Filter Chromacicity	White	x	θ = ϕ = 0°	0.281	0.301	0.321		Note 6
		y		0.299	0.319	0.339		
		Y		28.98	29	29.02		
	Red	x	θ = ϕ = 0°	0.63	0.65	0.67		
		y		0.32	0.34	0.36		
		Y		21.38	21.4	21.42		
	Green	x	θ = ϕ = 0°	0.258	0.278	0.298		
		y		0.582	0.602	0.622		
		Y		52.78	52.8	52.82		
	Blue	x	θ = ϕ = 0°	0.119	0.139	0.159		
		y		0.084	0.104	0.124		
		Y		12.68	12.7	12.72		
	NTSC			--	70%	-		

Note 1.Ambient condition：25℃±2℃，60±10%RH，under 10 Lunx in the darkroom。
Note 2.Measure device：BM-5A (TOPCON)，viewing cone=1°，I_L=20mA。

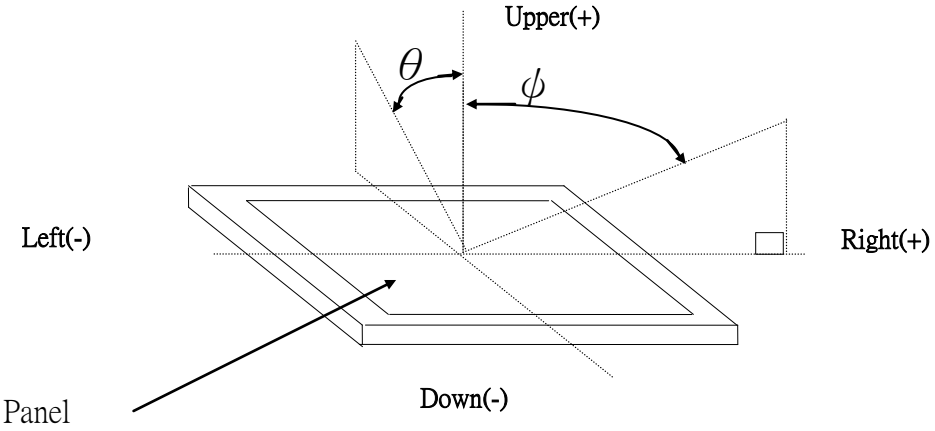


Note 3. Definition of Contrast Ratio：
CR = White Luminance (ON) / Black Luminance (OFF)

Note 4. Definition of response time：The response time is defined as the time interval between the 10% and 90% amplitudes.



Note 5. Definition of view angle(θ，ψ)：



Note 6. Light source: C light.

8. HANDLING PRECAUTIONS FOR EMPTY CELL

Item	Min.	Max.	Unit	Remark
Storage Temperature	-26	20	˚C	
Storage Humidity	50	58	% (RH)	
Storage Time	—	1	month	