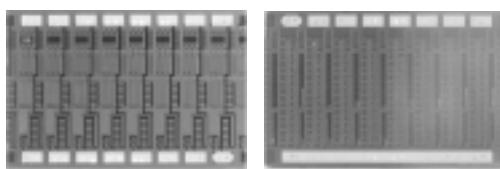


Thin Film Eight Resistor Array



Product may not
be to scale

The CLA and CLB resistor arrays are the hybrid equivalent to the eight resistor common connection and isolated networks available in SIPS or DIPS. The resistors are spaced on 0.010 inches centers resulting in minimal space requirements. These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The CLA and CLBs are 100% electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

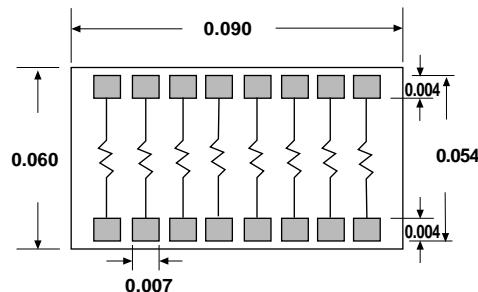
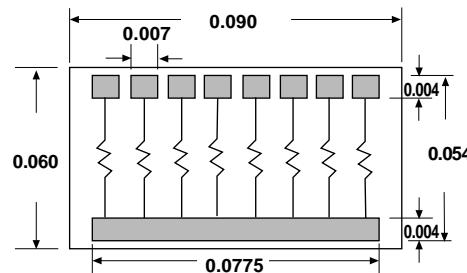
The CLA and CLB thin film resistor arrays are designed for hybrid packages requiring up to eight resistors of the same resistance value and tolerance, as well as excellent TCR tracking. For such hybrids, they afford great savings in cost and space.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES									
Tightest Standard Tolerance Available									
PROCESS CODE <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 2px;">CLASS H*</th><th style="text-align: center; padding: 2px;">CLASS K*</th></tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">026</td><td style="text-align: center; padding: 2px;">054</td></tr> <tr> <td style="text-align: center; padding: 2px;">017</td><td style="text-align: center; padding: 2px;">049</td></tr> <tr> <td style="text-align: center; padding: 2px;">008</td><td style="text-align: center; padding: 2px;">045</td></tr> </tbody> </table>	CLASS H*	CLASS K*	026	054	017	049	008	045	<small>*MIL-PRF-38534</small>
CLASS H*	CLASS K*								
026	054								
017	049								
008	045								

STANDARD ELECTRICAL SPECIFICATIONS	
PARAMETER	
TCR tracking spread	$\pm 5\text{ppm}/^\circ\text{C}$
Noise, MIL-STD-202, Method 308 100Ω - 250kΩ < 100Ω or > 251kΩ	- 35dB typical - 20dB typical
Moisture resistance, MIL-STD-202, Method 106	$\pm 0.5\%$ maximum ΔR/R
Stability, 1000 hours, + 125°C, 25mW Absolute Ratio	$\pm 0.25\%$ maximum ΔR/R $\pm 0.05\%$ maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202 Method 107, Test condition F	$\pm 0.1\%$ maximum ΔR/R
High temperature exposure $\pm 150^\circ\text{C}$, 100 hours	$\pm 0.2\%$ maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V
DC power rating at + 70°C, (derated to zero at 175°C)	50mW per resistor
5 x rated power short-time overload, + 25°C, 5 seconds	$\pm 0.1\%$ maximum ΔR/R

VISHAY ELECTRO-FILMS • FRANCE +33.4.93.37.28.24 FAX: +33.4.93.37.27.31 • GERMANY +49.9287.710 FAX: +49.9287.70435 • ISRAEL +972.3.557.0945 FAX: +972.3.558.9121
 • ITALY +39.2.300.11911 FAX: +39.2.300.11999 • JAPAN +81.42.729.0661 FAX: +81.42.729.3400 • SINGAPORE +65.788.6668 FAX: +65.788.0988
 • SWEDEN +46.8.594.70590 FAX: +46.8.594.70581 • UK +44 191 514 8237 FAX: +44 1953 457 722 • USA: (401) 738-9150 FAX: (401) 738-4389

DIMENSIONS in inches

CLA

CLB


MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip size	0.060 x 0.090 ± 0.002 (1.50 x 2.26 ± 0.05mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO ₂
Resistor material	Tantalum nitride, self-passivating
Bonding pads	0.004 x 0.007 (0.10 x 0.178mm)
Number of top pads	CLA - 16 CLB - 9
Pad material	10kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

OPTIONS: Gold backing for eutectic die attach
For custom configurations, Consult Applications Engineer

 RESISTOR
ARRAYS

ORDERING INFORMATION

Example: 100% visualized, 10kΩ, ± 1%, ± 100ppm/°C TCR, CLA Format, Alum Pads, Class H

P/N:	W INSPECTION /PACKAGING	CLA PRODUCT FAMILY	008 PROCESS CODE	1000 RESISTANCE VALUE	1 MULTIPLIER CODE	F TOLERANCE CODE
	W = 100% visually inspected parts per MIL-STD-883 in matrix trays		See Process Code table	Use first 4 significant digits of the resistance	D = 0.0001 C = 0.001 B = 0.01 A = 0.1 0 = 1 1 = 10 2 = 100 3 = 1000 4 = 10000	B = 0.1% C = 0.2% D = 0.5% F = 1.0% G = 2.0% H = 2.5% J = 5.0% K = 10% M = 20% L = 25% N = 50%
	X = Sample, visually inspected loaded in matrix trays (4% AQL)					