National Semiconductor

Comlinear CLC503
180MHz, Differential-Output Amplifier

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General Description

The Comlinear CLC503 is a single-ended to differential amplifier. It utilizes a pair of closed-loop transconductance amplifiers to provide wideband, high fidelity, differential output signals. Internal resistors set the differential gain to 2V/V. With a ground-centered $2V_{pp}$ input signal, the CLC503 will produce a $4V_{pp}$ differential output signal. This differential output signal is centered around an adjustable common mode voltage. An independent input controls the common mode output voltage. The CLC503 has harmonic distortion products of -77dBc or less, and a signal to noise ratio of 72dB. The output stage is optimized for loads with signal ranges between +0.7 and +3.9 volts, such as those found on single supply CMOS ADCs. Overdrive recovery time of the CLC503 and following circuitry is optimized by the output limiting of the CLC503. The power down pin (P_{DN}) allows for power savings in applications where unused circuitry is placed in a low power mode.

The CLC503 is an ideal amplifier to drive the differential inputs of the Comlinear CLC949, 12-bit, 20MSPS, analog-to-digital converter. It is tailored for driving single supply, differential input, analog-to-digital converters which require fast settling, high fidelity inputs.

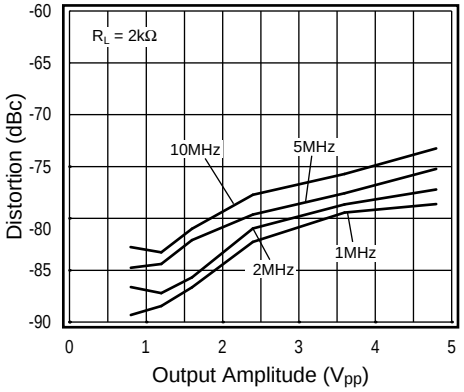
Features

- -77dBc distortion (10MHz, $4V_{pp}$)
- 72dB SNR ($4V_{pp}$)
- 15ns settling (0.1%)
- 180MHz bandwidth

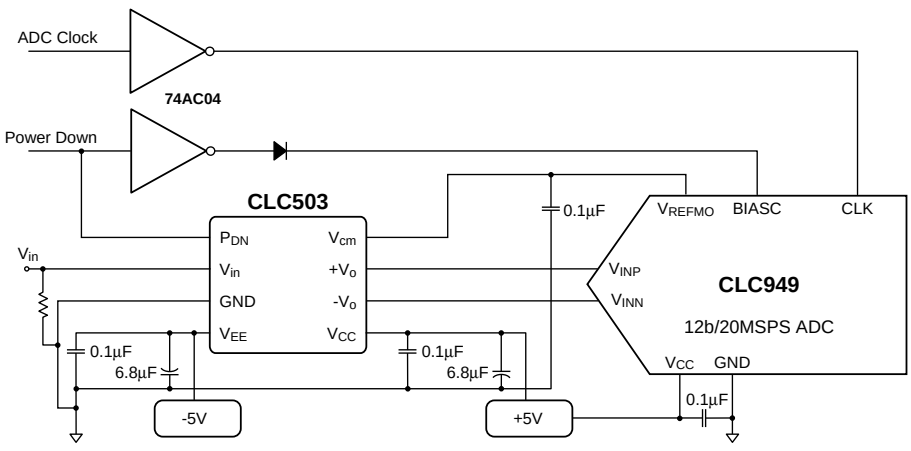
Applications

- Single-to-differential conversion
- Single supply ADC signal conditioner

Harmonic Distortion vs. Amplitude

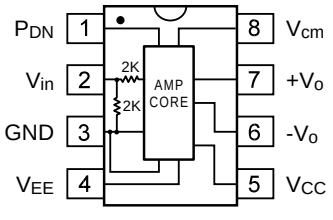


Typical Application Diagram



Pinout

SOIC



Electrical Characteristics (V_{CC} = + 5V, V_{EE} = - 5V, V_{cm} = 2.25V, C_L = 5pF, V_o = 4V_{pp} unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS		UNITS	NOTES
Ambient Temperature	CLC503	+25˚C	+25˚C	-40 to 85˚C		
FREQUENCY DOMAIN RESPONSE						
Differential Amp						
large signal bandwidth	V_o < 4.0V_{pp}	180	80	70	MHz	
gain flatness	DC to 10MHz	0.3	0.5	0.5	dB	
Common-Mode Amp						
-3dB bandwidth	V_o < 4.0V_{pp}	15	10	10	MHz	
TIME DOMAIN RESPONSE						
Differential Amp						
rise and fall time	2V step	2.1	2.5	3.0	ns	
settling time to 0.1%	2V step	15	22	25	ns	
overshoot	2V step	0			%	
slew rate	2V step	800	500	500	V/µs	
Common-Mode Amp						
recovery from power down	0.1% output settling	40	100	100	ns	
DISTORTION AND NOISE RESPONSE						
2nd harmonic distortion	4V_{pp}, 1MHz	-78	-74	-70	dBc	B
	4V_{pp}, 10MHz	-75	-71	-71	dBc	B
3rd harmonic distortion	4V_{pp}, 1MHz	-85	-80	-79	dBc	B
	4V_{pp}, 10MHz	-77	-72	-72	dBc	B
SNR	4V_{pp}	72	71	70	dB	
integrated output noise voltage	R_s = 50Ω					
	10kHz – 500MHz	325	380	460	µV_{rms}	
STATIC DC PERFORMANCE						
Differential Amp						
gain	V_o(Diff)/V_{in}	2	1.75 - 2.25	1.75 - 2.25	V/V	A
output offset voltage	V_{in} = 0	10	90	100	mV	A
INL		0.015	0.03	0.05	%	A
R_{in}		2	1.6 - 2.4	1.6 - 2.4	kΩ	
Common-Mode Amp						
gain	V_{ocm}/V_{cm}	0.97	0.9 - 1.1	0.9 - 1.1	V/V	
output offset voltage		100	200	200	mV	A
R_{in}		10	5	5	MΩ	
input voltage range		1.5 - 3.5			V	
power supply rejection ratio	DC	50	30	30	dB	A
supply current	R_L = ∞	25	30	30	mA	A
supply current, power down		4.5	6	6	mA	A
MISCELLANEOUS PERFORMANCE						
power down input	CMOS levels	0.5 - 4.8			V	C
V_{IL}	on	1			V	
V_{IH}	off	4.5			V	C
power down dissipation	P_{DN} = “Hi”	45	60	60	mW	A
output voltage range	single output	0.7 - 3.9	0.85 - 3.7	0.9 - 3.5	V	
differential output resistance		500	400 - 600	375 - 625	Ω	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

supply voltage	±6V
maximum input range	±6V
maximum output range (±V)	0 to V_{CC}
maximum operating temperature range	-40˚C to +85˚C
maximum junction temperature	+175˚C
maximum storage temperature range	-65˚C to +150˚C
maximum lead temperature (soldering 10 sec)	+300˚C
ESD rating (human body model)	500V

Recommended Operating Conditions

supply voltage	±4.5 to ±5.5Vdc
input voltage	±1V
output voltage	+0.8 to +3.75V
ambient temperature range	-40°C to +85°C

Notes

A) J-level: spec is 100% tested at +25˚C, sample tested at +85˚C.
LC/MC-level: spec is 100% wafer probed at +25˚C.
B) J-level: spec is sample tested at +25˚C.
C) **POWER DOWN** must be 1V higher than V_{cm}.

Ordering Information

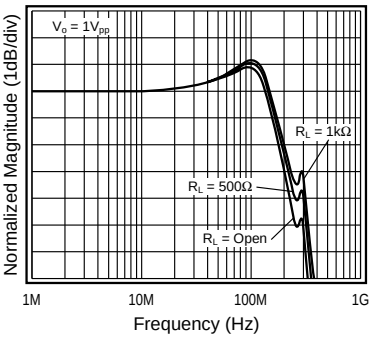
Model	Temperature Range	Description
CLC503AJE	-40°C to +85°C	8-pin SOIC

Package Thermal Resistance

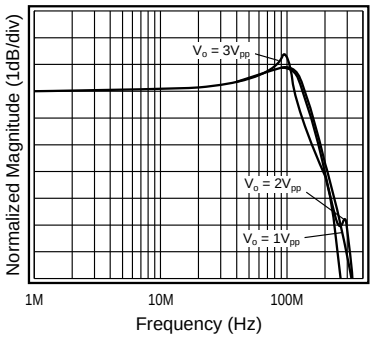
Package	θ_{JC}	θ_{JA}
SOIC (AJE)	65°C/W	90°C/W

Typical Performance Characteristics (V_{CC} = + 5V, V_{EE} = - 5V, V_{cm} = 2.25V, C_L = 5pF, V_o = 4V_{pp} unless specified)

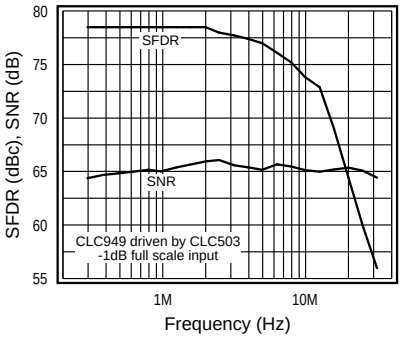
Frequency Response vs. R_L



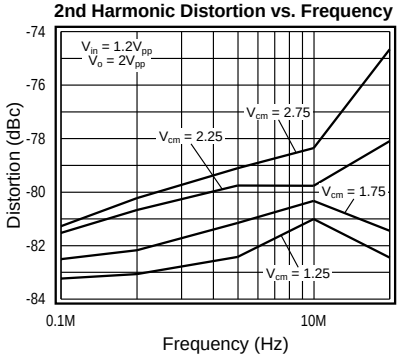
Frequency Response vs. V_o



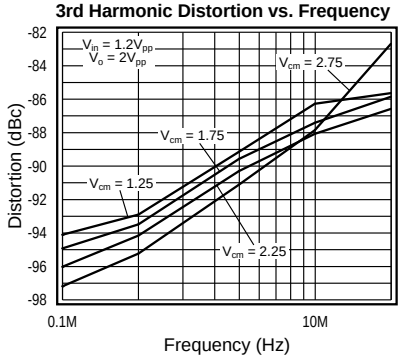
SNR and SFDR



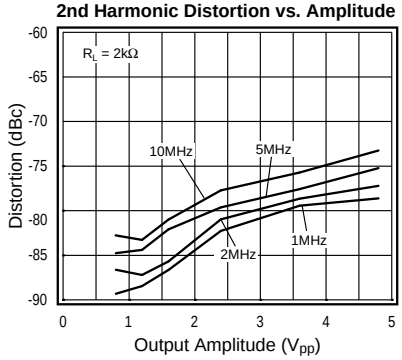
2nd Harmonic Distortion vs. Frequency



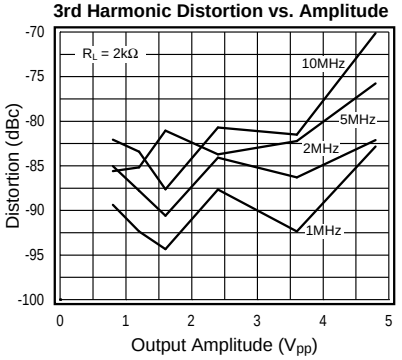
3rd Harmonic Distortion vs. Frequency



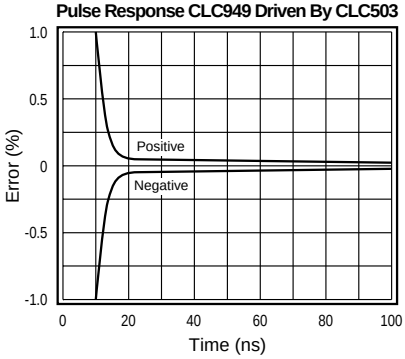
2nd Harmonic Distortion vs. Amplitude



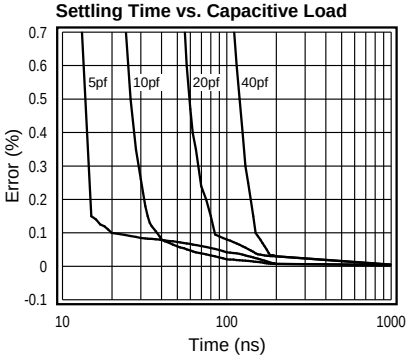
3rd Harmonic Distortion vs. Amplitude



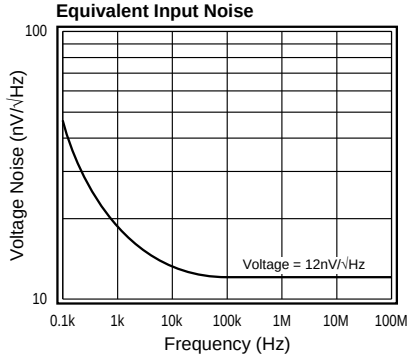
Pulse Response CLC949 Driven By CLC503



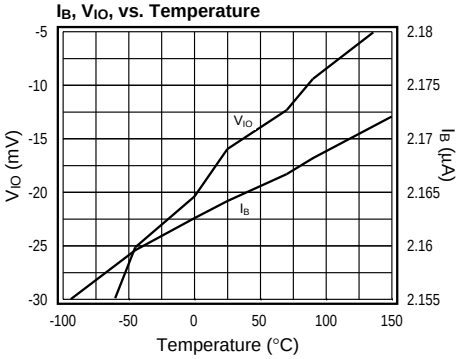
Settling Time vs. Capacitive Load



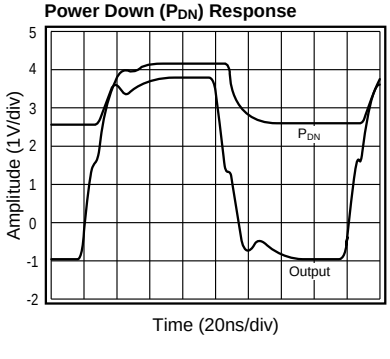
Equivalent Input Noise



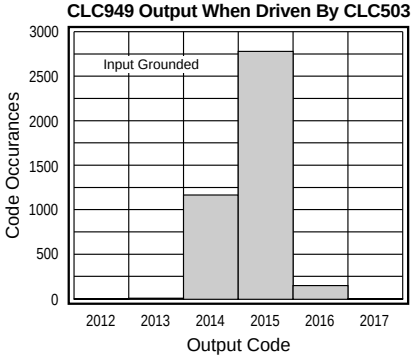
I_B, V_{IO}, vs. Temperature



Power Down (P_{DN}) Response



CLC949 Output When Driven By CLC503



APPLICATION CONSIDERATIONS

Theory of Operation

Figure 1 is a simplified schematic of the CLC503.

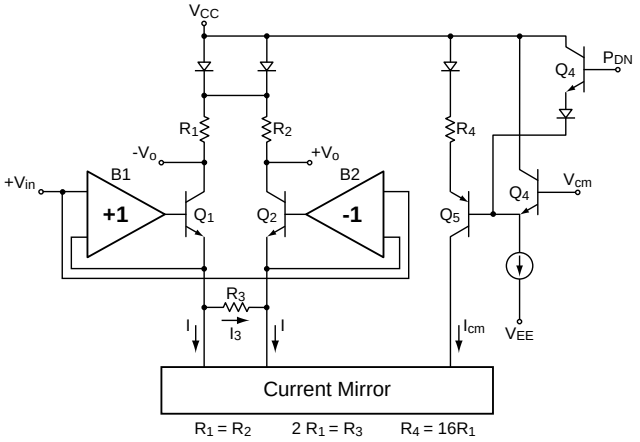


Figure 1: Simplified Block Diagram

The input voltage drives a unity gain buffer, B_1, and an inverting buffer, B_2. These buffers drive emitter followers, Q_1 and Q_2. Resistor, R_3, is the gain set resistor. The combination of B_1, B_2, Q_1, Q_2 and R_3 form a transconductance stage. The input voltage across R_3 is converted to an in-phase and out-of-phase current through the collectors of Q_1 and Q_2. The current through R_3 is:

$$I_3 = \frac{2V_{in}}{R_3}$$

$$V_{odiff} = I_3R_1 + I_3R_2 \qquad R_1 = R_2$$

$$V_{odiff} = I_3(2R_1)$$

$$V_{odiff} = \frac{2V_{in}}{R_3}(2R_1) \qquad 2R_1 = R_3$$

$$V_{odiff} = 2V_{in}$$

The common mode voltage across R_4 is converted to a current. Transistor Q_5 has a collector current equal to:

$$I_{cm} \approx \frac{V_{CC} - V_{cm} - V_{diode}}{R_4} \qquad R_4 = 16R_1$$

The common mode current is scaled and mirrored back to Q_1 and Q_2. These currents, I, are converted back to a voltage at the collector load resistors, R_1 and R_2. This forms the common-mode output voltage.

$$\frac{I = V_{CC} - V_{cm} - V_{diode}}{R_1}$$

$$V_{ocm} = V_{CC} - V_{diode} - R_1I$$

$$I = 16I_{cm}$$

$$V_{ocm} = V_{cm}$$

Figure 2 depicts the differential output voltage limits of the CLC503.

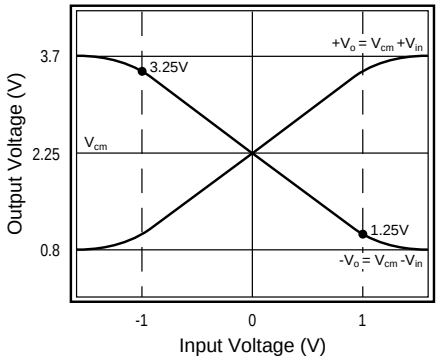


Figure 2: Differential Output Voltage

Centered around V_{cm}, the outputs are derived from the following equations.

$$+V_o = V_{cm} + V_{in}$$

$$-V_o = V_{cm} - V_{in}$$

$$V_{odiff} = +V_o - (-V_o) = 2V_{in}$$

The input to output relationship is shown in Figure 3.

V_{in}	V_{odiff}
±1V $2V_{pp}$ ±1.4V max	±2V $4V_{pp}$ ±2.8V max

Figure 3: Input vs. Output Relationship

Pulling the power down line (P_{DN}) high decreases the quiescent supply current. This turns off the current flowing in Q_5, and therefore Q_1 and Q_2, allowing the output voltages to drift high, to approximately 4.3V. Since the signal is not significantly attenuated, P_{DN} does not effectively isolate the input from the output. This part is not recommended for use as a multiplexer. Refer to ***Pin Descriptions - Power Down pin*** - section. No damage occurs to the device when P_{DN} is high and the input is driven to the supply voltage.

Pin Descriptions

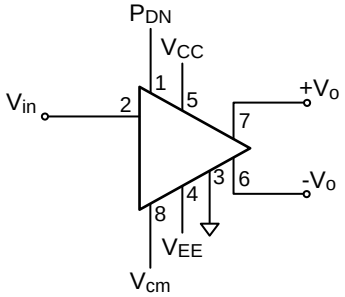


Figure 4: CLC503 Functional Pin Descriptions

■ **Pin 1**

Power Down (P_{DN}): The power down pin takes CMOS input levels. Use this to decrease the power from 250mW to 40mW. This is not a signal disable pin. A CMOS gate will drive this input. The quiescent supply current will be decreased when P_{DN} is at least 1V higher than V_{cm}. When the current is turned off, the output voltage V_o, will go to approximately 4.3V. An internal pull down resistor of 10k allows P_{DN} to be left open when not used.

■ **Pin 2**

Input Voltage (V_{in}): This is the signal input. The recommended input range is ±1V. The linear operating range is approximately ±1.4V This input controls the differential output voltage. Because of the closed loop nature of the trans-conductance stage, the transfer function is highly linear. Refer to ***Output Voltage*** pin for output signal limitations.

■ **Pin 3**

Ground (GND): Tie to low impedance analog ground.

■ **Pins 4 and 5**

Power Supplies (V_{EE} and V_{CC}): For optimum performance, use linear ±5V power supplies. Use bypass capacitors of 0.1µF and 6.8µF on the power supply lines to decrease any noise that could be injected into the circuit by the power supplies. Place the bypass capacitors as close to the device pins as possible. Remove the ground plane from the board underneath the device to eliminate parasitic capacitance. Refer to ***Printed Circuit Board Layout*** section for more layout suggestions.

■ **Pins 6 and 7**

Output Voltage ($-V_o$ and $+V_o$): These are the differential signal output pins. The output voltage at these pins is limited to 0.7V to 3.9V. The output recovery time after exceeding these limits is approximately 40ns. The output voltage can be defined as:

$$+V_o = V_{cm} + V_{in}$$
$$-V_o = V_{cm} - V_{in}$$
$$V_{odiff} = +V_o - (-V_o) = 2V_{in}$$
$$V_{ocm} = \frac{+V_o - (-V_o)}{2} = V_{cm}$$

■ **Pin 8**

Common-Mode Voltage (V_{cm}): This input sets the common-mode output operating points. The common mode input voltage can range from 1.5V to 3.5V. Refer to ***Output Voltage*** pin discussion for limitations on the output range.

Design Information

Load: The CLC503 is intended to drive high speed CMOS analog-to-digital converters, such as the CLC949. Resistive loading will affect the gain and common mode offset. It is not recommended to drive resistive loads below 10kΩ with this part. See Figure 5 for gain vs. load with specified range in device output resistance.

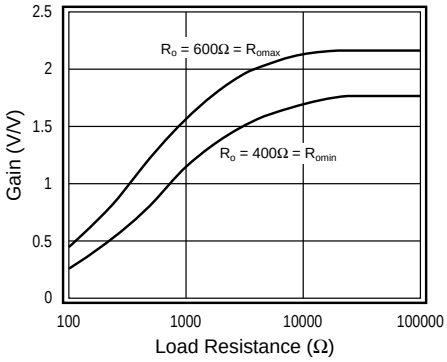


Figure 5: Gain vs. Resistive Load

Settling Time: The CLC503 settles to 0.1% in 15ns with a 5pF load, the input capacitance of the CLC949. Refer to the ***Settling Time vs. Capacitive Load*** plot in the ***Typical Performance Characteristics*** section.

Power Dissipation

To calculate the power dissipation, P_T, for the CLC503, use the following equation:

$$P_T = I_{CC}\left(V_{CC} - V_{EE}\right)$$

Printed Circuit Board Layout

The performance of the CLC503 is strongly dependent on proper layout, and adequate power supply decoupling. The parasitic capacitance at the output of the CLC503 and the input to the CLC949, or any other analog-to-digital converter, must be kept to a minimum. Consider the following guidelines:

- Use a ground plane.
- Bypass power supply pins with monolithic capacitors of 0.1µF and with 6.8µF tantalum capacitors. Place the capacitors less than 0.1" (3mm) from the pin.
- Remove the ground plane underneath the device and 0.1" (3mm) from all input/output pads.

Interfacing the CLC503 with the CLC949

The CLC503 can be easily interfaced with the CLC949 as shown in Figure 6. An evaluation board is available for proto-typing and measurements.

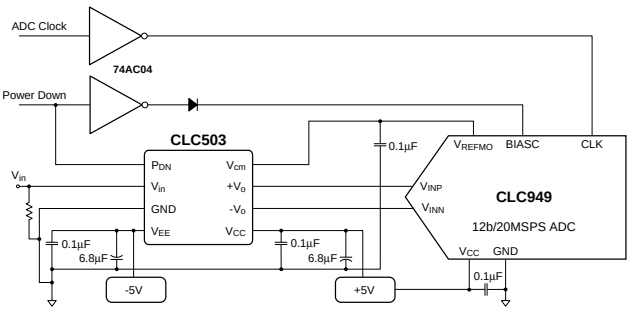


Figure 6: Interfacing the CLC503 with the CLC949

Extended Use Considerations

Designed to drive the CLC949, the CLC503 can be used with other analog-to-digital converters. The user will want to consider the following parameters of the device that the CLC503 will drive.

- Input impedance of the A/D. Refer to Figure 5 for the Gain vs. Resistive Load. The CLC503 operates best when driving resistive loads greater than 10kΩ and capacitive loads of less than 10pF.
- Resistive loading will affect the gain and common mode offset. The gain setting resistors are fixed internally. The voltage gain equation is:

$$A_{V_{new}} = A_{V_{old}}\left(\frac{500\Omega \,||\, R_L}{500\Omega}\right)$$

where R_L equals the input resistance of the A/D. The impact of lower values of R_L is shown in Figure 5. The tolerance on the 500Ω is ±20%.

- Capacitive loading will affect the settling time. The settling time equation is:

$$t_{settle} = R_s \cdot C_L \cdot \ln\left(\frac{100\%}{\%settling}\right)$$

where R_s = 250Ω ±15% and %settling ≥ 0.1%. Refer to the ***Settling Time vs. Capacitive Load*** plot in the ***Typical Performance Characteristics*** section.

- Other considerations
  - Output signal swing must be within the specified output range.
  - Common mode range must meet the specified common mode range.
  - Distortion will be affected when V_{in} and V_{cm} drive the output out of the linear operating range.

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