CM1421

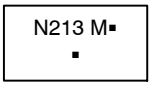
4-Channel LCD EMI Filter Array and ESD Protection Array

ON Semiconductor®

http://onsemi.com

WLCSP15
CP SUFFIX
CASE 567BS

MARKING DIAGRAM



N213 = CM1421−03CP
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
CM1421−03CP	CSP−15 (Pb−Free)	3500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Product Description

The CM1421 is a multichannel array consisting of four low−pass filters with integrated ESD protection and four ESD−only protection channels designed to reduce EMI/RFI emissions on LCD data lines in mobile handsets. The CM1421 has component values of 15 pF − 100 Ω − 15 pF. These devices include ESD protection diodes on every pin, which provide a very high level of protection for sensitive electronic components that may be subjected to electrostatic discharge (ESD). The ESD diodes connected to the filter ports safely dissipate ESD strikes of ±15 kV, exceeding the maximum requirement of the IEC 61000−4−2 international standard. Using the MIL−STD−883 (Method 3015) specification for Human Body Model (HBM) ESD, the pins are protected for contact discharges at greater than ±30 kV.

This device is particularly well−suited for portable electronics (e.g. wireless handsets, PDAs, notebook computers) because of its small package and easy−to−use pin assignments. In particular, the CM1421 is ideal for EMI filtering and protecting data lines from ESD for the LCD display in clamshell handsets.

The CM1421 incorporates *OptiGuard*™ coating which results in improved reliability. The CM1421 is available in space−saving, low−profile chip scale packages with RoHS−compliant lead−free finishing.

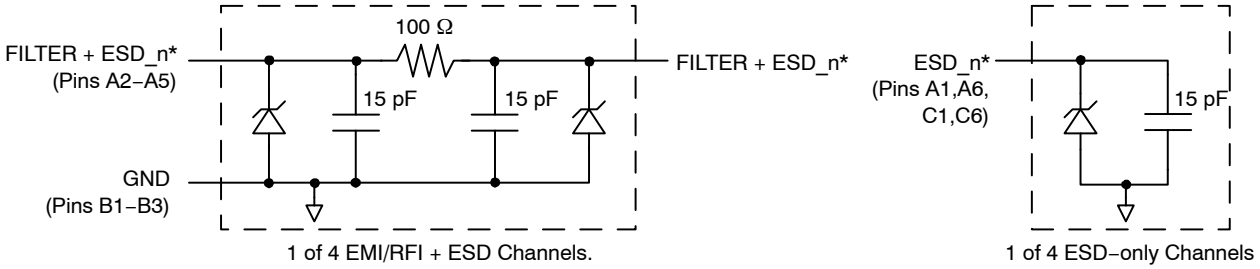
Features

- Functionally and Pin−Compatible with CSPEMI607 Device
- Four Channels of Combined EMI/RFI Filtering + ESD Protection
- Four Additional Channels of ESD−Only Protection
- Better Than 30 dB Attenuation (Typical) at 1 GHz
- ±15 kV ESD Protection on All Channels (IEC 61000−4−2 Level 4, Contact Discharge)
- ±30 kV ESD Protection on All Channels (HBM)
- Chip Scale Package Features Extremely Low Lead Inductance for Optimum Filter and ESD Performance
- 15−Bump, 2.960 mm X 1.330 mm Footprint
- *OptiGuard*™ Coated for Improved Reliability
- These Devices are Pb−Free and are RoHS Compliant

Applications

- LCD Data Lines in Mobile Handsets
- EMI Filtering and ESD Protection for Both Data and I/O Ports
- Mobile Handsets
- Handheld PCs / PDAs
- Notebook Computers

BLOCK DIAGRAM

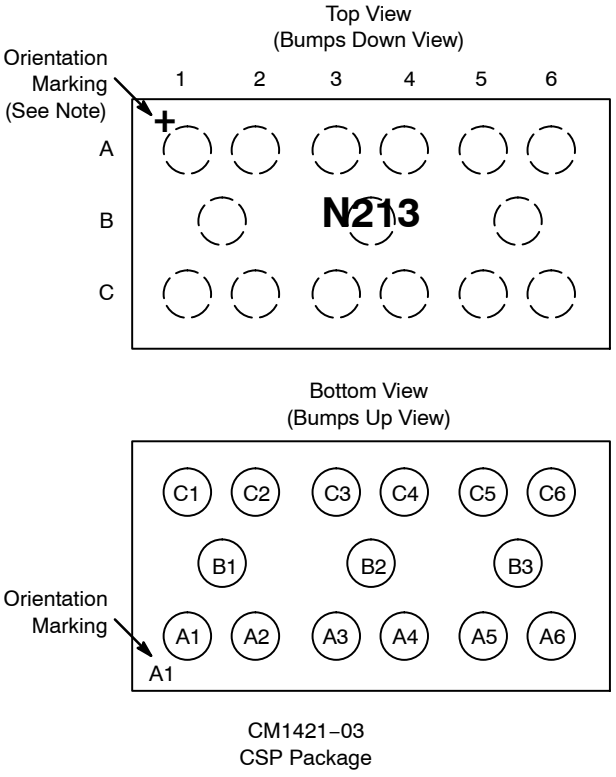


*See Package/Pinout Diagrams for expanded pin information.

Table 1. PIN DESCRIPTIONS

15−bump CSP Package		
Pin	**Name**	**Description**
A1	ESD_1	ESD Channel 1
A2	FILTER + ESD_1	Filter + ESD Channel 1
A3	FILTER + ESD_2	Filter + ESD Channel 2
A4	FILTER + ESD_3	Filter + ESD Channel 3
A5	FILTER + ESD_4	Filter + ESD Channel 4
A6	ESD_2	ESD Channel 2
B1−B3	GND	Device Ground
C1	ESD_3	ESD Channel 3
C2	FILTER + ESD_1	Filter + ESD Channel 1
C3	FILTER + ESD_2	Filter + ESD Channel 2
C4	FILTER + ESD_3	Filter + ESD Channel 3
C5	FILTER + ESD_4	Filter + ESD Channel 4
C6	ESD_4	ESD Channel 4

PACKAGE / PINOUT DIAGRAMS



CM1421−03
CSP Package

Note: Lead−free devices are specified by using a “+” character for the top side orientation mark.

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Storage Temperature Range	−65 to +150	°C
DC Power per Resistor	100	mW
DC Package Power Rating	500	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	−40 to +85	°C

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R	Resistance		80	100	120	Ω
C	Capacitance	At 2.5 V DC	12	15	18	pF
V_{DIODE}	Diode Standoff Voltage	I_{DIODE} = 10 μA		6.0		V
I_{LEAK}	Diode Leakage Current (reverse bias)	V_{DIODE} = +3.3 V		100	300	nA
V_{SIG}	Signal Voltage Positive Clamp Negative Clamp	I_{LOAD} = 10 mA	 5.6 −1.5	 6.8 −0.8	 9.0 −0.4	V
V_{ESD}	In−system ESD Withstand Voltage a) Human Body Model, MIL−STD−883, Method 3015 b) Contact Discharge per IEC 61000−4−2 Level 4	(Note 2)	 ±30 ±15			kV
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients			 1.6 0.44		V
f_C	Cut−off Frequency Z_{SOURCE} = 50 Ω, Z_{LOAD} = 50 Ω	R = 100 Ω, C = 15 pF		120		MHz

1. T_A = 25°C unless otherwise specified.
2. ESD applied to input and output pins with respect to GND, one at a time.

PERFORMANCE INFORMATION

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

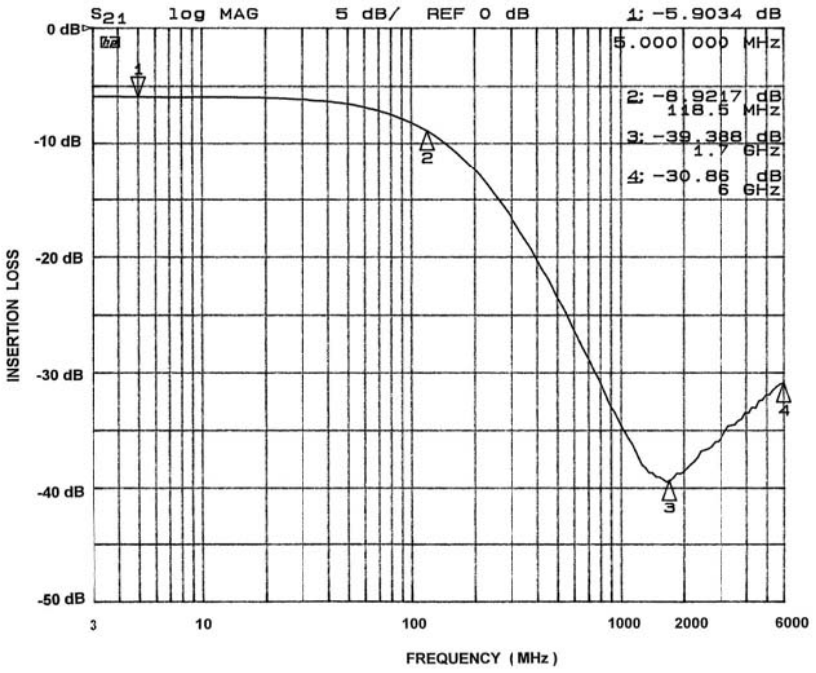


Figure 1. Insertion Loss vs. Frequency (A1−C1 to GND B1)

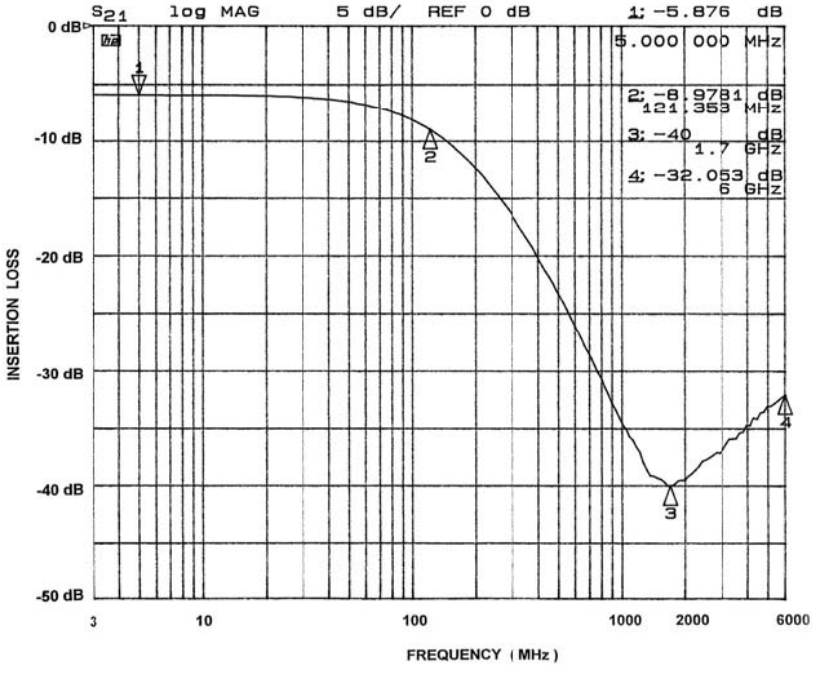


Figure 2. Insertion Loss vs. Frequency (A2−C2 to GND B1)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

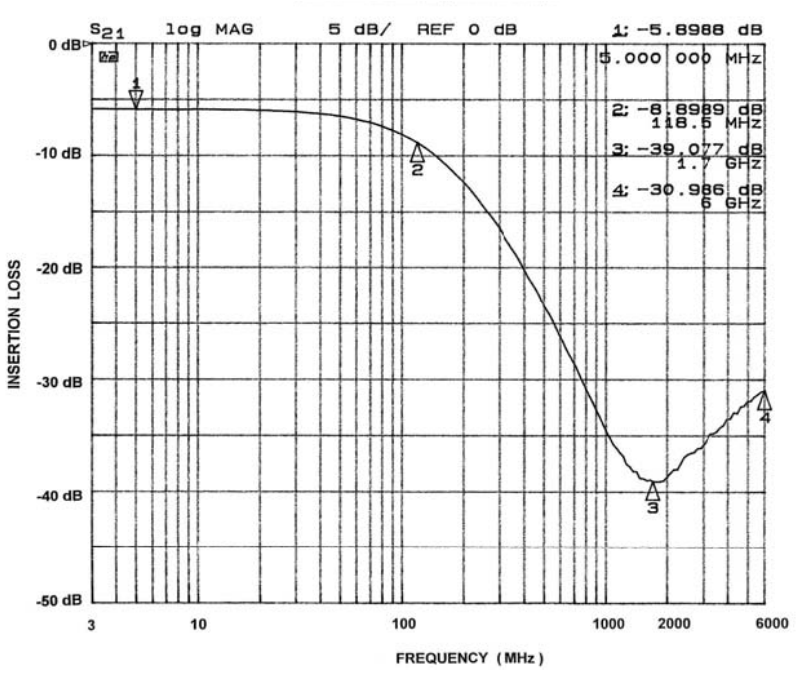


Figure 3. Insertion Loss vs. Frequency (A3−C3 to GND B2)

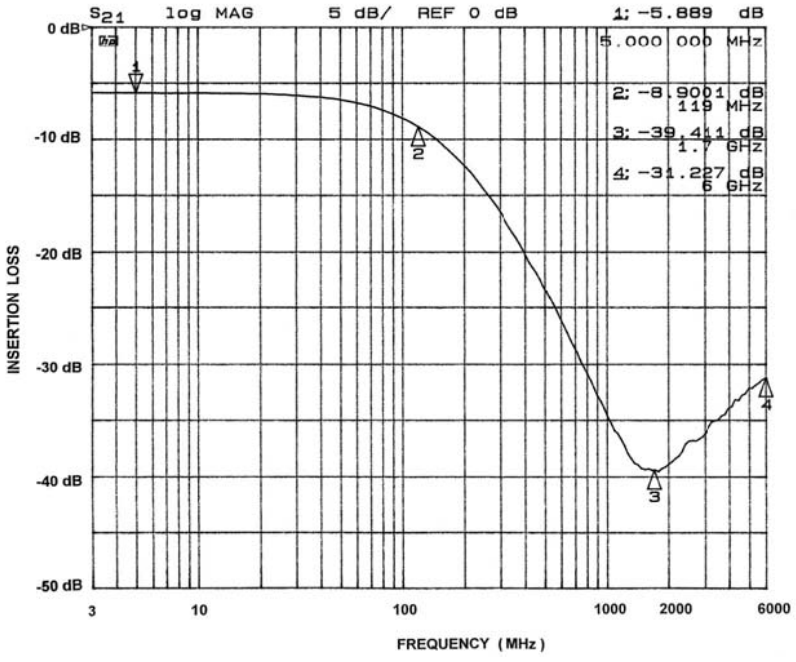


Figure 4. Insertion Loss vs. Frequency (A4−C4 to GND B2)

PERFORMANCE INFORMATION (Cont'd)

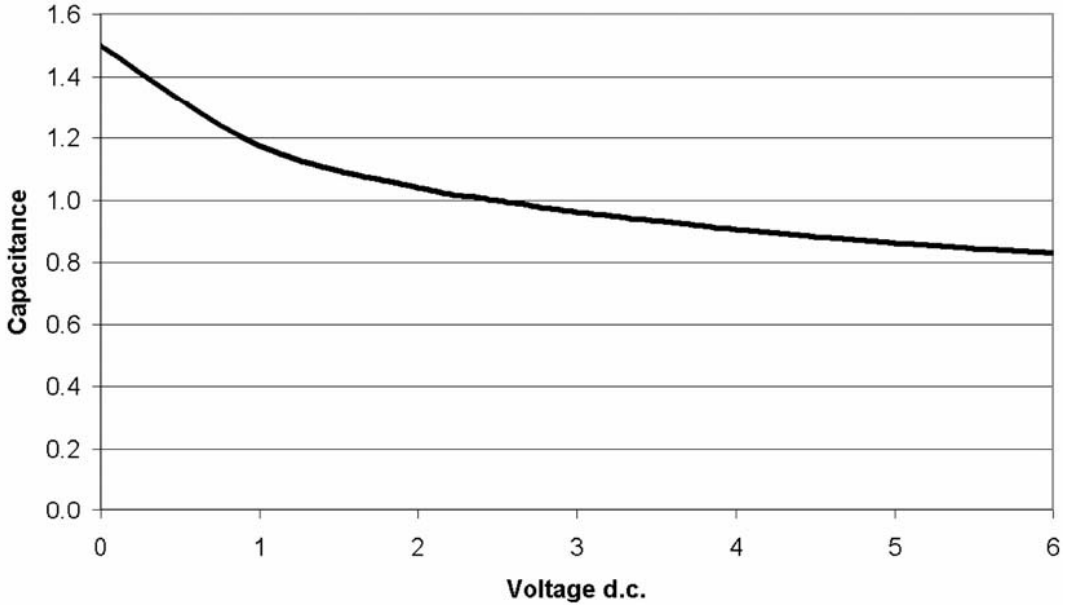


Figure 5. Filter Capacitance vs. Input Voltage (normalized to capacitance at 2.5 VDC and 25°C)

APPLICATION INFORMATION

Table 5. PRINTED CIRCUIT BOARD RECOMMENDATIONS

Parameter	Value
Pad Size on PCB	0.240 mm
Pad Shape	Round
Pad Definition	Non−Solder Mask defined pads
Solder Mask Opening	0.290 mm Round
Solder Stencil Thickness	0.125 − 0.150 mm
Solder Stencil Aperture Opening (laser cut, 5% tapered walls)	0.300 mm Round
Solder Flux Ratio	50/50 by volume
Solder Paste Type	No Clean
Pad Protective Finish	OSP (Entek Cu Plus 106A)
Tolerance − Edge To Corner Ball	±50 μm
Solder Ball Side Coplanarity	±20 μm
Maximum Dwell Time Above Liquidous	60 seconds
Maximum Soldering Temperature for Lead−free Devices using a Lead−free Solder Paste	260°C

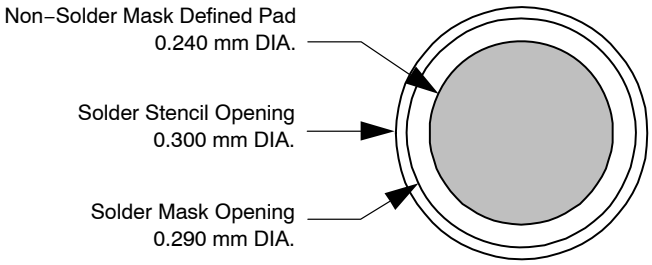


Figure 6. Recommended Non−Solder Mask Defined Pad Illustration

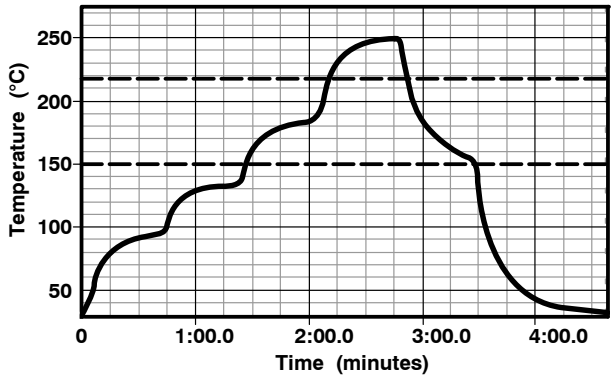
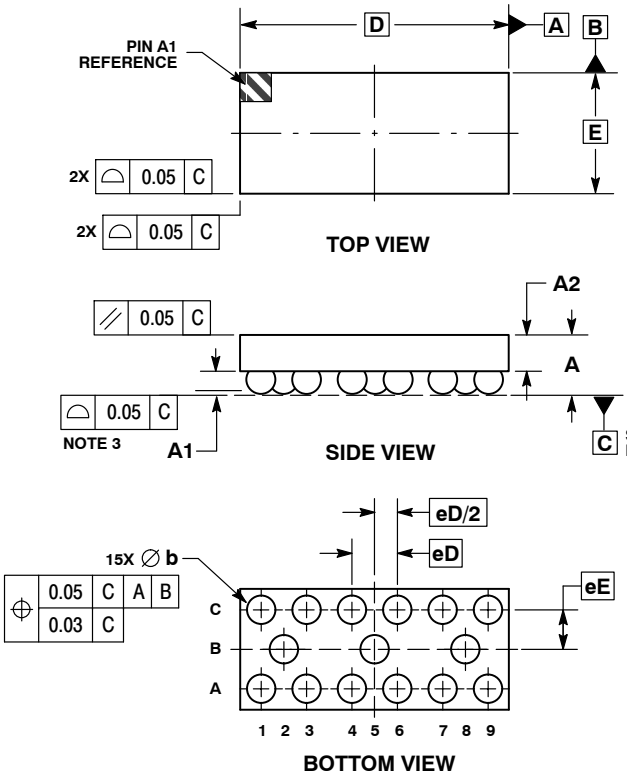


Figure 7. Lead−free (SnAgCu) Solder Ball Reflow Profile

PACKAGE DIMENSIONS

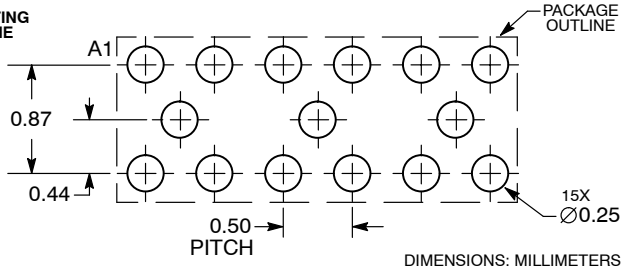
WLCSP15, 2.96x1.33
CASE 567BS−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.56	0.65
A1	0.21	0.27
A2	0.40 REF	
b	0.29	0.35
D	2.96 BSC	
E	1.33 BSC	
eD	0.50 BSC	
eE	0.435 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
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