



### Features

- HDMI 1.3 compliant
- Supports thin dielectric and 2-layer boards
- Minimizes TMDS skew with 0.05pF matching
- Long HDMI cable support with integrated I<sup>2</sup>C accelerator
- Active termination and slew rate limiting for CEC
- Supports direct connection to CEC microcontroller
- Integrated I<sup>2</sup>C level shifting to CMOS level including low logic level voltages
- Integrated 8kV ESD protection and backdrive protection on all external I/O lines
- Integrated overcurrent output protection per HDMI 1.3
- Multiport I<sup>2</sup>C support eliminates need for analog mux on DDC lines
- Simplified layout with matched 0.5mm trace spacing
- RoHS-compliant, lead-free packaging

### Applications

- PC and consumer electronics
- Set top box, DVD RW, PC, graphics cards

### Product Description

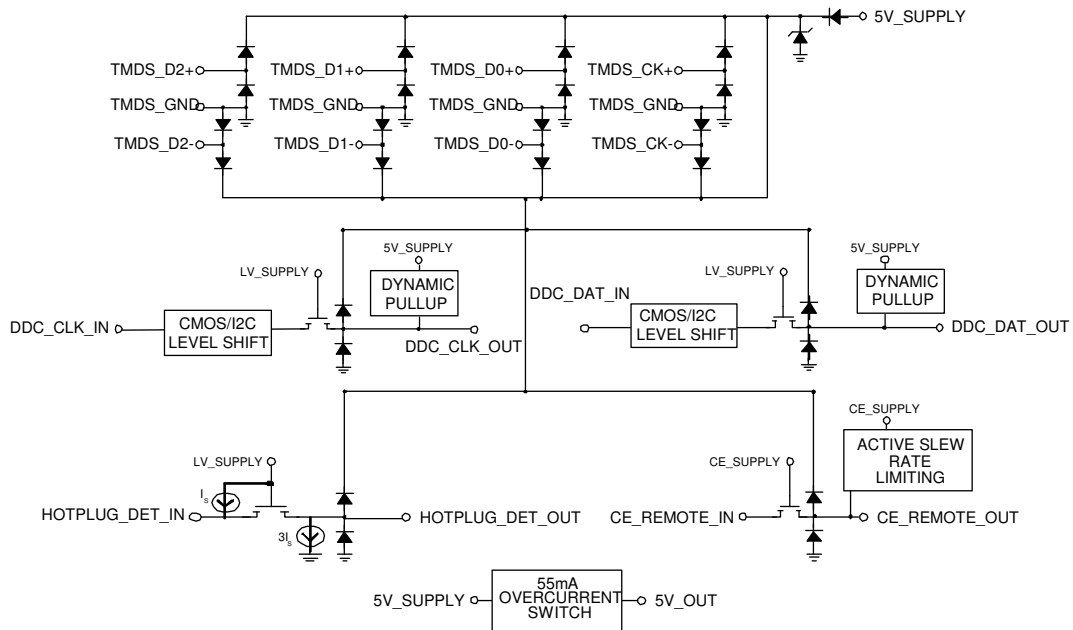
The CM2030 HDMI Transmitter Port Protection and Interface Device is specifically designed for next generation HDMI Host interface protection.

An integrated package provides all ESD, slew rate limiting on CEC line, level shifting/isolation, overcurrent output protection and backdrive protection for an HDMI port in a single 38-pin TSSOP package.

The CM2030 part is specifically designed to provide the designer with the most reliable path to HDMI 1.3 CTS compliance.

The CM2030 also incorporates a silicon overcurrent protection device for +5V supply voltage output to the connector.

**Electrical Schematic**



**PACKAGE / PINOUT DIAGRAM**

**TOP VIEW**

|                |    |    |                 |
|----------------|----|----|-----------------|
| 5V_SUPPLY      | 1  | 38 | 5V_OUT          |
| LV_SUPPLY      | 2  | 37 | CE_SUPPLY       |
| GND            | 3  | 36 | GND             |
| TMDS_D2+       | 4  | 35 | TMDS_D2+        |
| TMDS_GND       | 5  | 34 | TMDS_GND        |
| TMDS_D2-       | 6  | 33 | TMDS_D2-        |
| TMDS_D1+       | 7  | 32 | TMDS_D1+        |
| TMDS_GND       | 8  | 31 | TMDS_GND        |
| TMDS_D1-       | 9  | 30 | TMDS_D1-        |
| TMDS_D0+       | 10 | 29 | TMDS_D0+        |
| TMDS_GND       | 11 | 28 | TMDS_GND        |
| TMDS_D0-       | 12 | 27 | TMDS_D0-        |
| TMDS_CK+       | 13 | 26 | TMDS_CK+        |
| TMDS_GND       | 14 | 25 | TMDS_GND        |
| TMDS_CK-       | 15 | 24 | TMDS_CK-        |
| CE_REMO TE_IN  | 16 | 23 | CE_REMO TE_OUT  |
| DDC_CLK_IN     | 17 | 22 | DDC_CLK_OUT     |
| DDC_DAT_IN     | 18 | 21 | DDC_DAT_OUT     |
| HOTPLUG_DET_IN | 19 | 20 | HOTPLUG_DET_OUT |

Note: This drawing is not to scale.

38-PIN TSSOP PACKAGE

## PIN DESCRIPTIONS

|   |                 | ESD Level          | DESCRIPTION   |
|---|-----------------|--------------------|---|
| 4, 35                                     | TMDS_D2+        | 8kV <sup>3</sup>   | TMDS 0.9pF ESD protection. <sup>1</sup>   |
| 6, 33                                     | TMDS_D2-        | 8kV <sup>3</sup>   | TMDS 0.9pF ESD protection. <sup>1</sup>   |
| 7, 32                                     | TMDS_D1+        | 8kV <sup>3</sup>   | TMDS 0.9pF ESD protection. <sup>1</sup>   |
| 9, 30                                     | TMDS_D1-        | 8kV <sup>3</sup>   | TMDS 0.9pF ESD protection. <sup>1</sup>   |
| 10, 29                                    | TMDS_D0+        | 8kV <sup>3</sup>   | TMDS 0.9pF ESD protection. <sup>1</sup>   |
| 12, 27                                    | TMDS_D0-        | 8kV <sup>3</sup>   | TMDS 0.9pF ESD protection. <sup>1</sup>   |
| 13, 26                                    | TMDS_CK+        | 8kV <sup>3</sup>   | TMDS 0.9pF ESD protection. <sup>1</sup>   |
| 15, 24                                    | TMDS_CK-        | 8kV <sup>3</sup>   | TMDS 0.9pF ESD protection. <sup>1</sup>   |
| 16  | CE_REMOTE_IN    | 2kV <sup>4</sup>   | CE_SUPPLY referenced logic level in.  |
| 23  | CE_REMOTE_OUT   | 8kV <sup>3</sup>   | 5V_SUPPLY referenced logic level out plus 10pF ESD. <sup>6</sup>  |
| 17  | DDC_CLK_IN      | 2kV <sup>4</sup>   | LV_SUPPLY referenced logic level in.  |
| 22  | DDC_CLK_OUT     | 8kV <sup>3</sup>   | 5V_SUPPLY referenced logic level out plus 10pF ESD. <sup>6</sup>  |
| 18  | DDC_DAT_IN      | 2kV <sup>4</sup>   | LV_SUPPLY referenced logic level in.  |
| 21  | DDC_DAT_OUT     | 8kV <sup>3</sup>   | 5V_SUPPLY referenced logic level out plus 10pF ESD. <sup>6</sup>  |
| 19  | HOTPLUG_DET_IN  | 2kV <sup>4</sup>   | LV_SUPPLY referenced logic level in.  |
| 20  | HOTPLUG_DET_OUT | 8kV <sup>3</sup>   | 5V_SUPPLY referenced logic level out plus 10pF ESD. A 0.1μF bypass ceramic capacitor is recommended on this pin. <sup>2</sup> |
| 2   | LV_SUPPLY       | 2kV <sup>4</sup>   | Bias for CE / DDC / HOTPLUG level shifters.   |
| 37  | CE_SUPPLY       | 2kV <sup>4,2</sup> | CEC bias voltage. Previously CM2020 ESD_BYN pin.  |
| 1   | 5V_SUPPLY       | 2kV <sup>4</sup>   | Current source for 5V_OUT, VREF for DDC I <sup>2</sup> C voltage references, and bias for 8kV ESD pins.                       |
| 38  | 5V_OUT          | 8kV <sup>3</sup>   | 55mA minimum overcurrent protected 5V output. This output must be bypassed with a 0.1μF ceramic capacitor.                    |
| 3, 5, 8, 11,<br>14, 25,<br>28, 31, 34, 36 | GND / TMDS_GND  | N/A                | GND reference.  |

Note 1: These 2 pins need to be connected together in-line on the PCB. See recommended layout diagram.

Note 2: This output can be connected to an external 0.1μF ceramic capacitor/pads to maintain backward compatibility with the CM2020.

Note 3: Standard IEC 61000-4-2, C<sub>DISCHARGE</sub>=150pF, R<sub>DISCHARGE</sub>=330Ω, 5V\_SUPPLY and LV\_SUPPLY within recommended operating conditions, GND=0V, 5V\_OUT (pin 38), and HOTPLUG\_DET\_OUT (pin 20) each bypassed with a 0.1μF ceramic capacitor connected to GND.

Note 4: Human Body Model per MIL-STD-883, Method 3015, C<sub>DISCHARGE</sub>=100pF, R<sub>DISCHARGE</sub>=1.5kΩ, 5V\_SUPPLY and LV\_SUPPLY within recommended operating conditions, GND=0V, 5V\_OUT (pin 38), and HOTPLUG\_DET\_OUT (pin 20) each bypassed with a 0.1μF ceramic capacitor connected to GND.

Note 5: These pins should be routed directly to the associated GND pins on the HDMI connector with single point ground vias at the connector.

Note 6: The slew-rate control and active acceleration circuitry dynamically offsets the system capacitive load on these pins.

## Backdrive Protection and Isolation

Backdrive current is defined as the undesirable current flow through an I/O pin when that I/O pin's voltage exceeds the related local supply voltage for that circuitry. This is a potentially common occurrence in multimedia entertainment systems with multiple components and several power plane domains in each system.

For example, if a DVD player is switched off and an HDMI connected TV is powered on, there is a possibility of reverse current flow back into the main power supply rail of the DVD player from pull-ups in the TV. As little as a few milliamps of backdrive current flowing back into the power rail can charge the DVD player's bulk bypass capacitance on the power rail to some intermediate level. If this level rises above the power-on-reset (POR) voltage level of some of the integrated circuits in the DVD player, then these devices may not reset properly when the DVD player is turned back on.

If any SOC devices are incorporated in the design which have built-in level shifter and/or ESD protection structures, there can be a risk of permanent damage due to backdrive. In this case, backdrive current can forward bias the on-chip ESD protection structure. If the current flow is high enough, even as little as a few milliamps, it could destroy one of the SOC chip's internal DRC diodes, as they are not designed for passing DC.

To avoid either of these situations, the CM2030 was designed to block backdrive current, guaranteeing less than 5 $\mu$ A into any I/O pin when the I/O pin voltage exceeds its related operating CM2030 supply voltage.

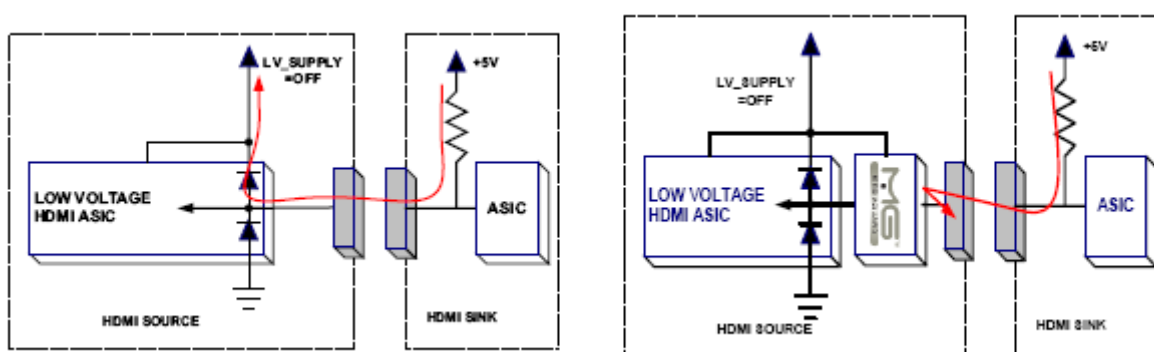


Figure 1. Backdrive Protection Diagram.

## Display Data Channel (DDC) lines

The DDC interface is based on the I<sup>2</sup>C serial bus protocol for EDID configuration.

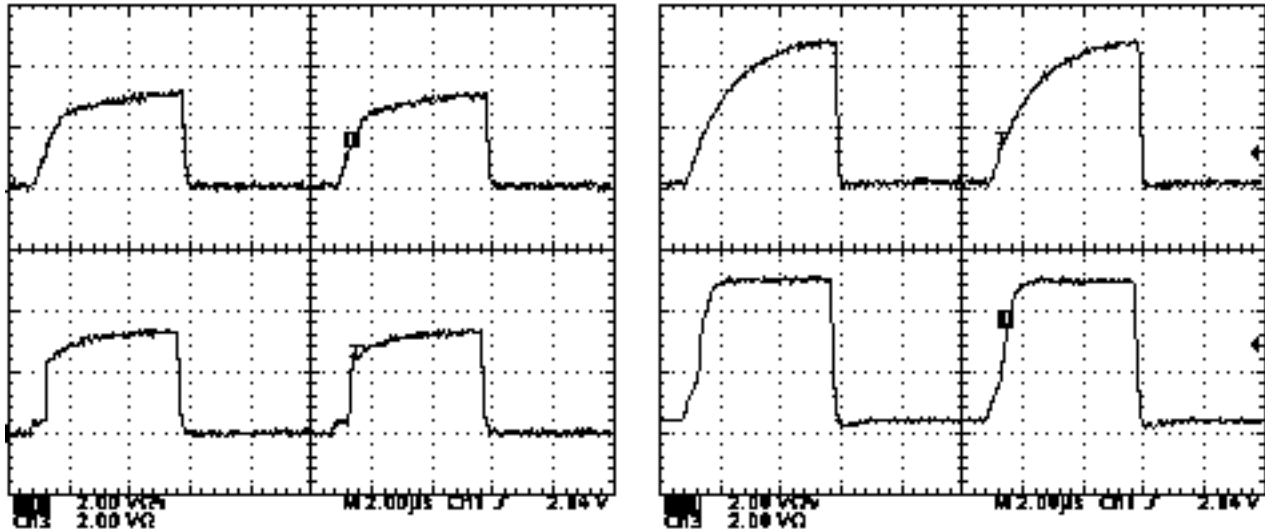
### DYNAMIC PULLUPS

Based on the HDMI specification, the maximum capacitance of the DDC line can approach 800pF (50pF from source, 50pF from sink, and 700pF from cable). At the upper range of capacitance values (i.e. long cables), it becomes impossible for the DDC lines to meet the I<sup>2</sup>C timing specifications with the minimum pull-up resistor of 1.5k $\Omega$ .

For this reason, the CM2030 was designed with an internal I<sup>2</sup>C accelerator to meet the AC timing specification even with very long and non-compliant cables.

The internal accelerator increases the positive slew rate of the DDC\_CLK\_OUT and DDC\_DAT\_OUT lines whenever the sensed voltage level exceeds  $0.3 \cdot 5V\_SUPPLY$  (approximately 1.5V). This provides faster overall risetime in heavily loaded situations without overloading the multi-drop open drain I<sup>2</sup>C outputs elsewhere.

### DYNAMIC PULLUPS (CONT'D)



**Figure 2. Dynamic DDC Pullups** (Discrete - Top, CM2030 - Bottom; 3.3V ASIC - Left, 5V Cable - Right.)

Figure 2 demonstrates the “worst case” operation of the dynamic CM2030 DDC level shifting circuitry (bottom) against a discrete NFET common-gate level shifter circuit with a typical 1.5kW pullup at the source (top.) Both are shown driving an off-spec, but unfortunately readily available 31m HDMI cable which exceeds the 700pF HDMI specification. Some widely available HDMI cables have been measured at *over 4nF*.

When the standard I/OD cell releases the NFET discrete shifter, the risetime is limited by the pullup and the parasitics of the cable, source and sink. For long cables, this can extend the risetime and reduce the margin for reading a valid “high” level on the data line. In this case, an HDMI source may not be able to read uncorrupted data and will not be able to initiate a link.

With the CM2030’s dynamic pullups, when the ASIC driver releases its DDC line and the “OUT” line reaches at least  $0.3 \cdot VDD$  (of  $5V\_SUPPLY$ ), then the “OUT” active pullups are enabled and the CM2030 takes over driving the cable until the “OUT” voltage approaches the  $5V\_SUPPLY$  rail.

The internal pass element and the dynamic pullups also work together to damp reflections on the longer cables and keep them from glitching the local ASIC.

### I<sup>2</sup>C LOW LEVEL SHIFTING

In addition to the Dynamic Pullups described in the previous section, the CM2030 also incorporates improved I<sup>2</sup>C low-level shifting on the DDC\_CLK\_IN and DDC\_DAT\_IN lines for enhanced compatibility.

Typical discrete NFET level shifters can advertise specifications for low  $R_{DS(on)}$ , but usually state relatively high  $V_{GS}$  test parameters, requiring a 'switch' signal (gate voltage) as high as 10V or more. At a sink current of 4mA for the ASIC on DDC\_XX\_IN, the CM2030 guarantees no more than 140mV increase to DDC\_XX\_OUT, even with a switching control of 2.5V on LV\_SUPPLY.

When I<sup>2</sup>C devices are driving the external cable, an internal pulldown on DDC\_XX\_IN guarantees that the VOL seen by the ASIC on DDC\_XX\_IN is equal to or lower than DDC\_XX\_OUT.

### Multipoint DDC Multiplexing

By switching LV\_SUPPLY, the DDC/HPD blocks can be independently disabled by engaging their inherent “backdrive” protection. This allows N:1 multiplexing of the low-speed HDMI signals without any additional FET switches.

### Consumer Electronics Control (CEC)

The Consumer Electronics Control (CEC) line is a high level command and control protocol, based on a single wire multidrop open drain communication bus running at approximately 1kHz (See Figure 3). While the HDMI link provides only a single point-to-point connection, up to ten (10) CEC devices may reside on the bus, and they may be daisy chained out through other physical connectors including other HDMI ports or other dedicated CEC links. The high level protocol of CEC can be implemented in a simple microcontroller or other interface with any I/OD (input/open-drain) GPIO.

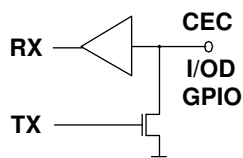


Figure 3. Typical  $\mu$ C I/OD Driver

To limit possible EMI and ringing in this potentially complex connection topology, the rise- and fall-time of this line are limited by the specification. However, meeting the slew-rate limiting requirements with additional discrete circuitry in this bi-directional block is not trivial without an additional RX/TX control line to limit the output slew-rate without affecting the input sensing (See Figure 4).

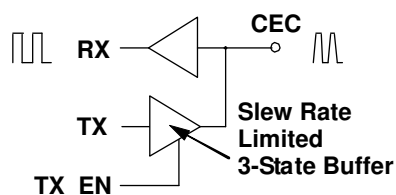
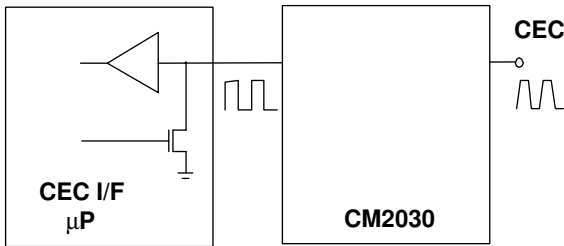


Figure 4. Three-Pin External Buffer Control

Simple CMOS buffers cannot be used in this application since the load can vary so much (total pullup of 27k $\Omega$  to less than 2k $\Omega$ , and up to 7.3nF total capacitance.) The CM2030 targets an output drive slew-rate of less than 100mV/ms regardless of static load for the CEC line. Additionally, the same internal circuitry will perform active termination, thus reducing ringing and overshoot in entertainment systems connected to legacy or poorly designed CEC nodes.

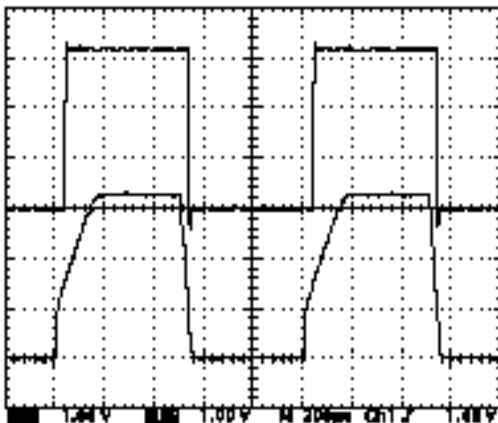
The CM2030's bi-directional slew rate limiting is integrated into the CEC level-shifter functionality thus allowing the designer to directly interface a simple low voltage CMOS GPIO directly to the CEC bus and simultaneously guarantee meeting all CEC output logic levels and HDMI slew-rate and isolation specifications (See Figure 5).



**Figure 5. Integrated CM2030 Solution**

The CM2030 also includes an internal backdrive protected static pullup 120μA current source from the CE\_SUPPLY rail in addition to the dynamic slew rate control circuitry.

Figure 6 shows a typical shaped CM2030 CEC output (bottom) against a ringing uncontrolled discrete solution (top).

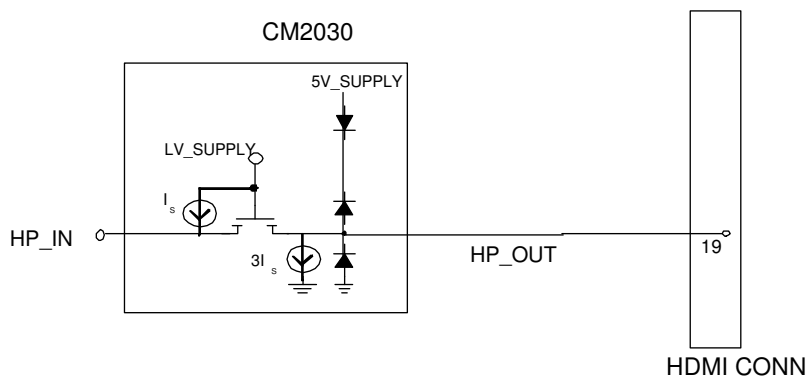


**Figure 6. CM2030 CEC Output**

## Hotplug Detect Logic

The CM2030 ensures that the local ASIC will properly detect an HDMI compliant Sink. The current sink maintains a local logic “low” when no system is connected.

A valid pullup on the HDMI connector pin will overdrive the internal pulldown and deliver a logic “high” to the local ASIC.



**Figure 7. Hotplug Detect Circuit**



## Ordering Information

| PART NUMBERING INFORMATION |          |             |             |
|----------------------------|----------|-------------|-------------|
| Package                    | Package  | Part Number | Part Number |
| 38                         | TSSOP-38 | CM2030-A0TR | CM2030-A0TR |

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

## Specifications

| ABSOLUTE MAXIMUM RATINGS        |                            |      |
|---------------------------------|----------------------------|------|
| PARAMETER                       | Value                      | Unit |
| VCC5, VCCLV                     | 6.0                        | V    |
| DC Voltage at any Channel Input | [GND - 0.5] to [VCC + 0.5] | V    |
| Storage Temperature Range       | 65 to +150                 | °C   |

| STANDARD (RECOMMENDED) OPERATING CONDITIONS |                             |       |       |       |      |
|---|-----------------------------|-------|-------|-------|------|
| SYMBOL                                      | PARAMETER                   | Value | Value | Value | Unit |
| 5V_SUPPLY                                   | Operating Supply Voltage    |       | 5     | 5.5   | V    |
| LV_SUPPLY                                   | Bias Supply Voltage         | 1     | 3.3   | 5.5   | V    |
| CE_SUPPLY                                   | Bias Supply Voltage         | 3     | 3.3   | 3.6   | V    |
|   | Operating Temperature Range | 40    |       | 85    | °C   |

**ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)**

| SYMBOL            | PARAMETER  | CONDITIONS  | MIN  | TYP  | MAX  | UNITS |
|-------------------|--|---|------|------|------|-------|
| ICC5              | Operating Supply Current   | 5V_SUPPLY = 5.0V,<br>CEC_OUT = 3.3V, LV_SUPPLY=<br>3.3V, CE_SUPPLY = 3.3V, DDC=5V;<br>Note6 |      | 300  | 350  | μA    |
| ICCLV             | Bias Supply Current  | LV_SUPPLY=3.3V; Note 6  |      | 60   | 150  | μA    |
| ICCCE             | Bias Supply Current  | CE_SUPPLY=3.3V, CEC_OUT=0V;<br>Notes 6 and 7  |      | 60   | 150  | μA    |
| ICEC              | Current source on CEC pin  | CE_SUPPLY=3.3V,   | 111  | 120  | 128  | μA    |
| VDROP             | 5V_OUT Overcurrent Out put Drop  | 5V_SUPPLY=5.0V, IOOUT=55mA  |      | 65   | 100  | mV    |
| ISC               | 5V_OUT Short Circuit Current Limit   | 5V_SUPPLY=5.0V, 5V_OUT=GND  | 90   | 135  | 175  | mA    |
| IOFF              | OFF state leakage current, level shifting NFET   | LV_SUPPLY=0V  |      | 0.1  | 5    | μA    |
| IBACKDRIVECEC     | Current through CE-REMOTE_OUT when powered down  | CE-REMOTE_IN = CE_SUPPLY < CE_REMOTE_OUT  |      | 0.1  | 1.8  | μA    |
| IBACKDRIVETMDS    | Current through TMDS pins when powered down  | All Supplies = 0V; TMDS_[2:0]+/, TMDS_CK+/- = 4V  |      | 0.1  | 5    | μA    |
| IBACKDRIVE5V_OUT  | Current through 5V_OUT when powered down   | All Supplies = 0V; 5V_OUT_PIN = 5V  |      | 0.1  | 5    | μA    |
| IBACKDRIVEDDC     | Current through DDC_DAT/CLK_OUT when powered down  | All Supplies = 0V;<br>DDC_DAT/CLK_OUT = 5V;<br>DDC_DAT/CLK_IN = 0V                          |      | 0.1  | 5    | μA    |
| IBACKDRIVEHOTPLUG | Current through HOTPLUG_DET_OUT when powered down  | All Supplies = 0V;<br>HOTPLUG_DET_OUT = 5V;<br>HOTPLUG_IN = 0V                              |      | 0.1  | 5    | μA    |
| CECSL             | CEC Slew Limit   | Measured from 10-90% or 90-10%  |      | 0.26 | 0.65 | V/μs  |
| CECRT             | CEC Rise Time  | Measured from 10-90%<br>Assumes a signal swing from 0-3.3V                                  | 26.4 |      | 250  | μs    |
| CECFT             | CEC Fall Time  | Measured from 90-10%<br>Assumes a signal swing from 0-3.3V                                  | 4    |      | 50   | μs    |
| VACC              | Turn On Threshold of I2C/DDC Accelerator   | Voltage is $0.3 \pm 10\%$ X 5V_Supply;<br>Note 2  | 1.35 | 1.5  | 1.65 | V     |
| VON(DDC_OUT)      | Voltage drop across DDC level shifter  | LV_SUPPLY=3.3V, 3mA Sink at DDCIN, DDCOUT < VACC  |      | 150  | 225  | mV    |
| VOL(DDC_IN)       | Logic Level (ASIC side) when I2C/DDC Logic Low Applied; (I2C pass-through compatibility) | DDC_OUT=0.4V,<br>LV_SUPPLY=3.3V, 1.5kΩ pullup on DDC_OUT to 5.0V; Note 2                    |      | 0.3  | 0.4  | V     |
| tr(DDC)           | DDC_OUT Line Risetime, VACC < VDDC_OUT <   | DDC_IN floating,<br>LV_SUPPLY=3.3V, 1.5kΩ pullup on   |      |      | 1    | μs    |

|             |   |  |            |              |              |        |
|-------------|---|--|------------|--------------|--------------|--------|
|             | (5V_Supply-0.5V)  | DDC_OUT to 5.0V, Bus Capacitance = 1500pF                            |            |              |              |        |
| VF          | Diode Forward Voltage<br>Top Diode<br>Bottom Diode                  | IF = 8mA, TA = 25°C  | 0.6<br>0.6 | 0.85<br>0.85 | 0.95<br>0.95 | V<br>V |
| VESD        | ESD Withstand Voltage (IEC)   | Pins 4, 7, 10, 13, 20, 21, 22, 23, 24, 27, 30, 33, TA = 25°C; Note 2 | ±8         |              |              | kV     |
| VESD        | ESD Withstand Voltage (HBM)   | Pins 1, 2, 16, 17, 18, 19, 37, 38, TA = 25°C                         | ±2         |              |              | kV     |
| VCL         | Channel Clamp Voltage<br>Positive Transients<br>Negative Transients | TA=25°C, IPP = 1A, tP = 8/20µS; Note 5                               |            | 11.0<br>2.0  |              | V<br>V |
| RDYN        | Dynamic Resistance<br>Positive Transients<br>Negative Transients    | TA=25°C, IPP = 1A, tP = 8/20µS Any I/O pin to Ground; Note5          |            | 1.4<br>0.9   |              | Ω<br>Ω |
| ILEAK       | TMDS Channel Leakage Current  | TA = 25°C  |            | 0.01         | 1            | µA     |
| CIN, TMDS   | TMDS Channel Input Capacitance                                      | 5V_SUPPLY=5.0V, Measured at 1MHz, VBIAS=2.5V                         |            | 0.9          | 1.2          | pF     |
| ΔCIN, TMDS  | TMDS Channel Input Capacitance Matching                             | 5V_SUPPLY=5.0V, Measured at 1MHz, VBIAS=2.5V; Note 4                 |            | 0.05         |              | pF     |
| CMUTUAL     | Mutual Capacitance between signal pin and adjacent signal pin       | 5V_SUPPLY=0V, Measured at 1MHz, VBIAS=2.5V                           |            | 0.07         |              | pF     |
| CIN, DDCOUT | Level Shifting Input Capacitance, Capacitance to GND                | 5V_SUPPLY=0V, Measured at 100KHz, VBIAS=2.5V                         |            | 10           |              | pF     |
| CIN, CECOUT | Level Shifting Input Capacitance, Capacitance to GND                | 5V_SUPPLY=0V, Measured at 100KHz, VBIAS=1.65V                        |            | 10           |              | pF     |
| CIN, HPOUT  | Level Shifting Input Capacitance, Capacitance to GND                | 5V_SUPPLY=0V, Measured at 100KHz, VBIAS=2.5V                         |            | 10           |              | pF     |

Note 1: Operating Characteristics are over Standard Operating Conditions unless otherwise specified.

Note 2: Standard IEC61000-4-2, C<sub>DISCHARGE</sub>=150pF, R<sub>DISCHARGE</sub>=330Ω, 5V\_SUPPLY=5V, 3.3V\_SUPPLY=3.3V, LV\_SUPPLY=3.3V, GND=0V.

Note 3: Human Body Model per MIL-STD-883, Method 3015, C<sub>DISCHARGE</sub>=100pF, R<sub>DISCHARGE</sub>=1.5kΩ, 5V\_SUPPLY=5V, 3.3V\_SUPPLY=3.3V, LV\_SUPPLY=3.3V, GND=0V.

Note 4: Intra-pair matching, each TMDS pair (i.e. D+, D-)

Note 5: These measurements performed with no external capacitor on V<sub>p</sub> (V<sub>p</sub> floating)

Note 6: These static measurements do not include AC activity on controlled I/O lines.

Note 7: This measurement does not include supply current for the 120µA current source on the CEC pin.

## Performance Information

Typical Filter Performance ( $T_A=25^\circ\text{C}$ , DC Bias=0V, 50 Ohm Environment)

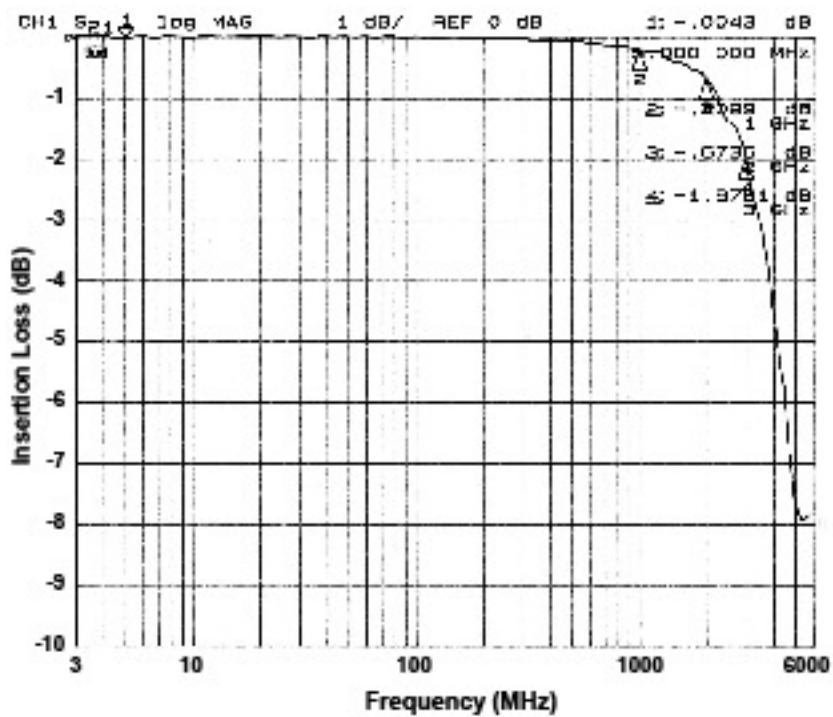


Figure 8. Insertion Loss vs. Frequency (TMD5\_D1- to GND)

## Application Information

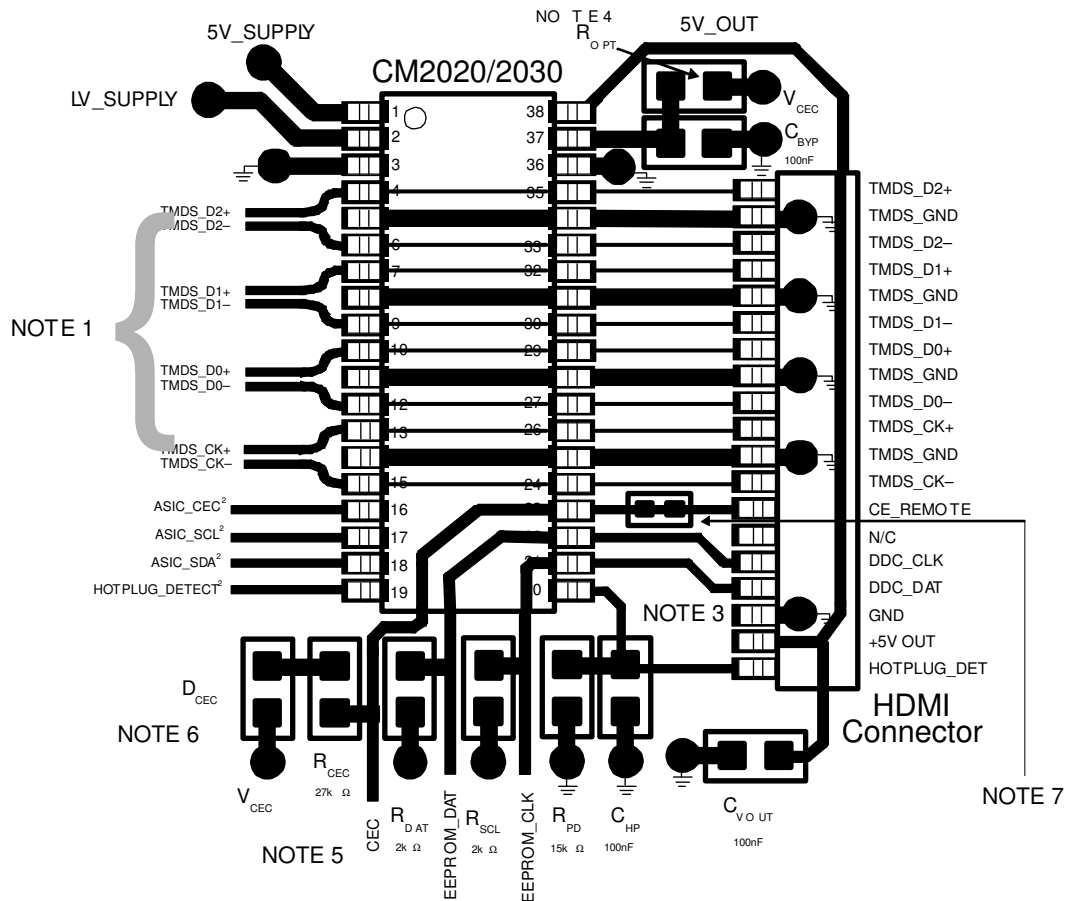


Figure 9. Typical Application for CM2030

### LAYOUT NOTES

1. Differential TMDS Pairs should be designed as normal 100Ω HDMI Microstrip. Single Ended (decoupled) TMDS traces underneath MediaGuard™, and traces between MediaGuard™ and Connector should be tuned to match chip/connector IBIS parasitics.

² Level Shifter signals should be biased with a weak pullup to the desired local LV\_SUPPLY. If the local ASIC includes sufficient pullups to register a logic high, then external pullups may not be needed.

³ Place MediaGuard™ as close to the connector as possible, and as with any controlled impedance line always avoid placing any silk-screen printing over TMDS traces.

⁴ CM2020/CM2030 footprint compatibility - For the CM2030, Pin 37 becomes the V\_CEC power supply pin for the slew-rate limiting circuitry. This can be supplied by a 0W jumper to V\_CEC which should be depopulated to utilize the CM2020. The 100nF C\_BYP is recommended for all applications.

⁵ CEC pullup isolation. The 27k R\_CEC and a Schottky D\_CEC provide the necessary isolation for the CEC pullup.

Note: *This circuitry is used only in the CM2020.* Depopulate the components for CM2030 applications in a CM2020/ CM2030 dual footprint layout.

<sup>6</sup> Footprint compatibility - The CM2030 has (built-in) internal backdrive protection.

The CM2020 does not have internal backdrive protection and requires the external  $R_{CEC}$  and  $D_{CEC}$  components.

<sup>7</sup> (For CM2030) If CEC firmware *is not* implemented, *do not* populate with 0  $\Omega$  resistor. If CEC firmware is implemented, then populate with 0  $\Omega$  resistor.

(For CM2020) Populate with 0  $\Omega$  resistor in either case.

## Application Information (cont'd)

### Design Considerations

#### 1. 5V out (pin 38)

Maximum overcurrent protection output drop at 55mA on 5V\_OUT is 100mV. To meet HDMI output requirements of 4.8-5.3V, an input of greater than 4.9V should be used (i.e. 5.1V  $\pm$ 4%)

#### 2. DUT On vs. DUT Off

Many HDMI CTS tests require a power off condition on the System Under Test. Many discrete ESD diode configurations can be forward biased when their VDD rail is lower than the I/O pin bias, thereby exhibiting extremely high apparent capacitance measurements, for example. The *MediaGuard*<sup>™</sup> backdrive isolation circuitry limits this current to less than 5mA, and will help ensure HDMI compliance.

**Please review all of the current HDMI design guidelines available at:**

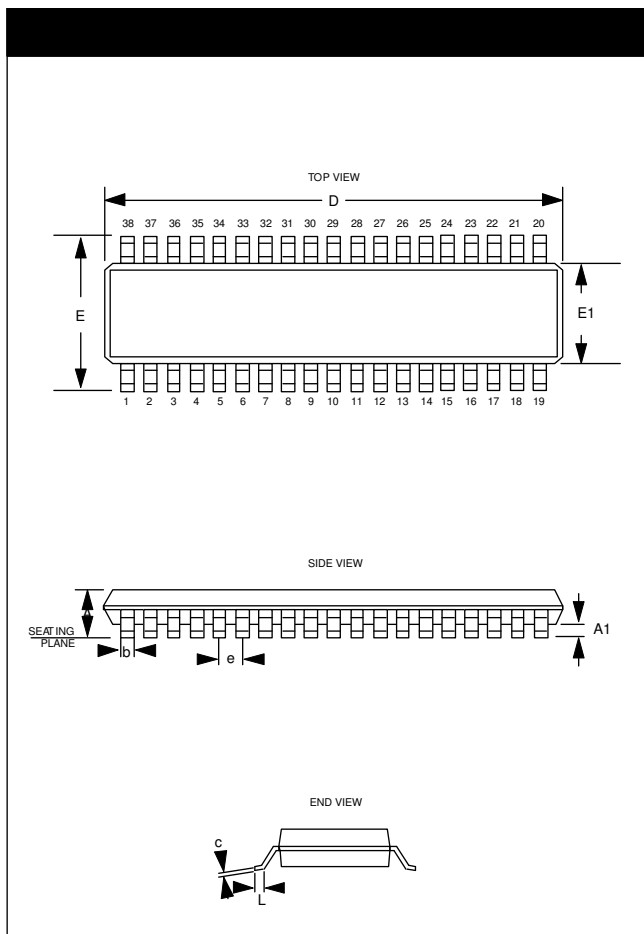
<http://www.calmicro.com/applications/customer/downloads/current-cmd-mediaguard-design-guidelines.zip>

## Mechanical Details

### TSSOP-38 Mechanical Specifications

CM2030 devices are supplied in 38-pin TSSOP packages. Dimensions are presented below.

| PACKAGE DIMENSIONS |                         |      |           |       |
|--------------------|-------------------------|------|-----------|-------|
|                    | TSSOP                   |      |           |       |
|                    | MO-153 (Variation BD-1) |      |           |       |
|                    | 38                      |      |           |       |
|                    |                         |      |           |       |
|                    | —                       | 1.20 | —         | 0.047 |
|                    | 0.05                    | 0.15 | 0.002     | 0.006 |
|                    | 0.17                    | 0.27 | 0.007     | 0.011 |
|                    | 0.09                    | 0.20 | 0.004     | 0.008 |
|                    | 9.60                    | 9.80 | 0.378     | 0.386 |
|                    | 6.40 BSC                |      | 0.252 BSC |       |
|                    | 4.30                    | 4.50 | 0.169     | 0.177 |
|                    | 0.50 BSC                |      | 0.020 BSC |       |
|                    | 0.45                    | 0.75 | 0.018     | 0.030 |
|                    | 2500 pieces             |      |           |       |
|                    |                         |      |           |       |

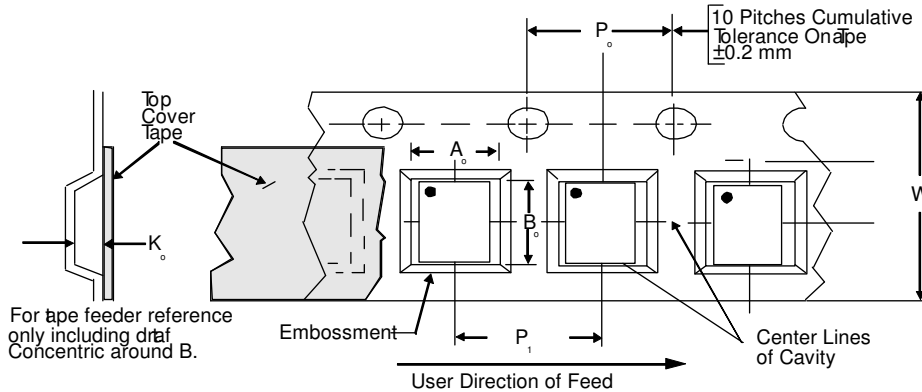



## Package Dimensions for TSSOP-38



Tape and Reel Specifications

| PART NUMBER | PACKAGE SIZE (mm)  | POCKET SIZE (mm)<br>$B_0 \times A_0 \times K_0$ | TAPE WIDTH<br>W | REEL DIAMETER | QTY PER REEL | $P_0$ | $P_1$ |
|-------------|--------------------|---|-----------------|---------------|--------------|-------|-------|
| CM2030      | 9.70 X 6.40 X 1.20 | 10.20 X 6.90 X 1.80                             | 16mm            | 330mm (13")   | 2500         | 4mm   | 12mm  |



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