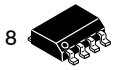
CM3106

2 Amp Source/ Sink Bus Termination Regulator

ON Semiconductor®

http://onsemi.com



SOIC−8
SM SUFFIX
CASE 751

Product Description

The CM3106 is a sinking and sourcing regulator specifically designed for providing power to DDR memory terminating resistors and companion chip set V_{TT} power. The output voltage accurately tracks $V_{DDQ}/2$. The CM3106 can source and sink current up to 2 A, ideal for DDR−I memory systems, and 1.2 A for DDR−II systems, while maintaining a load regulation of 0.5% in either application.

The CM3106 provides over current and over temperature protection which protects the device from excessive heating due to high current and high temperature. A shutdown capability using an external transistor reduces power consumption and provides a high impedance output.

The CM3106 is housed in an 8−lead SOIC RoHS−compliant package.

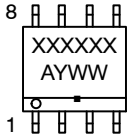
Features

- Ideal for DDR−I and DDR−II V_{TT} Applications
- Sinks and Sources 2.0A for DDR−I
- Over Current Protection
- Over Temperature Protection
- Integrated Power MOSFETs
- Excellent Accuracy (0.5% Load Regulation)
- Pin and Functionally Compatible with LP2995
- 8−Lead SOIC Package
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Single and Dual Channel DDR Memory Bus Termination
- Active Termination Buses
- Graphics Card Memory Termination

MARKING DIAGRAM



XXXXXX = CM3106−12SM
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
CM3106−12SM	SOIC−8 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

SIMPLIFIED ELECTRICAL SCHEMATIC

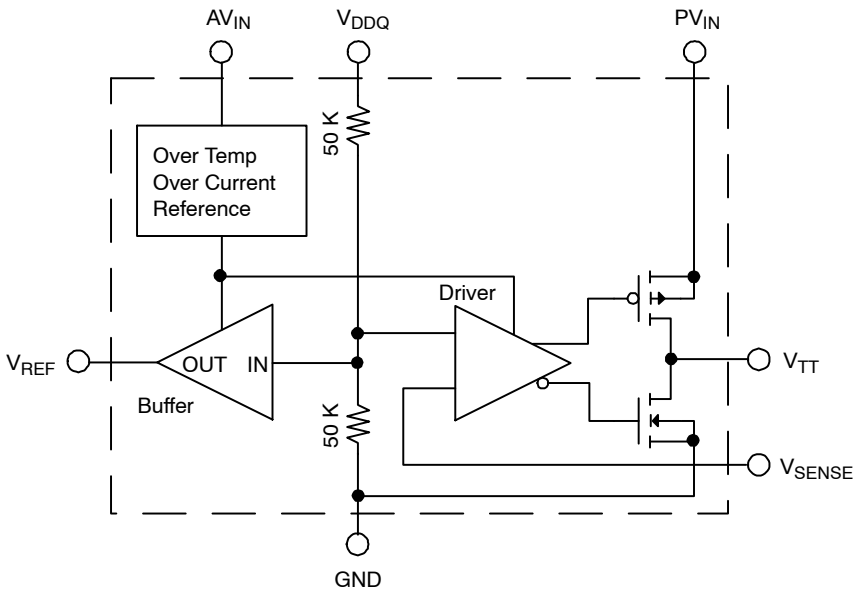
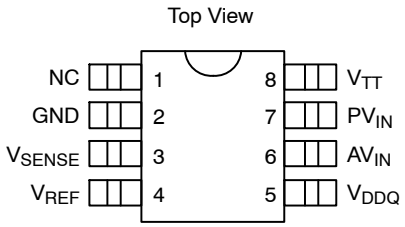


Table 1. PIN DESCRIPTIONS

Lead(s)	Name	Description
1	NC	No Connect
2	GND	Ground
3	V_{SENSE}	Feedback
4	V_{REF}	Reference Output, VDDQ/2
5	V_{DDQ}	V_{DDQ} Input
6	AV_{IN}	Analog Input
7	PV_{IN}	Power Input
8	V_{TT}	Output

PACKAGE / PINOUT DIAGRAM



8−Lead SOIC

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
AV_{IN} Operating Supply Voltage	7	V
V_{DDQ} Input Voltage	7	V
Pin Voltages V_{TT} Output Any other pins	 7 7	V
ESD (HBM)	±2000	V
Storage Temperature Range	−40 to +150	°C
Operating Temperature Range Ambient Junction	 −40 to +85 (Note 1) −40 to +150	°C
Power Dissipation (Note 1)	Internally Limited	W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. These devices must be derated based on thermal resistance at elevated temperatures. The device packaged in an 8−lead SOIC leadframe must be derated at θ_{JA} = 151°C/W. θ_{JA} of the 8−lead PSOP is 40°C/W.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
V_{DDQ}	2.5	V
AV_{IN}	2.5	V
PV_{IN}	2.5	V
Ambient Operating Temperature	0 to +70	°C
C_{TT}	220 ±20%	μF

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range V_{DDQ} AV_{IN}		 2.2 2.2	 2.5 2.5	 AV_{IN} 5.5	V
I_{CC}	AV_{IN} Quiescent Current	I_{VTT} = 0 A		450		μA
V_{RLOAD}	Load Regulation	0 A ≤ I_{VTT} ≤ 2.0 A or −2.0 A ≤ I_{VTT} ≤ 0 A		6.25		mV
V_{REF}	Output Reference Voltage	V_{DDQ} = 2.5 V, I_{REF} = 0 A	1.225	1.25	1.275	V
VOS_{VTT}	Output Offset from V_{REF}		−20		20	mV
Z_{REF}	V_{REF} Output Impedance	−5 μA ≤ I_{REF} ≤ 5 μA		5		kΩ
Z_{VDDQ}	V_{DDQ} Input Impedance			100		kΩ
I_{LIM}	V_{TT} Current Limit			2.5		A
$T_{DISABLE}$ T_{HYST}	Shutdown Temperature Thermal Hysteresis			150 50		°C °C

1. Operating Characteristics are over Standard Operating Conditions unless otherwise specified.

PERFORMANCE INFORMATION

Typical DC Characteristics (nominal conditions unless otherwise specified)

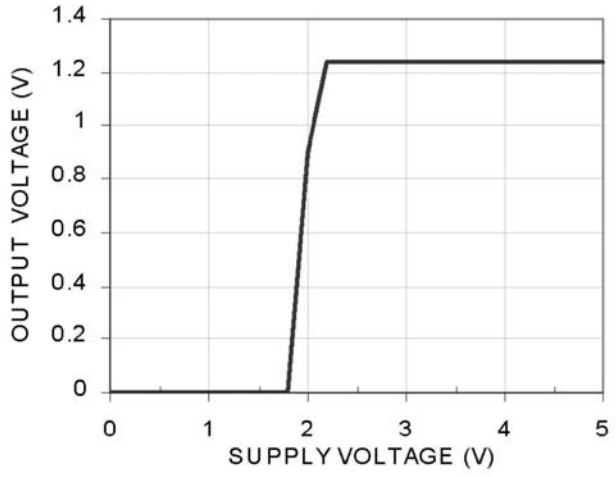


Figure 1. Output Voltage with AV_{IN} Supply (V_{DDQ} = 2.5 V)

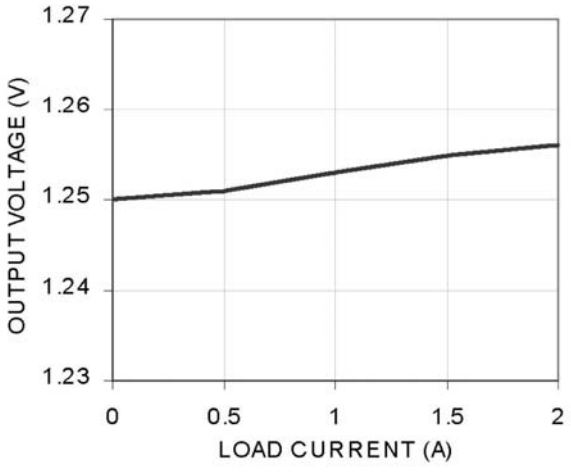


Figure 2. Load Regulation (Sink)

PERFORMANCE INFORMATION (Cont'd)

Typical DC Characteristics (nominal conditions unless otherwise specified)

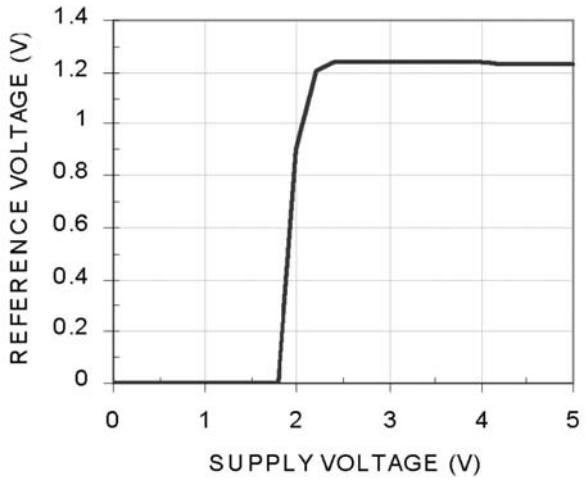


Figure 3. Reference Voltage with AV_{IN} Supply (V_{DDQ} = 2.5 V)

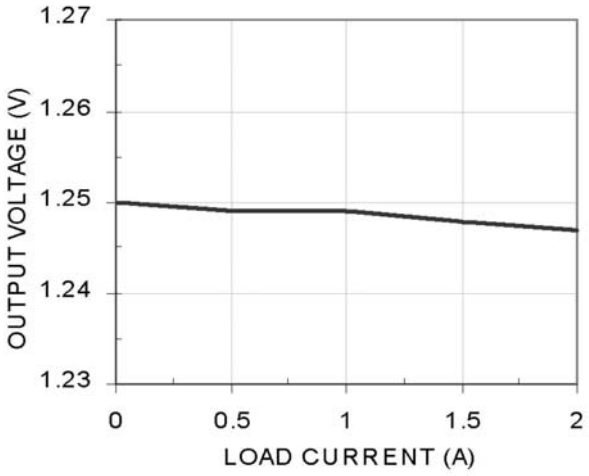


Figure 4. Load Regulation (Source)

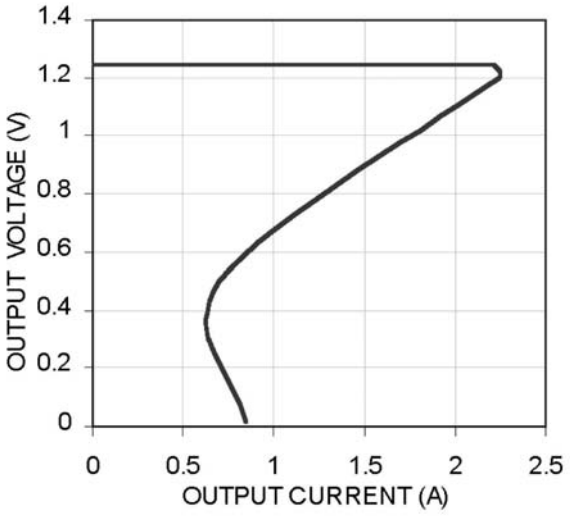


Figure 5. Over Current Limit (Sink)

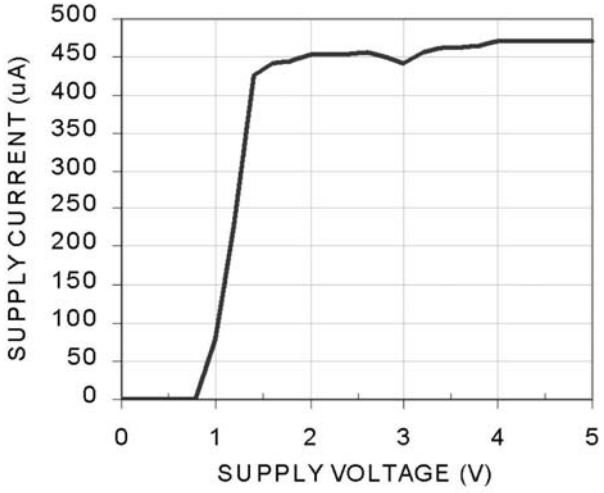


Figure 6. AV_{IN} Supply Current with Supply Voltage

PERFORMANCE INFORMATION (Cont'd)

Typical DC Characteristics (nominal conditions unless otherwise specified)

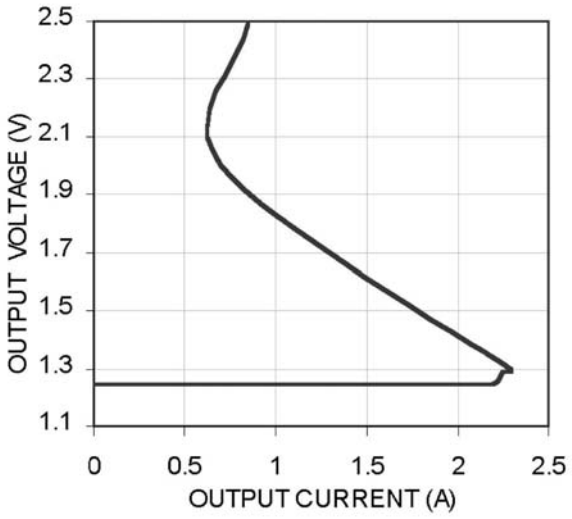


Figure 7. Over Current Limit (Source)

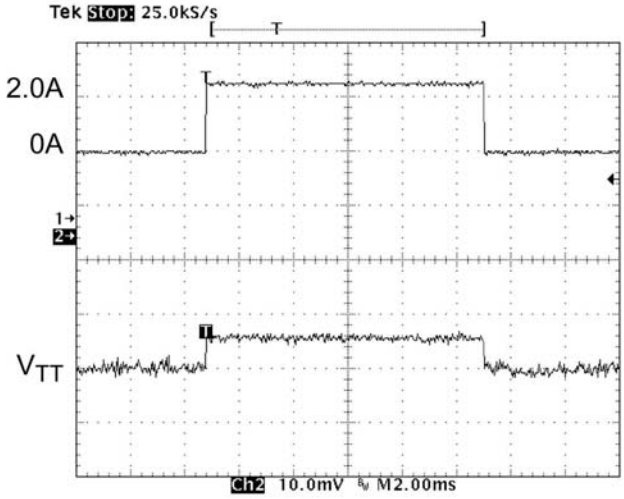


Figure 8. Load Transient (0 A to 2.0 A Sink)

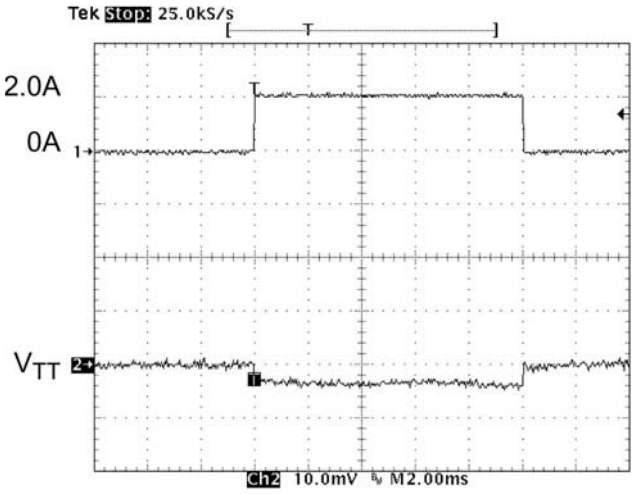


Figure 9. Line Transient (0 A to 2.0 A Sink)

PERFORMANCE INFORMATION (Cont'd)

Typical Thermal Characteristics (nominal conditions unless otherwise specified)

The overall junction to ambient thermal resistance (θ_{JA}) for device power dissipation (P_D) consists primarily of two paths in series. The first path is the junction to the case (θ_{JC}) which is defined by the package style, and the second path is case to ambient (θ_{CA}) thermal resistance which is dependent on board layout. The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$T_{JUNC} = T_{AMB} + P_D (\theta_{JC}) + P_D (\theta_{CA})$$
$$= T_{AMB} + P_D (\theta_{JA})$$

When a CM3106−12SM is mounted on a double sided printed circuit board with two square inches of copper allocated for "heat spreading", the resulting θ_{JA} is 151°C/W. Based on the over temperature limit of 150°C with an ambient of 70°C, the available power of this package will be:

$$P_D = (150°C - 85°C) / 151°C/W = 0.43\ W$$

Since the θ_{JA} of the CM3106−12SB (PSOP) is 40°C/W, the available power for this package will be:

$$P_D = (150°C - 85°C) / 40°C/W = 1.625\ W$$

DDR Memory Application

Since the output voltage is 1.25 V, and the device can either source current from V_{DD} or sink current to Ground, the power dissipated in the device at any time is 1.25 V times the current load. This means the the maximum average RMS current (in either direction) is 0.344 A for the CM3106−12SM and 1.3 A for the CM3106−12SB. The maximum instantaneous current is specified at 2 A, so this condition should not be exceeded for more than 17% of the time for the CM3106−12SM and 65% of the time for the CM3106−12SB. It is highly unlikely in most usage of DDR memory that this might occur, because it means the DDR memory outputs are either all high or all low for 17% (SOIC) and 65% (PSOP) of the time.

If the ambient temperature is 40°C instead of 85°C, which is typically the maximum in most DDR memory applications, the power dissipated (P_D) can be 0.73 W, for the CM3106−12SM and 2.75 W for the CM3106−12SB. So the maximum average RMS current increases from 0.42 A to 0.58 A for the CM3106−12SM and a maximum instantaneous current of 2 A should not be exceeded for more than 29% of the time. For CM3106−12SB, the maximum RMS current increases from 1.3 A to 2.2 A. Thus, the maximum continuous current can be 2 A all the time.

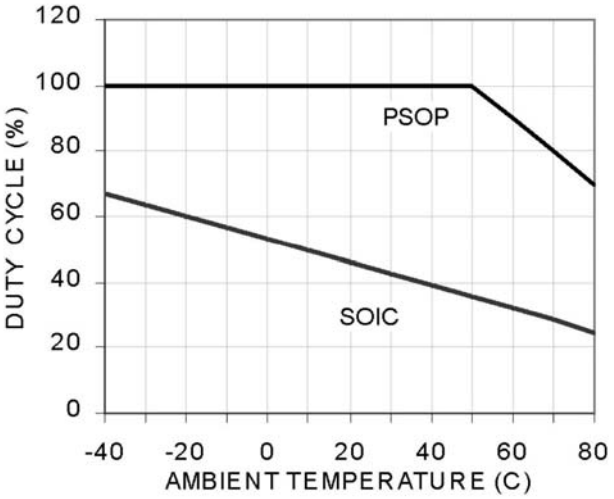


Figure 10. Duty Cycle vs. Ambient Temperature (I_{LOAD} = 2.0 A)

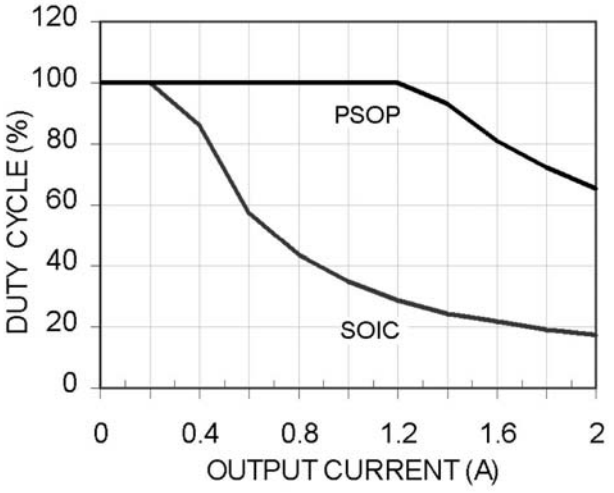


Figure 11. Duty Cycle vs. Output Current (Temp = 70°C)

PERFORMANCE INFORMATION (Cont'd)

Typical Thermal Characteristics (cont'd) (nominal conditions unless otherwise specified)

The theoretical calculations of these relationships show the safe operating area of the CM3106 in the SOIC package.

Thermal characteristics were measured using a double sided board with two square inches of copper area connected to the GND pins for "heat spreading".

Measurements showing performance up to a junction temperature of 150°C were performed under light load conditions (5 mA). This allows the ambient temperature to be representative of the internal junction temperature.

NOTE: The use of multi−layer board construction with separate ground and power planes will further enhance the overall thermal performance.

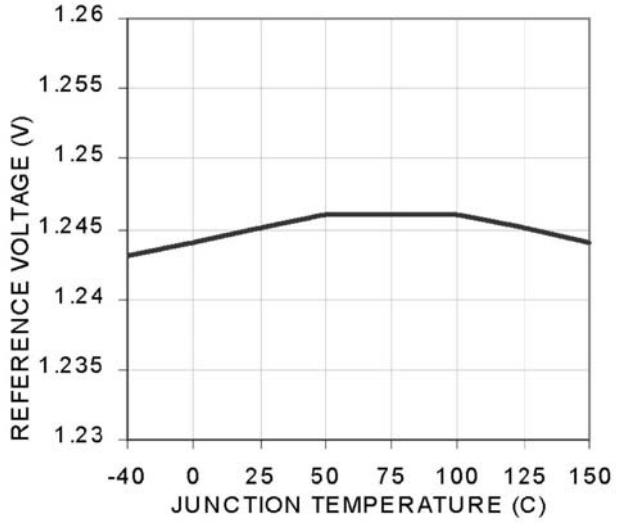


Figure 12. Reference Voltage vs. Temperature

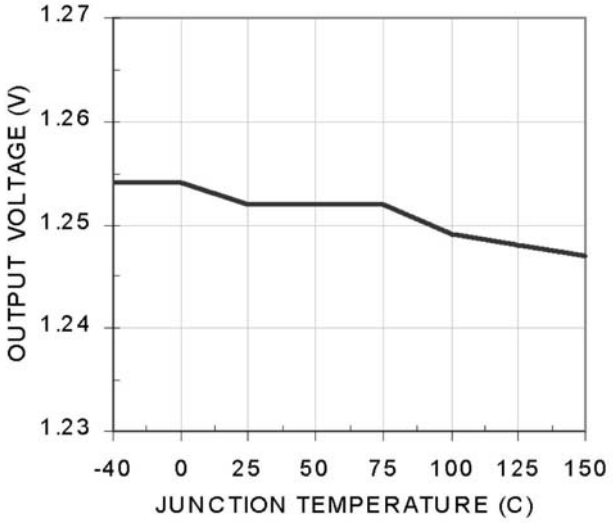


Figure 13. V_{TT} Output Voltage vs. Temperature (5 mA load)

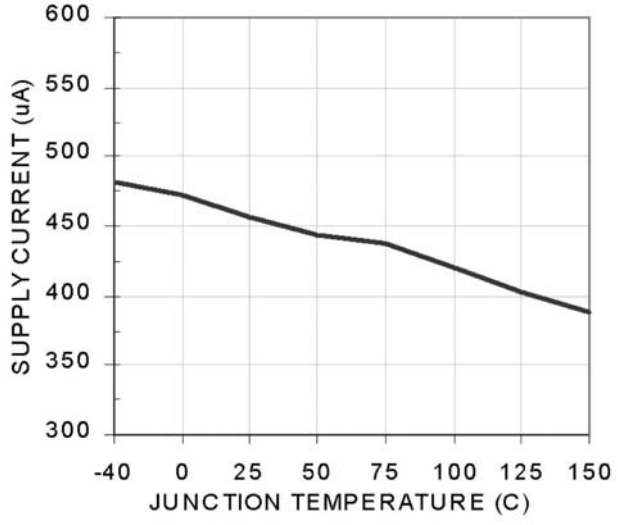


Figure 14. AV_{IN} Quiescent Current vs. Temperature

APPLICATION INFORMATION

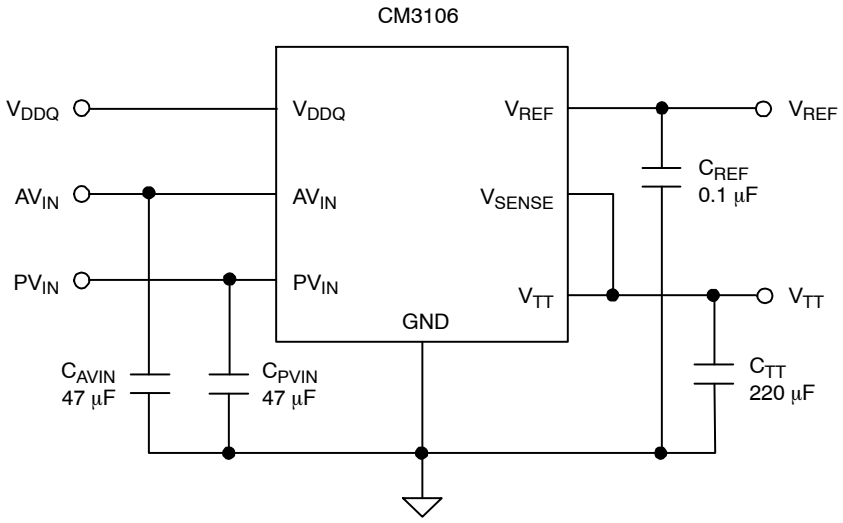


Figure 15. Typical Application Circuit

PCB Layout Considerations

The CM3106−12SB has a heat spreader attached to the underneath of the PSOP−8 package in order for heat to be transferred much easier from the package to the PCB. The heat spreader is a copper pad of dimensions just smaller than the package itself. By positioning the matching pad on the PCB top layer to connect to the spreader during manufacturing, the heat will be transferred between the two pads. The drawing below shows the recommended PCB layout. Note that there are six vias on either side to allow the heat to dissipate into the ground and power planes on the inner layers of the PCB. Vias can be placed underneath the chip, but this can cause blockage of the solder. The ground and power planes should be at least 2 sq in. of copper by the vias. It also helps dissipation to spread if the chip is positioned away from the edge of the PCB, and not near other heat dissipating devices. A good thermal link from the PCB pad to the rest of the PCB will ensure a thermal link from the CM3106 package to ambient, θ_{JA}, of around 40°C/W.

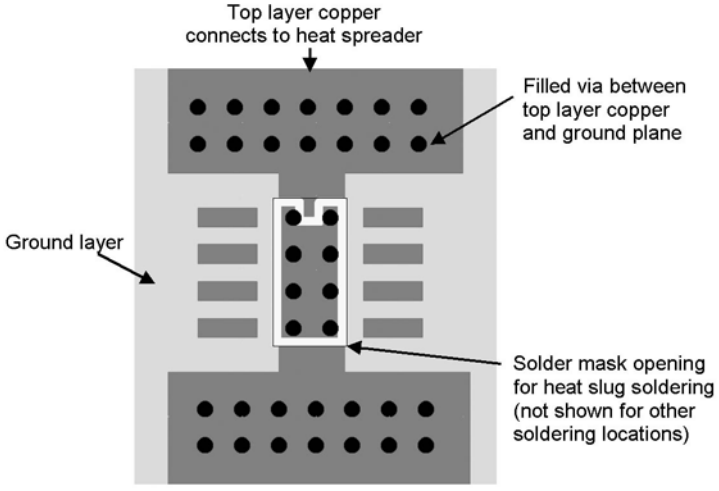
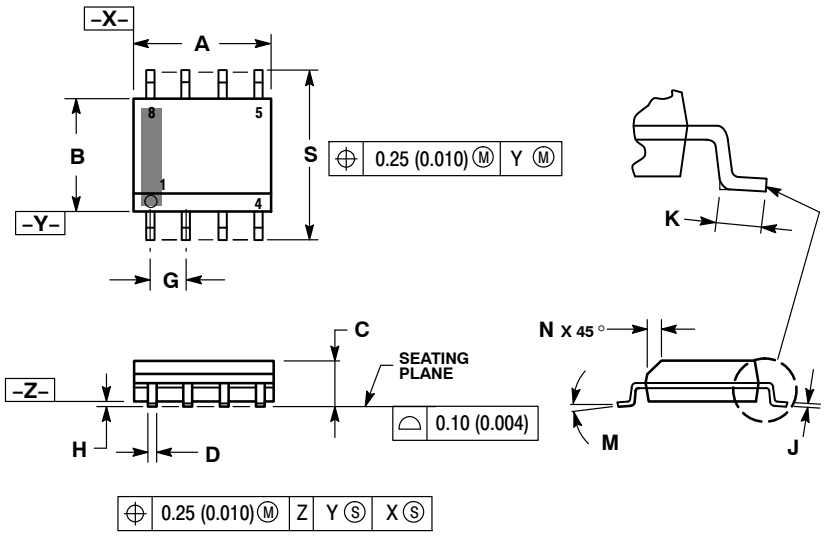


Figure 16. Recommended Heat Sink PCB Layout

PACKAGE DIMENSIONS

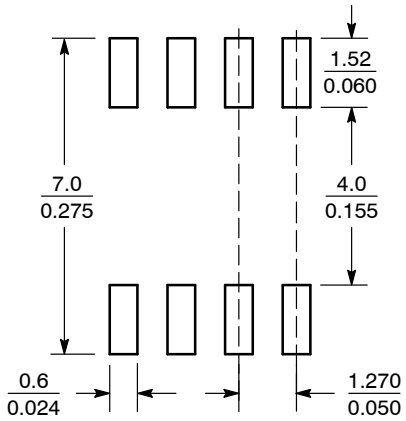
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative