2 Amp Source/ Sink Bus Termination Regulator for DDR Memory and Front Side Bus Applications

Features

- Ideal for Intel 865 Front Side Bus V_{TT} and DDR V_{TT} applications
- Sinks and sources 2 Amps
- Over current protection
- Over temperature protection
- Integrated power MOSFETs
- Excellent accuracy (0.5% load regulation)
- Selectable output (1.225V/1.45V or $V_{DDQ}/2$)
- 8-lead SOIC and PSOP packages
- Lead-free versions available

Applications

- Intel 865/845 Front Side Bus termination
- Single and dual DDR memory termination
- Active termination buses
- Graphics card DDR memory termination

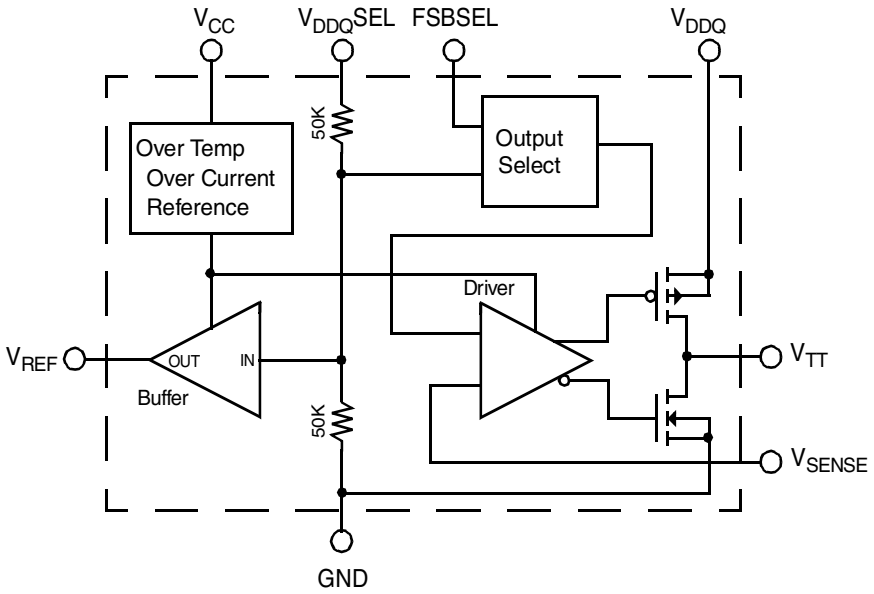
Product Description

The CM3107 is a sinking and sourcing regulator specifically designed for series-parallel bus termination for high-speed chip set busses as well as DDR memory systems. It can source and sink current up to 2.0A with a load regulation of 0.5%. The V_{TT} output voltage is selectable by V_{DDQ}SEL and FSBSEL pins. The V_{DDQ}SEL pin controls whether the CM3107 is in DDR memory mode with $V_{TT}=V_{DDQ}/2$, or in FSB mode. In FSB mode, FSBSEL controls whether V_{TT} is 1.225V or 1.45V. This allows the same chip to be used in two different circuits on an Intel 865-based motherboard.

The CM3107 provides over current and over temperature protection, which protect the chip from excessive heating due to high current and high temperature. A shutdown capability using an external transistor reduces power consumption and provides a high impedance output.

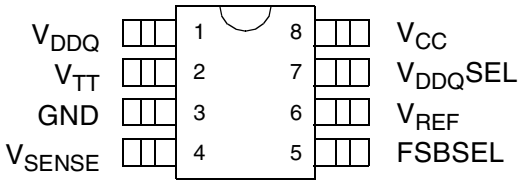
The CM3107 is housed in 8-lead SOIC and PSOP packages and is available with optional lead-free finishing.

Simplified Electrical Schematic



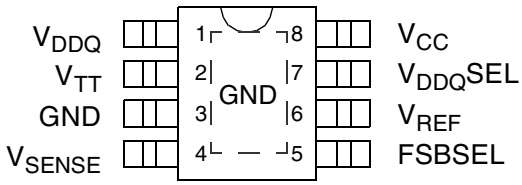
PACKAGE / PINOUT DIAGRAM

TOP VIEW



8-lead SOIC

TOP VIEW



8-lead PSOP

Note: This drawing is not to scale.

PIN DESCRIPTIONS

SOIC-8 LEAD(S)	NAME	DESCRIPTION
1	V_{DDQ}	V_{DDQ}
2	V_{TT}	Outputs either 1.225V/1.45V FSB or V_{DDQ}/2 DDR (See note 1)
3	GND	Ground
4	V_{SENSE}	Feedback voltage input
5	FSBSEL	Selects FSB output for either V_{TT}=1.225V or 1.45V
6	V_{REF}	1.25V reference voltage input for DDR bus
7	V_{DDQ}SEL	Select output to support FSB or DDR applications
8	V_{CC}	Power for internal control circuits

Note 1: Assumes V_{DDQ} and V_{DDQ}SEL are tied together in DDR application.

Ordering Information

PART NUMBERING INFORMATION

Pins	Package	Standard Finish		Lead-free Finish	
		Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
8	PSOP-8	CM3107-00SB	CM3107-00SB	CM3107-12SH	CM3107-00SH
8	SOIC-8	CM3107-00SN	CM310701S	CM3107-00SM	CM3107-00SM

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
V_{CC} Operating Supply Voltage	7	V
V_{DDQ} Input Voltage	7	V
Pin Voltages V_{TT} Output Any other pins	 7 7	 V V
ESD (HBM)	±2000	V
Storage Temperature Range	-40 to +150	°C
Operating Temperature Range Ambient Junction	 -40 to +85 -40 to +150	 °C °C
Power Dissipation (see note 1)	Internally Limited	W

Note 1: These devices must be derated based on thermal resistance at elevated temperatures. The device packaged in a 8-lead SOIC leadframe must be derated at θ_{JA} = 151°C/W . θ_{JA} of the 8-lead PSOP is 40°C/W.

STANDARD OPERATING CONDITIONS		
PARAMETER	**VALUE**	**UNITS**
V_{DDQ}	2.5 to 3.3	V
V_{CC}	2.5 to 3.3	V
Ambient Operating Temperature	0 to +70	°C
CV_{OUT}	220 ±20%	µF

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{IN}	Input Voltage Range V_{DDQ} V_{CC}		 2.2 2.2	 2.5 2.5	 V_{CC} 5.5	 V V
I_{CC}	V_{CC} Quiescent Current	I_{VTT} = 0A		450		µA
V_{TT}	Output Voltage	I_{VTT} = 0A, V_{DDQ} = 2.5V, V_{DDQ}SEL= logic "1" = 2.5V V_{DDQ}SEL= logic "0", FSBSEL= logic "0" V_{DDQ}SEL = logic "0", FSBSEL = logic "1" I_{VTT} = 0A, V_{DDQ} = 3.3V, V_{DDQ}SEL= logic "0", FSBSEL= logic "0" V_{DDQ}SEL = logic "0", FSBSEL = logic "1"	 1.225 1.200 1.425 1.200 1.425	 1.250 1.225 1.450 1.225 1.450	 1.275 1.250 1.475 1.250 1.475	 V V V V V V
V_{RLOAD}	Load Regulation	0A ≤ I_{VTT} ≤ 2.0A or 0A ≤ I_{VTT} ≤ -2.0A		6.25		mV
V_{REF}	Output Reference Voltage	V_{DDQ}SEL = 2.5V, I_{VREF}=0A	1.225	1.250	1.275	V
VOS_{VTT}	Output Offset from V_{REF}		-20		20	mV
Z_{REF}	V_{REF} Output Impedance	-5µA ≤ I_{VREF} ≤ 5µA		5		kΩ
$Z_{VDDQSEL}$	$V_{VDDQSEL}$ Input Impedance			100		kΩ
CL_{VTT}	V_{TT} Current Limit			2.5		A
V_{FSBSEL}	Output Selection Logic (FSBSEL) Logic "1" Level Logic "0" Level		1.5		 0.4	 V V
$T_{DISABLE}$ T_{HYST}	Shutdown Temperature Thermal Hysteresis			150 50		°C °C

Note 1: Operating Characteristics are over Standard Operating Conditions unless otherwise specified.

Performance Information

Typical DC Characteristics (nominal conditions unless otherwise specified)

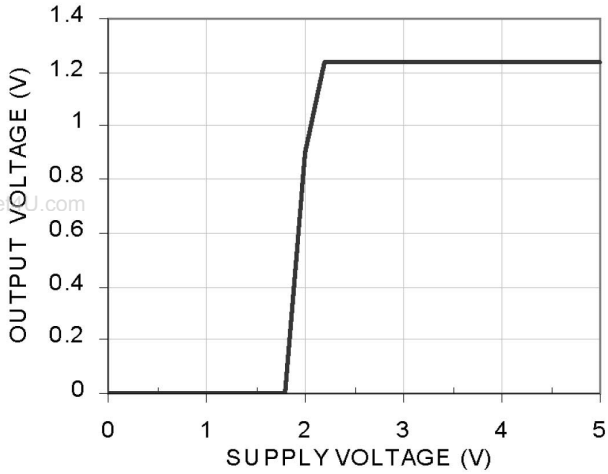


Figure 1. Output Voltage with V_{CC} Supply (V_{DDQ}SEL= 2.5V)

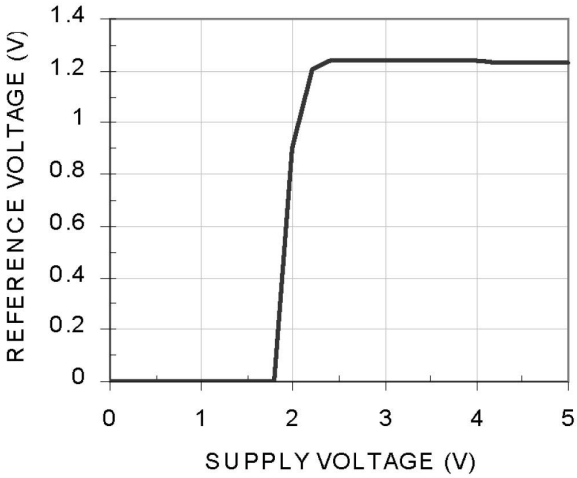


Figure 3. Reference Voltage with V_{CC} Supply (V_{DDQ}SEL= 2.5V)

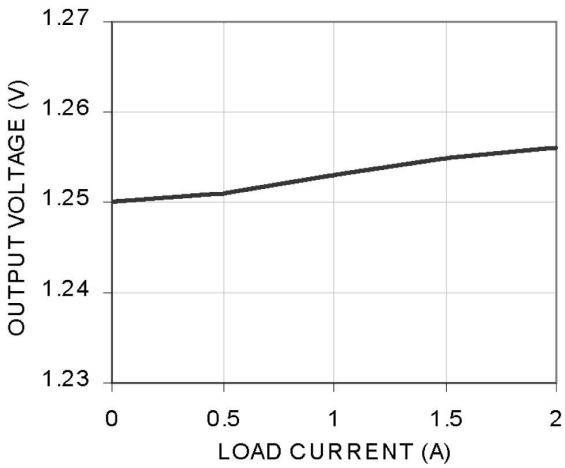


Figure 2. Load Regulation (Sink)

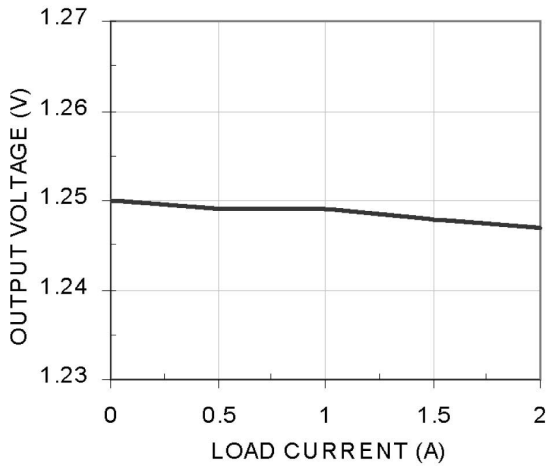


Figure 4. Load Regulation (Source)

Performance Information (cont'd)

Typical DC Characteristics (nominal conditions unless otherwise specified)

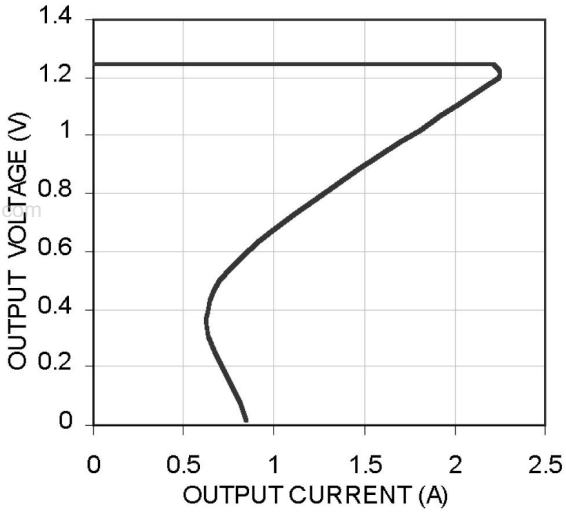


Figure 5. Over Current Limit (Sink)

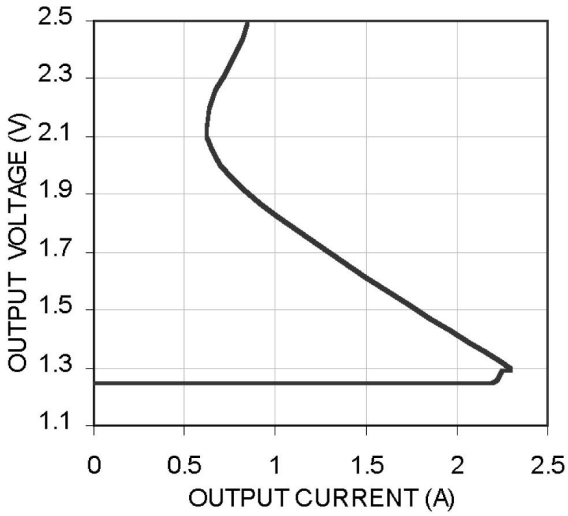


Figure 7. Over Current Limit (Source)

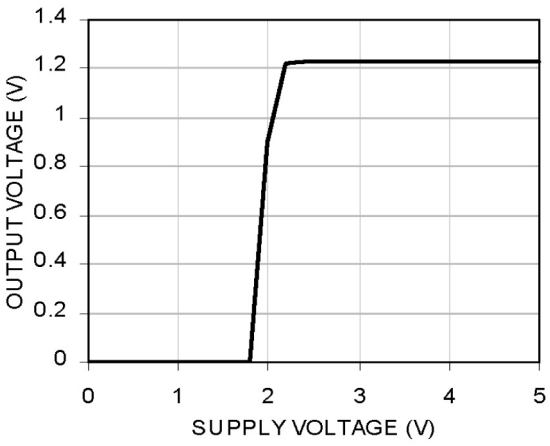


Figure 6. Output Voltage with V_{CC} Supply Voltage (V_{DDQ}SEL = 0V, FSBSEL = 0V)

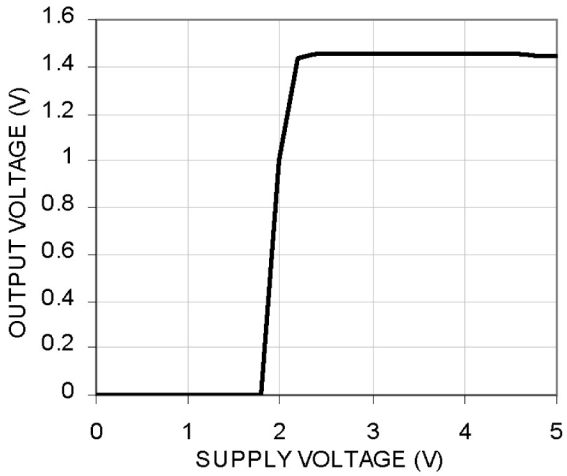


Figure 8. Output Voltage with V_{CC} Supply Voltage (V_{DDQ}SEL = 0V, FSBSEL = 2.5V)

Performance Information (cont'd)

Typical DC Characteristics (nominal conditions unless otherwise specified)

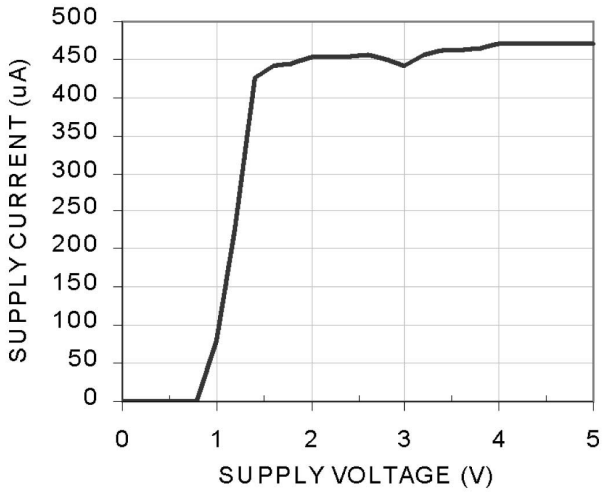


Figure 9. V_{CC} Supply Current with Supply Voltage

Typical Transient Characteristics (nominal conditions unless otherwise specified)

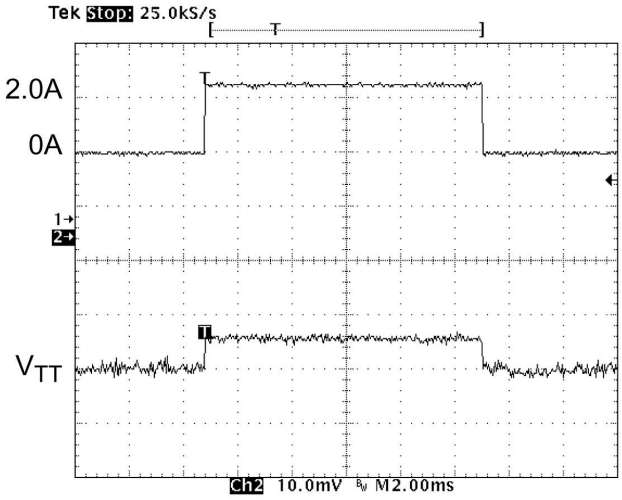


Figure 10. Load Transient (0A to 2.0A Sink)

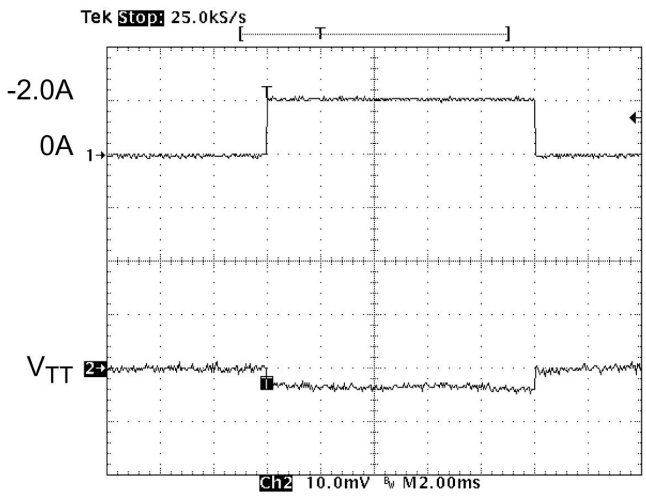


Figure 11. Line Transient (0A to 2.0A Source)

Performance Information (cont'd)

Typical Thermal Characteristics

The overall junction to ambient thermal resistance (θ_{JA}) for device power dissipation (P_D) consists primarily of two paths in series. The first path is the junction to the case (θ_{JC}) which is defined by the package style, and the second path is case to ambient (θ_{CA}) thermal resistance which is dependent on board layout. The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$T_{JUNC} = T_{AMB} + P_D (\theta_{JC}) + P_D (\theta_{CA})$$

$$= T_{AMB} + P_D (\theta_{JA})$$

When a CM3107-00SN (SOIC) is mounted on a double sided printed circuit board with two square inches of copper allocated for "heat spreading", the resulting θ_{JA} is 151°C/W. Based on the over temperature limit of 150°C with an ambient of 85°C, the available power of this package will be:

$$P_D = (150°C - 85°C) / 151°C/W = 0.43W$$

For the CM3107-00SB (PSOP), the θ_{JA} is 40°C/W and the available power for this package will be:

$$P_D = (150°C - 85°C) / 40°C/W = 0.1.625W$$

DDR Memory Application

Since the output voltage is 1.25V, and the device can either source current from VDDQ or sink current to Ground, the power dissipated in the device at any time is 1.25V times the current load. This means the maximum average RMS current (in either direction) is 0.344A for CM3107-00SN and 1.3A for CM3107-00SB. The maximum instantaneous current is specified at 2A, so this condition should not be exceeded 17% and 65% of the time for CM3107-00SN and CM3107-00SB, respectively. It is highly unlikely in most usage of DDR memory that this might occur, because it means the DDR memory outputs are either all high or all low for 17% (SOIC) and 65% (PSOP) of the time..

If the ambient temperature is 40°C instead of 85°C, which is typically the maximum in most DDR memory applications, the power dissipated PD can be 0.73W for CM3107-00SN and 2.75W for CM3107-00SB. So the maximum average RMS current increases from 0.42A to 0.58A for CM3107-00SN and maximum instantaneous current of 2A should not be exceeded 29% of the time. For CM3107-00SB, the maximum RMS current increases from 1.3A to 2.2A. Thus, the maximum continuous current can be 2A all the time.

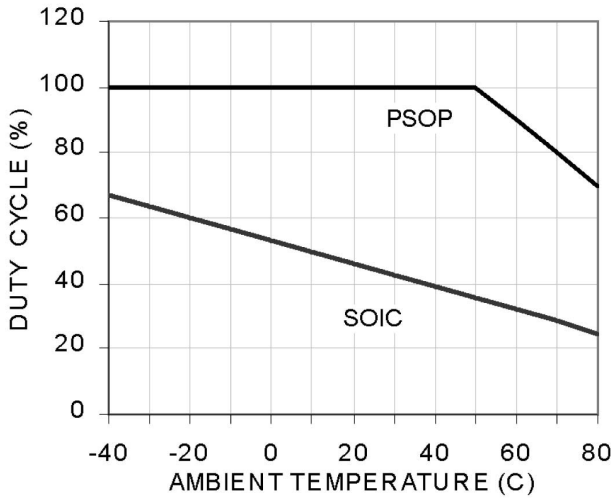


Figure 12. Duty Cycle vs. Ambient Temperature (I_{LOAD} = 2A)

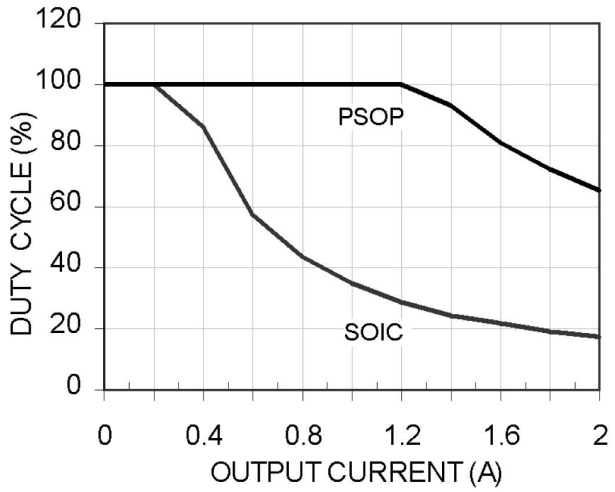


Figure 13. Duty Cycle vs. Output Current (Temp=70°C)

Performance Information (cont'd)

Typical Thermal Characteristics (cont'd)

Front Side Bus Application

If the CM3107-00SN is instead used for the Front Side Bus application, where VDDQ could be connected to the 3.3V VCC rail for ease of connectivity, the power dissipated will increase to [3.3V-1.4V] = 1.9V times the sourcing current, or [1.4V - 0V] = 1.4V times the sinking current.

So the worst case is with all FSB outputs low for a period of time, such that the maximum average source current at an ambient of 40°C is [0.73W / 1.9V] = 0.38A. If this average current is exceeded, the device will go over-temperature and the output will drop to 0V. If it is likely that this average current will be exceeded for the FSB application, then the version with the heat spreader, CM3107-00SB, should be used, or for commonality of device type for both applications, the VDDQ pin should instead be connected to 2.5V. The maximum average source current at an ambient of 40°C is [2.75W/1.9V] = 1.45A.

The theoretical calculations of these relationships show the safe operating area of the CM3107 in the SOIC and PSOP packages.

Thermal characteristics were measured using a double sided board with two square inches of copper area connected to the GND pins for "heat spreading".

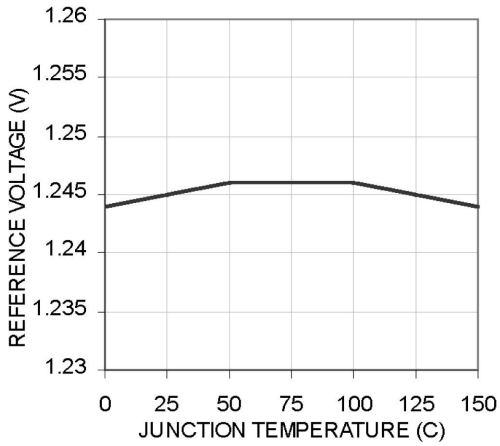


Figure 14. Reference Voltage vs. Temperature

Measurements showing performance up to a junction temperature of 150°C were performed under light load conditions (5mA). This allows the ambient temperature to be representative of the internal junction temperature.

Note: The use of multi-layer board construction with separate ground and power planes will further enhance the overall thermal performance.

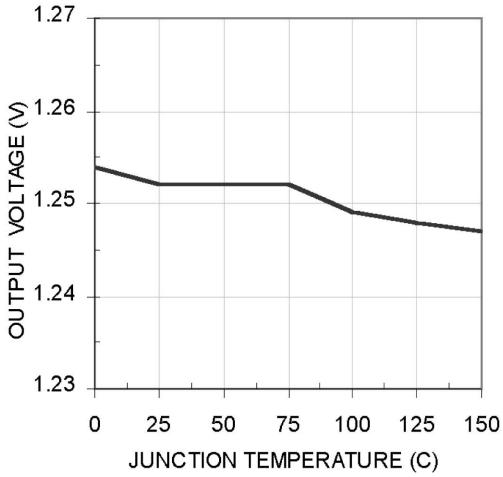


Figure 15. Output Voltage vs. Ambient Temperature (I_{LOAD}=5mA)

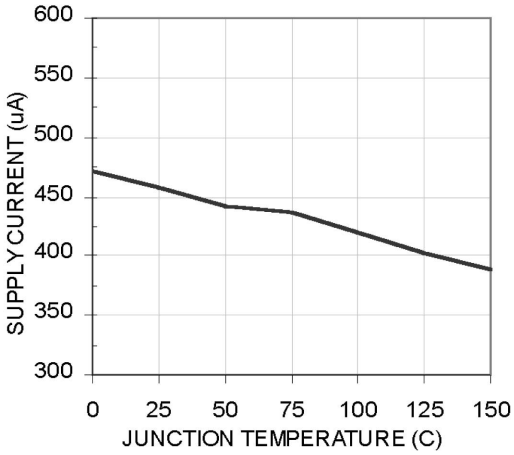


Figure 16. Quiescent Current vs. Temperature

Figure 17.

Application Information

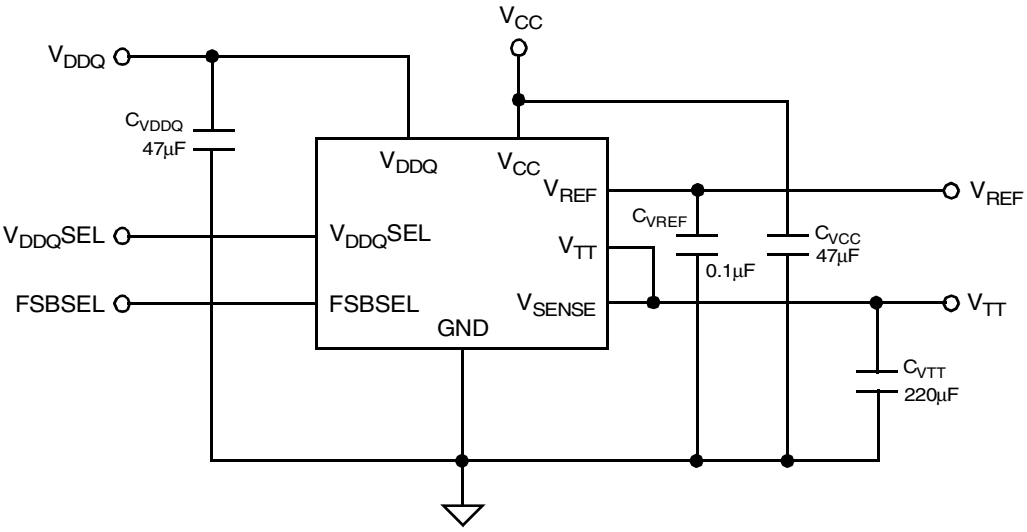


Figure 18. Typical Application Circuit

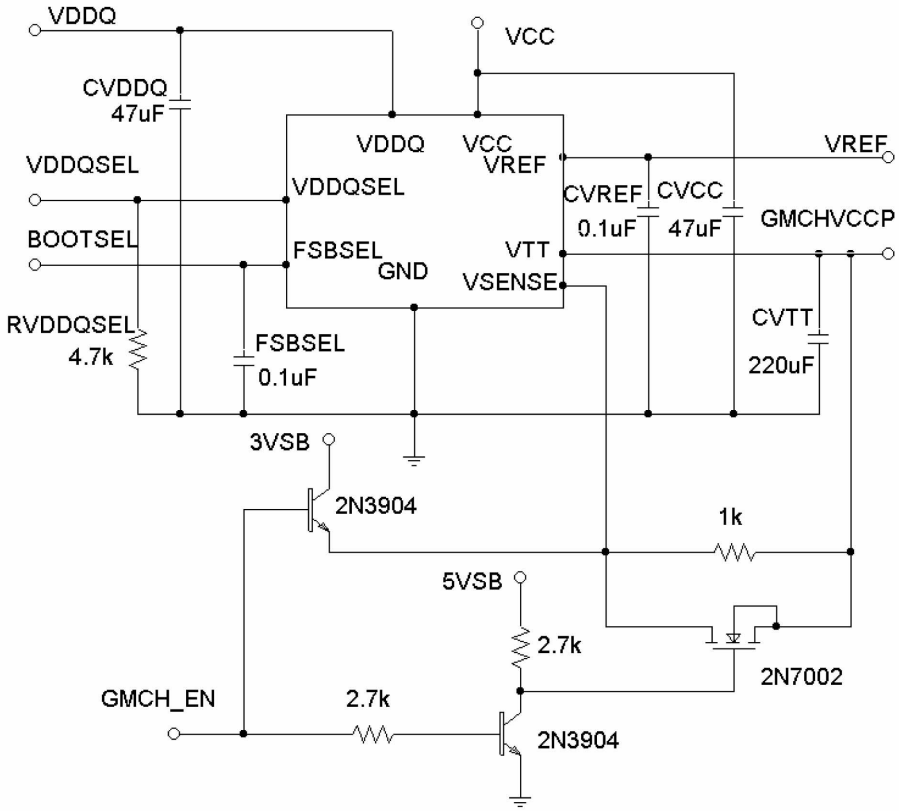


Figure 19. Typical Front Side Bus with Suspend to RAM Application Circuit

Application Information (cont'd)

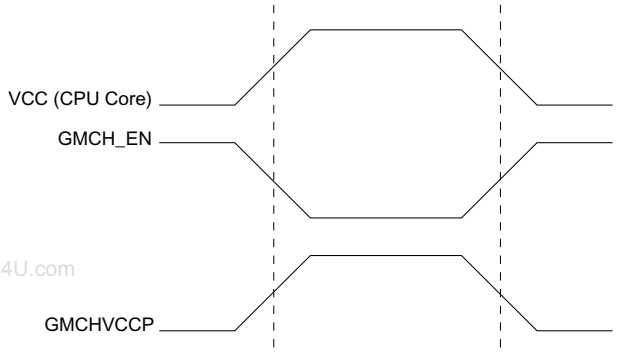


Figure 20. Front Side Bus Timing diagram

V_{DDQSEL}	FSBSEL	V_{TT}	NOTE
"1"	Don't Care	$V_{DDQSEL}/2$ (Note1)	For DDR
Open or "0"	"0"	1.225V	For FSB
Open or "0"	"1"	1.45V	For FSB

Note 1:Assumes V_{DDQ} and V_{DDQSEL} are tied together in DDR application.

Table 1: V_{TT} Output Selection Truth Table.

PCB Layout Considerations

The CM3107-00SB has a heat spreader attached to the underneath of the PSOP-8 package in order for heat to be transferred much easier from the package to the PCB. The heat spreader is a copper pad of dimensions just smaller than the package itself. By positioning the matching pad on the PCB top layer to connect to the spreader during manufacturing, the heat will be transferred between the two pads. The drawing below shows the recommended PCB layout. Note that there are six vias on either side to allow the heat to dissipate into the ground and power planes on the inner layers of the PCB. Vias can be placed underneath the chip, but this can cause blockage of the solder. The ground and power planes should be at least 2 sq in. of copper by the vias. It also helps dissipation to spread if the chip is positioned away from the edge of the PCB, and not near other heat dissipating devices. A good thermal link from the PCB pad to the rest of the PCB will ensure a thermal link from the CM3107 package to ambient, θ_{JA}, of around 40°C/W.

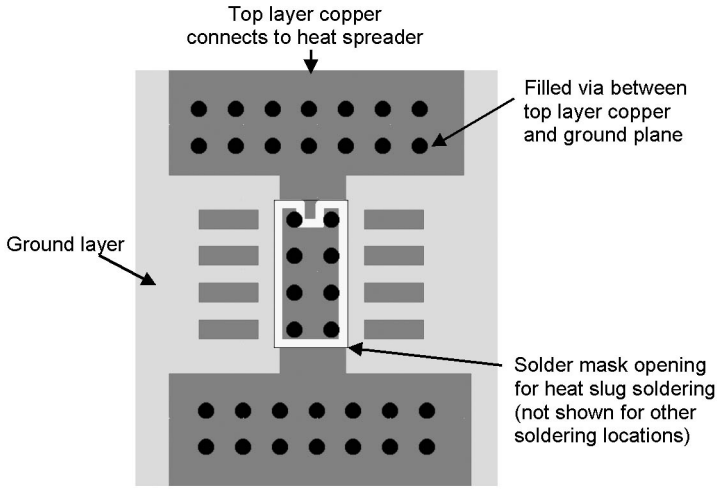


Table 2: Recommended Heat Sink PCB Layout

Mechanical Details

The CM3107 is available in an 8-lead SOIC and PSOP package.

SOIC-8 Mechanical Specifications

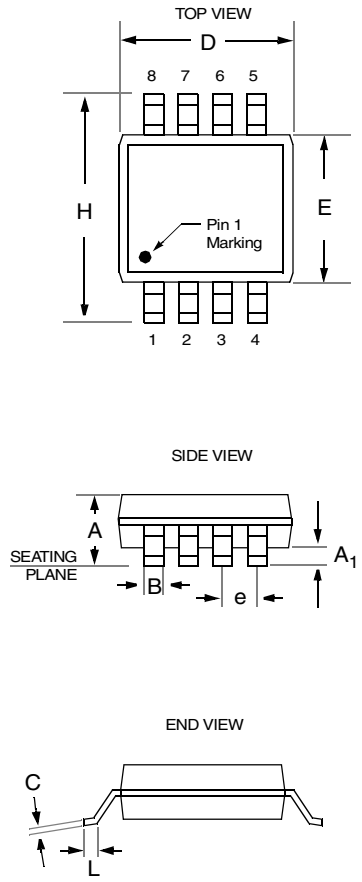
Dimensions for CM3107 devices packaged in 8-pin SOIC packages are presented below.

For complete information on the SOIC-8 package, see the California Micro Devices SOIC Package Information document.

PACKAGE DIMENSIONS				
Package	SOIC			
Leads	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.19	0.150	0.165
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
# per tube	100 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: inches				

* This is an approximate number which may vary.

Mechanical Package Diagrams



Package Dimensions for SOIC-8

Mechanical Details

PSOP-8 Mechanical Specifications

Dimensions for CM3107 devices packaged in 8-pin PSOP packages with an intagrated heatslug are presented below.

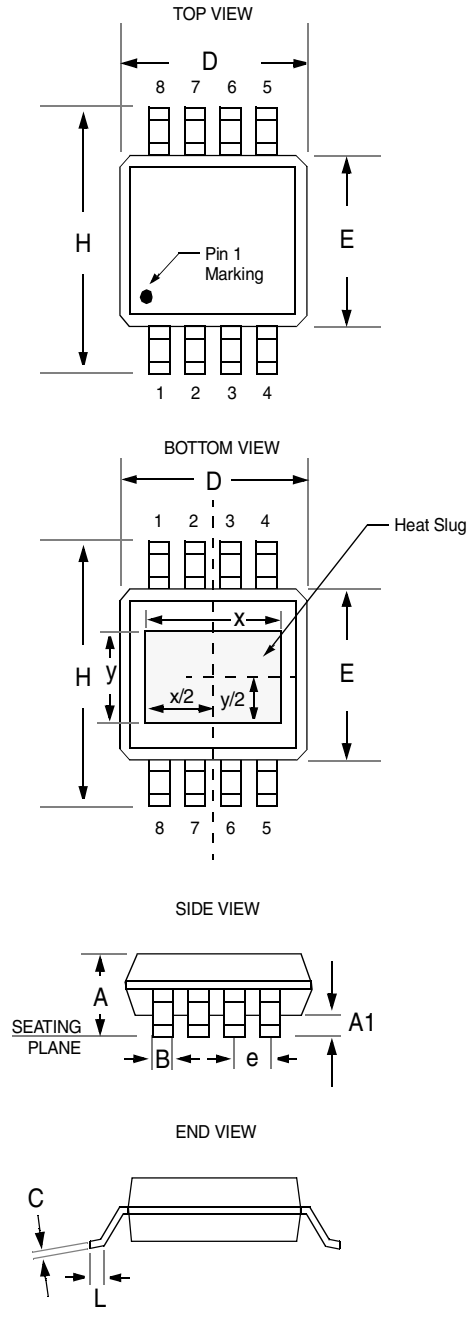
For complete information on the PSOP-8 package, see the California Micro Devices PSOP-8 Package Information document.

PACKAGE DIMENSIONS				
Package	PSOP-8			
Leads	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.30	1.62	0.051	0.064
A_1	0.03	0.10	0.001	0.004
B	0.33	0.51	0.013	0.020
C	0.18	0.25	0.007	0.010
D	4.83	5.00	0.190	0.197
E	3.81	3.99	0.150	0.157
e	1.02	1.52	0.040	0.050
H	5.79	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
x**	3.56	4.06	0.130	0.150
y**	2.29	2.79	0.090	0.110
# per tube	100 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: inches				

* This is an approximate number which may vary.

** Centered on package centerline.

Mechanical Package Diagrams



Package Dimensions for PSOP-8