Dual Linear Voltage Regulator for DDR-I and DDR-II Memory

Features

- Fully integrated power solution for DDR memory ICs
- Ideal for DDR-I ($2.5V_{DDQ}$) and DDR-II ($1.8V_{DDQ}$)
- Lowest system cost and smallest footprint with just two external output capacitors
- Two linear regulators:
  - V_{DDQ} regulator with a maximum output current of 1.5A shared by DRAM and V_{TT} regulator
  - source-sink V_{TT} regulator with maximum output current of 0.5A (DDR-I) or 0.3A (DDR-II)
- Fault output indicates overcurrent condition in either regulator, under voltage lock-out and overtemperature condition
- Reverse current protection if host is powered off
- PSOP-8 package with integrated heat spreader
- Lead-free versions available

Applications

- DDR-I and DDR-II memory power for:
  - Set Top Boxes, DVD Players, Games
  - Digital TVs, Flat Panel Displays
  - Printers, Digital Projectors
  - Embedded systems
  - Communications systems

Product Description

The CM3121 provides an integrated power solution for DDR-I and DDR-II memory systems in consumer electronics applications. The CM3121 is ideal for a 2.8V to 3.6V supply for DDR-I memory and 2.2V to 2.8V for DDR-II memory. The CM3121 features two independent linear regulators for V_{DDQ} and V_{TT} supply regulation. The default voltage for V_{DDQ} is 2.5V. The V_{DDQ} regulator SENSE pin allows for setting V_{DDQ} in the 2.2V to 2.8V range, or DDR-II memories from 1.7V to 1.9V. The V_{TT} regulator output is always half the V_{DDQ} voltage, derived internally. A capacitor should be connected to each of the two outputs.

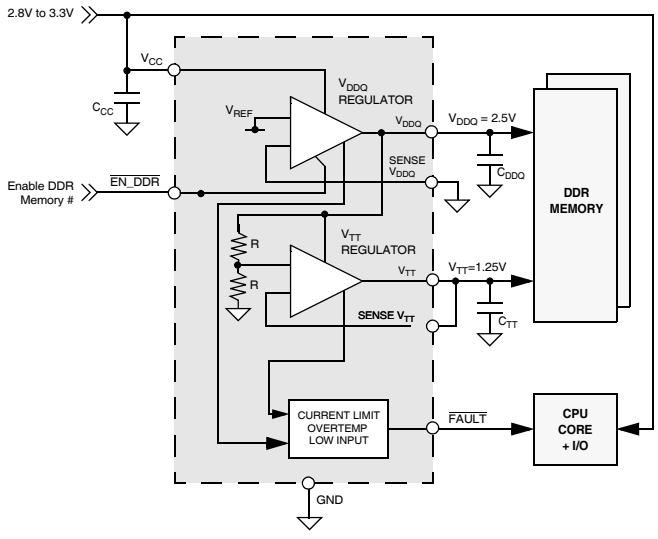
When $\overline{EN\_DDR}$ is set high, the two DDR regulators are disabled to minimize overall system power dissipation such as when memory is in standby.

The $\overline{FAULT}$ pin goes low whenever either of the two regulators goes into current limit mode, the input voltage drops too far or if overtemp occurs.

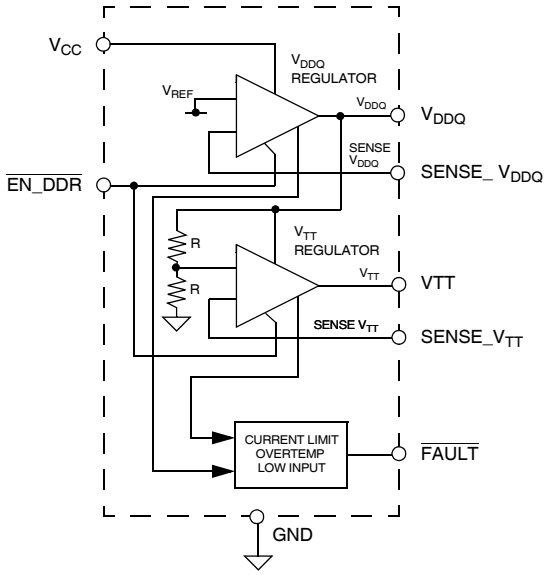
The CM3121 is available in a PSOP-8 package that has excellent thermal dissipation. It is available with optional lead-free finishing.

.

Typical Application Circuit



Circuit Schematic



Functional Description

The CM3121 provides power for DDR-I/DDR-II memories from two voltage regulators on-chip. There is an over-temperature thermal shutdown if any of the regulators overheat. Each regulator also has reverse current protection in the event of any being shut down.

The V_{DDQ} linear regulator can provide 2.5V/1.8V for DDR-I/-II memory at up to 1.5A. An external feedback resistor divider R1 and R2, when connected to the SENSE_V_{DDQ} pin, enables selection of V_{DDQ} output voltages from 2.2V to 2.8V for use with DDR-I memories requiring other than 2.5V for V_{DDQ} (see Figure 5). In this mode, the voltage on VDDQ is detemined as follows:

$$V_{DDQ} = 1.25V \times \frac{(R1+R2)}{R2}$$

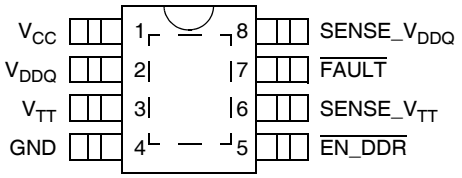
When SENSE_V_{DDQ} is connected to GND or left open, V_{DDQ} is fixed at 2.50V (and V_{TT} at 1.25V). For DDR-II operation, V_{DDQ} can be set from 1.7V to 1.9V. The V_{TT} regulator is a linear source-sink regulator powered from the V_{DDQ} output that supplies the V_{TT} supply required by DDR-I memory termination resistors. This regulator sinks or sources up to 0.5A. The V_{TT} output voltage accurately tracks $V_{DDQ}/2$ to 1%. When there is no V_{CC} provided, V_{TT} is powered down and its output is 0V. This regulator has overload current limiting of 0.6A minimum.

The $\overline{EN\_DDR}$ pin when set active low enables the CM3121 to operate in normal mode with V_{DDQ} and V_{TT} active. When $\overline{EN\_DDR}$ is high, the CM3121 is disabled and both V_{DDQ} and V_{TT} are set to 0V.

The $\overline{FAULT}$ output is normally at logic high but when an overcurrent occurs on either V_{DDQ} or V_{TT} outputs, $\overline{FAULT}$ goes active low, and remains low as long as the overcurrent fault persists. Also if the chip goes into thermal overload, or the input voltage V_{CC} drops sufficiently that the chip goes into Under Voltage Lock-Out mode (UVLO), $\overline{FAULT}$ goes active low, and remains low as long as the condition persists.

PACKAGE / PINOUT DIAGRAM

TOP VIEW



8-Lead PSOP

Note: This drawing is not to scale.

PIN DESCRIPTIONS

LEAD	NAME	DESCRIPTION
1	V_{CC}	Input supply.
2	V_{DDQ}	V_{DDQ} output.
3	V_{TT}	V_{TT} output for termination resistors or V_{REF}
4	GND	Ground reference.
5	$\overline{EN\_DDR}$	Enable DDR power. Active low input.
6	SENSE_V_{TT}	Sense input for V_{TT} rail adjustment.
7	$\overline{FAULT}$	Overcurrent Fault / UVLO indication, active low output.
8	SENSE_V_{DDQ}	Sense input for V_{DDQ} rail adjustment.
PAD	GND	Tied to ground reference.

Ordering Information

PART NUMBERING INFORMATION					
		Standard Finish		Lead-free Finish	
Leads	Package	Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
8	PSOP-8	CM3121-02SB	CM3121 02SB	CM3121-02SH	CM3121 02SH

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
ESD (Human Body Model)	±2000	V
Pin Voltages V_{CC} $\overline{EN\_DDR}$, SENSE_V_{DDQ}, SENSE_V_{TT}	 [GND - 0.6] to [+6.5] [GND - 0.6] to [V_{CC} + 0.6]	 V V
Storage Temperature Range	-40 to +150	°C
Operating Temperature Range Ambient Junction	 -40 to +85 0 to +125	 °C °C

STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
Ambient Operating Temperature Range	-40 to +85	°C
1. V_{DDQ} Regulator		
DDR-I Supply Voltage V_{CC}	[V_{DDQ} + 0.3] to 3.6	V
DDR-II Supply Voltage V_{CC}	2.2 to 2.8	V
Load Current (note 1)	0 to 1500	mA
C_{CC}, C_{DDQ}	10, 10	µF
2. V_{TT} Regulator		
DDR-I Supply Voltage V_{DDQ}	2.3 to 2.8	V
DDR-II Supply Voltage V_{DDQ}	1.7 to 1.9	V
DDR-I Load Current	0 to ±500	mA
DDR-II Load Current	0 to ±300	mA
C_{TT}	47	µF

Note 1: The V_{DDQ} regulator provides power for both the memory load and the V_{TT} regulator, supplying a total of 1.5A to the V_{DDQ} and V_{TT} outputs. For example, if the V_{DDQ} load current is 1.2A, then the maximum V_{TT} load current will be 0.3A, regardless of the actual V_{TT} output current rating.

Specifications (cont'd)

DDR-I Specifications

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
General Parameters						
T_{OVER}	Shutdown Junction Temperature		-	150	-	°C
T_{HYST}	Junction Temp Hysterisis	IC in shutdown	-	25	-	°C
I_{CCN}	Normal Mode V_{CC} Supply Current	$\overline{EN\_DDR}$ = logic "0", EN_CORE =logic "0"		700	1100	µA
I_{CCQ}	Shutdown Mode V_{CC} Supply Current	$\overline{EN\_DDR}$ = logic "1", V_{DDQ} = 0V, V_{TT} = 0V		2	10	µA
V_{IH}	$\overline{EN\_DDR}$ Input High Threshold	V_{CC} =3.3V	2.0			V
V_{IL}	$\overline{EN\_DDR}$ Input Low Threshold	V_{CC} =3.3V			0.4	V
UVLO	Under Voltage Lock-Out	I_{DDQ} = 10mA			1.8	V
t_{RISE}	V_{DDQ} Rise TIme	V_{CC} = 3.3V, C_{DDQ} = 10µF		0.5		ms
V_{DDQ} Regulator Parameters						
$V_{CC\ MIN}$	Input Voltage	V_{DDQ} = 2.5V, I_{DDQ} = 1.5A, SENSE_V_{DDQ} = 0V, Note 2	2.80			V
$V_{DDQ\ DEF}$	Default Output Voltage Range	I_{DDQ} = 0.01A, 2.8V ≤ V_{CC} ≤ 3.6V, SENSE_V_{DDQ} = 0V, Note 2	2.45	2.50	2.55	V
$V_{DDQ\ ADJ}$	Adjustable Output Voltage Range	V_{CC} = 3.6V, SENSE_V_{DDQ} tied to external resistors R1 and R2, Note 2	1.6		2.8	V
$V_{DDQ\ LD}$	Load Regulation	T_A = 25°C, V_{CC} = 3.3V, 0.01A ≤ I_{DDQ} ≤ 1.0A, Note 2	-	-	2.5	%
$V_{DDQ\ LINE}$	Line Regulation	T_A = 25°C, I_{DDQ} = 0.01A, 2.8V ≤ V_{CC} ≤ 3.6V, Note 2	-1.0	-	1.0	%
$e_{N\ DDQ}$	Output Noise Voltage	BW = 10Hz - 100kHz, C_{DDQ} = 10µF		49		µVrms
$I_{DDQ\ LIM}$	Current Limit	Note 2	1.7	2.0		A
$I_{DDQ\ SC}$	Short Circuit Current	V_{DDQ} < 0.3V		0.5		A

ELECTRICAL OPERATING CHARACTERISTICS (CONT'D) (SEE NOTE1)						
V_{TT} Regulator Parameters						
V_{TT}	Output Voltage Range	V_{DDQ} = 2.5V, I_{TT} = 0.01A,	1.20	1.25	1.30	V
$V_{TT\ REF}$	Output Voltage Range	V_{DDQ} = 2.500V, I_{TT} = 0.01A	1.225	1.250	1.275	V
$V_{TT\ LD}$	Load Regulation	T_A = 25°C, V_{DDQ} = 2.5V, 0.01A ≤ I_{TT} ≤ ±0.5A	-1.0	-	1.0	%
$V_{TT\ LINE}$	Line Regulation	T_A = 25°C, I_{TT} = 0.01A, 2.8V ≤ V_{CC} ≤ 3.6V, Note 2	-1.0	-	1.0	%
$e_{N\ TT}$	Output Noise Voltage	BW = 10Hz - 100kHz, C_{TT} = 10µF		51		µVrms
$I_{TT\ LIM}$	Current Limit		0.6	0.8		A
$I_{TT\ SC}$	Short Circuit Current	V_{TT} < 0.3V		0.3		A

Note 1: All parameters specified at T_A = -40°C to +85°C unless otherwise noted.

Note 2: Note that the I_{DDQ} current specified is the load current output from the V_{DDQ} pin. V_{DDQ} also supplies current internally to the V_{TT} regulator when it is sourcing current. The maximum source current can be up to 0.5A. So the maximum total current from the V_{DDQ} regulator is the external V_{DDQ} current I_{DDQ} added to the maximum V_{TT} sourcing current I_{TT}. All load currents are specified as such, but the V_{DDQ} current limit is specified at a current just above the total maximum current.

DDR-II Specifications

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 3)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
General Parameters						
T_{OVER}	Shutdown Junction Temperature		-	150	-	°C
T_{HYST}	Junction Temp Hysterisis	IC in shutdown	-	25	-	°C
I_{CCN}	Normal Mode V_{CC} Supply Current	$\overline{EN\_DDR}$ = logic "0",		700	1100	µA
I_{CCQ}	Shutdown Mode V_{CC} Supply Current	$\overline{EN\_DDR}$ = logic "1", V_{DDQ} = 0V, V_{TT} = 0V		2	10	µA
V_{IH}	$\overline{EN\_DDR}$ Input High Threshold	V_{CC} =3.3V	2.0			V
V_{IL}	$\overline{EN\_DDR}$ Input Low Threshold	V_{CC} =3.3V			0.4	V
UVLO	Under Voltage Lock-Out	I_{DDQ} = 10mA			1.8	V
t_{RISE}	V_{DDQ} Rise TIme	V_{CC} = 3.3V, C_{DDQ} = 10µF		0.5		ms

ELECTRICAL OPERATING CHARACTERISTICS (CONT'D) (SEE NOTE 3)

V_{DDQ} Regulator Parameters						
$V_{CC\ MIN}$	Input Voltage	V_{DDQ} = 2.5V, I_{DDQ} = 1.5A, SENSE_V_{DDQ} = 0V, Note 4	2.2			V
V_{DDQ}	Default Output Voltage Range	I_{DDQ} = 0.01A, V_{CC} = 3.3V, SENSE_V_{DDQ} = 0V, Note 4	1.75	1.80	1.85	V
$V_{DDQ\ ADJ}$	Adjustable Output Voltage Range	V_{CC} = 3.3V, SENSE_V_{DDQ} tied to external resistors R1 and R2, Note 4	1.6		2.8	V
$V_{DDQ\ LD}$	Load Regulation	T_A = 25°C, V_{CC} = 2.5V, 0.01A ≤ I_{DDQ} ≤ 1.0A, Note 4	-	-	2.5	%
$V_{DDQ\ LINE}$	Line Regulation	T_A = 25°C, I_{DDQ} = 0.01A, 2.2V ≤ V_{CC} ≤ 2.8V, Note 4	-1.0	-	1.0	%
$e_{N\ DDQ}$	Output Noise Voltage	BW = 10Hz - 100kHz, C_{DDQ} = 10µF		49		µVrms
$I_{DDQ\ LIM}$	Current Limit	Note 4	1.7	2.0		A
$I_{DDQ\ SC}$	Short Circuit Current	V_{DDQ} < 0.3V		0.5		A
V_{TT} Regulator Parameters						
V_{TT}	Output Voltage Range	V_{DDQ} = 1.8V, I_{TT} = 0.01A,	0.86	0.90	0.94	V
$V_{TT\ LD}$	Load Regulation	T_A = 25°C, V_{DDQ} = 1.8V, 0.01A ≤ I_{TT} ≤ ±0.3A	-1.0	-	1.0	%
$V_{TT\ LINE}$	Line Regulation	T_A = 25°C, I_{TT} = 0A, 2.2V ≤ V_{CC} ≤ 2.8V	-1.0	-	1.0	%
$e_{N\ TT}$	Output Noise Voltage	BW = 10Hz - 100kHz, C_{TT} = 10µF		51		µVrms
$I_{TT\ LIM}$	Current Limit		0.4	0.6		A
$I_{TT\ SC}$	Short Circuit Current	V_{TT} < 0.3V		0.3		A

Note 3: All parameters specified at T_A = -40°C to +85°C unless otherwise noted.

Note 4: Note that the I_{DDQ} current specified is the load current output from the V_{DDQ} pin. V_{DDQ} also supplies current internally to the V_{TT} regulator when it is sourcing current. The maximum source current can be up to 0.5A. So the maximum total current from the V_{DDQ} regulator is the external V_{DDQ} current I_{DDQ} added to the maximum V_{TT} sourcing current I_{TT}. All load currents are specified as such, but the V_{DDQ} current limit is specified at a current just above the total maximum current.

V_{CC}(1)	$\overline{EN\_DDR}$	$V_{DDQ\ OUT}$	$V_{TT\ OUT}$
2.8V to 3.6V	Low	V_{DDQ}	V_{DDQ} / 2
X	High	0V	0V

Table 1: Truth Table for CM3121

Performance Information

Power Supply Ripple Rejection
C_{CC} = 10μF, V_{CC} = 3.3V, I_{LOAD} = 50mA, PSRR measured with 50mV pk-pk sin wave on V_{CC}.

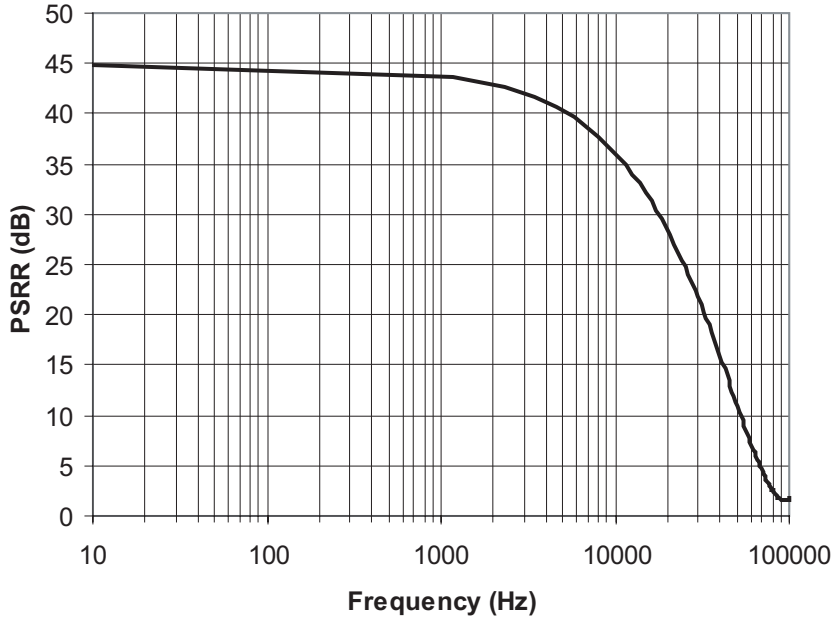


Figure 1. V_{DDQ} PSRR (V_{DDQ} = 2.5V)

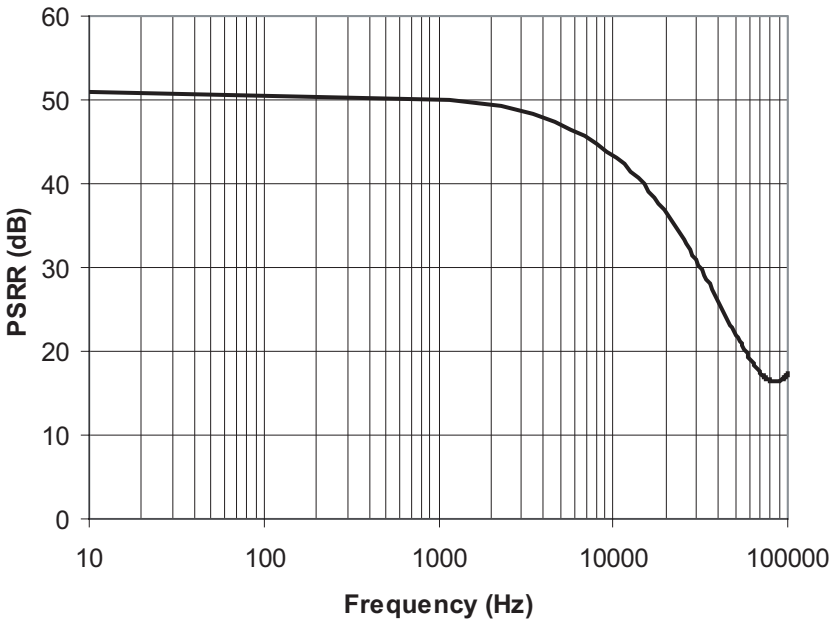


Figure 2. V_{TT} PSRR (V_{TT} = 1.25V)

Performance Information (cont'd)

Typical Thermal Characteristics

The overall junction to ambient thermal resistance (θ_{JA}) for device power dissipation (P_D) consists primarily of two paths in series. The first path is the junction to the case (θ_{JC}) which is defined by the package style, and the second path is case to ambient (θ_{CA}) thermal resistance which is dependent on board layout. The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$T_{JUNC} = T_{AMB} + P_D (\theta_{JC}) + P_D (\theta_{CA})$$

$$= T_{AMB} + P_D (\theta_{JA})$$

When a CM3121-02SB/SH (PSOP-8) is mounted on a double-sided printed circuit board with two square inches of copper allocated for "heat spreading," the resulting θ_{JA} is 40°C/W. Based on the over temperature limit of 150° C with an ambient of 70°C, the available power of this package will be:

$$P_D = \frac{150^\circ C - 70^\circ C}{40^\circ C/ W} = 2W$$

PCB Layout Considerations

The CM3121-02SB/SH has a heat spreader attached to the bottom of the PSOP-8 package in order for heat to be transferred more easily from the package to the PCB. The heat spreader is a copper pad of dimensions just smaller than the package itself. By positioning the matching pad on the PCB top layer to connect to the spreader during manufacturing, the heat will be transferred between the two pads. The drawing below shows the recommended PCB layout. Note that there are six vias on either side to allow the heat to dissipate into the ground and power planes on the inner layers of the PCB. Vias can be placed underneath the chip, but this can cause blockage of the solder. The ground and power planes should be at least 2 sq in. of copper by the vias. It also helps dissipation if the chip is positioned away from the edge of the PCB, and not near other heat-dissipating devices. A good thermal link from the PCB pad to the rest of the PCB will assure the best heat transfer from the CM3121 package to ambient, θ_{JA}, of around 40°C/W.

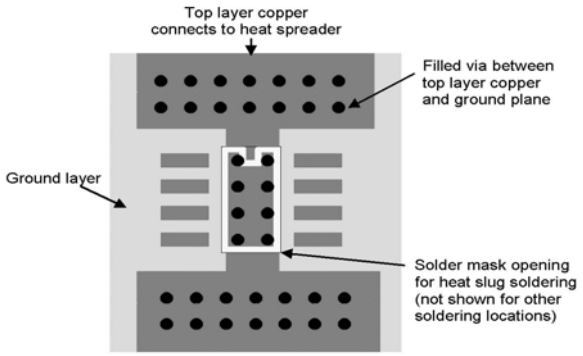


Figure 3. Recommended Heat Sink PCB Layout

Application Information

Other Applications

The CM3121 can be used without any external resistors if a V_{DDQ} voltage of 2.5V is required by connecting the SENSE_V_{DDQ} pin to GND.

Also in applications where a reference voltage (V_{REF}) is required, a PCB trace directly from the V_{TT} pin can be used. The V_{TT} output pin has an error relative to $V_{DDQ}/2$ of up to +/-25mV, which is well within most DDR system specs of +/-50mV. This is because the V_{TT} output internally tracks the V_{DDQ} output very closely due to the matched on-chip resistors R that tap down from the V_{DDQ} rail, and the low offset voltage of the V_{TT} regulator. It is recommended that the V_{REF} trace be connected directly to the V_{TT} pin, to eliminate noise and ripple on the V_{TT} line caused by current switching

.

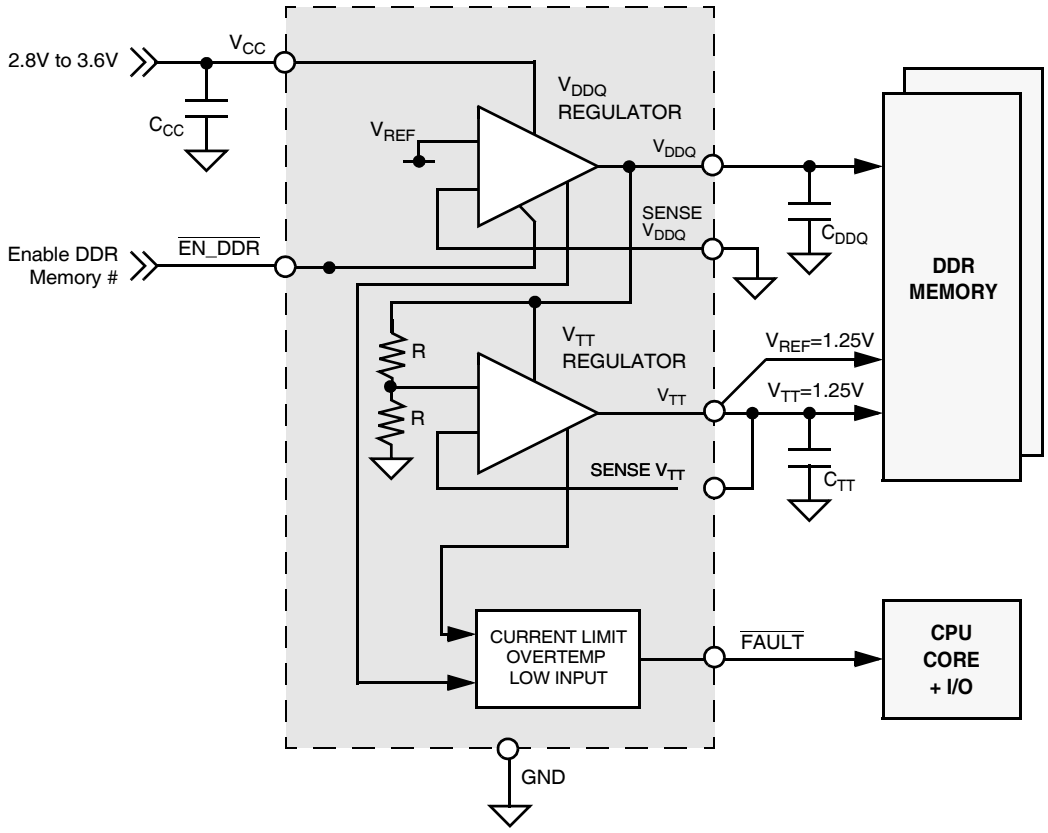


Figure 4. Typical Application for the CM3121

Application Information (cont'd)

DDR-II Application

For DDR-II applications, it is recommended that a lower input voltage than 3.3V be applied to reduce overall power dissipation. The input voltage can be as low as 2.1V worst case, so an input voltage of 2.4V ±10% would be the best input voltage for the least power dissipation. Also to obtain a V_{DDQ} voltage of 1.8V, a resistor divider comprising R1 = 56K and R2 = 130K would result in an output voltage of 1.79V for V_{DDQ}, and a V_{TT} of 0.895V.

The maximum current I_{DDQ} for the CM3121 in a DDR-II application is 1.5V, and the maximum for I_{TT} is 0.3V. This should be satisfactory for most DDR- II applications because the DDR- II memories do not require a V_{TT}, so the only current needed is for either a reference voltage or a controller input.

.

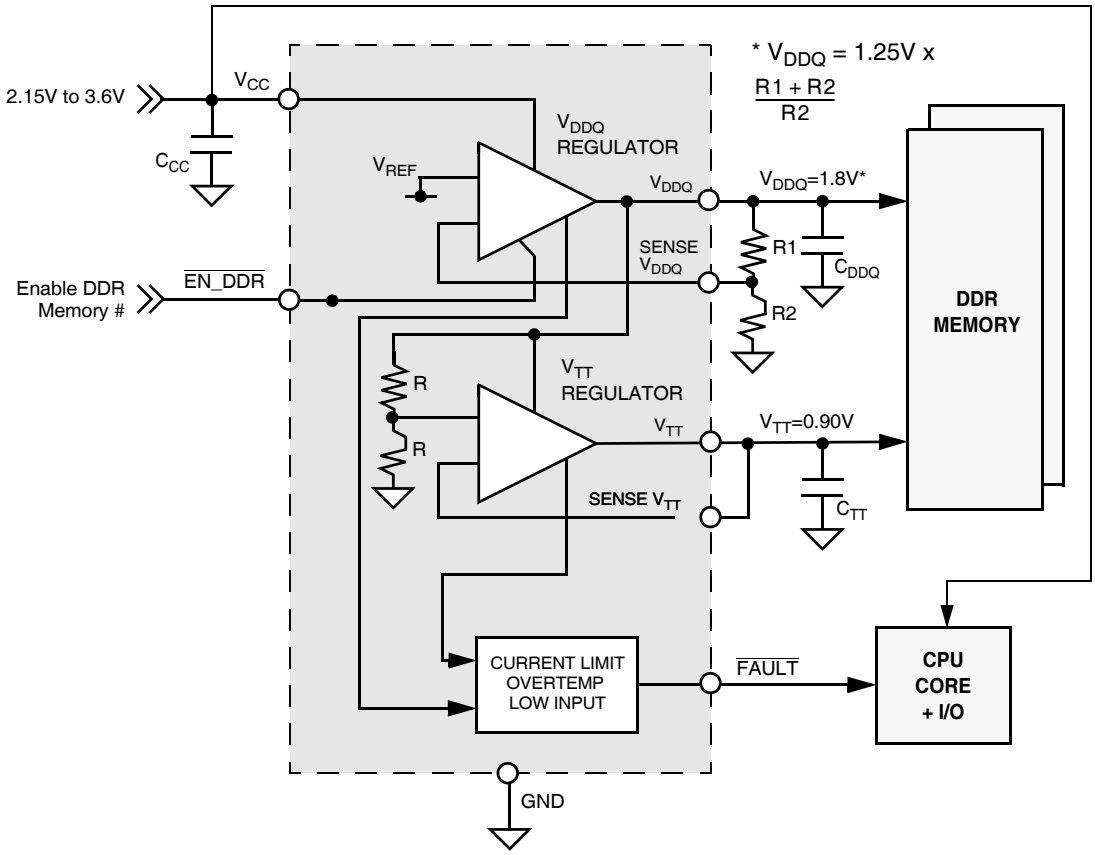


Figure 5. Minimal CM3132 DDR-II power solution.

Mechanical Details

PSOP-8 Mechanical Specifications

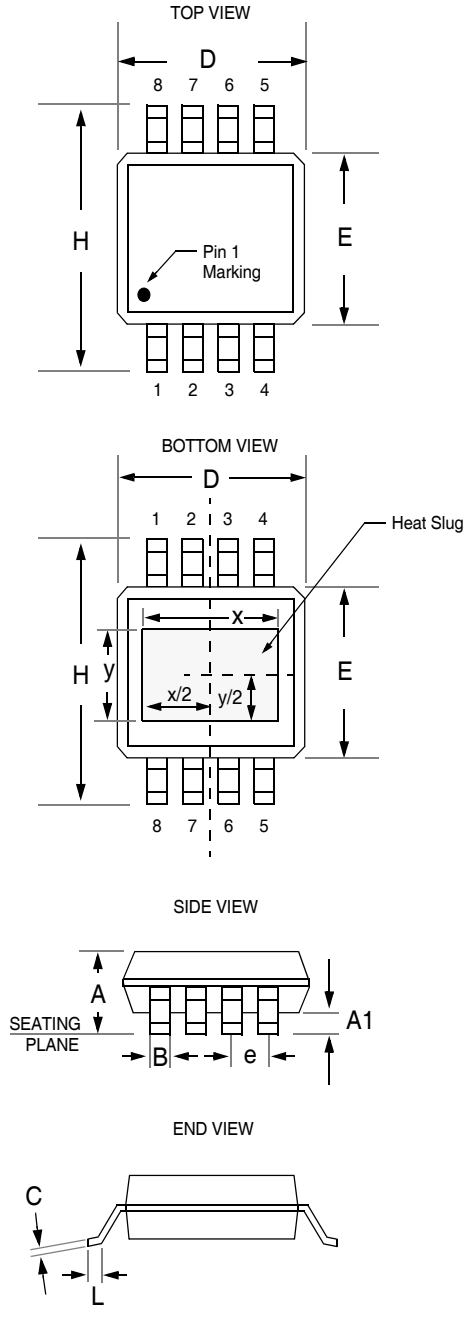
Dimensions for CM3121 devices packaged in an 8-lead PSOP package with a heatspreader are shown below.

PACKAGE DIMENSIONS				
Package	PSOP-8			
Leads	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.30	1.62	0.051	0.064
A_1	0.03	0.10	0.001	0.004
B	0.33	0.51	0.013	0.020
C	0.18	0.25	0.007	0.010
D	4.83	5.00	0.190	0.197
E	3.81	3.99	0.150	0.157
e	1.02	1.52	0.040	0.060
H	5.79	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
x**	3.30	3.81	0.130	0.150
y**	2.29	2.79	0.090	0.110
# per tube	100 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: inches				

* This is an approximate number which may vary.

** Centered on package centerline.

Mechanical Package Diagrams



Package Dimensions for PSOP-8