Triple Linear Voltage Regulator for DDR-I/-II Memory

Features

- Integrated power solution for DDR-I and DDR-II memory systems with few external components
- Three all-linear regulators for V_{DDQ}, V_{TT} and V_{STBY} power supply applications
- Lowest system cost and smallest footprint for DDR power solutions
- V_{DDQ} regulator/driver utilizes external N-FET to provide up to 15A current at 2.5V/1.8V
- V_{TT} source/sink regulator provides up to 2A at 1.25V for DDR-I systems or 0.65A at 0.9V for the DDR-II memory controller (not DDR-II memory)
- LDO standby regulator provides up to 500mA at 2.5V for DDR-I and at 1.8V for DDR-II systems
- Can be ganged for higher current applications
- Over temperature and reverse current protection
- Over current protection for V_{STBY} and V_{TT} regulator
- Available in 8 lead and 14 lead PSOP packages
- Lead-free versions available

Applications

- Desktop PCs, notebooks, and workstations
- Set top boxes, digital TVs, printers
- Embedded systems

Product Description

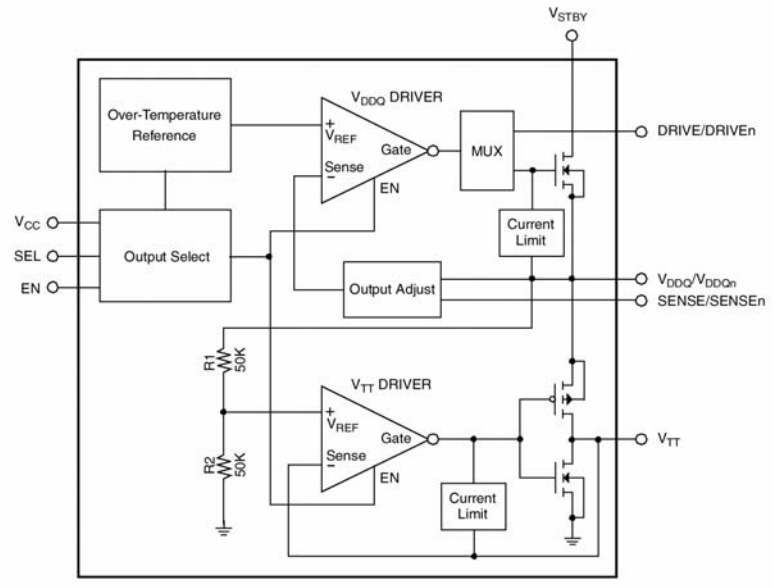
The CM3131 family of all-linear regulators provides an integrated power solution for DDR-I/-II memory systems in both run-time and standby modes of operation. The CM3131 is ideal for designs incorporating both a main 3.3V and a standby (3.3V or 5V) supply. The CM3131 features three independent linear regulators for V_{DDQ}, V_{TT} and V_{STBY} supply regulation and will maintain an accuracy of ±1% across the operating temperature range.

The CM3131 is offered in two configurations. The CM3131-01/11 drives a single external N-FET on a single V_{DDQ} rail. The CM3131-02 drives two external unmatched N-FETs on two V_{DDQ} rails. Each V_{DDQ} rail incorporates an adjustment pin (SENSE) to enable setting V_{DDQ} in the 2.2V to 2.8V range, supporting DIMMs with different supply requirements or DDR-II type devices.

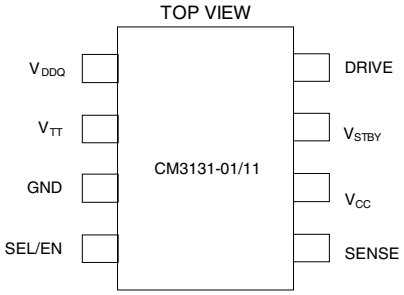
The CM3131-01/11 is available in 8-lead PSOP package and the CM3131-02 is available in 14-lead PSOP package.

The CM3131 devices are also available with optional lead-free finishing.

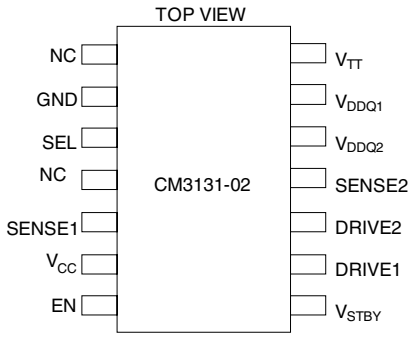
Electrical Schematic



PACKAGE / PINOUT DIAGRAM



PSOP-8



PSOP-14

Note: These drawings are not to scale.

PIN DESCRIPTIONS

PART NUMBER			NAME	DESCRIPTION
-01	-11	-02		
1	1	13	V_{DDQ} / V_{DDQ1}	V_{DDQ} input for V_{REF} and V_{DDQ} Output in Standby
2	2	14	V_{TT}	V_{TT} Output for termination resistors
		1	NC	No connection
3	3	2	GND	Ground
4		3	SEL	Select Input, active low
		4	NC	No connection
	4	7	EN	Enable Input, active high
5	5	5	SENSE / SENSE1	Sense Input, Adjusts V_{DDQ} Rail
6	6	6	V_{CC}	3.3V Main Input Supply
7	7	8	V_{STBY}	3.3V or 5V Standby Input Supply
8	8	9	DRIVE / DRIVE1	Drive Output for V_{DDQ} External n-FET
		10	DRIVE2	Drive Output for V_{DDQ} External n-FET
		11	SENSE2	Sense Input, Adjusts V_{DDQ} Rail
		12	$V_{DDQ\,2}$	V_{DDQ} Input for V_{REF} and V_{DDQ} Output in Standby

Ordering Information

PART NUMBERING INFORMATION

PINS	PACKAGE	STANDARD FINISH		LEAD-FREE FINISH	
		ORDERING PART NUMBER[1]	PART MARKETING	ORDERING PART NUMBER[1]	PART MARKING
8	PSOP-8	CM3131-01SB	CM3131-01SB	CM3131-01SH	CM3131-01SH
8	PSOP-8	CM3131-11SB	CM3131-11SB	CM3131-11SH	CM3131-11SH
14	PSOP-14	CM3131-02SB	CM3131-02SB	CM3131-02SH	CM3131-02SH

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Functional Description

The CM3131-01 / -11 and CM3131-02 provide power for DDR-I/DDR-II memories from three voltage regulators on-chip with either one or two external N-FETs respectively. There is an over-temperature thermal shutdown if any of the regulators overheat. Each regulator has reverse current protection in the event of any being shut down.

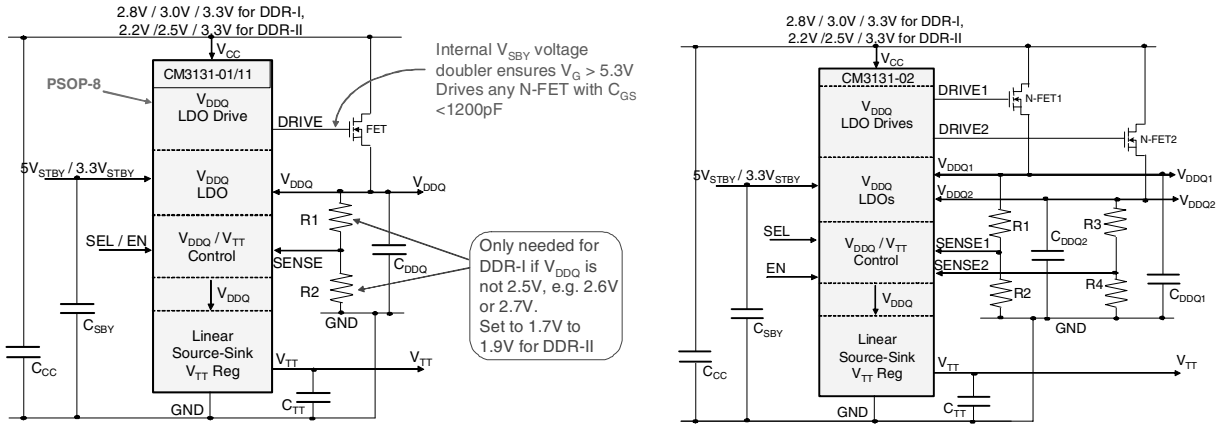
The linear regulator-driver/s with external N-FET/s can provide up to 15A at 2.5V/1.8V for the V_{DDQ} of DDR-I/-II memory, from an input supply voltage of 2.8V-3.6V. An external feedback resistor divider, connected to the SENSE1 pin, enables selection of V_{DDQ} output voltages from 2.2V to 2.8V for use with DDR-I memories requiring other than 2.5V for V_{DDQ}. V_{DDQ} = 1.25V x (R1+R2)/R2. When SENSE1 is connected to GND or left open, V_{DDQ} is fixed at 2.50V (and VTT at 1.25V). For DDR-II operation, V_{DDQ} can be set from 1.7V to 1.9V.

The V_{TT} regulator is a linear source-sink regulator powered from the V_{DDQ} output that supplies the V_{TT} supply required by DDR-I memory termination resistors. This regulator sinks or sources up to 2A at 1.25V to or from the DDR-I bus termination resistors. For DDR-II applications, the regulator sinks or sources 0.65A at 0.9V. The V_{TT} output voltage accurately tracks V_{DDQ}/2 to 1%. When there is no V_{CC} provided, V_{TT} is powered down and its output is 0V. This regulator has overload current limiting of 2.5A.

The standby regulator is a LDO regulator that is powered from a standby voltage, V_{STBY}, of 3.3V or 5V, and supplies a regulated output of up to 500mA to the V_{DDQ} of the DDR memory to enable it to retain its contents during the standby mode. It provides 2.5V for DDR-I and 1.8V for DDR-II.

The CM3131-01 and CM3131-11 differ with regards the selection of truth table for determining which S0-S5 sequencing matrix the chip is set for. The CM3131-02 has both EN and SEL pins to more accurately define each Sx stage without monitoring the V_{CC} or V_{STBY} voltages.

Two CM3131s can be ganged together to provide V_{DDQ} power to dual channels of DDR memory, and the memory controller chip of any chip set.



Examples of Single and Dual N-FET Drive Configurations

Functional Description (cont'd)

V_{CC}	V_{STBY}	SEL	$V_{DDQ\ 1,2}$	V_{TT}
3V/3.3V	5V/3.3V	ON	V_{DDQ}	V_{DDQ} / 2
X	5V/3.3V	OFF	$V_{DDQ\ STBY}$	0V
$<V_{CC\ MIN}$	X	ON	0V	0V
X	$<V_{STBY\ MIN}$	OFF	0V	0V

Truth Table for CM3131-01

S to R	V_{CC}	V_{STBY}	SEL	$V_{DDQ\ OUT}$	$V_{TT\ OUT}$
S0	3V/3.3V	5V/3.3V	ON	V_{DDQ}	V_{DDQ} / 2
S1	3V/3.3V	5V/3.3V	ON	V_{DDQ}	V_{DDQ} / 2
S2	3V/3.3V	5V/3.3V	ON	V_{DDQ}	V_{DDQ} / 2
S3	3V/3.3V	5V/3.3V	OFF	$V_{DDQ\ STBY}$	0V
S4	$<V_{CC\ MIN}$	5V/3.3V	OFF	0V	0V
S5	$<V_{CC\ MIN}$	5V/3.3V	OFF	0V	0V

Sequencing Matrix for CM3131-01 for Suspend to RAM operation

No S to R	V_{CC}	V_{STBY}	SEL	$V_{DDQ\ OUT}$	$V_{TT\ OUT}$
S0	3V/3.3V	5V/3.3V	ON	V_{DDQ}	V_{DDQ} / 2
S1	3V/3.3V	5V/3.3V	ON	V_{DDQ}	V_{DDQ} / 2
S2	3V/3.3V	5V/3.3V	ON	V_{DDQ}	V_{DDQ} / 2
S3	$<V_{CC\ MIN}$	5V/3.3V	ON	0V	0V
S4	$<V_{CC\ MIN}$	5V/3.3V	ON	0V	0V
S5	$<V_{CC\ MIN}$	5V/3.3V	ON	0V	0V

Sequencing Matrix for CM3131-01 for Suspend to RAM Not Supported

V_{CC}	V_{STBY}	EN	$V_{DDQ\ OUT}$	$V_{TT\ OUT}$
3V/3.3V	5V/3.3V	ON	V_{DDQ}	V_{DDQ} / 2
$<V_{CC\ MIN}$	5V/3.3V	ON	$V_{DDQ\ STBY}$	0V
$<V_{CC\ MIN}$	X	OFF	0V	0V
X	$<V_{STBY\ MIN}$	OFF	0V	0V

Truth Table for CM3131-11

Functional Description (cont'd)

S to R	V_{CC}	V_{STBY}	EN	$V_{DDQ\ OUT}$	$V_{TT\ OUT}$
S0	3V/3.3V	5V/3.3V	ON	V_{DDQ}	V_{DDQ} / 2
S1	3V/3.3V	5V/3.3V	ON	V_{DDQ}	V_{DDQ} / 2
S2	3V/3.3V	5V/3.3V	ON	V_{DDQ}	V_{DDQ} / 2
S3	$<V_{CC\ MIN}$	5V/3.3V	ON	$V_{DDQ\ STBY}$	0V
S4	$<V_{CC\ MIN}$	5V/3.3V	OFF	0V	0V
S5	$<V_{CC\ MIN}$	5V/3.3V	OFF	0V	0V

Sequencing Matrix for CM3131-11 for Suspend to RAM operation

V_{CC}	V_{STBY}	SEL	EN	$V_{DDQ\ OUT}$	$V_{TT\ OUT}$
3V/3.3V	5V/3.3V	ON	ON	V_{DDQ}	V_{DDQ} / 2
$<V_{CC\ MIN}$	5V/3.3V	OFF	ON	$V_{DDQ\ STBY}$	0V
X	$<V_{STBY\ MIN}$	OFF	ON	0V	0V
0V	X	ON	ON	0V	0V
$<V_{CC\ MIN}$	X	X	OFF	0V	0V

Truth Table for CM3131-02

Table 3	V_{CC}	V_{STBY}	SEL	EN	$V_{DDQ\ OUT}$	$V_{TT\ OUT}$
S0	3V/3.3V	5V/3.3V	ON	ON	V_{DDQ}	V_{DDQ} / 2
S1	3V/3.3V	5V/3.3V	ON	ON	V_{DDQ}	V_{DDQ} / 2
S2	3V/3.3V	5V/3.3V	ON	ON	V_{DDQ}	V_{DDQ} / 2
S3	$<V_{CC\ MIN}$	5V/3.3V	OFF	ON	$V_{DDQ\ STBY}$	0V
S4	$<V_{CC\ MIN}$	X	ON	OFF	0V	0V
S5	$<V_{CC\ MIN}$	X	ON	OFF	0V	0V

Sequencing Matrix for CM3131-02 for Suspend to RAM operation

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	RATING	UNITS
ESD (Human Body Model)	± 2000	V
V_{CC}, V_{STBY}, DRIVEx	(GND – 0.6) to (+6.5)	V
SEL, SENSEx	(GND – 0.6) to (V_{CC} + 0.6)	V
V_{DDQX}, V_{TT}	(GND – 0.6) to (V_{CC} + 0.6)	V
Operating Temperature Range		
Ambient	0 to +70	°C
Junction	0 to +125	°C
Storage Temperature Range	-40 to +150	°C

STANDARD OPERATING CONDITIONS		
PARAMETER	RATING	UNITS
Temperature Range (Ambient)	0 to +70	°C
1. V_{DDQ} Regulator-Driver		
Supply Voltage V_{CC}	2.8 to 3.6	V
Load Current	0 to 15	A
C_{CC}, C_{DDQ}	4.7, 220	µF
2. V_{TT} Regulator		
Supply Voltage V_{DDQ}	1.8 or 2.5	V
Load Current	0 to +/- 0.9 or +/- 2.0	A
C_{TT}	220	µF
3, V_{STBY} Regulator		
Supply Voltage V_{STBY}	3.0 to 5.5	V
Load Current	0 to 500	mA

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
General Parameters						
T_{OVER}	Shutdown Junction Temperature		-	150	-	°C
V_{DDQ} Regulator/Driver Parameters (with FDP6030L or similar MOSFET as an external transistor)						
$V_{CC\ MIN}$	Input Voltage	V_{DDQ} = 2.5V, I_{DDQ} = 6A, each channel, SENSE = 0V	2.80			V
V_{DDQ}	Output Voltage Range	I_{DDQ} = 2.5A, V_{CC} = 3.3V, SENSE = 0V	2.45	2.50	2.55	V
$V_{DRIVE\ H\ 5}$	DRIVE High Output Voltage	V_{STBY} = 5V, V_{CC} = 3.3V		9.50		V
$V_{DRIVE\ H\ 3}$	DRIVE High Output Voltage	V_{STBY} = 3.3V, V_{CC} = 3.3V		6.1		V
C_{LOAD}	External FET Gate Capacitance	V_{STBY} = 5V, V_{CC} = 3.3V		1200		pF
t_{RISE}	DRIVE Voltage Rise Time	V_{STBY} = 5V, V_{CC} = 3.3V, C_{LOAD} = 1200pF		2.5		ms
$V_{DDQ\ LOAD}$	Load Regulation @ 25°C	V_{CC} = 3.3V, I_{DDQ} = 0.1A to 6A each channel	-1.0	-	1.0	%
$V_{DDQ\ LINE}$	Line Regulation @ 25°C	I_{DDQ} = 2.5A, V_{CC} = 2.8V to 3.6V	-1.0	-	1.0	%
V_{TT} Regulator Parameters						
V_{TT}	Output Voltage Range	V_{DDQ} = 2.50V, I_{TT} = 0A	1.20	1.25	1.30	V
$V_{TT\ LOAD}$	Load Regulation @ 25C	I_{TT} = 0.1A to 2A, V_{DDQ} = 2.5V	-1.0	-	1.0	%
$V_{TT\ LINE}$	Line Regulation @ 25C	I_{TT} = 0A, V_{CC} = 2.8V to 3.6V	-1.0	-	1.0	%
$I_{TT\ LIM}$	Current Limit		2.3			A
$I_{TT\ SC}$	Short Circuit Current Limit	V_{TT} < 1V	0.6			A
V_{STBY} Regulator Parameters						
$V_{DDQ\ STBY}$	Output Voltage Range	I_{DDQ} =150mA, V_{STBY} = 5V, SENSE =0V	2.45	2.50	2.55	V
$V_{DDQSB\ LD}$	Load Regulation @ 25C	I_{DDQ} = 10mA to 500mA, V_{STBY} = 5V	-1.0	-	1.0	%
$V_{DDQ\ SBLN}$	Line Regulation @ 25C	I_{DDQ} = 150mA, V_{STBY} = 3.0V to 5.5V	-1.0	-	1.0	%
$V_{DROPOUT}$	Dropout Voltage	I_{DDQ} = 250mA, each channel		250	450	mV
$I_{STBY\ LIM}$	Overload Current Limit		400			mA
$I_{STBY\ SC}$	Short Circuit Current Limit	V_{DDQ} < 1V	170			mA

Note 1: All parameters specified at T_A = 0°C to +70°C unless otherwise noted.

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS (Cont'd)						
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
All Regulators						
I_{CCN}	Normal Mode V_{CC} Supply Current	Normal mode (S0-S2) ($V_{DDQ1,2}$=V_{DDQ} ,V_{TT}=V_{DDQ}/2)			5	µA
I_{STBYN}	Normal Mode V_{STBY} Supply Current	Normal mode (S0-S2) ($V_{DDQ1,2}$=V_{DDQ} ,V_{TT}=V_{DDQ}/2)		1650	2450	µA
I_{STBYS}	Standby Mode V_{STBY} Supply Current	Standby mode (S3) ($V_{DDQ1,2}$=$V_{DDQSTBY}$,V_{TT}=0)		550	850	µA
I_{STBYQ}	Shutdown Mode Quiescent Current	Shutdown mode (S4-S5) ($V_{DDQ1,2}$=0 ,V_{TT}=0)		70	120	µA

Mechanical Details

8-lead PSOP Package Dimensions

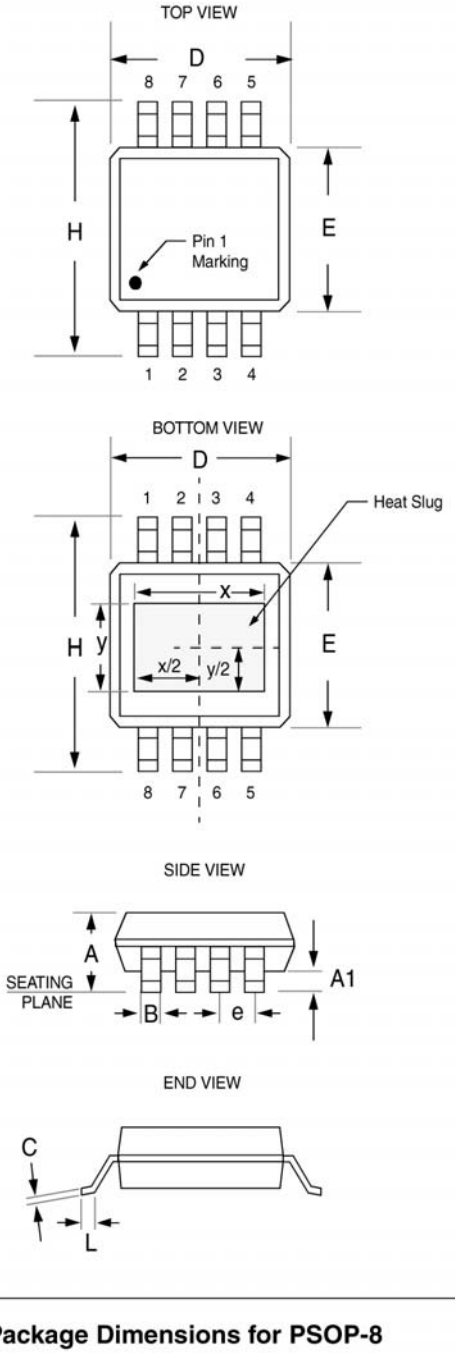
Dimensions for PSOP-8 devices packaged in 8-pin PSOP packages with an intagrated heatslug are presented below.

PACKAGE DIMENSIONS				
Package	PSOP-8			
Leads	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.30	1.62	0.051	0.064
A_1	0.03	0.10	0.001	0.004
B	0.33	0.51	0.013	0.020
C	0.18	0.25	0.007	0.010
D	4.83	5.00	0.190	0.197
E	3.81	3.99	0.150	0.157
e	1.02	1.52	0.040	0.060
H	5.79	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
x**	3.30	3.81	0.130	0.150
y**	2.29	2.79	0.090	0.110
# per tube	100 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: inches				

* This is an approximate number which may vary.

** Centered on package centerline.

Mechanical Package Diagrams



Package Dimensions for PSOP-8

Mechanical Details (cont'd)

14-lead PSOP Package Dimensions

Dimensions for devices packaged in a 14-pin PSOP package with an integrated heat slug are presented below.

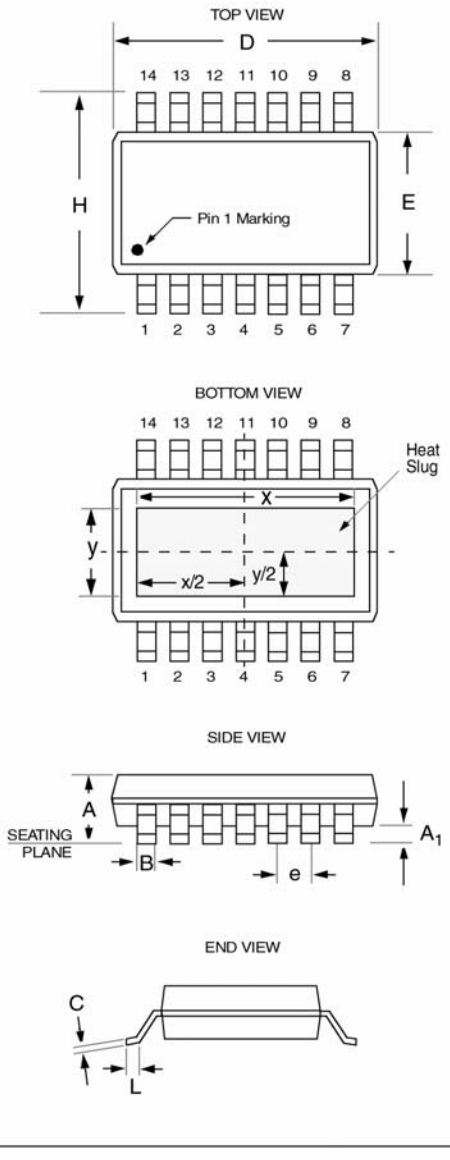
PACKAGE DIMENSIONS				
Package	PSOP			
Pins	14			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	1.37	1.73	0.054	0.068
A_1	0.025	0.102	0.001	0.004
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.007	0.010
D	8.55	8.75	0.337	0.344
E	3.81	3.94	0.150	0.155
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
x*	6.60	7.11	0.260	0.280
y*	2.29	2.79	0.090	0.110
# per tube	55 pieces***			
# per tape and reel	2500 pieces			
Controlling dimension: inches				

*Centered on package centerline.

** Contact the factory for heat slug dimensions.

*** This is an approximate number which may vary.

Mechanical Package Diagrams



Package Dimensions for PSOP-14