2A Sink/Source DDR-I, -II Bus Termination Regulator

Features

- Ideal for DDR-I, -II V_{TT} applications
- Sinks and sources 2A for DDR-I, 0.6A for DDR-II
- Shutdown input to support ACPI states
- Operates down to 1.5V input voltage
- Integrated power MOSFETs
- Overcurrent protection
- Over temperature protection
- Excellent accuracy
  $V_{TT} = V_{REF} \pm 30mV$
  $V_{TT} = V_{DDQ}/2 \pm 2\%$
- 8-pin SOIC or PSOP package
- Lead-free versions available

Applications

- DDR-I, -II memory termination
- Active termination buses
- Graphics card memory termination

Product Description

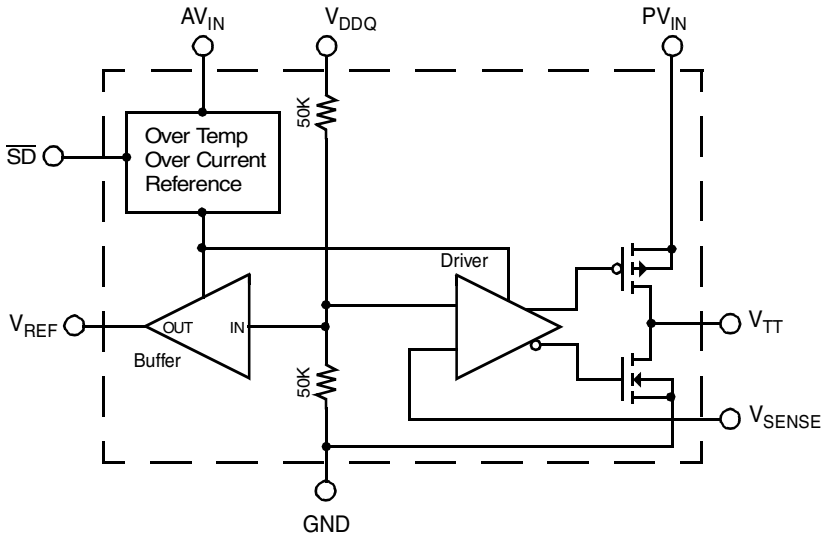
The CM3196 is a sinking and sourcing regulator specifically designed for DDR-I, -II V_{TT} bus termination. The output voltage accurately tracks $V_{DDQ}/2$. For DDR-I it can source and sink current up to 2A with a load regulation of 0.5%. This current adequately serves both single and dual channel DDR-I memory systems. For power conscious notebook applications, the CM3196 also operates from a V_{DDQ} of 1.5V or 1.8V with less current drive. For DDR-II applications, the CM3196 provides up to 0.6A at 0.9V to drive the memory controller V_{TT}.

For boards which support Suspend to RAM (STR) functionality, the CM3196 provides a Shutdown ($\overline{SD}$) pin. When $\overline{SD}$ is set low, V_{TT} will be in tri-state mode, causing the output to go high impedance. In this mode, CM3196 power is saved by significantly reducing the quiescent current. V_{REF} voltage remains $V_{DDQ}/2$.

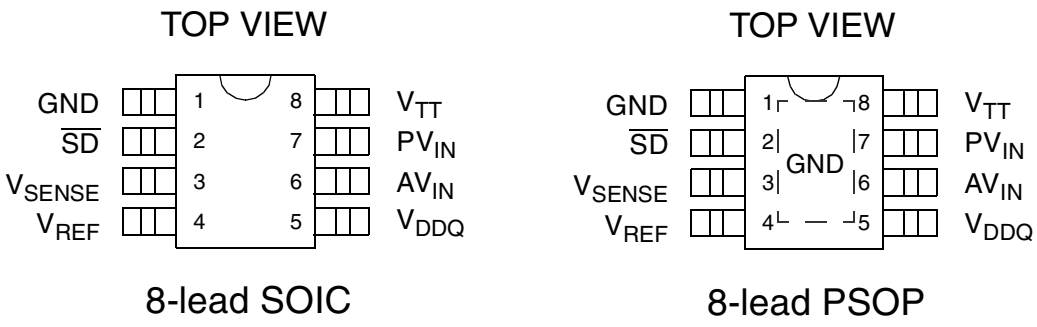
The CM3196 provides overcurrent and over temperature protection. These features protect the chip from excessive heating due to high current and high temperature.

The CM3196 is housed in an 8-pin SOIC or PSOP package and is available with optional lead-free finishing.

Simplified Electrical Schematic



PACKAGE / PINOUT DIAGRAM



Note: This drawing is not to scale.

PIN DESCRIPTIONS

LEAD(S)	NAME	DESCRIPTION
1	GND	Ground
2	$\overline{SD}$	Shutdown input, active low
3	V_{SENSE}	Feedback from V_{TT} input
4	V_{REF}	Reference output, $V_{DDQ}/2$
5	V_{DDQ}	V_{DDQ} input
6	AV_{IN}	Analog circuit power input
7	PV_{IN}	Power transistor input
8	V_{TT}	Output

Ordering Information

PART NUMBERING INFORMATION

		Standard Finish		Lead-free Finish	
Pins	Package	Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
8	SOIC-8	CM3196-12SN	CM3196-12SN	CM3196-12SM	CM3196-12SM
8	PSOP-8	CM3196-12SB	CM3196-12SB	CM3196-12SH	CM3196-12SH

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
AV_{IN} Operating Supply Voltage	7	V
V_{DDQ} Input Voltage	7	V
Pin Voltages V_{TT} Output Any other pins	 7 7	 V V
Storage Temperature Range	-40 to +150	°C
Operating Temperature Range Ambient Junction	 -40 to +85 -40 to +150	 °C °C
Power Dissipation (See note 1)	Internally Limited	W

Note 1: These devices must be derated based on thermal resistance at elevated temperatures. The device packaged in an 8-pin SOIC package must be derated at θ_{JA} = 151°C/W and the 8-pin PSOP must be derated at θ_{JA} = 43°C/W.

Specifications (cont'd)

DDR-I Features

STANDARD OPERATING CONDITIONS		
PARAMETER	**VALUE**	**UNITS**
V_{DDQ}	2.5	V
AV_{IN}	2.5	V
PV_{IN}	2.5	V
Ambient Operating Temperature	-40 to +85	°C
C_{VOUT}	220 ±20%	µF

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{IN}	Input Voltage Range PV_{IN} pin AV_{IN} pin		 2.2 2.2	 2.5 2.5	 AV_{IN} 5.5	 V V
I_{CC}	AV_{IN} Quiescent Current	I_{TT} = 0A		450		µA
I_{CCSD}	AV_{IN} Quiescent Current in Shut Down	V_{SD} = logic "0"		115		µA
V_{TT}	V_{TT} Output Voltage PV_{IN} = 2.5V PV_{IN} = 1.8V PV_{IN} = 1.5V	 I_{LOAD} = 0 to 2A or I_{LOAD} = -2A to 0A I_{LOAD} = 0 to 0.75A or I_{LOAD} = -0.75A to 0A I_{LOAD} = 0 to 0.3A or I_{LOAD} = -0.3A to 0A	 1.225 1.225 1.225	 1.250 1.250 1.250	 1.275 1.275 1.275	 V V V
V_{REF}	Output Reference Voltage	V_{DDQ} = 2.5V, I_{REF} = 0A	1.225	1.250	1.275	V
VOS_{VTT}	Output Offset from V_{REF}		-30		30	mV
Z_{REF}	V_{REF} Output Impedance	I_{REF} = -5µA to 5µA		5		kΩ
Z_{VDDQ}	V_{DDQ} Input Impedance			100		kΩ
I_{LIM}	V_{TT} Current Limit			2.5		A
V_{SD}	Shutdown Logic Logic "1" Level Logic "0" Level		 1.5		 0.4	 V V
$T_{DISABLE}$ T_{HYST}	Shutdown Temperature Thermal Hysteresis			150 30		°C °C

Note 1: Operating characteristics are over Standard Operating Conditions unless otherwise specified.

Specifications (cont'd)

DDR-II Features

STANDARD OPERATING CONDITIONS		
PARAMETER	**VALUE**	**UNITS**
V_{DDQ}	1.8	V
AV_{IN}	3.3	V
PV_{IN}	1.8	V
Ambient Operating Temperature	-40 to +85	°C
C_{VOUT}	220 ±20%	µF

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{IN}	Input Voltage Range PV_{IN} pin AV_{IN} pin		 1.5 2.2	 1.8 3.3	 AV_{IN} 5.5	 V V
I_{CC}	AV_{IN} Quiescent Current	I_{TT} = 0A		450		µA
I_{CCSD}	AV_{IN} Quiescent Current in Shut Down	V_{SD} = logic "0"		115		µA
V_{TT}	V_{TT} Output Voltage PV_{IN} = 1.8V PV_{IN} = 1.5V $AV_{IN} \geq 2.2V$, $PV_{IN} \geq 2.2V$	 I_{LOAD} = 0 to 0.6A or I_{LOAD} = -0.6A to 0A I_{LOAD} = 0 to 0.3A or I_{LOAD} = -0.3A to 0A I_{LOAD} = 0 to 1.2A or I_{LOAD} = -1.2A to 0A	 0.882 0.882 0.882	 0.9 0.9 0.9	 0.918 0.918 0.918	 V V V
V_{REF}	Output Reference Voltage	V_{DDQ} = 1.8V, I_{REF} = 0A	0.882	0.9	0.918	V
VOS_{VTT}	Output Offset from V_{REF}		-30		30	mV
Z_{REF}	V_{REF} Output Impedance	I_{REF} = -5µA to 5µA		5		kΩ
Z_{VDDQ}	V_{DDQ} Input Impedance			100		kΩ
I_{LIM}	V_{TT} Current Limit			2.5		A
V_{SD}	Shutdown Logic Logic "1" Level Logic "0" Level		 1.5		 0.4	 V V
$T_{DISABLE}$ T_{HYST}	Shutdown Temperature Thermal Hysteresis			150 30		°C °C

Note 1: Operating characteristics are over Standard Operating Conditions unless otherwise specified.

Performance Information

Typical DC Characteristics (nominal conditions unless otherwise specified)

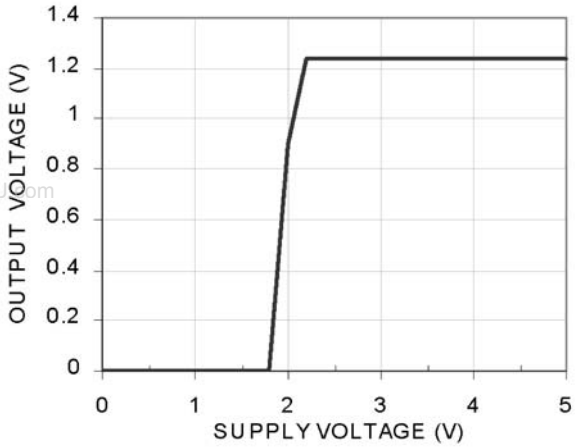


Figure 1. Output Voltage with Supply (V_{DDQ} = 2.5V)

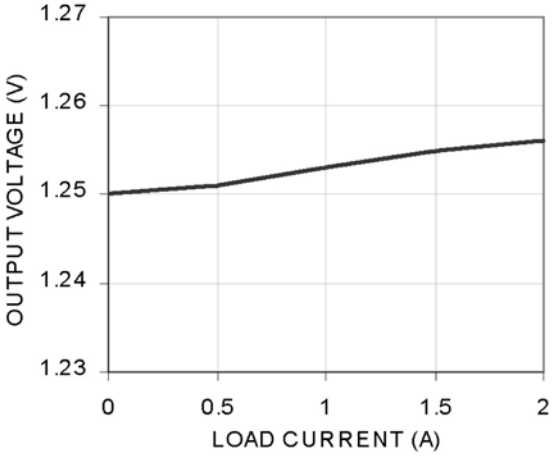


Figure 3. Load Regulation (Sink)

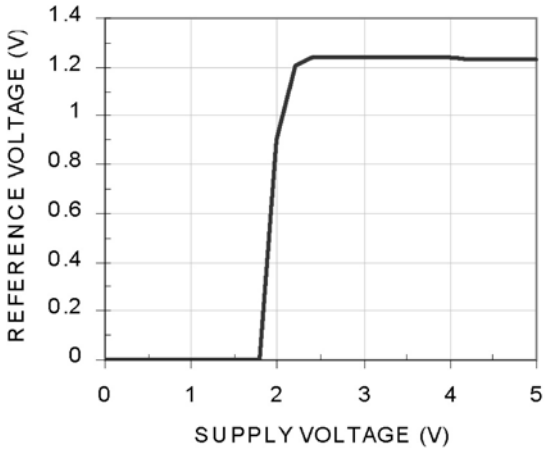


Figure 2. Reference Voltage with Supply (V_{DDQ} = 2.5V)

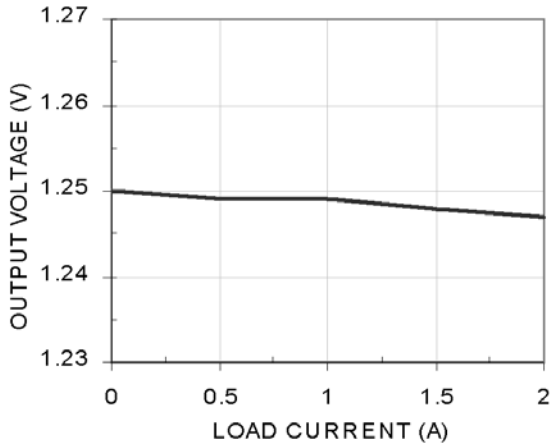


Figure 4. Load Regulation (Source)

Performance Information (cont'd)

Typical DC Characteristics (nominal conditions unless otherwise specified)

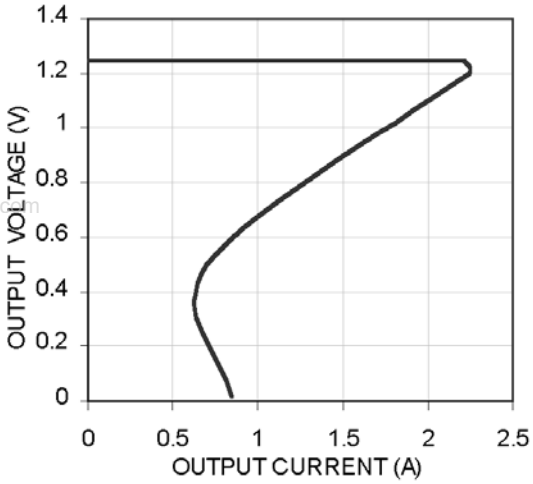


Figure 5. Over Current Limit (Sink)

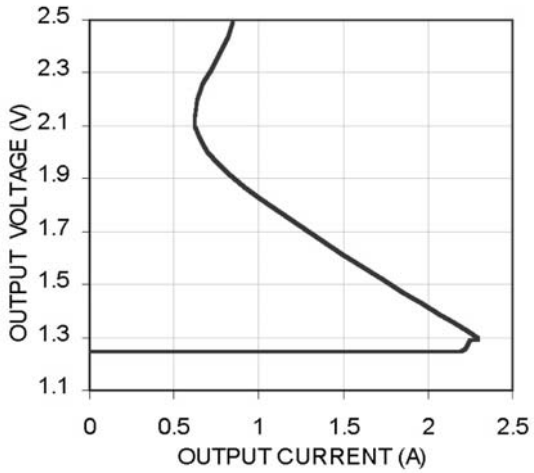


Figure 7. Over Current Limit (Source)

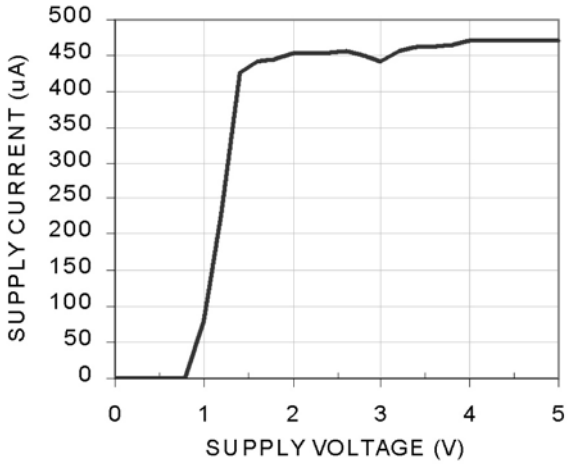


Figure 6. Supply Current with Supply Voltage

Performance Information (cont'd)

Typical Transient Characteristics (nominal conditions unless otherwise specified)

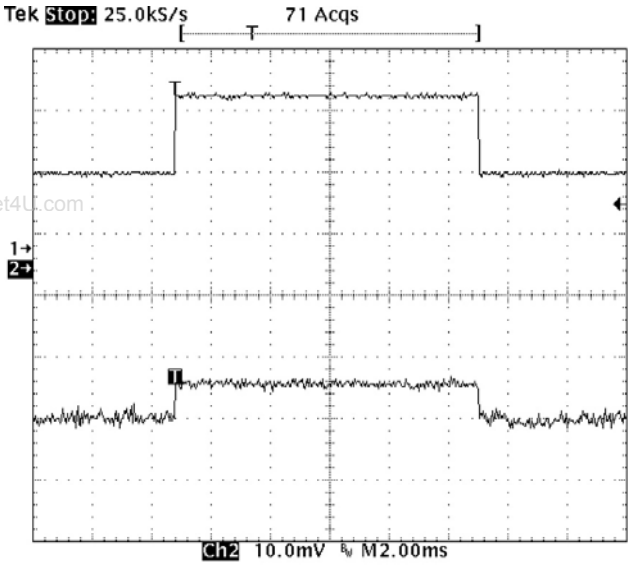


Figure 8. Load Transient (0A to 2.0A Sink)

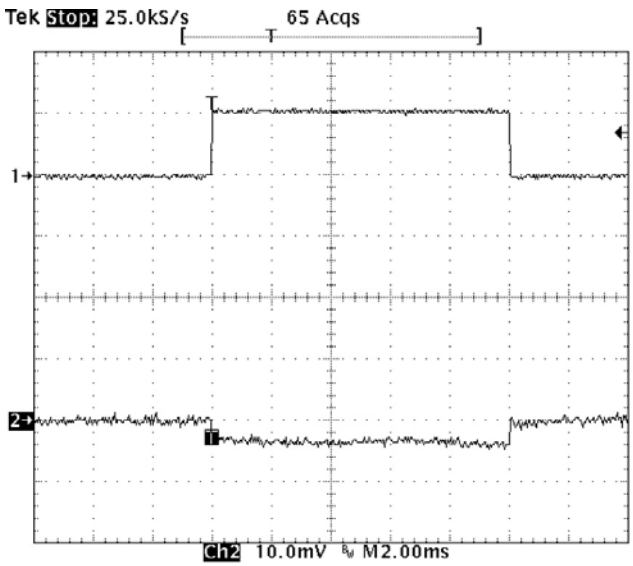


Figure 9. Line Transient (0A to 2.0A Source)

Performance Information (cont'd)

Typical Thermal Characteristics

The overall junction to ambient thermal resistance (θ_{JA}) for device power dissipation (P_D) consists primarily of two paths in series. The first path is junction to case (θ_{JC}) which is defined by the package style, and the second path is case to ambient (θ_{CA}) thermal resistance which is dependent on board layout. The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$T_{JUNC} = T_A + P_D (\theta_{JC}) + P_D (\theta_{CA})$$

$$= T_A + P_D (\theta_{JA})$$

When a CM3196-12SN (SOIC) is mounted on a double-sided printed circuit board with two square inches of copper allocated for "heat spreading," the resulting θ_{JA} is 151°C/W. Based on the over temperature limit of 150°C with an ambient of 85°C, the available power of this package will be:

$$P_D = (150°C - 85°C) / 151°C/W = 0.43W$$

For the CM3196-12SB (PSOP), θ_{JA} is 40°C/W and the available power for this package will be:

$$P_D = (150°C - 85°C) / 40°C/W = 1.625W$$

DDR Memory Application

Since the output voltage is 1.25V, and the device can either source current from V_{DD} or sink current to Ground, the power dissipated in the device at any time is 1.25V times the current load. This means the maximum average RMS current (in either direction) is 0.344A for CM3196-12SN and 1.3A for CM3196-12SB. The maximum instantaneous current is specified at 2A, so this condition should not be exceeded 17% and 65% of the time for CM3196-12SN and CM3196-12SB, respectively. It is highly unlikely in the use of DDR memory that this would occur, because it means the DDR memory outputs are either all high or all low for 17% (SOIC) and 65% (PSOP) of the time.

If the ambient temperature is 40°C instead of 85°C, which is typically the maximum in most DDR memory applications, the power dissipated (P_D) can be 0.73W for CM3196-12SN and 2.75W for CM3196-12SB. So the maximum average RMS current increases from 0.42A to 0.58A for CM3196-12SN and maximum instantaneous current of 2A should not be exceeded 29% of the time. For CM3196-12SB, the maximum RMS current increases from 1.3A to 2.2A. Thus, the maximum continuous current can be 2A all the time.

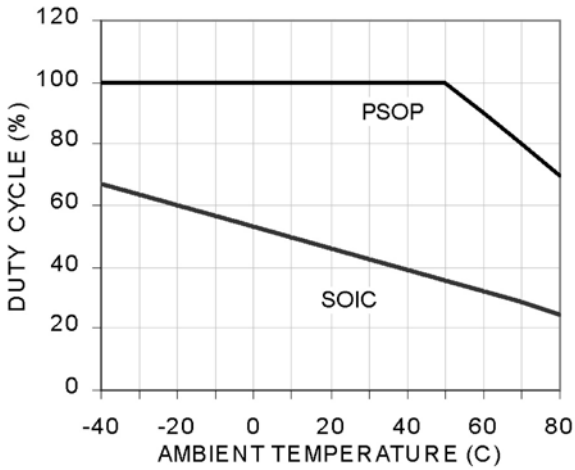


Figure 10. Duty Cycle vs. Ambient Temperature (I_{LOAD} = 2A)

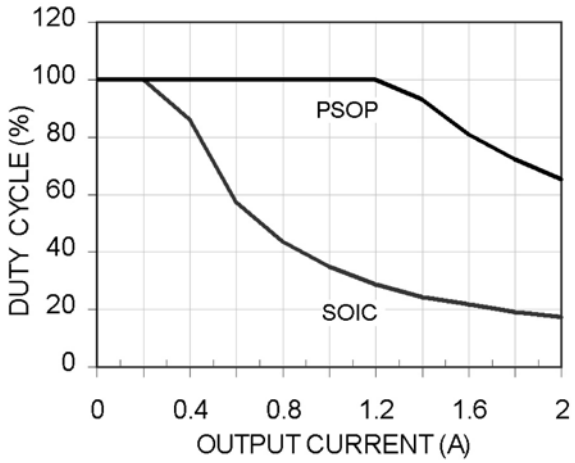


Figure 11. Duty Cycle vs. Output Current (Temp=70°C)

Performance Information (cont'd)

Typical Thermal Characteristics (cont'd)

The theoretical calculations of these relationships show the safe operating area of the CM3196 in the SOIC package.

Thermal characteristics were measured using a double-sided board with two square inches of copper area connected to the GND pins for "heat spreading."

Measurements showing performance up to a junction temperature of 150°C were performed under light load conditions (5mA). This allows the ambient temperature to be representative of the internal junction temperature.

Note: The use of multi-layer board construction with separate ground and power planes will further enhance the overall thermal performance.

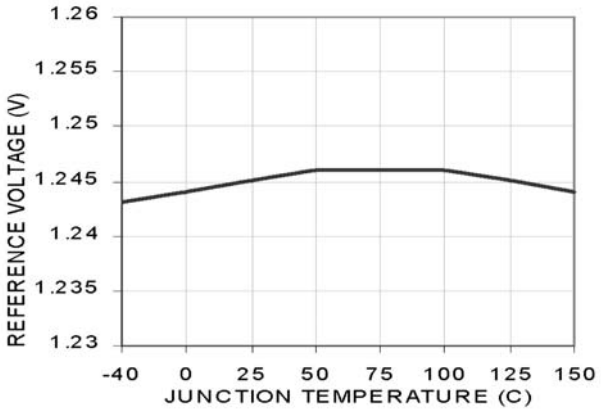


Figure 12. Reference Voltage vs. Temperature

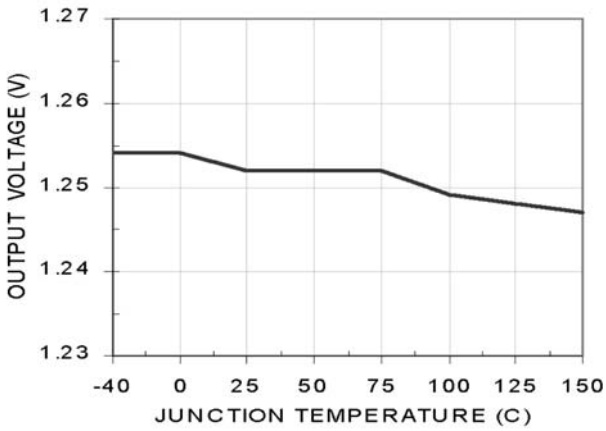


Figure 13. Output Voltage vs. Ambient Temperature (I_{LOAD}=5mA)

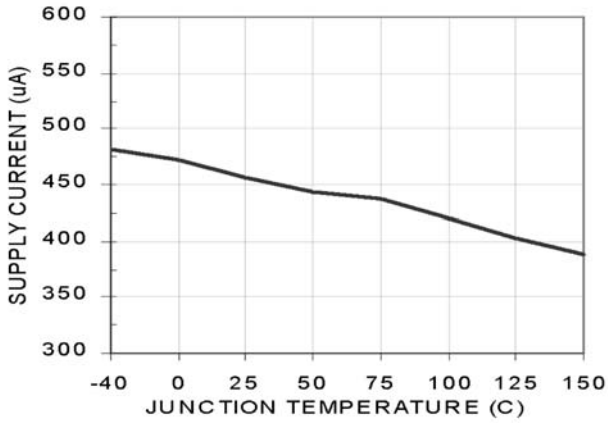


Figure 14. Quiescent Current vs. Temperature

Application Information

PCB Layout Considerations

The CM3196-12SB has a heat spreader attached to the underneath of the PSOP-8 package in order for heat to be transferred easily from the package to the PCB. The heat spreader is a copper pad of dimensions just smaller than the package itself. By positioning the matching pad on the PCB top layer to connect to the spreader during manufacturing, the heat will be transferred between the two pads. The drawing below shows the recommended PCB layout. Note that there are six vias on either side to allow the heat to dissipate into the ground and power planes on the inner layers of the PCB. Vias can be placed underneath the chip, but this can cause blockage of the solder. The ground and power planes should be at least 2 sq. in. of copper adjacent to the vias. It also helps if the chip is positioned away from the edge of the PCB, and not near other heat dissipating devices. A good thermal link from the PCB pad to the rest of the PCB will properly couple the CM3196 package to maintain an ambient junction temperature ($\theta_{JA)}$ of around 40°C/W.

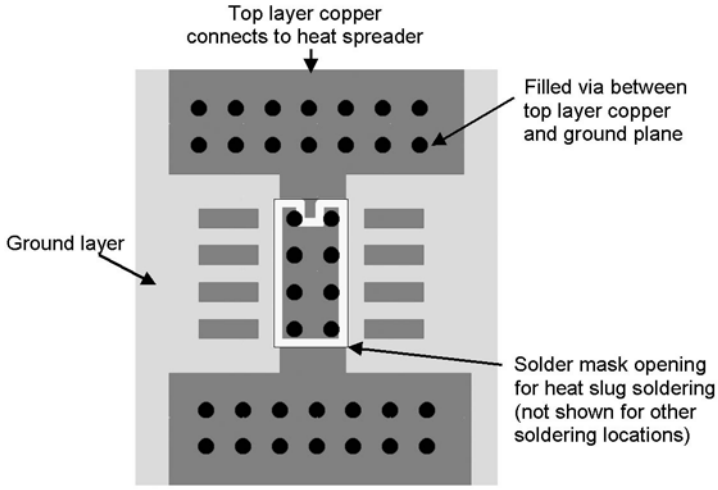


Figure 15. Recommended Heat Sink PCB Layout

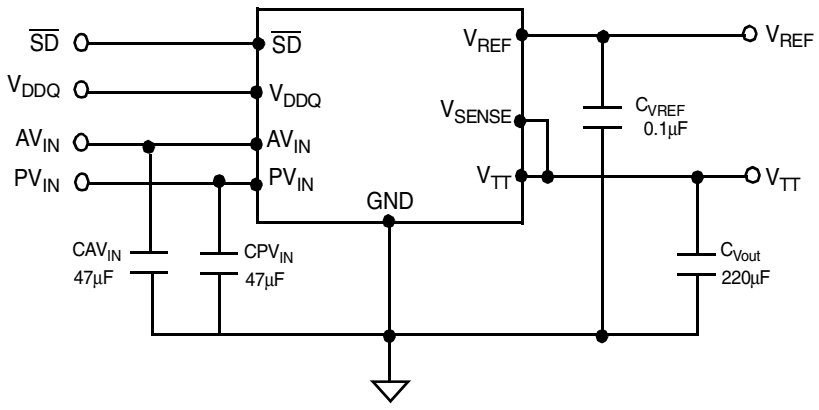


Figure 16. Typical Application Circuit

Mechanical Details

The CM3196 is available in an 8-lead SOIC and PSOP package.

SOIC-8 Mechanical Specifications

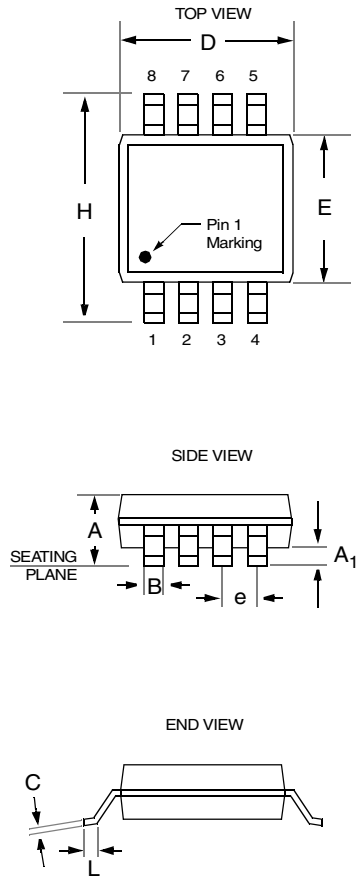
Dimensions for CM3196 devices packaged in 8-pin SOIC packages are presented below.

For complete information on the SOIC-8 package, see the California Micro Devices SOIC Package Information document.

PACKAGE DIMENSIONS				
Package	SOIC			
Leads	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.19	0.150	0.165
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
# per tube	100 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: inches				

* This is an approximate number which may vary.

Mechanical Package Diagrams



Package Dimensions for SOIC-8

Mechanical Details

PSOP-8 Mechanical Specifications

Dimensions for CM3196 devices packaged in 8-pin PSOP packages with an intagrated heatslug are presented below.

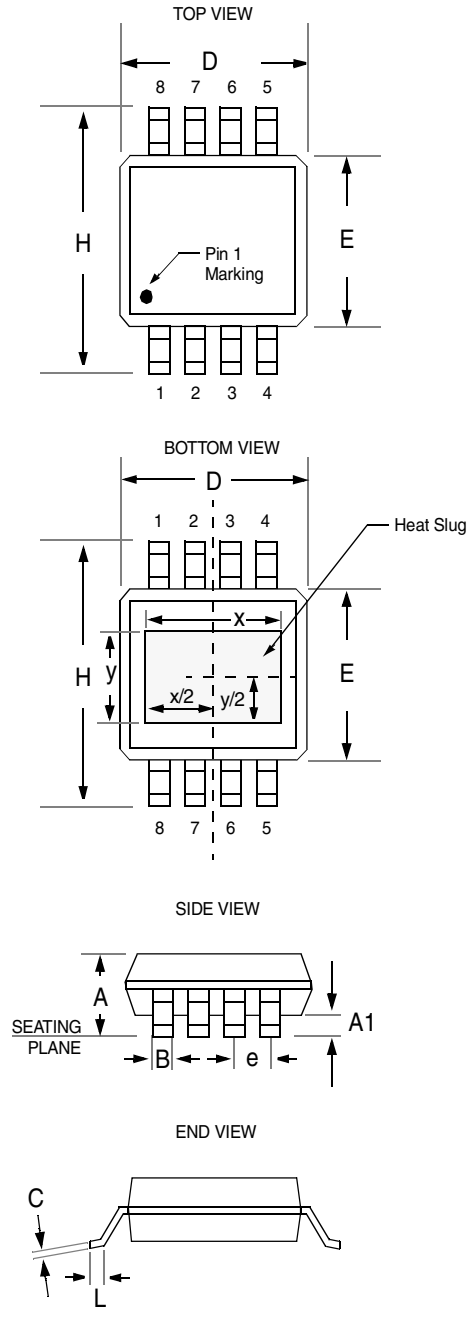
For complete information on the PSOP-8 package, see the California Micro Devices PSOP-8 Package Information document.

PACKAGE DIMENSIONS				
Package	PSOP-8			
Leads	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.30	1.62	0.051	0.064
A_1	0.03	0.10	0.001	0.004
B	0.33	0.51	0.013	0.020
C	0.18	0.25	0.007	0.010
D	4.83	5.00	0.190	0.197
E	3.81	3.99	0.150	0.157
e	1.02	1.52	0.040	0.050
H	5.79	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
x**	3.56	4.06	0.130	0.150
y**	2.29	2.79	0.090	0.110
# per tube	100 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: inches				

* This is an approximate number which may vary.

** Centered on package centerline.

Mechanical Package Diagrams



Package Dimensions for PSOP-8