CM6300

USB Audio Single Chip Specification

DESCRIPTION

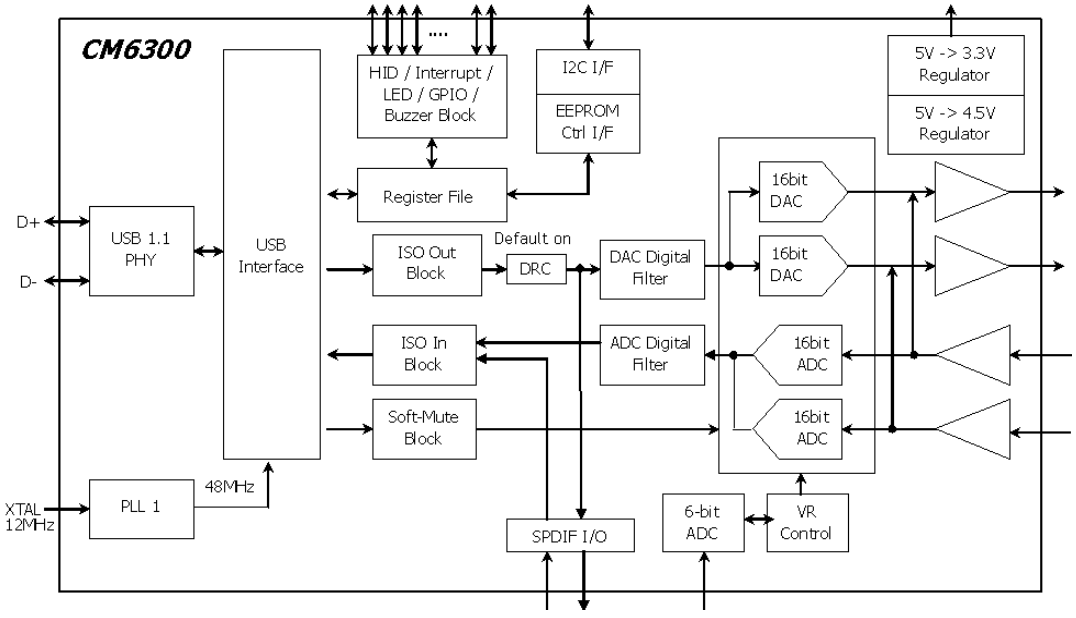
CM6300 is a highly integrated single chip for USB stereo speakers and headphone set application. With less external components, it can be used for building an USB speaker or headphone set solution easily. CM6300 needn't any proprietary driver for audio playback or recording and all of audio functions are supported by major OS. As well as CM6300 provides a truly plug-and-play features for external digital audio playback.

CM6300 contains embedded 2ch output with DRC managements. The Dynamic Range Control function can support high efficiency volume output and implement loudness sound effect, which is similar D class amplifier capability. Moreover, CM6300 supports USB standard HID Interface which provide Vol_up / Vol_dn / Play_mute Butoms and 3 LED indicator pins: On / Off / Operation / playback mute / recording mute / and controllable flash time (with PWM Functions)

FEATURES

- USB spec. 2.0 Full speed compatible and USB IF certification
- USB audio device class spec. 1.0 and USB HID class spec. 1.1 compliant
- Supporting control, interruption and isochroous data transfers
- Supporting USB suspend/resume and remote wake-up features
- Embedded USB transceiver and power-on reset circuit USB remote wake-up support
- Single 12MHz Crystal Input with On-chip PLL
- Supporting High-power (500mA) and Low-power (100mA) mode options
- Supporting series number string (16 Bytes) for operation system detection
- Serial EEPROM programming interface supports customized VID/PID/Product string/ Manufacture string
- Green Parts(Pb-free and Halogen-free) with RoHS Compliant

BLOCK DIAGRAM



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1 Description and Overview

CM6300 is a highly integrated single chip for USB stereo speakers and headphone set application. With less external components, it can be used for building an USB speaker or headphone set solution easily. CM6300 needn't any proprietary driver for audio playback or recording and all of audio functions are supported by major OS. As well as CM6300 provides a truly plug-and-play features for external digital audio playback. CM6300 contains embedded 2ch output with DRC managements. The Dynamic Range Control function can support high efficiency volume output and implement loudness sound effect, which is similar D class amplifier capability. Moreover, CM6300 supports USB standard HID Interface which provide Vol_up / Vol_dn / Play_mute Butoms and 3 LED indicator pins: On / Off / Operation / playback mute / recording mute / and controllable flash time (with PWM Functions)

Furthermore, the manufacturer string, product string, serial number, product ID, vendor ID, and initial playback and recording volumes can all be customized by an external EEPROM. More flexible and customized design is doable with GPIO pins, which are designed by different USB vendor's requests.

[Suggested Applications]:

(a) USB 2CH I/O Speaker

(b) USB 2CH I/O Headphone Set

(c) USB 2CH I/O Adaptor

(d) USB 2CH Audio Box

(e) USB HUB with Audio Solutions (extra HUB controller IC is necessary)

(f) USB FM Audio System (extra FM tuner IC is necessary)

2 Features

- USB spec. 2.0 Full speed compatible and USB IF certification
- USB audio device class spec. 1.0 and USB HID class spec. 1.1 compliant
- Supporting control, interruption and isochroous data transfers
- Supporting USB suspend/resume and remote wake-up features
- Embedded USB transceiver and power-on reset circuit
- Single 12MHz Crystal Input with On-chip PLL
- Supporting High-power (500mA) and Low-power (100mA) mode options
- Supporting series number string (16 Bytes) for operation system detection
- Serial EEPROM programming interface supports customized VID/PID/Product string/ Manufacture string for device name changed and configuration
- Supporting EEPROM interface 24C02 data format

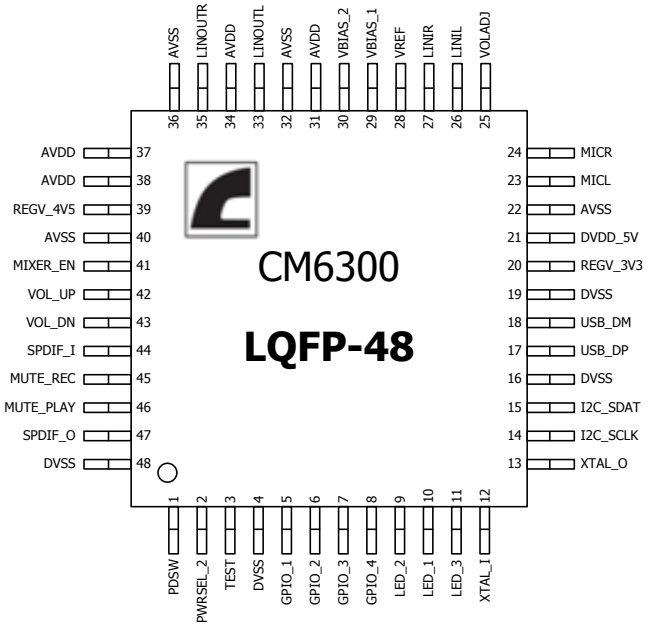
- For Mixer disable mode, USB Audio Function Topology has 2 input Terminals, 2 Output Terminals, one Mixer Unit, one Selector Unit and 2 Feature Units.
- 2 CH DAC output
  DAC sampling rate from 8KHz, 16KHz, 44.1KHz to 48KHz with 16-bit resolution
  Dynamic Range 95dB, THD+N -85dB ~ -91dB (Vista Premium certification)
  Earphone buffer driving for output
  1.2 Vrms biased at 2.25V output swing
- 2 CH ADC Input
  ADC sampling rate from 8KHz, 16KHz, 44.1KHz to 48KHz with 16-bit resolution
  Dynamic Range 88db, THD+N -79dB ~ -84dB
  Digital Linear Microphone Gain Control function (-6dB~33dB)
  1.0 Vrms biased at 2.25V input swing Supported Stereo Mixer function
- Playback with soft-mute function
- Microsoft HID Volume control with Vol_Up, Vol_Dn, Playback_Mute and Record_Mute
- Support I2C control interface for external controller controls
- MCU read/write supports 8 bytes data transfer bandwidth
- I2C interface support master / slave mode and with extra Interrupt Output pin
- Supporting one Control Endpoint, one Isochronous out Endpoint, one Isochronous in Endpoint, and one Interrupt in Endpoint
- Supporting 3 LED indicator pins:
  1. On / Off / Operation
  2. Playback mute
  3. Recording mute
- Supporting 4 GPIO pins
- Isochronous transfer uses Adaptive Mode with Internal PLL for Synchronization
- Embedded Power-On-Reset Block
- Single 5V power supply with embedded 5V to 3.3V regulator
- Industry standard LQFP-48 Pin package
- Compatible with Win2000 / WinXP / Vista without additional driver
- Supporting 2CH mode for MAC OS
- Supporting Linux Red Hat and Fedora with plug in play
- Green Parts(Pb-free and Halogen-free) with RoHS Compliant
- Supported Software
  1. Support Hardware SDK tool for third-party software

3 Pin Descriptions

3.1 Pin Assignment by Pin Number

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	PDSW	13	XTAL_O	25	VOLADJ	37	AVDD
2	PWRSEL_2	14	I2C_SCLK	26	LINIL	38	AVDD
3	TEST	15	I2C_SDAT	27	LINR	39	REGV_4V5
4	DVSS	16	DVSS	28	VREF	40	AVSS
5	GPIO_1	17	USB_DP	29	VBIAS_1	41	MIXER_EN
6	GPIO_2	18	USB_DM	30	VBIAS_2	42	VOL_UP
7	GPIO_3	19	DVSS	31	AVDD	43	VOL_DN
8	GPIO_4	20	REGV_3V3	32	AVSS	44	SPDIF_I
9	LED_2	21	DVDD_5V	33	LNOUTL	45	MUTE_REC
10	LED_1	22	AVSS	34	AVDD	46	MUTE_PLAY
11	LED_3	23	MICL	35	LNOUTR	47	※ SPDIF_O
12	XTAL_I	24	MICR	36	AVSS	48	DVSS

3.2 Pin-Out Diagram



※ S/PDIF out will not be implemented in default status. Unless with specific C-Media driver.

3.3 Pin Signal Descriptions

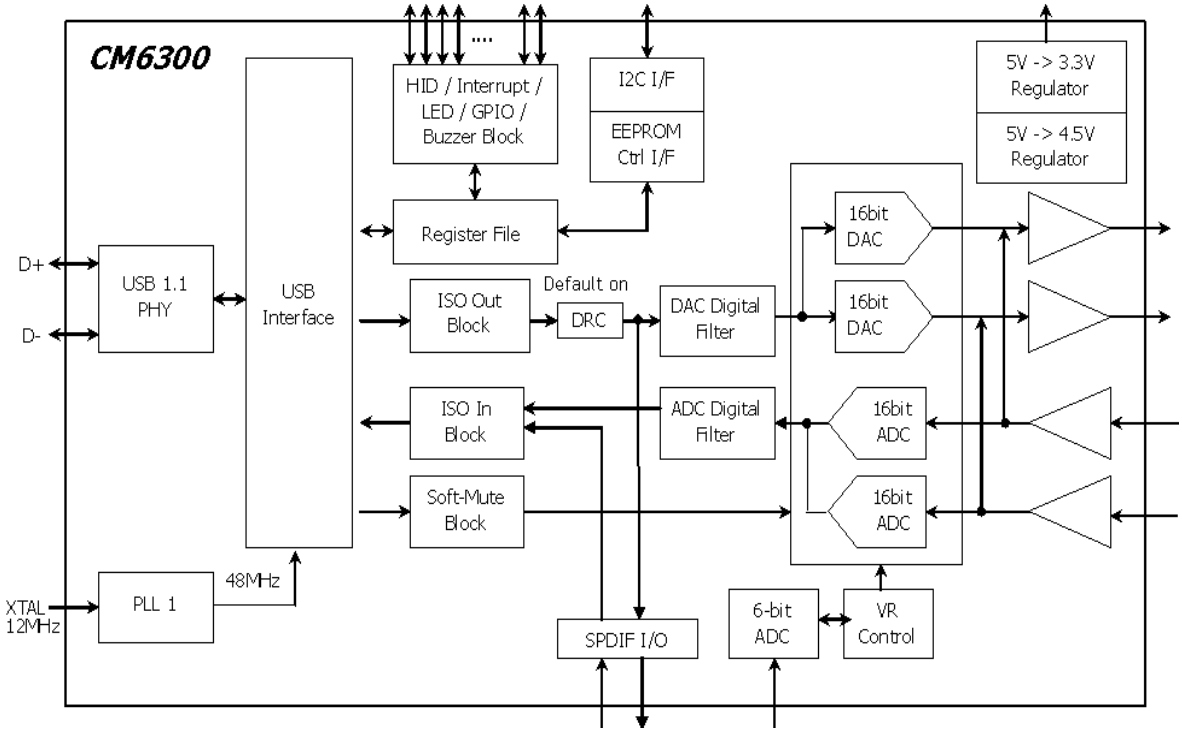
No.	Symbol	Type	Description
1	PDSW	OD, 5V	Power Down Switch Output (0:Normal Operation; 1:Suspend)
2	PWRSEL_2	DIO, PU	Power Consumption Selector (0:500mA; 1:100mA)
3	TEST	DI, PD	Test Mode Select (0:Normal Mode; 1:Test Mode)
4	DVSS	P	Digital Ground
5	GPIO_1	DIO	General Purpose I/O Pin
6	GPIO_2	DIO	General Purpose I/O Pin
7	GPIO_3	DIO	General Purpose I/O Pin
8	GPIO_4	DIO	General Purpose I/O Pin
9	LED_2	DO	LED (Mute Play)
10	LED_1	DO	LED (Play or Record)
11	LED_3	DO	LED (Mute Record)
12	XTAL_I	DI	Input Pin for 12MHz Oscillator
13	XTAL_O	DO	Output Pin for 12MHz Oscillator
14	I2C_SCLK	OD, DIO	I2C Serial Clock / EEPROM 24c02 Serial Clock
15	I2C_SDAT	OD, DIO	I2C Serial Data / EEPROM 24c02 Serial Data
16	DVSS	P	Digital Ground
17	USB_DP	AIO	USB D+
18	USB_DM	AIO	USB D-
19	DVSS	P	Digital Ground
20	REGV_3V3	AO	5V->3.3V Regulator Output
21	DVDD_5V	P	5V Power Supply to Internal Regulator
22	AVSS	P	Analog Ground
23	MICL	AI	MIC0 in left channel
24	MICR	AI	MIC0 in right channel
25	VOLADJ	AI	Analog Volume Adjustment, 0V ~ 2.25V: 0 dB ~ -46.5 dB (-1.5dB/step) > 3.5V: -3 dB
26	LINIL	AI	Line in left channel

27	LINIR	AI	Line in right channel
28	VREF	AO	2.25V reference Voltage output
29	VBIAS_1	AO	MIC bias Voltage
30	VBIAS_2	AO	MIC bias Voltage
31	AVDD	P	5V Analog Power for Analog Circuit
32	AVSS	P	Analog Ground
33	LNOUTL	AO	Differential Line out for left channel
34	AVDD	P	5V Analog Power for Analog Circuit
35	LINOUTR	AO	Differential Line out for right channel
36	AVSS	P	Analog Ground
37	AVDD	P	5V Analog Power for Analog Circuit
38	AVDD	P	5V Analog Power for Analog Circuit
39	REGV_4V5	AO	4.5V Regulator Output
40	AVSS	P	Analog Ground
41	MIXER_EN	DI, PU	Mixer AA-Path enable (0:Disable; 1:Enable)
42	VOL_UP	DI, PU	HID Volume Up
43	VOL_DN	DI, PU	HID Volume Down
44	SPDIF_I	DI	SPDIF IN
45	MUTE_REC	DI, PU	HID MIC Recording Mute
46	MUTE_PLAY	DI, PU	HID Master Volume Playback Mute
47	SPDIF_O	DI	SPDIF Output (Need C-Media specific driver)
48	DVSS	P	Digital Ground

***Notes:**

DI	**-> Digital Input**	**DO**	**-> Digital Output**	**DIO**	**-> Digital I/O**
AI	**-> Analog Input**	**AO**	**-> Analog Output**	**AIO**	**-> Analog I/O**
OD	**-> Open Drain**	**PU**	**-> Internal Pull Up**	**PD**	**-> Internal Pull Down**
5V	**-> 5V Torrent**	**P**	**-> Power**		

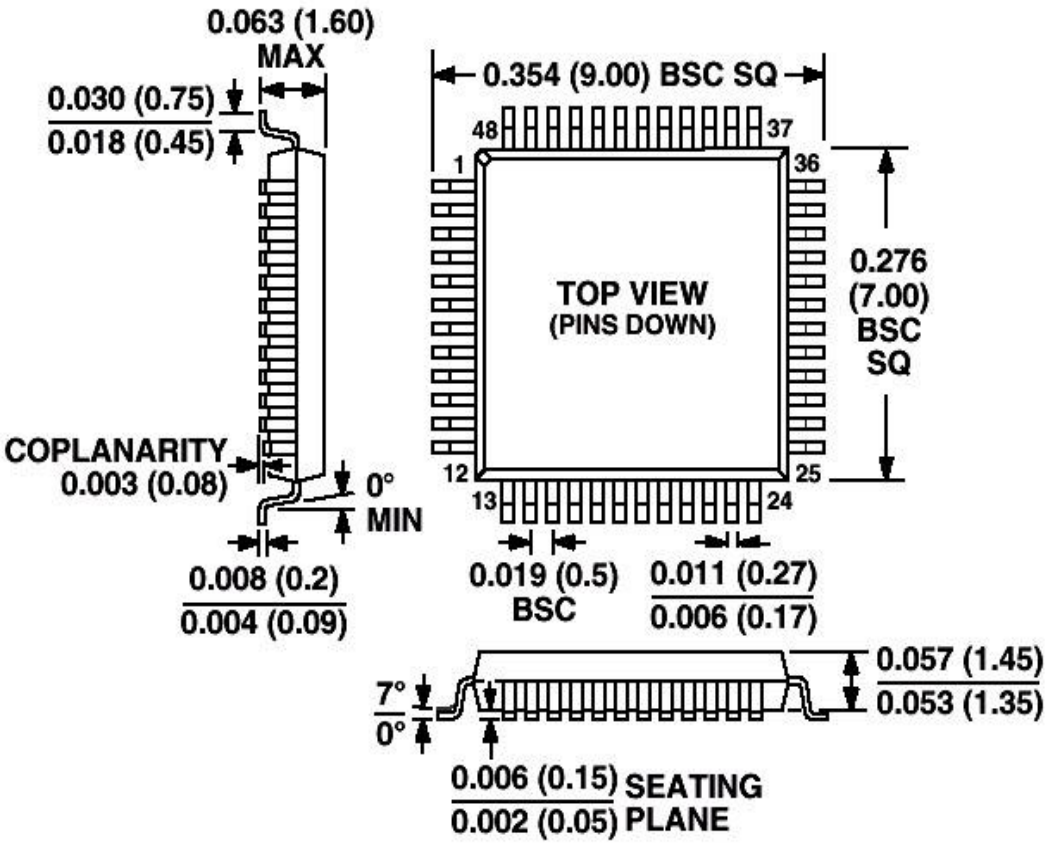
4 Block Diagram



5 Ordering Information

Model Number	Package	Operating Ambient Temperature	Supply Range
CM6300	48-Pin LQFP 7mm×7mm×1.4mm (Plastic)	0°C to +70°C	DVdd = 5V, AVdd = 5V

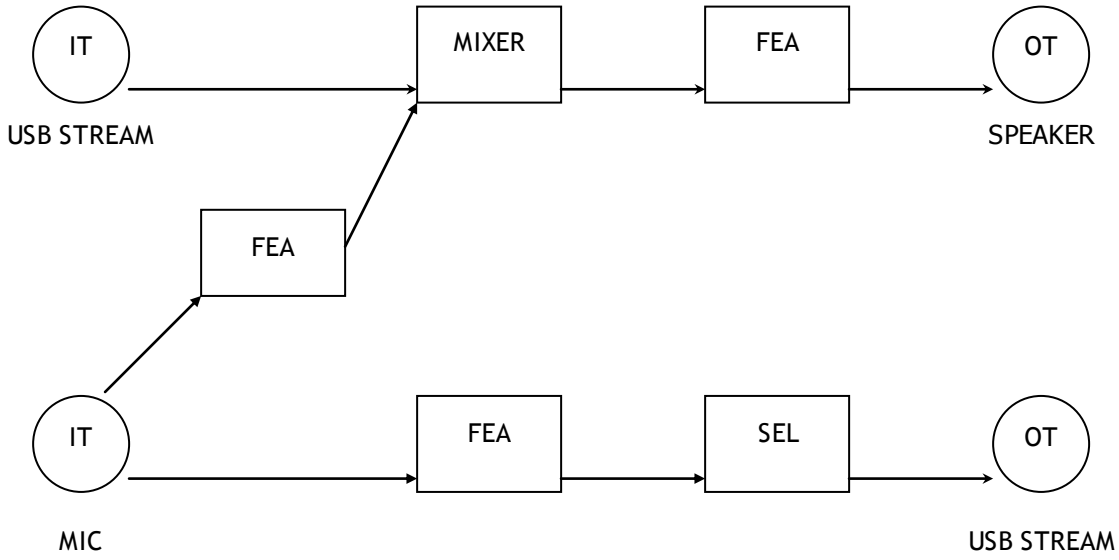
48-Lead Thin Plastic Quad Flatpack (LQFP)



Outline Dimensions *Dimensions shown in inches and (mm)

6 USB Audio Topology and Descriptors

6.1 USB Audio Topology



6.2 Device Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	12	Descriptor length
1	bDescriptorType	1	01	Device Descriptor
2	bcdUSB	2	0110	USB 1.1 compliant
4	bDeviceClass	1	00	Device class specified by interface
5	bDeviceSubClass	1	00	Device subclass specified by interface
6	bDeviceProtocol	1	00	Device protocol specified by interface
7	bMaxPacketSize0	1	40	Endpoint zero packet size
8	idVendor	2	0d8c	Vendor ID
10	idProduct	2	0105	Product ID
12	bcdDevice	2	0100	Device release number
14	iManufacturer	1	03	Index of string descriptor describing manufacturer
15	iProduct	1	01	Index of string descriptor describing product
16	iSerialNumber	1	00 or 02 (*)	Index of string descriptor describing serial number
17	bNumConfigurations	1	01	Number of configuration

Note 1: The numbers of VID & PID are default settings (0d8C/0105), when valid EEPROM is detected, Vendor ID and Product ID will be replaced by the content of EEPROM randomly.
Note 2: iSerialNumber will be valid only if external EEPROM contain this info.

6.3 Configuration Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	02	Configuration Descriptor
2	wTotalLength	2	0113	Total length of data returned for this configuration: 274 bytes
4	bNumInterfaces	1	04	Number of interfaces supported by this Configuration: 00: Control 01: ISO-Out 02: ISO-In 03: INT-IN (HID)
5	bConfigurationValue	1	01	Configuration value
6	iConfiguration	1	00	Index of string descriptor describing this configuration
7	bmAttributes	1	a0 or 80 or e0 or c0	Bus Power and support Remote Wakeup: 8'ha0 (PWRSEL_1 = 1, HID_EN = 1) Bus Power and no Remote Wakeup: 8'h80 (PWRSEL_1 = 1, HID_EN = 0) Self Power and support Remote Wakeup: 8'he0 (PWRSEL_1 = 0, HID_EN = 1)) Self Power and no Remote Wakeup: 8'hc0 (PWRSEL_1 = 0, HID_EN = 0))
8	bMaxPower	1	32 or fa	Maximum power consumption from bus = 100mA: 8'h32 (50x2 mA) (PWRSEL_2 = 1) Maximum power consumption from bus = 500mA: 8'hfa (250x2 mA) (PWRSEL_2 = 0)

6.4 Standard HID Interface Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	04	Interface Descriptor
2	bInterfaceNumber	1	03	Interface number: 03
3	bAlternateSetting	1	00	Alternate interface
4	bNumEndpoints	1	01	Number of endpoint used by this interface
5	bInterfaceClass	1	03	HID Interface Class
6	bInterfaceSubClass	1	00	Subclass code
7	bInterfaceProtocol	1	00	Protocol code
8	iInterface	1	00	Index of string descriptor describing this interface

Class-specific HID Interface Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	21	HID descriptor type
2	bcdHID	2	0100	HID class version
4	bCountryCode	1	00	No country code
5	bNumDescriptors	1	01	One HID class descriptor
6	bDescriptorType	1	22	Report Descriptor
7	wDescriptorLength	2	0032 / 001a	HID class descriptor length in byte: 50 / 26 bytes (Enable / Disable HID Button)

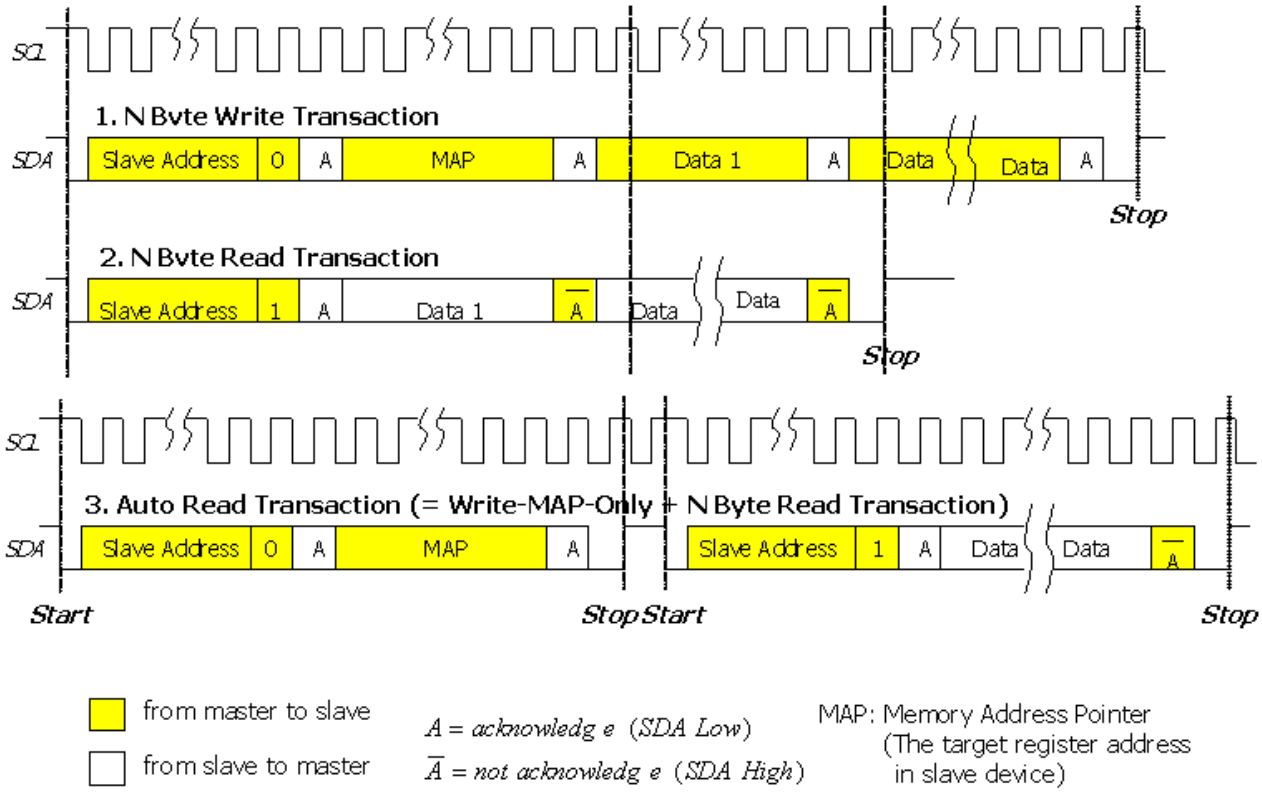
Standard HID Interrupt In Endpoint Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	07	Descriptor length
1	bDescriptorType	1	05	Endpoint Descriptor
2	bEndpointAddress	1	87	IN Endpoint, Endpoint number: 7
3	bmAttributes	1	03	Interrupt Endpoint
4	wMaxPacketSize	2	0010	Maximum packet size: 16 bytes
6	bInterval	1	01	1ms

7 Function Block Descriptions:

7.1 I Square C(I2C) Interface

7.1.1 Master Mode:



from master to slave

from slave to master

A = *acknowledge* (*SDA Low*)

$\overline{A}$ = *not acknowledge* (*SDA High*)

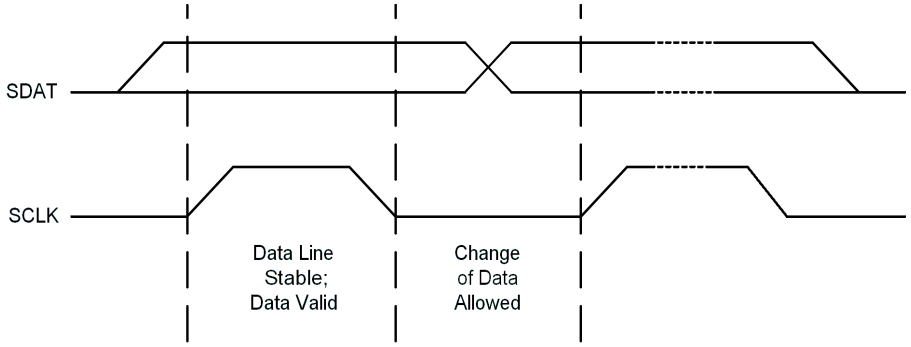
MAP: Memory Address Pointer
(The target register address in slave device)

7.1.2 Slave Mode:

"7-bit slave address = 7'b0111000"

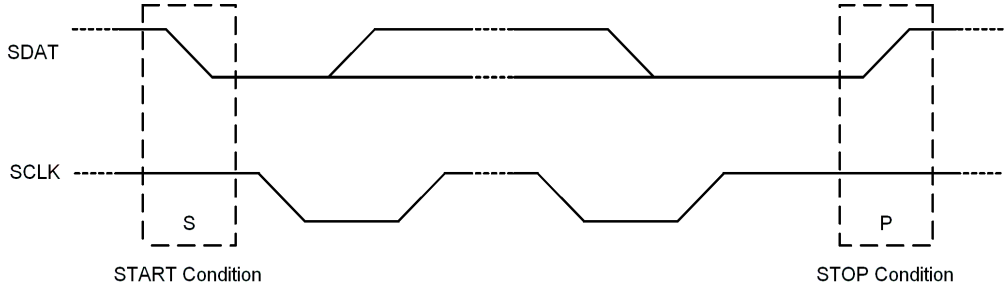
On the MCU serial interface, the CM6300 can serve as a slave device with bit rates up to 400Kbps (in fast mode). The MCU can write data to the CM6300 or read data from the CM6300 (No size limitations when using the I2C Interface). Since the host side and MCU can both access to the internal registers, access contention- when both host and MCU try to access the same register- should be avoided by the application. The 7-bit slave address of the CM6300 is assigned as 7'b0111000. When data is written by the MCU, the CM6300 will NOT transfer any interrupt to the PC until the INT bit of the I2C control Register has been set by the MCU.

The USB host will keep polling the upward HID report every 1ms. When any button is pressed or released, or MCU data is incoming, the CM6300 will transfer 16 bytes of HID report to the USB host. In I2C Slave Mode, the CM6300 has one open-drain input pin 'SCLK' where it receives the serial clock from the MCU, and one open-drain I/O pin 'SDAT' where it sends or receives serial signals to/from the MCU. As shown below, 'SDAT' should be stable when 'SCLK' is high, and can transition only when 'SCLK' is low.



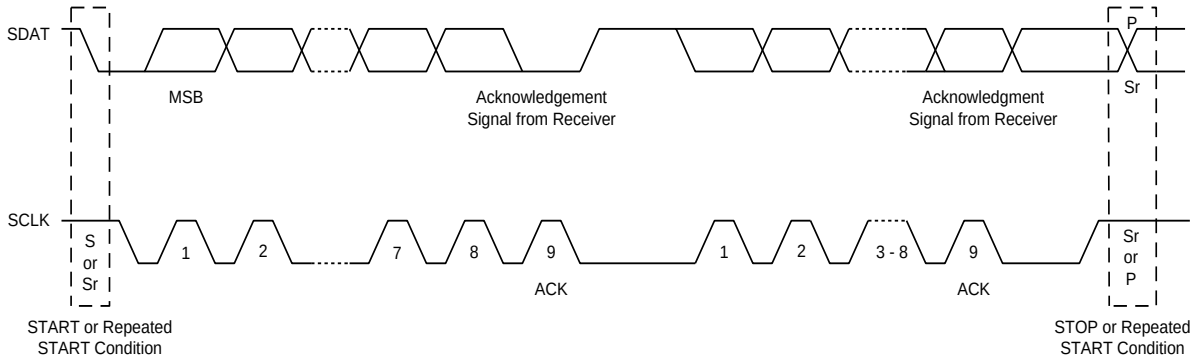
Bit Transfer on the MCU Interface

START and STOP conditions shown below are the exception. Every transaction begins from a START, and ends with a STOP, or another START (repeated START).

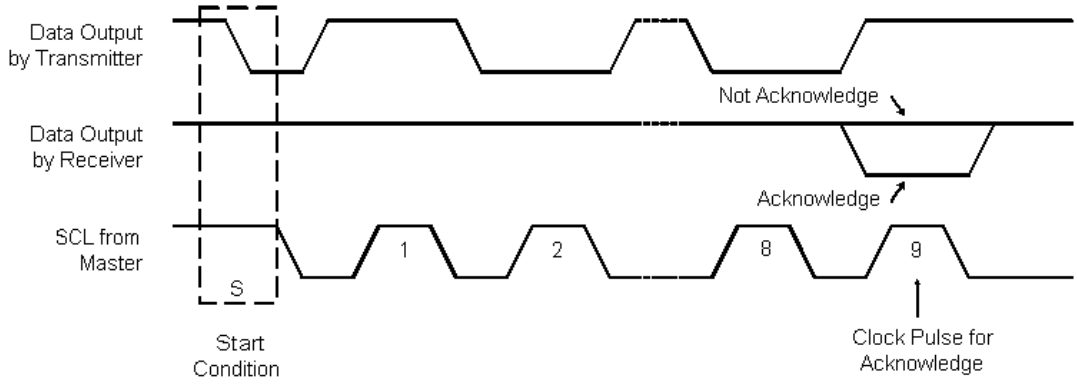


START and STOP Conditions

The figure below demonstrates a typical transaction. After every 8 bits sent by the transmitter, the receiver should send one bit low for positive acknowledgement or one bit high for negative acknowledgement. After the negative acknowledgement, a STOP or repeated START should follow. The next figure shows more details about the acknowledgement bit. Note that 'SCLK' is always driven by the master.

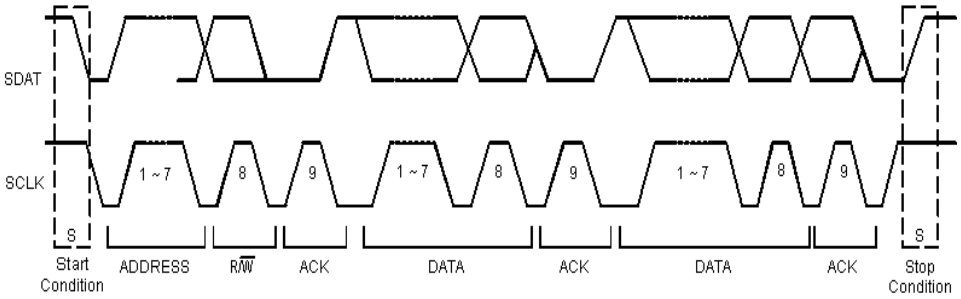


Data Transfer on the MCU Interface



Acknowledge on the MCU Interface

The figure below shows a complete data transfer. After a START, the MCU should send 7-bit slave address (7'b0111000) first, and then the 8th bit denotes a read transfer when it's high; or a write transfer when it's low. The first acknowledgement always comes from the CM6300.



A Complete Data Transfer

In the write transfer, the MCU continues to act as the master and the transfer direction is not changed. The following figure gives an example of a write transfer.

MCU write:

S	0x70	0	addr	0	Byte 0	0	Byte 1	0	....	0	Byte N	0	P

	From CM6300 to MCU		From MCU to CM6300
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte N	One byte data		

0x70 is the slave address of CM6300, and it also tells CM6300 that it's receiving a write command. CM6300 regards the first coming DATA byte as the register address. The second DATA byte is the DATA content that MCU writes at the register address. CM6300 will auto-increment the register address to the next register address for the following writes DATA. The figure below shows an example of read transfer. The MCU read command can not set the register address, so the MCU may use a write command to set the register address first and then start the read command. Because the CM6300 auto-increments the register address, the second DATA byte will be the register data on the next address.

MCU read:

S	0x70	0	addr	0							
S	0x71	0	Byte 0	0	Byte 1	0	…..	0	Byte N	1	P

	From CM6300 to MCU		From MCU to CM6300
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte n	One byte data		

The figure below gives a complete picture of a typical transaction between the MCU and CM6300. After a START, the MCU should send a 7-bit slave address (7'b0111000) first, and then the 8th bit denotes a read transfer when it's high; or a write transfer when it's low.

MCU write:

S	0x70	0	addr	0	Byte 0	0	Byte 1	0	…..	0	Byte N	0	P

MCU read:

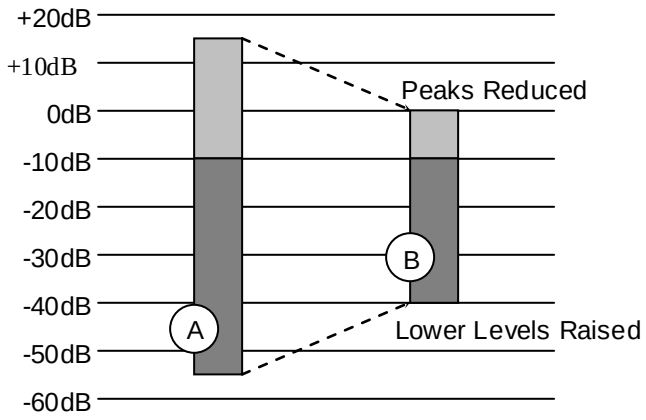
S	0x70	0	addr	0							
S	0x71	0	Byte 0	0	Byte 1	0	…..	0	Byte N	1	P

	From CM6300 to MCU		From MCU to CM6300
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte N	One byte data		

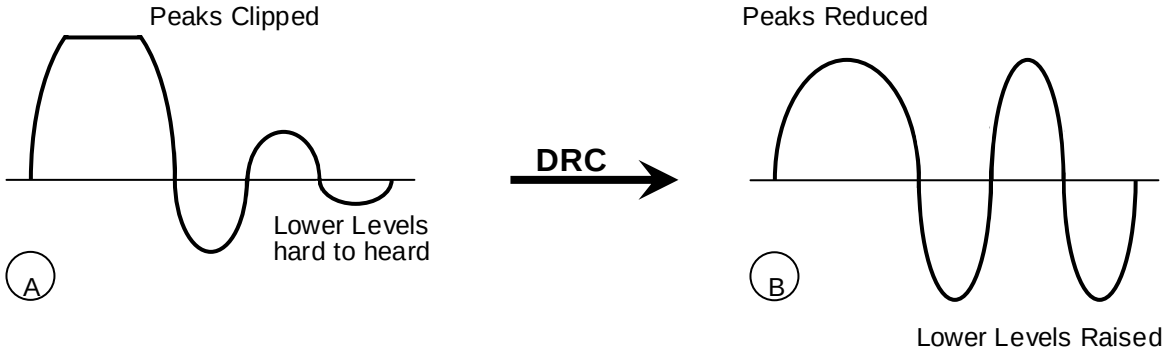
During a write transfer, the MCU continues acting as the transmitter. The CM6300 regards the first DATA byte as the start register address. The following DATA bytes are the content of the registers that the MCU requests. In a read transfer, two transactions are necessary. The MCU resets the start register address by the first transaction, then direction changes to get N of data.

7.2 DRC (Dynamic Range Control)

Dynamic Range is defined as the difference, in decibels (dB), between the loudest and quietest sounds in any particular piece of audio content. Classical music is a good example, with ranges from piano (soft) to forte to FFF (for extremely loud). Movies also typically have a wide dynamic range, which may cause you to have to turn the volume up and down as scenes change. For example, when watching a movie at home, you may be forced to turn up volume to hear the dialog in a quiet scene, and then quickly turn it down again during a car chase scene that follows. In this way, there may be times in a home theater environment when it would be useful to be able to control the dynamic range.



With Dynamic Range Control enabled, the full dynamic range (A) of the program is reduced (B).

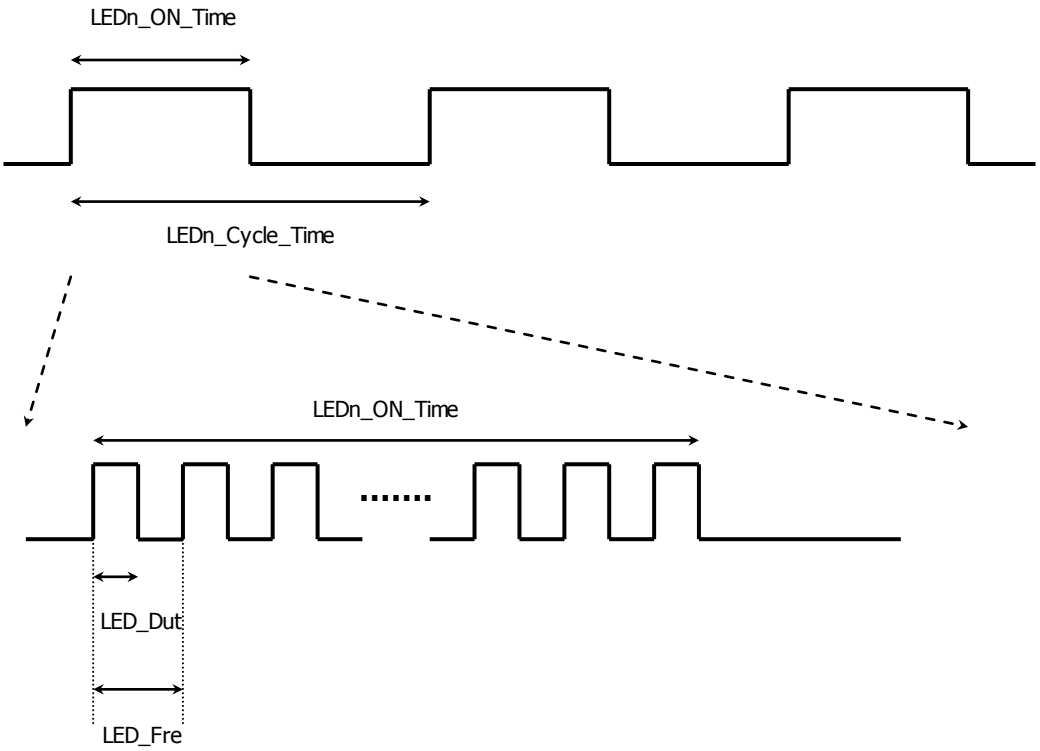


In CM6300, The Maxima Increase Level is +12.5dB.

7.3 LED Behavior and Software Control

LED1 (Config & Play/Rec)	3 times / sec
LED2 (Config & Play Mute)	Always On
LED3 (Config & Rec Mute)	1 time / sec

LED Signal is like a PWM wave form:



*** Notes: 1. Unit for LED_Duty / LED_Freq (Resolution) = 42.67 uS**

2. Unit for LEDn_ON_Time / LEDn_Cycle_Time (Resolution) = 21.85 mS

7.4 EEPROM Content Data Format

24c02 (256 x 8 bit)

[ADDR]	[DATA]
0x00,	Magic Word (“C”, 8’h43)
0x01,	Magic Word (“M”, 8’h4D)
0x02,	Total Data Length in EEPROM
0x03,	EEPROM Content Setting

bit 0:	Manufacture String Valid?	(0: No, 1: Yes)
bit 1:	Product String Valid?	(0: No, 1: Yes)
bit 2:	Serial Number Valid?	(0: No, 1: Yes)
bit 3:	Reserved	(Default 0)
bit 4:	Playback (DAC) Control Valid?	(0: No, 1: Yes)
bit 5:	Recording (ADC) Control Valid?	(0: No, 1: Yes)
bit 6:	Mixer (AA-Path) Control Valid?	(0: No, 1: Yes)
bit 7:	Enable Remote Wakeup?	(0: Disable, 1: Enable)

0x04, VR Volume Control Setting

bit[5:0]:	Constant VR Volume Value (6’h00 ~ 6’h3f, 0 ~ -46.5dB, -1.5dB/step)	
bit 6:	VR Volume Valid?	(0: No, 1: Yes)
bit 7:	Reserved	

0x05, Playback (DAC) Control

bit[5:0]:	DAC (Unit f9) initial Volume (6’h3f ~ 6’h1a, -2.6 ~ -34.5dB/Mute, linear step)	
bit 6:	Mute_f9 (DAC) initial Value	(0: Un-Mute, 1: Mute)
bit 7:	DRC initial Value	(0: Disable, 1: Enable)

0x06, Recording (ADC) Control

bit[4:0]:	ADC (Unit fa / fb) initial Volume (5’h1f ~ 5’h04, +33 ~ -6dB/Mute, -1.5dB/step)	

bit 5:	Reserved	(default set to 1)
bit 6:	Mute_fb (ADC Line) initial Value	(0: Un-Mute, 1: Mute)
bit 7:	Mute_fa (ADC Mic) initial Value	(0: Un-Mute, 1: Mute)

[ADDR] **[DATA]**

0x07, **Mixer (AA-Path) Control**

bit[5:0]:	AA-Path (Unit fd / fe) initial Volume (6'38 ~ 6'h10, +22.5 ~ -36dB/Mute, -1.5dB/step)	
bit 6:	Mute_fe (AA Line) initial Value	(0: Un-Mute, 1: Mute)
bit 7:	Mute_fd (AA Mic) initial Value	(0: Un-Mute, 1: Mute)

0x08, **VID (Low Byte)**

0x09, **VID (High Byte)**

0x0A, **PID (Low Byte)**

0x0B, **PID (High Byte)**

0x0C ~ 0x29 **Manufacture String (30 bytes)**

0x0c	[String1]
0x0d	[String2]
…	…
0x29	[String30]

0x2A ~ 0x65 **Product String (60 bytes)**

0x2A	[String1]
0x2B	[String2]
…	…
0x65	[String60]

0x66 ~ 0x75 **String of Serial Number (16 bytes)**

0x66	[String1]
0x67	[String2]
…	…
0x75	[String16]

0x76 ~ 0xFF **Reserved (Default 8'h00)**

8 Electrical Characteristics:

8.1 Absolute Maximum Rating

Symbol	Parameter	Value	Unit
Dvmin	Min Digital Supply Voltage	- 0.3	V
Dvmax	Max Digital Supply Voltage	+ 6	V
Avmin	Min Analog Supply Voltage	- 0.3	V
Avmax	Max Analog Supply Voltage	+ 6	V
Dvinout	Voltage on any Digital Input or Output Pin	-0.3 to +5.5	V
Avinout	Voltage on any Analog Input or Output Pin	-0.3 to +5.5	V
Tstg	Storage Temperature Range	-40 to +125	^{0}C
ESD (HBM)	ESD Human Body Mode	3500	V
ESD (MM)	ESD Machine Mode	200	V

8.2 Operation Conditions

Operation conditions				
	Min	**Typ**	**Max**	**Unit**
Analog Supply Voltage	4.5	5.0	5.5	V
Digital Supply Voltage	4.5	5.0	5.5	V
Operation Power Consumption, 4 Ohm Loading (*Notes)	-	300	330	mA
Operation Power Consumption, 10K Ohm Loading (*Notes)	-	110	120	mA
Standby Power Consumption	-	85	-	mA
Suspend Mode Power Consumption	-	380	-	uA
Operating ambient temperature	0	-	70	^{0}C

***Notes: Test Environment Under 25oC, 5.0V, 48K Sample Rate,**
Max Output is Playing 1K Full Scale Sin Wave, Typical Output is Playing Music.

8.3 Electrical Parameters

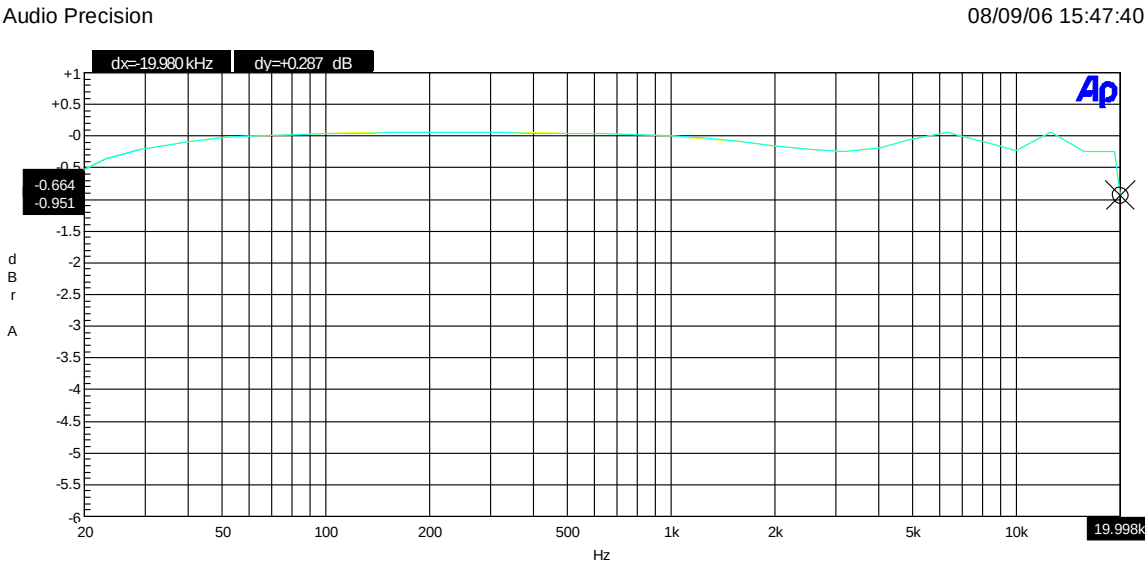
	Min	Typ	Max	Unit
DAC (10K Ohm Loading)				
Resolution	-	16	-	Bits
THD + N (20 ~ 20KHz)	-85	-	-91	dB
Dynamic Range (20 ~ 20KHz)	-	95	-	dB
Cross Talk (20 ~ 20KHz)	-100	-	-112	dB
Frequency Response 48KHz	20	-	20K	Hz
Frequency Response 44.1KHz	20	-	20K	Hz
Output Voltage (rms)	-	1.27	-	Vrms
Inter Channel Phase Delay	0.03	-	0.09	Deg.
ADC				
Resolution	-	16	-	bit
THD + N (20 ~ 20KHz)	-79	-	-84	dB
Dynamic Range (20 ~ 20KHz)	-	88	-	dB
Frequency Response 48KHz	20	-	20K	Hz
Frequency Response 44.1KHz	20	-	20K	Hz
Input Voltage (rms)	-	1	-	Vrms

***Notes: Test Environment Under 25oC, 5.0V, 10KOhm Loading**

9 Frequency Response Graphs

9.1 Digital Playback for Line Output Frequency (10K Ohm Loading)

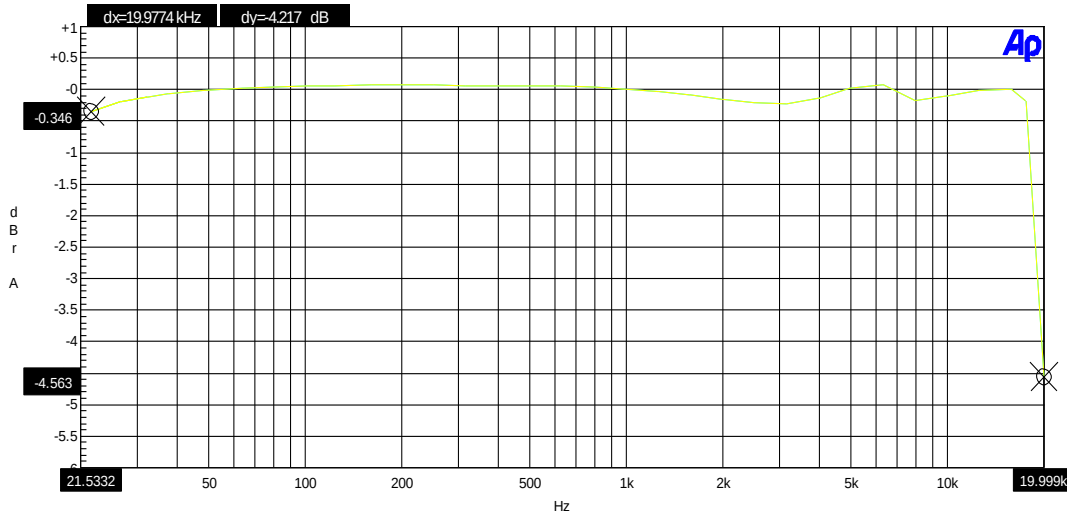
9.1.1 Frequency Response 48Ks/Sec (10K Ohm Loading)



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-0.951 dBr A	*-0.664 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-0.952 dBr A	-0.664 dBr A

Vista-Frequency Response-M48k.at27

9.1.2 Frequency Response 44.1Ks/Sec (10K Ohm Loading)



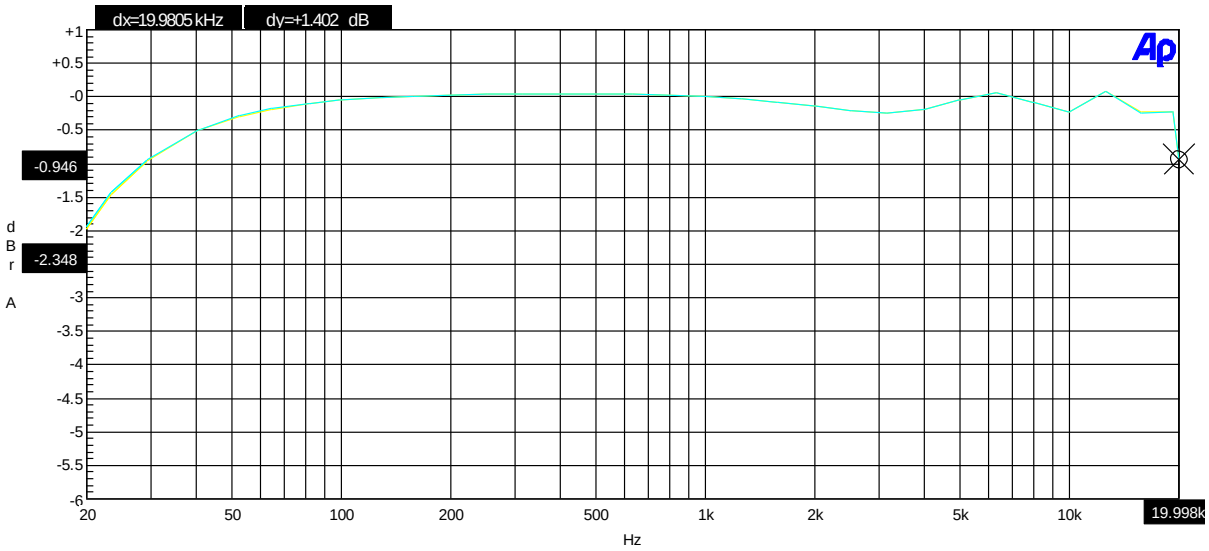
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-0.346 dBr A	*-4.563 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-0.346 dBr A	-4.564 dBr A

Vista-Frequency Response-M44k.at27

9.2 Digital Playback for Line Output Frequency (32 Ohm Loading)

9.2.1 Frequency Response 48Ks/Sec (32 Ohm Loading)

Audio Precision 08/09/06 16:30:39

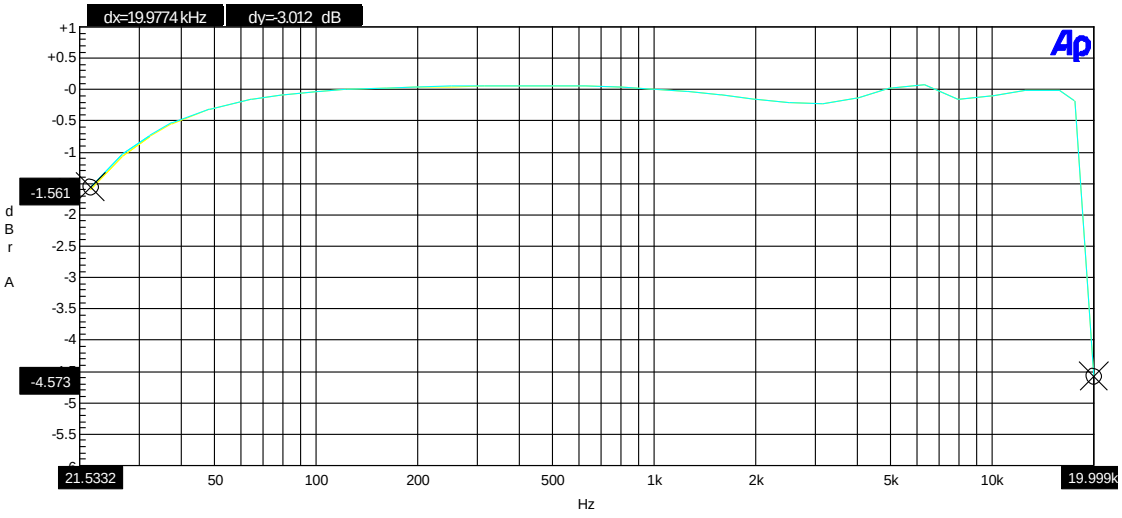


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-2.348 dBr A	*-0.946 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-2.387 dBr A	-0.946 dBr A

Vista-Frequency Response-M48k.at27

9.2.2 Frequency Response 44.1Ks/Sec (32 Ohm Loading)

Audio Precision 08/09/06 16:39:28



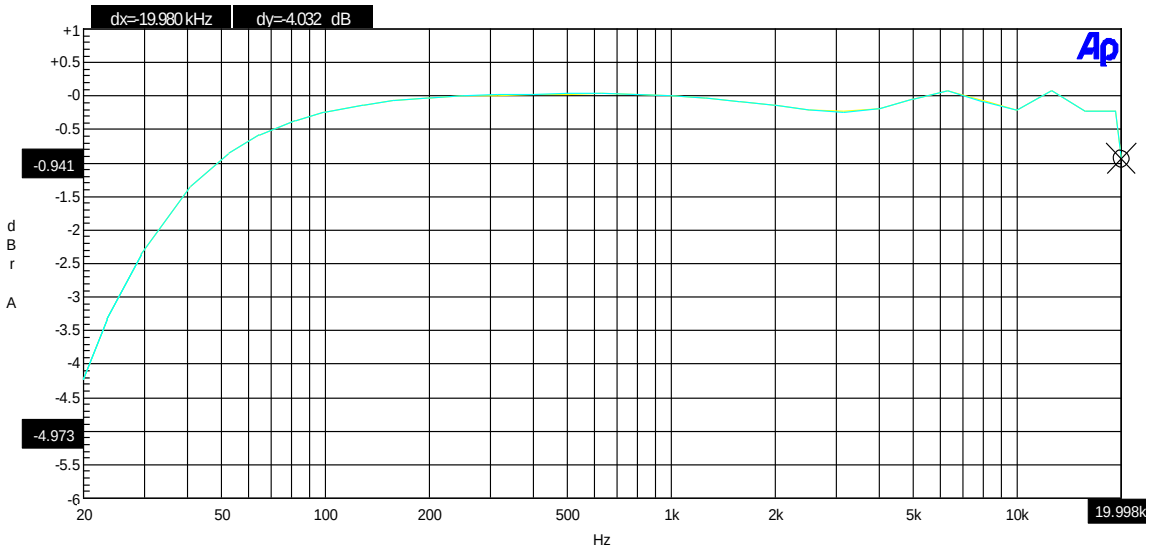
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-1.561 dBr A	*-4.573 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-1.590 dBr A	-4.572 dBr A

Vista-Frequency Response-M44k.at27

9.3 Digital Playback for Line Output Frequency (16 Ohm Loading)

9.3.1 Frequency Response 48Ks/Sec (16 Ohm Loading)

Audio Precision 08/09/06 16:56:01

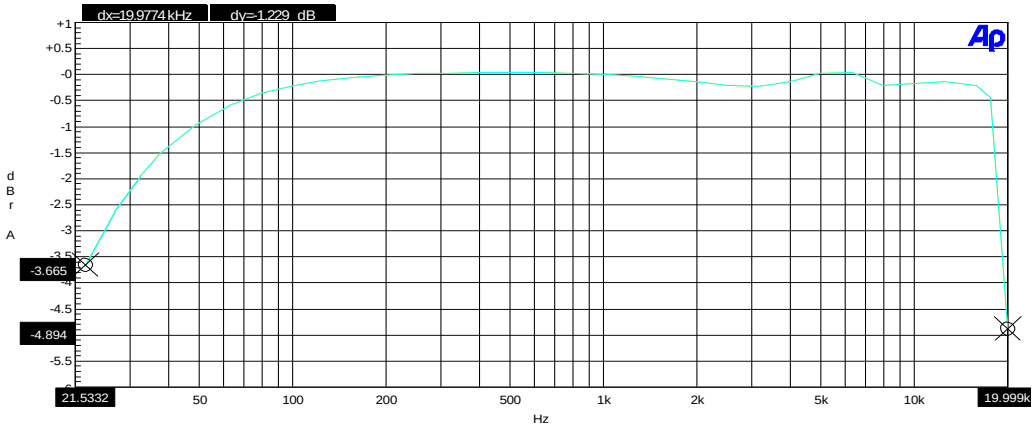


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-0.941 dBr A	*-4.973 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-0.940 dBr A	-4.962 dBr A

Vista-Frequency Response-M48k.at27

9.3.2 Frequency Response 44.1Ks/Sec (16 Ohm Loading)

Audio Precision 08/09/06 17:03:08

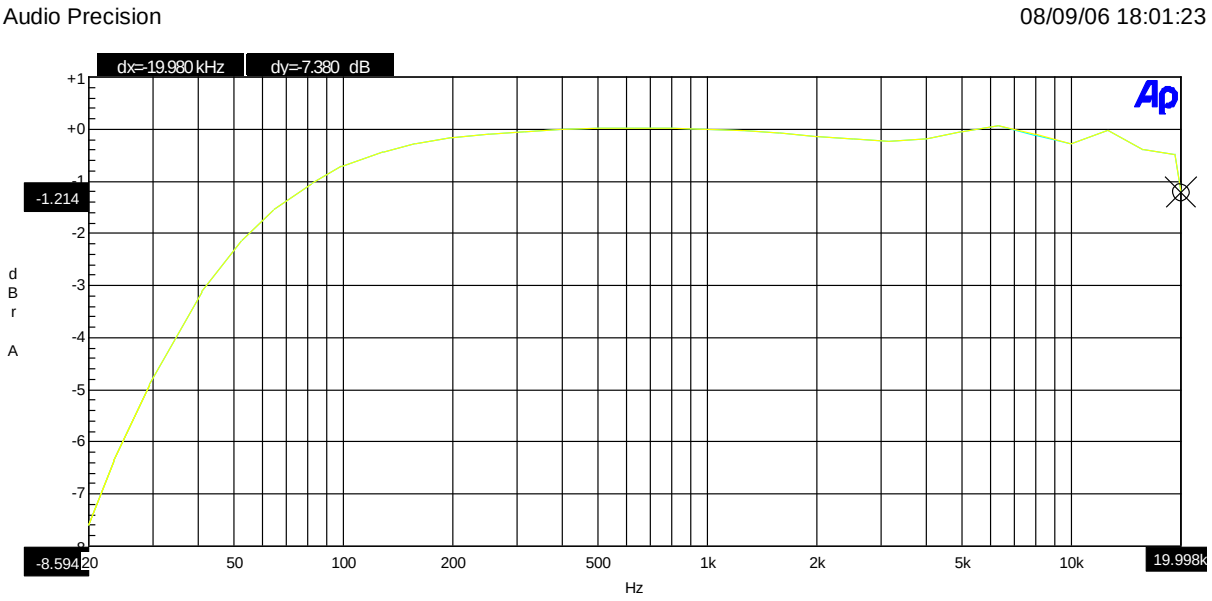


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-3.665 dBr A	*-4.894 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-3.657 dBr A	-4.893 dBr A

Vista-Frequency Response-M44k.at27

9.4 Digital Playback for Line Output Frequency (8 Ohm Loading)

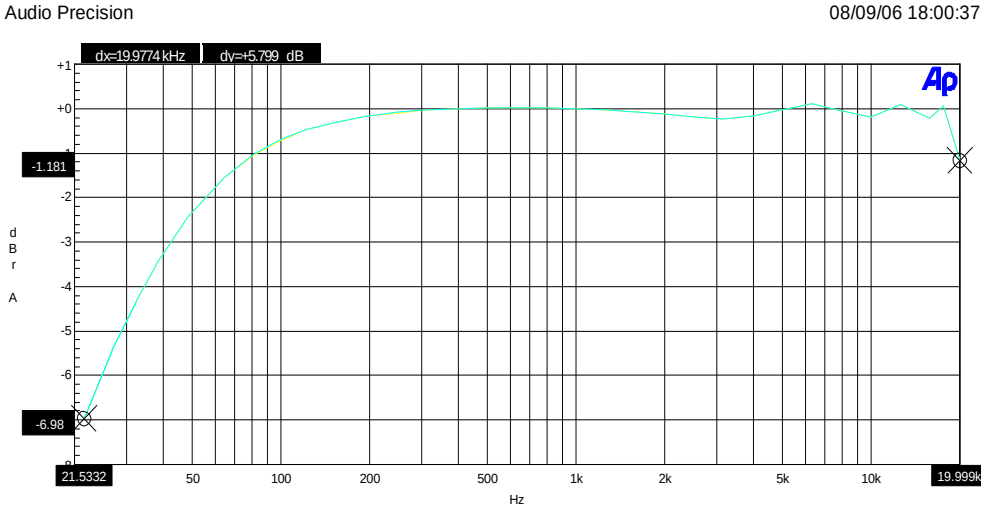
9.4.1 Frequency Response 48Ks/Sec (8 Ohm Loading)



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		-1.216 dBr A	-8.597 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		*-1.214 dBr A	*-8.594 dBr A

Vista-Frequency Response-M48k.at27

9.4.2 Frequency Response 44.1Ks/Sec (8 Ohm Loading)



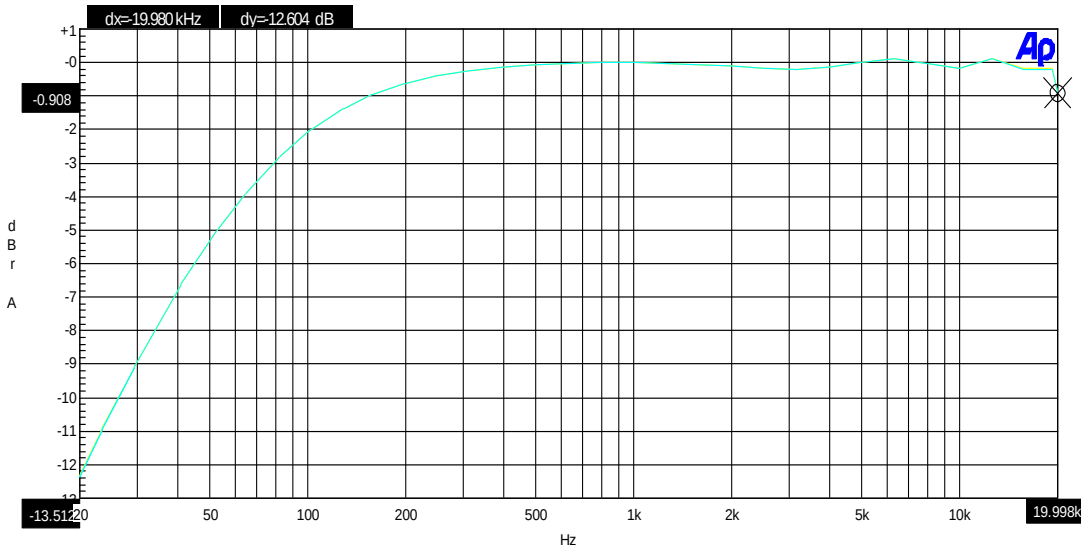
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-6.980 dBr A	*-1.181 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-6.977 dBr A	-1.179 dBr A

Vista-Frequency Response-M44k.at27

9.5 Digital Playback for Line Output Frequency (4 Ohm Loading)

9.5.1 Frequency Response 48Ks/Sec (4 Ohm Loading)

Audio Precision 08/09/06 17:39:57

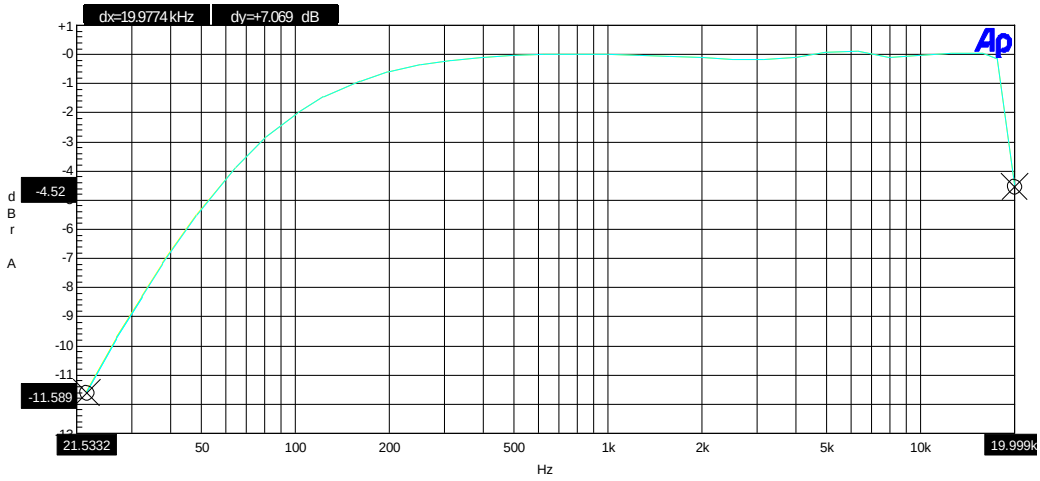


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-0.908 dBr A	*-13.512 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-0.904 dBr A	-13.481 dBr A

Vista-Frequency Response-M48k.at27

9.5.2 Frequency Response 44.1Ks/Sec (4 Ohm Loading)

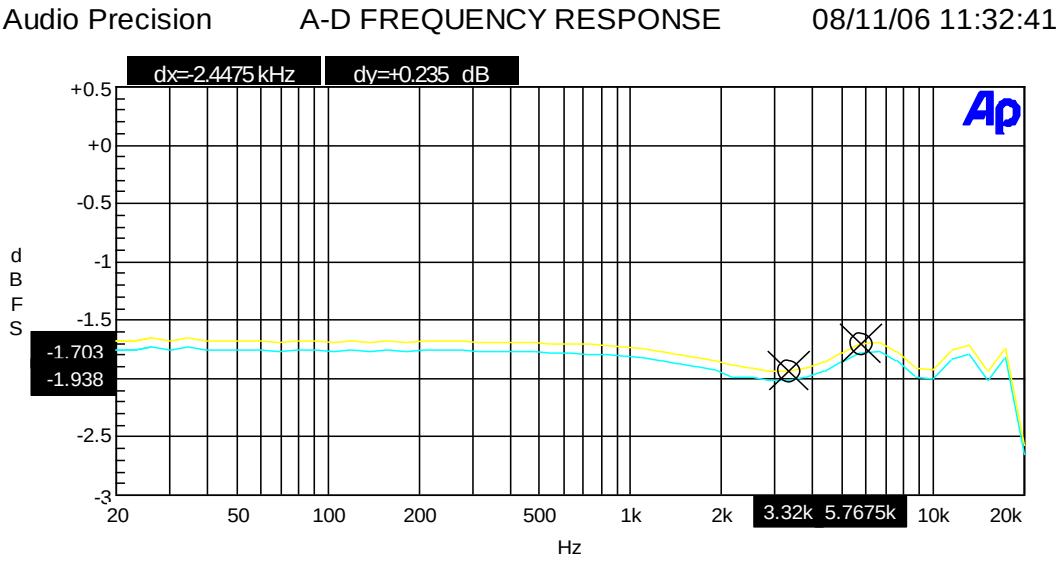
Audio Precision 08/09/06 17:52:58



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-11.589 dBr A	*-4.520 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-11.559 dBr A	-4.516 dBr A

Vista-Frequency Response-M44k.at27

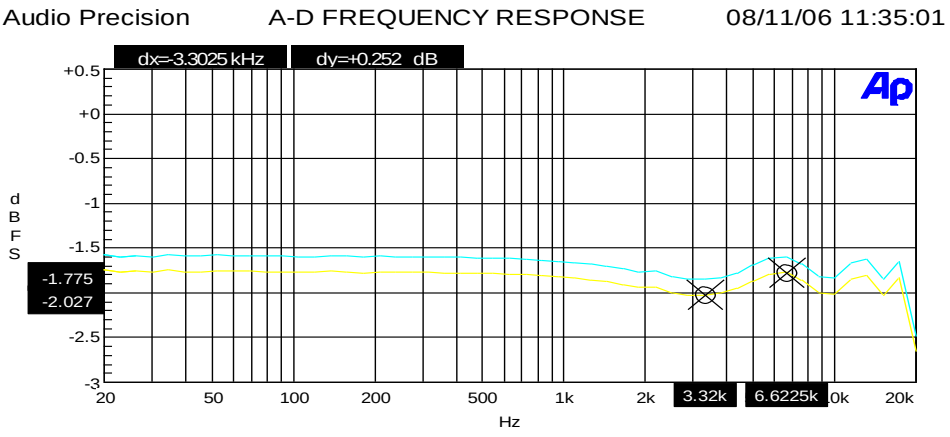
9.6 ADC (Line In) Frequency Response



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1
1	1	Yellow	Solid	1	DSP Anlr.Level A	Left		*-1.703 dBFS
1	2	Cyan	Solid	1	DSP Anlr.Level B	Left		-1.782 dBFS

Vista-A-D Frequency Response.at2c

9.7 ADC (Mic In) Frequency Response



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1
1	1	Yellow	Solid	1	DSP Anlr.Level A	Left		*-1.775 dBFS
1	2	Cyan	Solid	1	DSP Anlr.Level B	Left		-1.600 dBFS

Vista-A-D Frequency Response.at2c

REFERENCE

USB-IF, USB Specification, Revision 1.1 and 2.0, and USB Audio Device Class Specification, Revision 1.0,.

—End of Specifications—

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