CM6302

USB High-Quality Dolby® Headphone Solution

DESCRIPTION

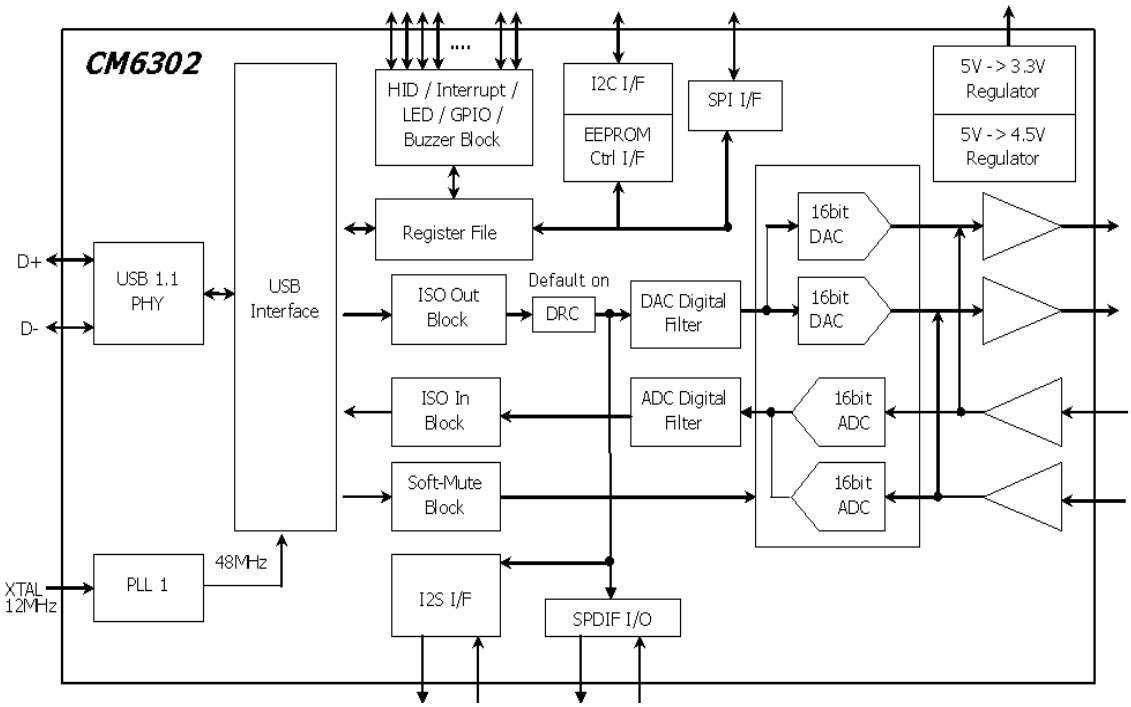
The CM6302 is a highly integrated single-chip USB audio solution. All essential analog and digital modules are integrated into the chip, including 2-ch DAC and 2-ch ADC, earphone/speaker driving capable, DRC (default off), linear microphone gain control, PLL, regulator and USB transceiver modules. As for DAC and ADC quality, this single chip supports 8khz/16Khz/ 44.1Khz/48Khz sampling rates with 16-bit resolution.

For higher performance, the CM6302 supported I2S and I2C interfaces communicate with external codecs or the MCU for further processing. The CM6302 is the world's first multi-channel software-integrated DSP with Xear 3D and Dolby® Digital sound. This audio solution is highly suitable for high-end USB headsets, earphone, audio interface box or proprietary wireless audio applications.

FEATURES

- USB specification 2.0 full speed-compliant and USB IF-certified
- Compatible with Win98SE/WinME/Win2000/ WinXP/Vista without additional drivers
- USB audio device specification 1.0 and USB HID specification 1.1-compliant
- Supports control/interrupt/isochroous data transfers
- USB suspend/resume and remote wake-up support
- Embedded USB transceiver and power-on reset circuit
- Single 12MHz crystal input with on-chip PLL
- Bus-power and self-power mode options
- High-power (500mA) and low-power (100mA) mode options
- SCMS-compliant (Serial Copy Management System)

BLOCK DIAGRAM



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1 Description and Overview

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Many features are programmable with jumper pins or by external EEPROM. In addition, audio adjustments can be easily controlled via specific HID-compliant volume control pins. Also, 8 GPIO pins can be accessed with customer application software for additional value-added applications.

Furthermore, Dolby® Headphone technology provides an amazing sound experience for PC audio and gaming entertainment. This technology works by creating an acoustic illusion: it makes you think you are hearing a five-speaker home theater system, when in fact you are listening to headphones. This illusion is based on a fundamental understanding of how we are able to judge which direction a sound is coming from, how far away it is, and whether it is in motion. It can even locate and track many sounds at the same time.

2 Features

- USB specification 2.0 full speed-compatible and USB IF-certified
- Compatible with Win98SE/WinME/Win2000/WinXP/Vista without additional drivers
- USB audio device class specification 1.0- and USB HID class specification 1.1-compliant
- Supports control/interrupt/isochroous data transfers
- USB suspend/resume and remote wake-up support
- Embedded USB transceiver and power-on reset circuit
- Single 12MHz crystal input with on-chip PLL
- Bus-power and self-power mode options supported
- High-power (500mA) and low-power (100mA) mode options supported
- For the mixer enable mode, the USB audio topology has 4 input terminals, 2 output terminals, 1 mixer unit, 1 selector unit and 5 feature units
- For mixer disable mode, USB audio function topology has 3 input terminals, 1 output terminals, 1 selector unit and 3 feature units
- AES/EBU IEC60958 specification-compliant (consumer format S/PDIF input/output with loop-back support)
- SCMS-compliant (Serial Copy Management System)

- Customizable PID/VID/product string/manufacturer string for device naming
- Supports a series number string for operation system detection
- Serial EEPROM programming interface supported for customizing VID/PID/product string,configuration and 24C02 data formats
- 2-channel DAC output:
  - DAC sampling rate from 8Khz, 16Khz, 44.1Khz to 48Khz, with 16-bit resolution
  - Dynamic range: 95db, THD+N -85db ~! -91dB
  - Earphone buffer driving for output
  - 1.2Vrms biased at 2.25V output swing
- 2CH ADC:
  - ADC sampling rate from 8Khz, 16Khz, 44.1Khz to 48Khz, with 16-bit resolution
  - Dynamic Range: 88db, THD+N -79db ~ -84dB
  - Digital linear microphone gain control function (-6db~33db)
  - 1Vrms biased at 2.25V input swing supported stereo-mixer function
- Playback with soft-mute function
- Microsoft HID volume control with Vol_Up, Vol_Dn, Playback_Mute and Record_Mute
- 2-ch MIC mode support with single mixer control on Microsoft mixer UI
- Supports I2C & SPI (master/slave) control interface for external controller used
- MCU read/write support 8-byte data transfer bandwidth
- Supports 3 LED indicator pins:
  1. On/Off/Operation
  2. Playback mute
  3. Recording mute
- I2S interface supports u-Law, A-Law, and linear PCM formats
- I2C interface support master/slave mode and with 3-wire serial interface
- I2C Interface to communicate with the MCU for advanced applications
- MCU/EEPROM/GPIO control via HID/vendor command interface
- Supports 8 GPIO pins
- Isochronous transfer adaptive mode with an internal PLL for synchronization
- Embedded power-on-reset block
- Single 5V power supply with embedded 5V to 3.3V regulator
- Embedded anti-pop circuit with internal feedback structure
- Industry-standard LQFP 64-pin package

Supported Xear-3D® and Dolby Digital® Added Software:

- Supports Dolby® Headphone DSP sound technology software for a high-performance listening experience
- Xear 3D Sound (C-Media patented driver) Software with Speaker Shifter and virtual 7.1-ch effects on Windows operation systems

Application Reference:

(a) High-quality USB Dolby-certified headsets

(b) High-end USB earphones

(c) USB audio interface boxes

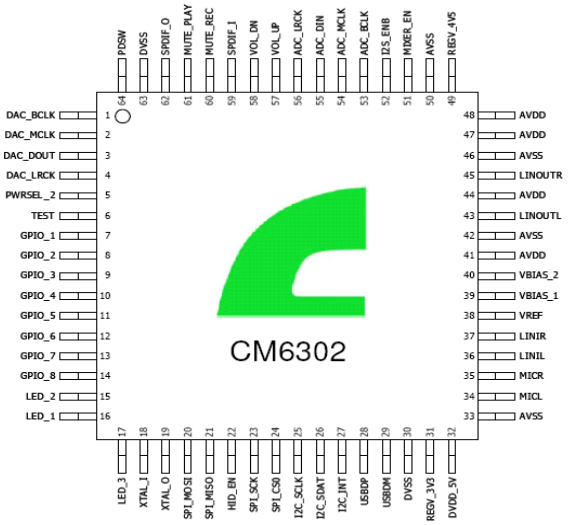
(d) Proprietary USB wireless audio

3 Pin Descriptions

3.1 Pin Assignment by Pin Number

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	DAC_BCLK	17	LED_3	33	AVSS	49	REGV_4V5
2	DAC_MCLK	18	XTAL_I	34	MICL	50	AVSS
3	DAC_DOUT	19	XTAL_O	35	MICR	51	MIXER_EN
4	DAC_LRCK	20	SPI_MOSI	36	LINIL	52	I2S_ENB
5	PWRSEL_2	21	SPI_MISO	37	LINIR	53	ADC_BCLK
6	TEST	22	HID_EN	38	VREF	54	ADC_MCLK
7	GPIO_1	23	SPI_SCK	39	VBIAS_1	55	ADC_DIN
8	GPIO_2	24	SPI_CS0	40	VBIAS_2	56	ADC_LRCK
9	GPIO_3	25	I2C_SCLK	41	AVDD	57	VOL_UP
10	GPIO_4	26	I2C_SDAT	42	AVSS	58	VOL_DN
11	GPIO_5	27	I2C_INT	43	LNOUTL	59	SPDIF_I
12	GPIO_6	28	USB_DP	44	AVDD	60	MUTE_REC
13	GPIO_7	29	USB_DM	45	LNOUTR	61	MUTE_PLAY
14	GPIO_8	30	DVSS	46	AVSS	62	SPDIF_O
15	LED_2	31	REGV_3V3	47	AVDD	63	DVSS
16	LED_1	32	DVDD_5V	48	AVDD	64	PDSW

3.2 Pin-Out Diagram



3.3 Pin Signal Description

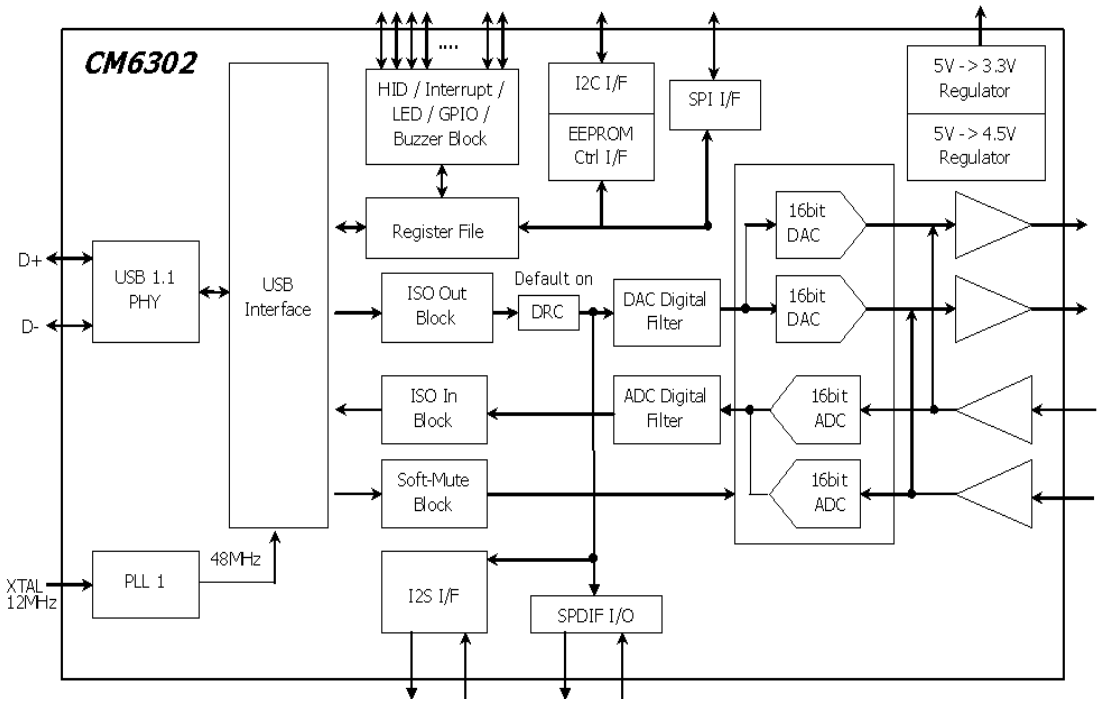
No.	Symbol	Type	Description
1	DAC_BCLK	DO	I2S bit clock for DAC
2	DAC_MCLK	DO	I2S master clock for DAC
3	DAC_DOUT	DO	I2S data output for DAC
4	DAC_LRCK	DO	I2S left/right word clock for DAC
5	PWRSEL_2	DIO, PU	Power consumption selector (0: 500mA; 1: 100mA)
6	TEST	DI, PD	Test mode select (0: Normal mode; 1: Test mode)
7	GPIO_1	DIO	General purpose I/O pin
8	GPIO_2	DIO	General purpose I/O pin
9	GPIO_3	DIO	General purpose I/O pin
10	GPIO_4	DIO	General purpose I/O pin
11	GPIO_5	DIO	General purpose I/O pin
12	GPIO_6	DIO	General purpose I/O pin
13	GPIO_7	DIO	General purpose I/O pin
14	GPIO_8	DIO	General purpose I/O pin
15	LED_2	DO	LED (Mute Play)
16	LED_1	DO	LED (Play or Record)
17	LED_3	DO	LED (Mute Record)
18	XTAL_I	DI	XTAL IN
19	XTAL_O	DO	XTAL OUT
20	SPI_MOSI	DIO	SPI
21	SPI_MISO	DIO	SPI
22	HID_EN	DI, PU	HID bottom function enable (0: Disable; 1: Enable)
23	SPI_SCK	DIO	SPI
24	SPI_CS0	DIO	SPI
25	I2C_SCLK	OD, DIO	I2C serial clock/EEPROM 24c02 serial clock
26	I2C_SDAT	OD, DIO	I2C serial data/EEPROM 24c02 serial data
27	I2C_INT	DO	I2C interrupt output
28	USB_DP	AIO	USB D+
29	USB_DM	AIO	USB D-
30	DVSS	P	Digital ground
31	REGV_3V3	AO	5V->3.3V regulator output
32	DVDD_5V	P	Digital power pin 5V
33	AVSS	P	Analog ground
34	MICL	AI	MIC0 in left channel
35	MICR	AI	MIC0 in right channel
36	LINIL	AI	Line in left channel
37	LINIR	AI	Line in right channel
38	VREF	AO	Bandgap reference output 2.25V
39	VBIAS_1	AO	Mic bias voltage 2.25V/4.5V
40	VBIAS_2	AO	Mic bias voltage 2.25V/4.5V
41	AVDD	P	Analog power
42	AVSS	P	Analog ground
43	LINOUTL	AO	Line out for left channel
44	AVDD	P	Analog power
45	LINOUTR	AO	Line out for right channel

No.	Symbol	Type	Description
46	AVSS	P	Analog ground
47	AVDD	P	Analog power
48	AVDD	P	Analog power
49	REGV_4V5	AO	4.5V regulator output
50	AVSS	P	Analog ground
51	MIXER_EN	DI, PU	Mixer AA-path enable (0: Disable; 1: Enable)
52	I2S_ENB	DI, PU	External I2S codec enable (0: Enable; 1: Disable)
53	ADC_BCLK	DO	I2S for ADC
54	ADC_MCLK	DO	I2S for ADC
55	ADC_DIN	DI, PD	I2S for ADC
56	ADC_LRCK	DO	I2S for ADC
57	VOL_UP	DI, PU	HID volume up
58	VOL_DN	DI, PU	HID volume down
59	SPDIF_I	DI	SPDIF IN
60	MUTE_REC	DI, PU	HID Recoding Mute
61	MUTE_PLAY	DI, PU	HID Playback Mute
62	SPDIF_O	DO	SPDIF OUT
63	DVSS	P	Digital ground
64	PDSW	OD, 5V tor	Power down switch output (0: Normal Operation; 1: Suspend)

***Notes:**

DI -> Digital Input **DO -> Digital Output** **DIO -> Digital I/O**
AI -> Analog Input **AO -> Analog Output** **AIO -> Analog I/O**
OD -> Open Drain **PU -> Internal Pull Up** **PD -> Internal Pull Down**
5V -> 5V Torrent **P -> Power**

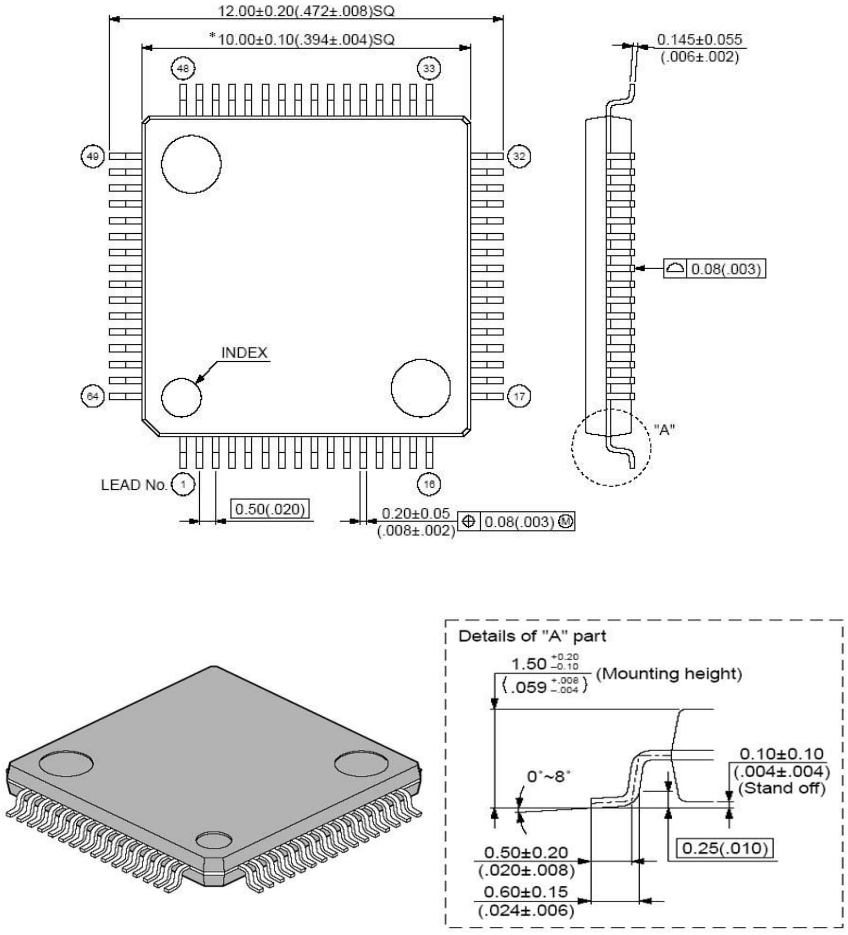
4 Block Diagram



5 Ordering Information

Model Number	Package	Operating Ambient Temperature	Supply Range
CM6302	64-Pin LQFP 10mm × 10mm × 1.7mm (plastic)	0°C to +70°C	DVdd = 5V, AVdd = 5V

Note: Physical Dimensions shown in inches and millimeters



64-Lead Thin Plastic Quad Flatpack (LQFP)

6 Introduction to Dolby Headphone Technology

Have you ever imagined having a home theater system that will not disturb your neighbors? Have you ever imagined watching a film and enjoy cinema-quality sound? Have you ever imagined you would enjoy listening to a symphony orchestra through earphones?

With Dolby® audio technology, your imagination can turn into reality. Dolby's earphone technology has a revolutionary signal processing system that can handle audio frequency signals on up to five sound channels, from any source, resulting in some serious 3D surround sound. C-media integrates this technology into its audio drivers.

Any kind of audio or video products can use Dolby's earphone technology if they have an audio frequency output interface. The more important thing is this technology can improve the sound quality of any pair of stereo earphones.

Dolby Headphone technology allows users to wear any set of headphones and listen to music, watch movies, or play video games with the dramatic surround effects of a 5.1-channel soundtrack. Listeners can enjoy the spacious, natural sound field for hours without feeling fatigued.

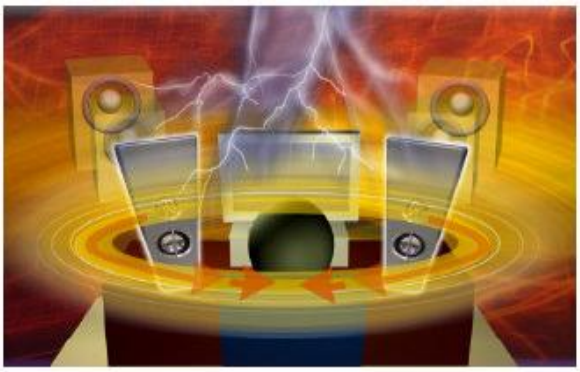
Also, Dolby's powerful processing technology offers specific filters that may be used with any type of program content. They differ in the sense of the "spatial dimension" they impart. These filters include:

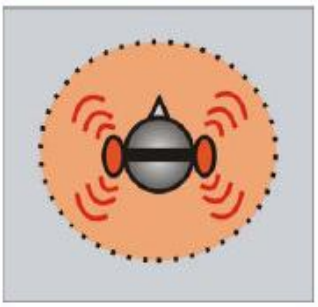
- DH1---Reference room: Small, acoustically damped room
- DH2---Livelier room: More acoustically live than DH1
- DH3---Larger room: Larger room than DH1; more distant and diffuse effect

***** Reference documents are from the Dolby website: http://www.dolby.com *****

Dolby Headphone Sound Effect

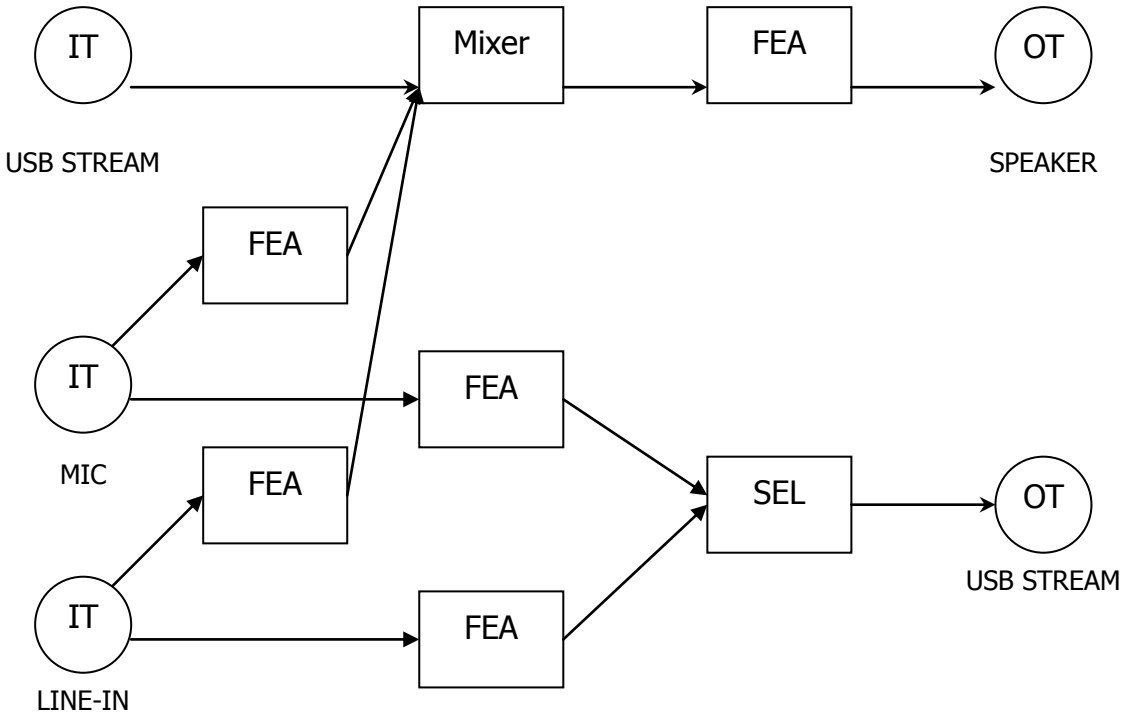
1.Reference Room	
2.Live Room	
3.Larger Room	





7 USB Audio Topology and Descriptors

7.1 USB Topology



7.2 Device Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	12	Descriptor length
1	bDescriptorType	1	01	Device descriptor
2	bcdUSB	2	0110	USB 1.1-compliant
4	bDeviceClass	1	00	Device class specified by interface
5	bDeviceSubClass	1	00	Device subclass specified by interface
6	bDeviceProtocol	1	00	Device protocol specified by interface
7	bMaxPacketSize0	1	40	Endpoint zero packet size
8	idVendor	2	0d8c	Vendor ID
10	idProduct	2	010F	Product ID
12	bcdDevice	2	0100	Device release number
14	iManufacturer	1	03	String descriptor Index describing manufacturer
15	iProduct	1	01	String descriptor Index describing product
16	iSerialNumber	1	00 or 02(*)	String descriptor Index describing serial number
17	bNumConfigurations	1	01	Number of configurations

Note 1: When a valid EEPROM is detected, the Vendor ID and Product ID will be replaced with the contents of the EEPROM
Note 2: iSerialNumber is valid only if the external EEPROM contains this information

7.3 Configuration Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	02	Configuration descriptor
2	wTotalLength	2	0131	Total length of data returned for this configuration: 305 bytes
4	bNumInterfaces	1	04	Number of interfaces supported by configuration: 00: Control 01: ISO-OUT 02: ISO-IN 03: INT-IN (HID)
5	bConfigurationValue	1	01	Configuration value
6	iConfiguration	1	00	String descriptor index describing this configuration
7	bmAttributes	1	a0 or 80 or e0 or c0	Bus-powered with remote wakeup support: 8'ha0 (PWRSEL_1 = 1, HID_EN = 1) Bus-powered with no remote wakeup: 8'h80 (PWRSEL_1 = 1, HID_EN = 0) Bus-powered with support remote wakeup: 8'he0 (PWRSEL_1 = 0, HID_EN = 1)) Bus-powered with no remote wakeup: 8'hc0 (PWRSEL_1 = 0, HID_EN = 0))
8	bMaxPower	1	32 or fa	Maximum power consumption from bus = 100mA: 8'h32 (50x2 mA) (PWRSEL_2 = 1) Maximum power consumption from bus = 500mA: 8'hfa (250x2 mA) (PWRSEL_2 = 0)

7.4 Standard HID Interface Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	**09**	Descriptor length
1	bDescriptorType	1	**04**	Interface descriptor
2	bInterfaceNumber	1	**03**	Interface number: 03
3	bAlternateSetting	1	**00**	Alternate interface
4	bNumEndpoints	1	**01**	Number of endpoints used by this interface
5	bInterfaceClass	1	03	HID interface class
6	bInterfaceSubClass	1	00	Subclass code
7	bInterfaceProtocol	1	00	Protocol code
8	iInterface	1	00	Interface string descriptor index

7.5 Class-specific HID Interface Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	21	HID descriptor type
2	bcdHID	2	0100	HID class version
4	bCountryCode	1	00	No country code
5	bNumDescriptors	1	01	One HID class descriptor
6	bDescriptorType	1	22	Report Descriptor
7	wDescriptorLength	2	0032 / 001a	HID class descriptor length in byte: 50/26 bytes (Enable/Disable HID Button)

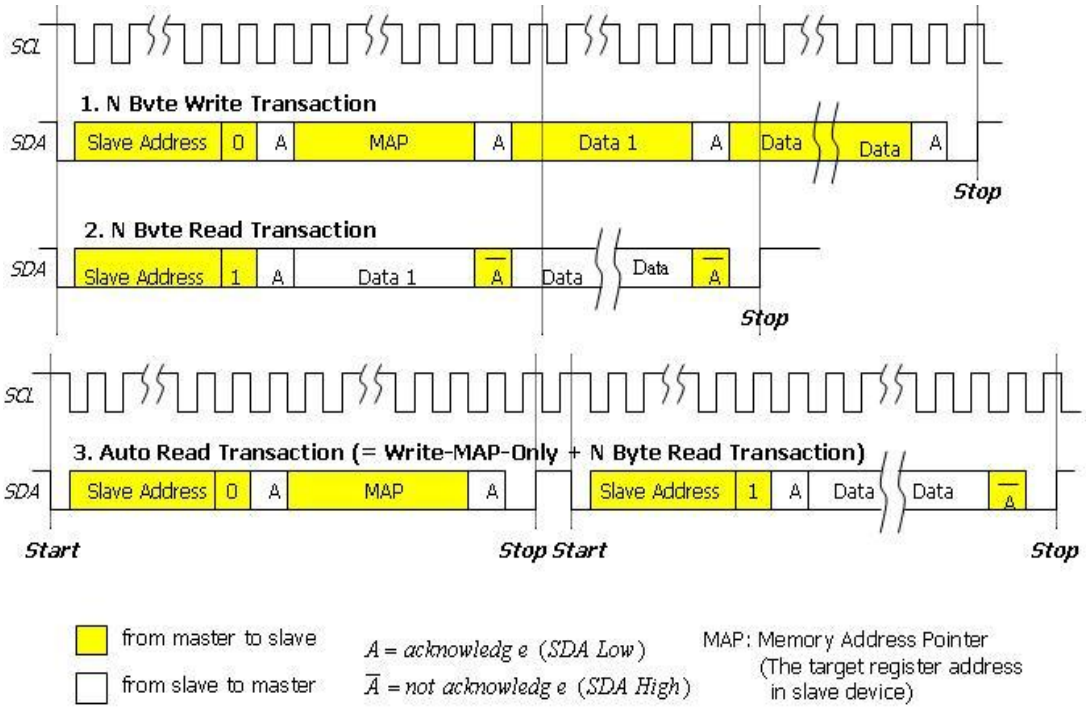
7.6 Standard HID Interrupt In Endpoint Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	07	Descriptor length
1	bDescriptorType	1	05	Endpoint descriptor
2	bEndpointAddress	1	87	IN endpoint, endpoint number: 7
3	bmAttributes	1	03	Interrupt endpoint
4	wMaxPacketSize	2	0010	Maximum packet size: 16 bytes
6	bInterval	1	01	1ms

8 Function Block Descriptions

8.1 I²C Interface

8.1.1 Master Mode



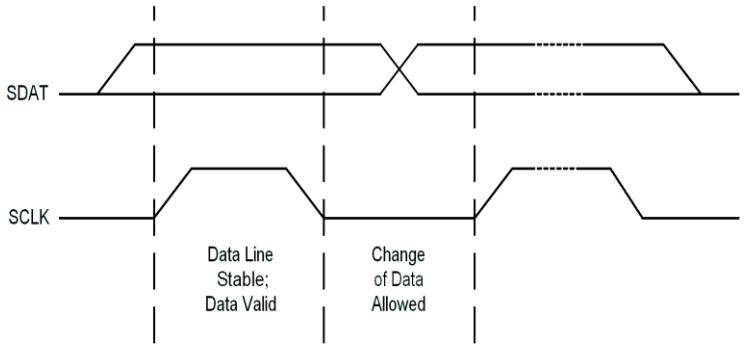
8.1.2 Slave Mode

"7-bit slave address = 7'b0111000"

On the MCU serial interface, the CM6302 serves as a slave device with bit rate up to 400Kbps (fast mode). The MCU can write data to the CM6302 or read data from the CM6302 (no size limitations when using the I2C Interface). Since the host side and MCU both have access to all the internal registers, access contention when both host and MCU try to access the same register should be avoided upon application. The CM6302's 7-bit slave address is assigned as 7'b0111000.

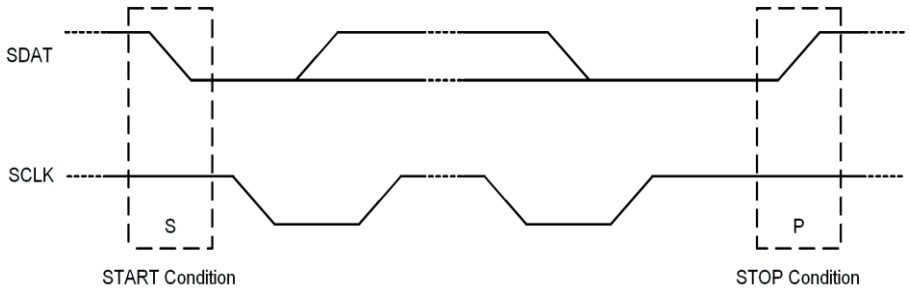
When data is written by the MCU, the CM6302 will NOT transfer any interrupts to the PC until the INT bit of the I2C control register has been set by the MCU. The USB host will keep polling the upward HID report every 1ms. When any button is pressed or released, or there is incoming MCU data, the CM6302 will transfer 16 bytes of HID report to the USB host.

In I2C Slave Mode, the CM6302 has one open-drain input pin (SCLK) from where it receives the serial clock from the MCU, and one open-drain I/O pin (SDAT) from where it sends or receives serial signals to/from the MCU. As shown below, SDAT should be stable when SCLK is high, and can transition only when SCLK is low.



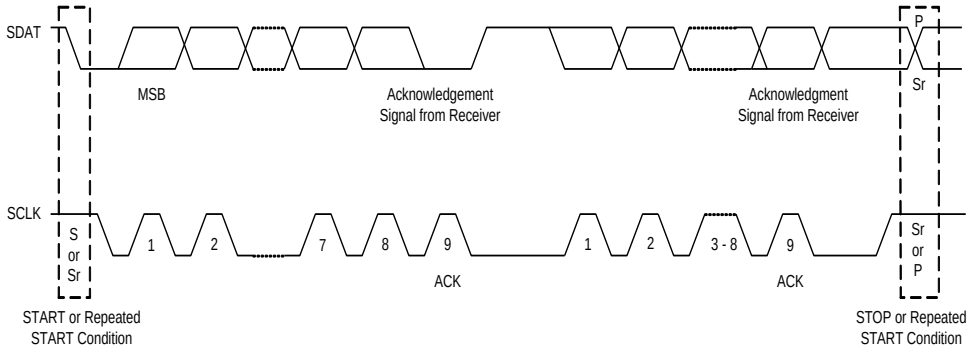
Bit Transfer on the MCU Interface

START and STOP conditions shown below are the exception. Every transaction begins from a START, and ends with a STOP, or another START (repeated START).

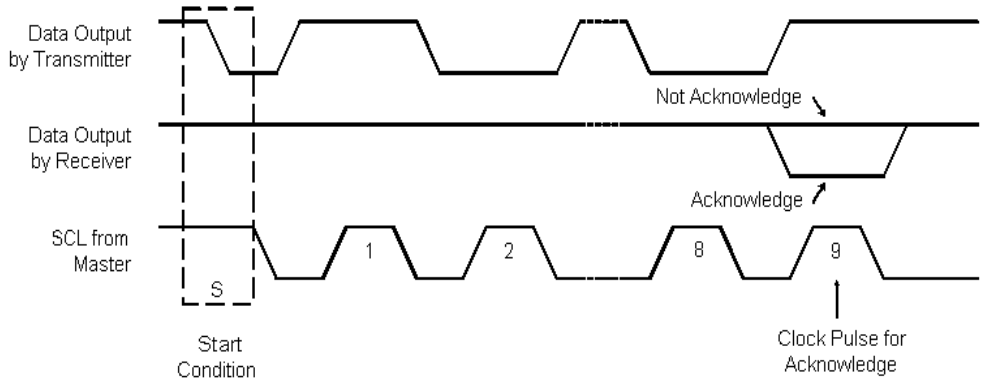


START and STOP Conditions

The figure below demonstrates a typical transaction. After every 8 bits sent by the transmitter, the receiver should send one bit low for positive acknowledgement or one bit high for negative acknowledgement. After the negative acknowledgement, a STOP or repeated START should follow. The next figure shows more details about the acknowledgement bit. Note that SCLK is always driven by the master.

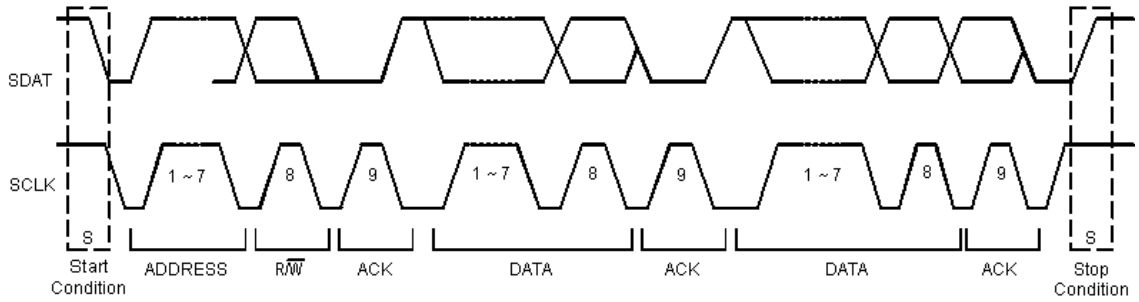


Data Transfer on the MCU Interface



Acknowledge on the MCU Interface

The figure below shows a complete data transfer. After a START, the MCU should send a 7-bit slave address (7'b0111000) first, with the 8th bit denoting a read transfer when it's high, or a write transfer when it's low. The first acknowledgement always comes from the CM6302.



A Complete Data Transfer

During the write transfer, the MCU continues acting as the master, and the transfer direction is not changed. The following figure gives an example of one byte write transfer.

MCU write:

S	0x70	0	addr	0	Byte 0	0	Byte 1	0	....	0	Byte N	0	P

	From CM6302 to MCU		From MCU to CM6302
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte N	One byte data		

0x70 is the slave address that tells the CM6400 when it's receiving a write command. The CM6302 regards the first incoming data byte as the register address. The second data byte is the content that the MCU writes at the register address. The CM6302 will then auto-increment the register address to the next register address for the following data writes.

The MCU read command cannot set the register address, so the MCU may use a write command to set the register address first, before starting the read command. Because the CM6302 auto-increments the register address, the second data byte will be the register data on the next address. The figure below shows an example of a read transfer:

MCU read:

S	0x70	**0**	**addr**	**0**							
S	0x71	**0**	**Byte 0**	**0**	**Byte 1**	**0**	**…..**	**0**	**Byte N**	**1**	**P**

	From CM6302 to MCU		**From MCU to CM6302**
S	**START condition**	**P**	**STOP condition**
0	**Positive acknowledge**	**1**	**Negative acknowledge**
Byte n	**One byte data**		

The figure below gives a complete picture of a typical transaction between the MCU and CM6302. After a START, the MCU should send a 7-bit slave address (7'b0111000) first, with the 8th bit denoting a read transfer when it's high, or a write transfer when it's low.

MCU write:

S	0x70	0	addr	0	Byte 0	0	Byte 1	0	…..	0	Byte N	0	P

MCU read:

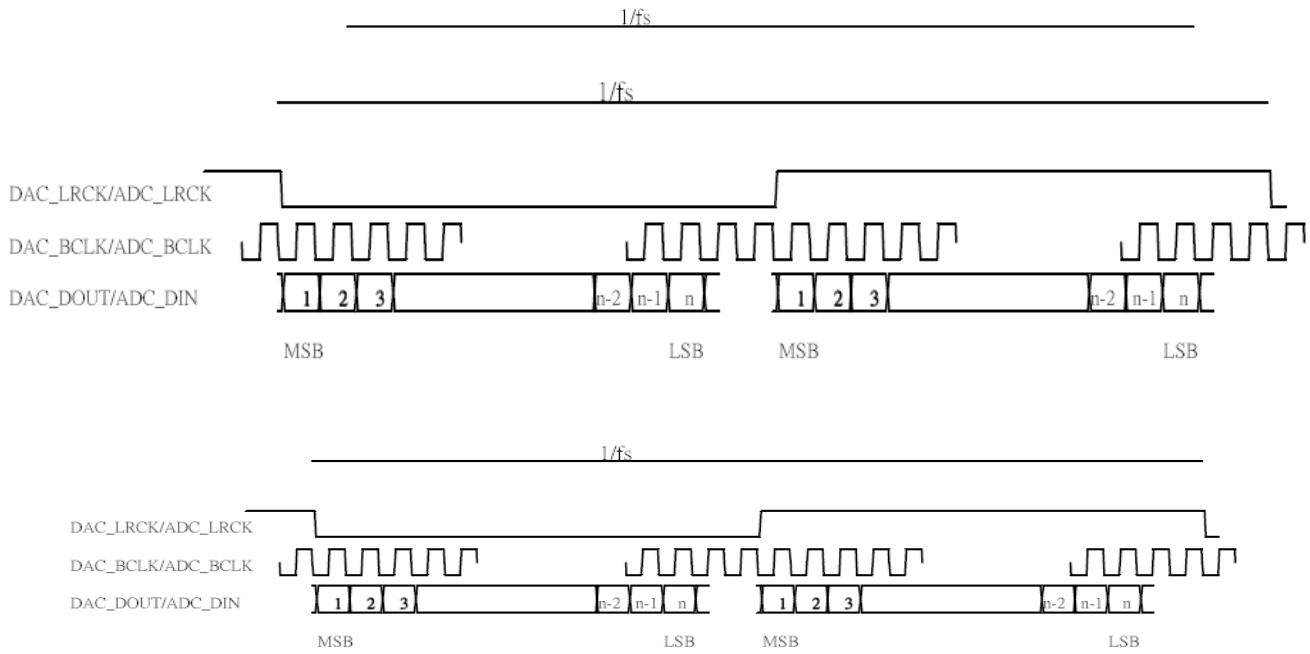
S	0x70	0	addr	0							
S	0x71	0	Byte 0	0	Byte 1	0	…..	0	Byte N	1	P

	From CM6302 to MCU		From MCU to CM6302
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte N	One byte data		

During a write transfer, the MCU acts as the transmitter. The CM6302 will regard the first byte of data received as the start register address. The following DATA bytes are the contents of the registers that the MCU has requested. In a read transfer, two transactions are necessary. The MCU resets the start register address by the first transaction, then direction changes for the MCU to receive data in the second transaction.

8.2 Square S Interface (I2S I/F)

8.2.1 I2S Mode



8.3 Serial Peripheral Interface

The SPI interface is used to transfer control data between the CM6302 and external codecs. However, it is not a standard interface. Every vendor has their own implementation, and each implementation is different. Generally speaking, all of them are comprised of four signals: *spi_cen*, *spi_clock*, *spi_data_o*, *spi_data_i*. Their meanings are as follows:

- ***spi_cen***: the SPI chip enable signal that is used to inform a codec when it should latch the data
- ***spi_clock***: the SPI clock signal
- ***spi_data_o***: the SPI data output to codec
- ***spi_data_i***: the SPI data input from codec

8.3.1 SPI Design Goal and SPI Transactions

Our goal is to design a robust SPI interface that suits all existing codecs. After analyzing the SPI codecs, we have listed the following difference among them:

1) An SPI interface that can read data from a codec and write data to a codec has 4 wires, but some codecs only support input data. In other words, the data in the codec registers cannot be retrieved by the audio processor. This later kind of codec only needs 3 wires.
2) An SPI transaction length is 2 or 3 bytes depending on the codec.
3) Some codec latch control data is at the SPI clock high state, but some codec latch control data is at the SPI clock low state
4) The upmost SPI clock frequencies are different for each codec.

In response to point one, we have designed a 4-wire SPI interface, which is able to accommodate the 3-wire SPI interface as well. For points 2 and 3, control bits in the SPI interface of the CM6302 are used to initiate 2-byte or 3-byte data transfers, and maintain SPI clock high or low at codec latching data. All of these can be observed in the following figures A ~ E.

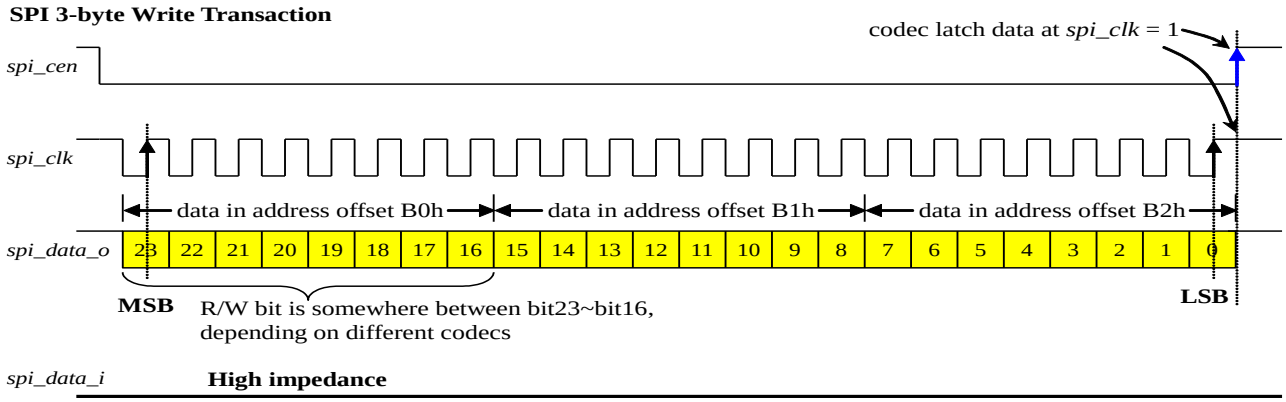


Fig. A. An SPI 3-byte write transaction with codec latching data at *spi_clk* high state

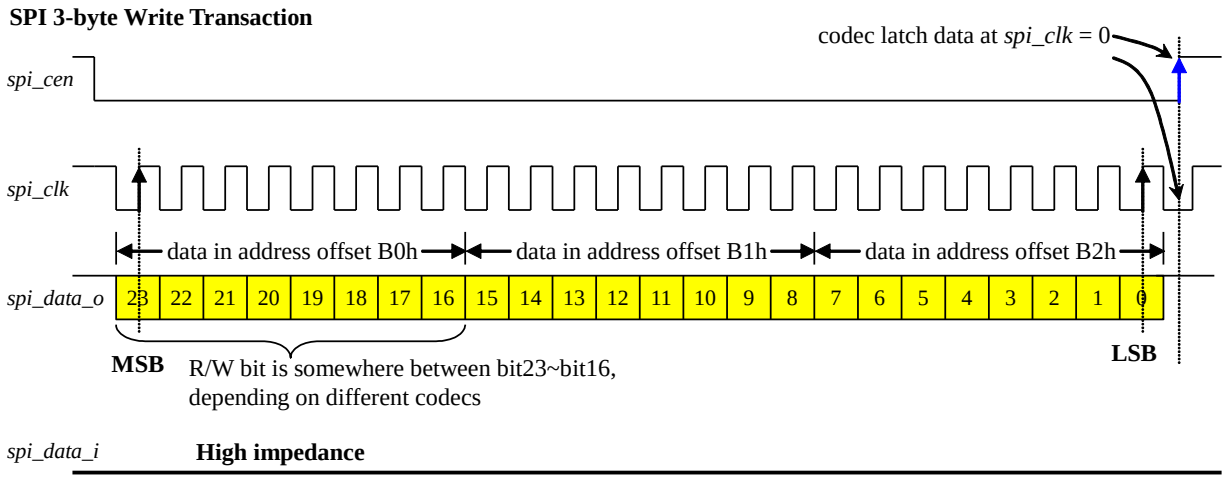


Fig. B. An SPI 3-byte write transaction with codec latching data at *spi_clk* low state

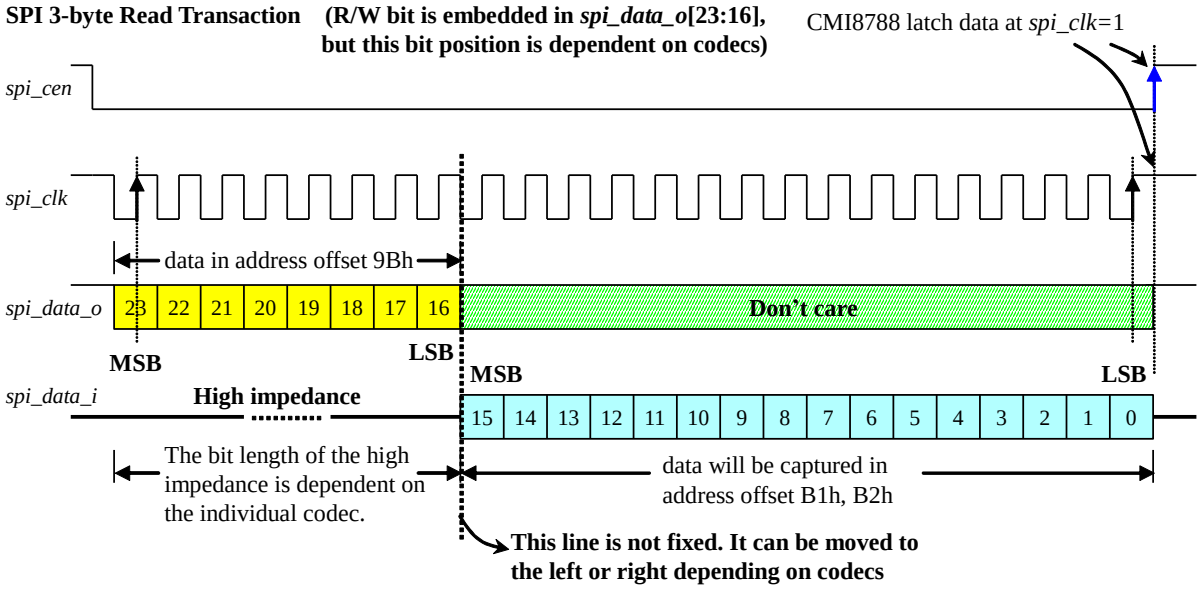


Fig. C. An SPI 3-byte read transaction with codec latching data at *spi_clk* high state.

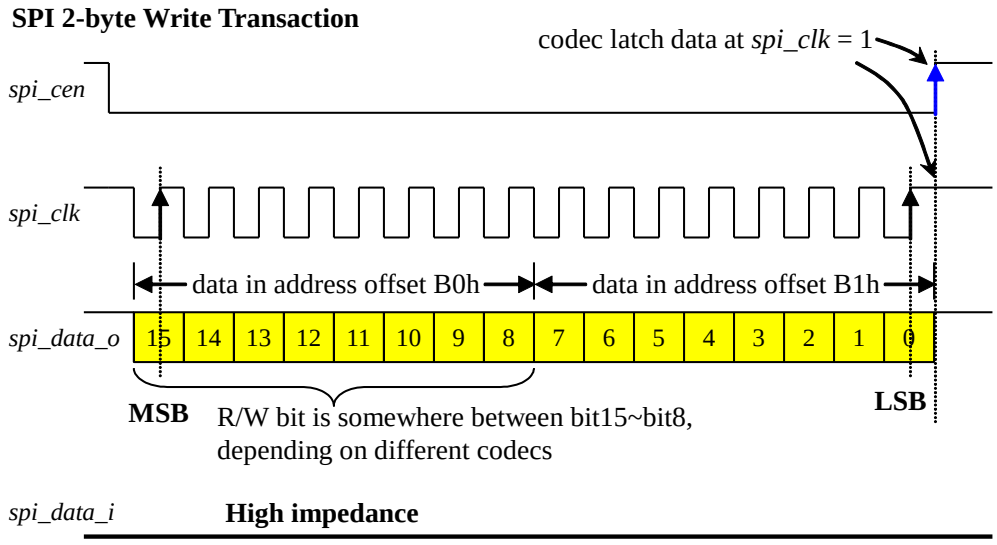


Fig. D. An SPI 2-byte write transaction with codec latching data at *spi_clk* high state.

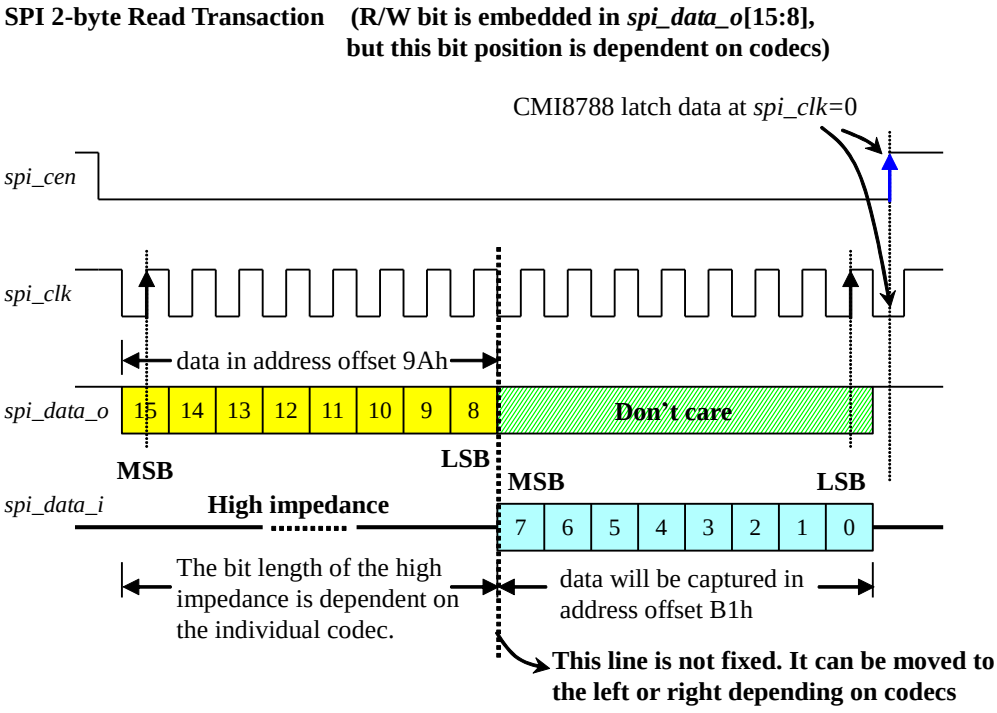


Fig. E. An SPI 2-byte read transaction with codecs latching data at *spi_clk* low state.

In order for our SPI interface to be capable of interfacing with all codecs, the content of the data registers (address offset 9Bh-99h, which includes address, r/w, and data bits) that are written to or read from the codec are not translated by the hardware SPI interface, but by the system driver. The meaning of the bits in this register should be interpreted according to the individual codec.

It is important to notice that the contents of this register, after a write transaction completes, have no meaning. However, after a read transaction completes, you should reference the codec's documentation to see how many bits in this register are valid. For example, if the codec is Analog Device AD1837, then SPI_Data_Reg[9:0] will be valid data.

As the highest SPI clock frequencies are different for many codecs, two control bits are used to adjust the spi_clk frequency to gain the maximum transfer speed. The CM6302 can control up to six codecs through the SPI interface, as shown in Fig. F below.

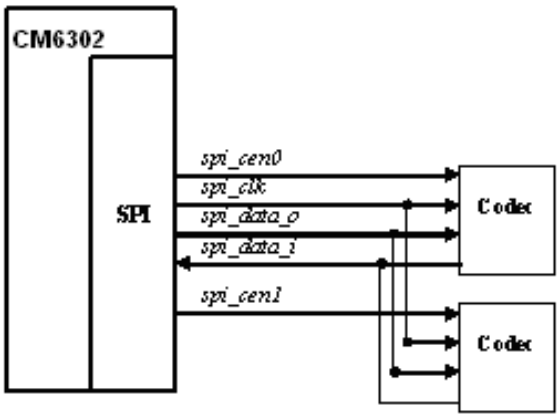
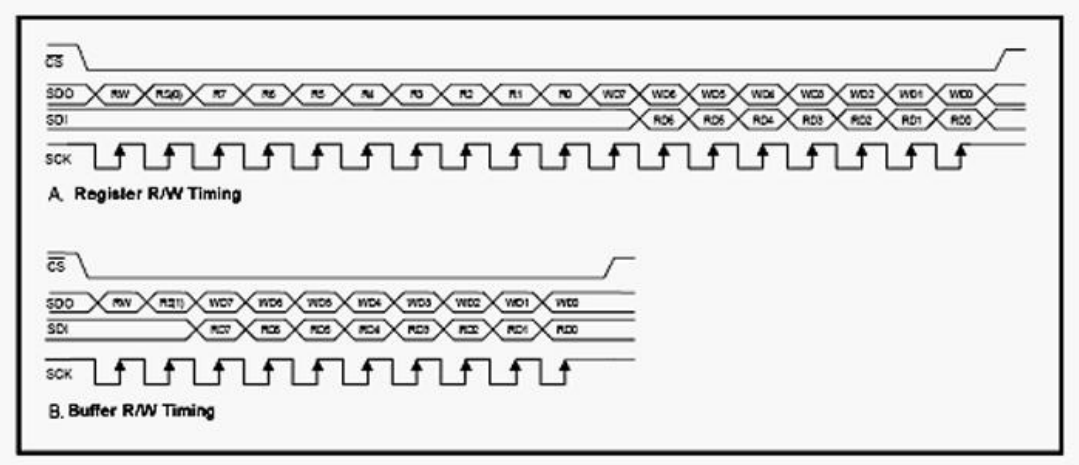


Fig. F. The SPI connection topology

8.3.2 2-bit Leading Mode

The 2-bit leading mode is designated for LCM controllers. Its waveform is almost the same as the general SPI except for two extra bits, RW and RS, in the beginning of each transaction. See the following figure:



8.3.3 The Serial Interface

The serial data is read from the serial data input pin on the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits of parallel data on the rising edge of the 8th serial clock cycle for the processing. The A0 input is used to determine whether or not the serial data input is displaying data or command data; when A0 = “H”, the data is display data, and when A0 = “L” then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip active. Figure 1 is a serial interface signal chart.

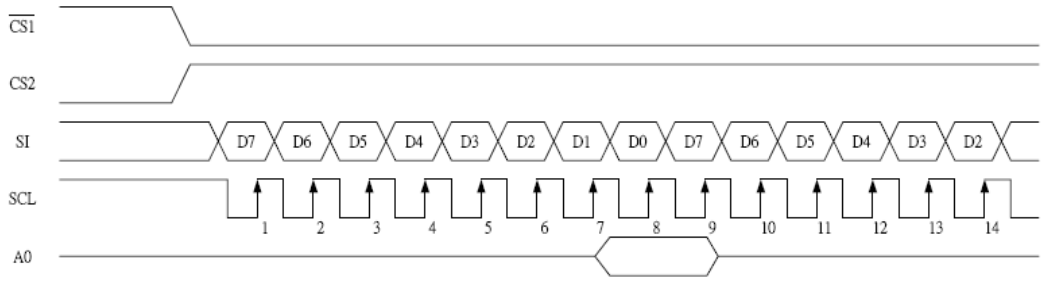
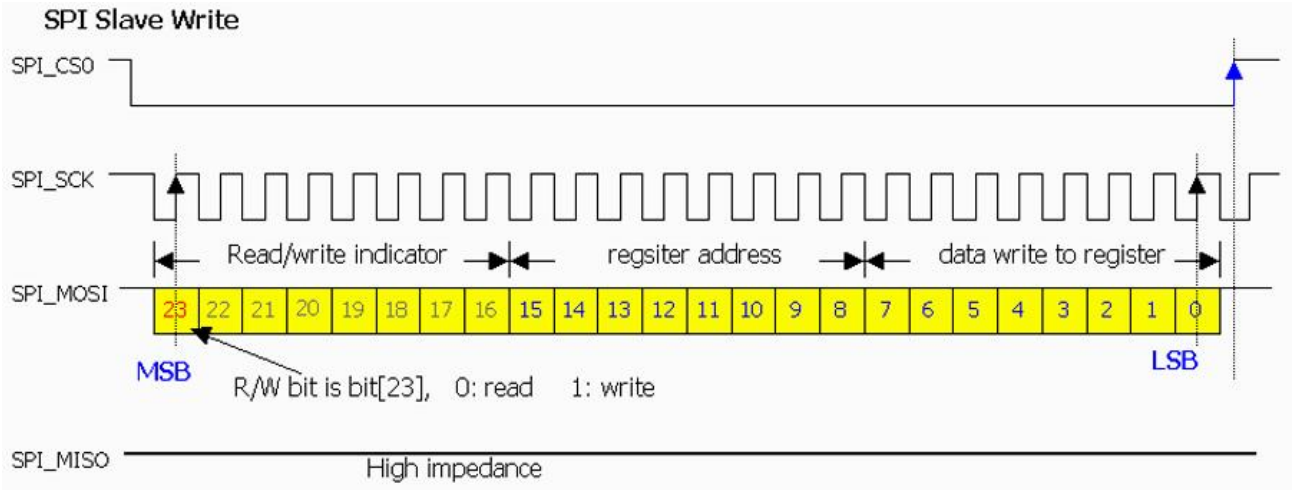
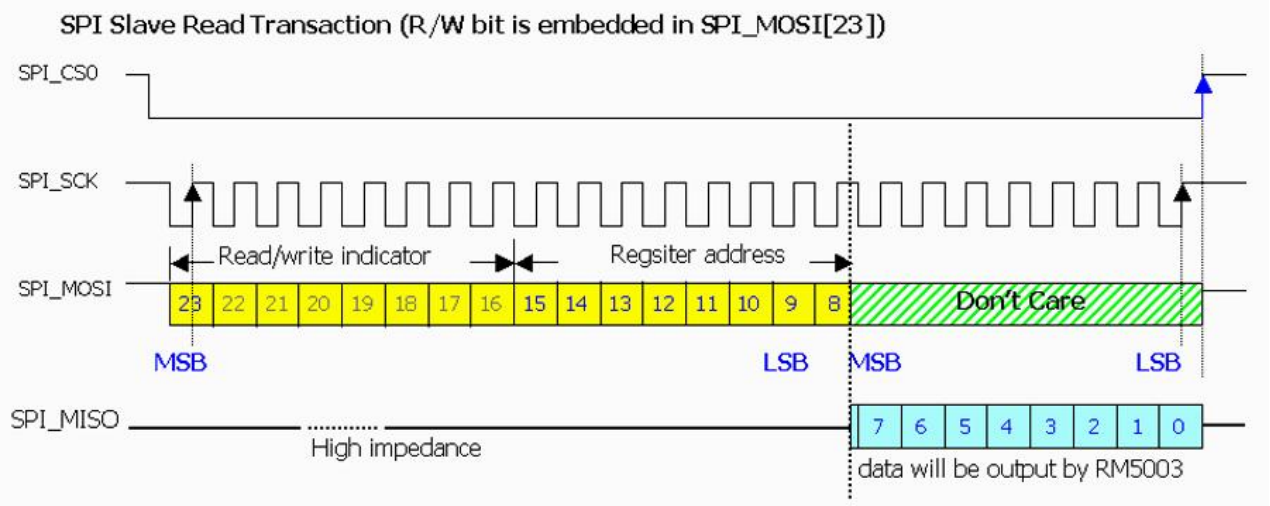


Figure 1

When the CM6302 acts as a SPI slave, the external MCU can read/write registers within the CM6302 through the SPI interface. Each transaction is 3-bytes long. The first byte is a read/write command indicator. When the MSB of the first byte is low, it means a read transaction is occurring; otherwise it is a write transaction. The other bits of the first byte are meaningless. The second byte is the address of the desired register. The third

byte, for a read transaction, is meaningless, and meanwhile the MISO would output the data of register. The third byte, for write transactions, is data.

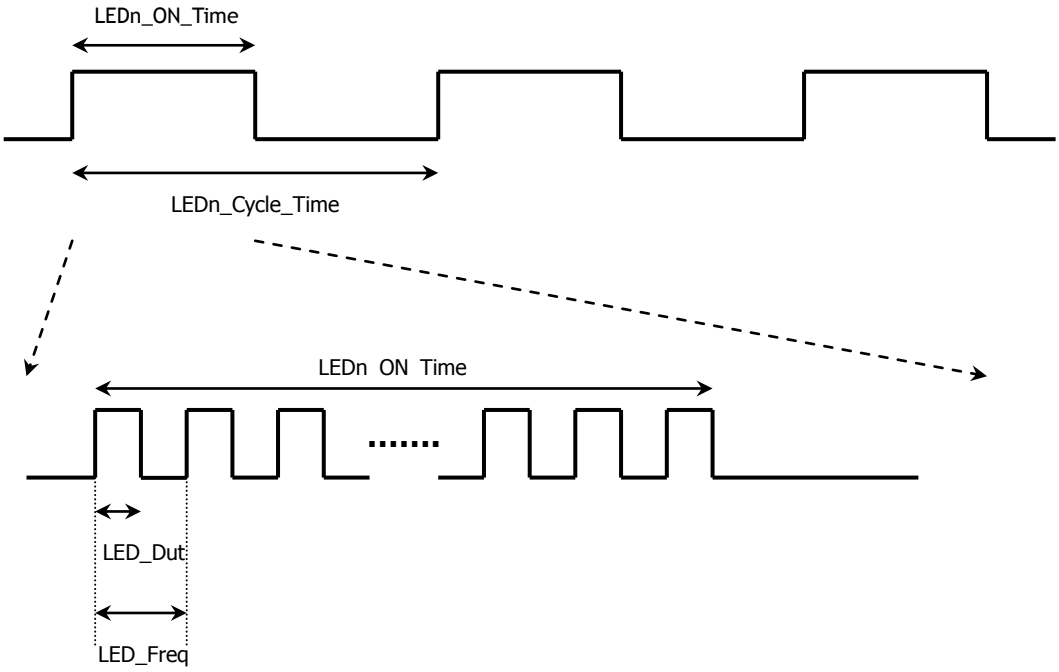




8.4 LED Behavior and Software Control

LED1 (Configure & Play/Rec)	3 times/sec
LED2 (Configure & Play Mute)	Always on
LED3 (Configure & Rec Mute)	1 time/sec

The LED Signal resembles a PWM waveform:



*** Notes: 1) Unit for LED_Duty / LED_Freq (Resolution) = 42.67 uS**
2) Unit for LEDn_ON_Time / LEDn_Cycle_Time (Resolution) = 21.85 mS

8.5 EEPROM Content Data Format

24c02 (256 x 8 bit)

[ADDR]	[DATA]
0x00,	Magic Word (“C”, 8’h43)
0x01,	Magic Word (“M”, 8’h4D)
0x02,	Total Data Length in EEPROM
0x03,	EEPROM Content Setting **bit 0: Manufacture String Valid? (0: No, 1: Yes)** **bit 1: Product String Valid? (0: No, 1: Yes)** **bit 2: Serial Number Valid? (0: No, 1: Yes)** **bit 3: Reserved (Default 0)** **bit 4: Playback (DAC) Control Valid? (0:No, 1:Yes)** **bit 5: Recording (ADC) Control Valid? (0: No, 1: Yes)** **bit 6: Mixer (AA-Path) Control Valid? (0: No, 1: Yes)** **bit 7: Enable Remote Wakeup? (0: Disable, 1: Enable)**
0x04,	Reserved
0x05,	Playback (DAC) Control **bit[5:0]: DAC (Unit f9) initial Volume (6’h3f ~ 6’h1a, -2.6 ~ -34.5dB/Mute, linear step)** **bit 6: Mute_f9 (DAC) initial Value (0: Un-Mute, 1: Mute)** **bit 7: DRC initial Value (0: Disable, 1: Enable)**
0x06,	Recording (ADC) Control **bit[4:0]: ADC (Unit fa / fb) initial Volume (5’h1f ~ 5’h04, +33 ~ -6dB/Mute, -1.5dB/step)** **bit 5: Reserved (Default 0)** **bit 6: Mute_fb (ADC Line) initial Value (0: Un-Mute, 1: Mute)** **bit 7: Mute_fa (ADC Mic) initial Value (0: Un-Mute, 1: Mute)**
0x07,	Mixer (AA-Path) Control **bit[5:0]: AA-Path (Unit fd / fe) initial Volume (6’38 ~ 6’h10, +22.5 ~ -36dB/Mute, -1.5dB/step)** **bit 6: Mute_fe (AA Line) initial Value (0: Un-Mute, 1: Mute)** **bit 7: Mute_fd (AA Mic) initial Value (0: Un-Mute, 1: Mute)**
0x08,	VID (Low Byte)
0x09,	VID (High Byte)
0x0A,	PID (Low Byte)
0x0B,	PID (High Byte)
0x0C ~ 0x29	Manufacture String (30 bytes)
0x2A ~ 0x65	Product String (60 bytes)
0x66 ~ 0x75	String of Serial Number (16 bytes)
0x76 ~ 0xFF	Reserved (Default 0x00)

9 Electrical Characteristics

9.1 Absolute Maximum Rating

Symbol	Parameter	Value	Unit
Dvmin	Min. digital supply voltage	- 0.3	V
Dvmax	Max. digital supply voltage	+ 6	V
Avmin	Min. analog supply voltage	- 0.3	V
Avmax	Max. analog supply voltage	+ 6	V
Dvinout	Voltage on any digital input or output pin	-0.3 to +5.5	V
Avinout	Voltage on any analog input or output pin	-0.3 to +5.5	V
T_{stg}	Storage temperature range	-40 to +125	^{0}C
ESD (HBM)	ESD human body mode	3500	V
ESD (MM)	ESD machine mode	200	V

9.2 Operation Conditions

Operation conditions				
	Min	Typ	Max	Unit
Analog supply voltage	4.5	5.0	5.5	V
Digital supply voltage	4.5	5.0	5.5	V
Operation power consumption, 4 Ohm loading*	-	300	330	mA
Operation power consumption, 10K Ohm loading*	-	110	120	mA
Standby power consumption	-	85	-	mA
Suspend mode power consumption	-	380	-	uA
Operating ambient temperature	0	-	70	^{0}C

***Notes: Test environment under 25°C, 5.0V, 48K sample rate**
Max. output is playing 1K full-scale sine wave, typical output is playing music

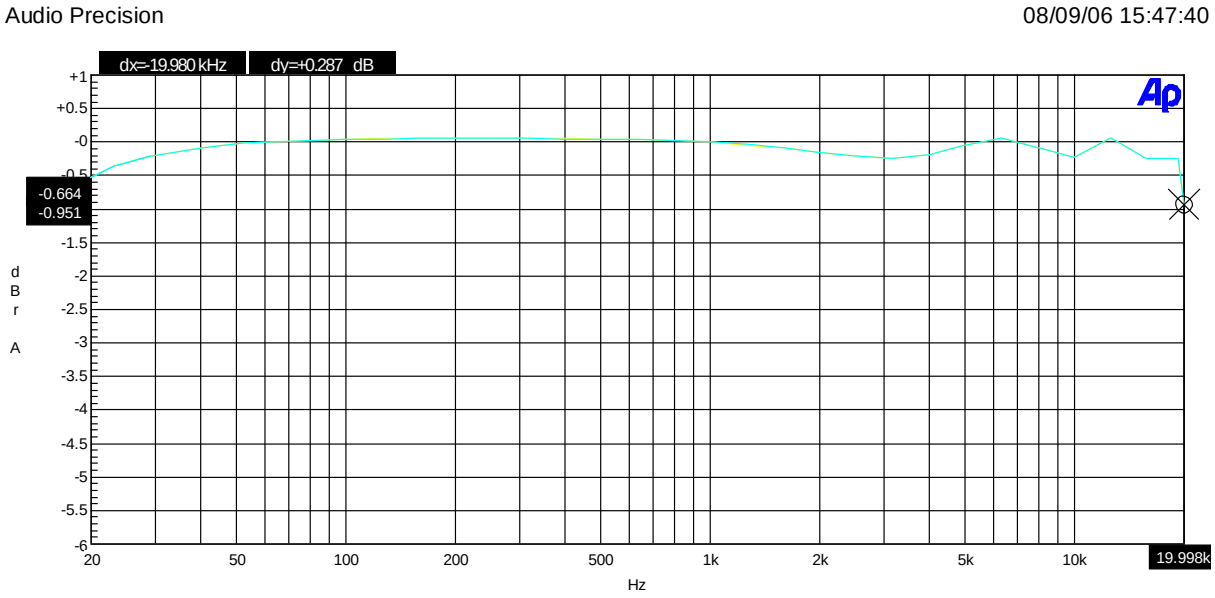
9.3 Electrical Parameters

	Min	Typ	Max	Unit
DAC (10K Ohm Loading)				
Resolution	-	16	-	Bits
THD + N (20 ~ 20KHz)	-85	-	-91	dB
Dynamic range (20 ~ 20KHz)	-	95	-	dB
Cross talk (20 ~ 20KHz)	-100	-	-112	dB
Frequency response 48KHz	20	-	20K	Hz
Frequency response 44.1KHz	20	-	20K	Hz
Output voltage (rms)	-	1.27	-	Vrms
Inter channel phase delay	0.03	-	0.09	Deg.
ADC				
Resolution	-	16	-	bit
THD + N (20 ~ 20KHz)	-79	-	-84	dB
Dynamic range (20 ~ 20KHz)	-	88	-	dB
Frequency response 48KHz	20	-	20K	Hz
Frequency response 44.1KHz	20	-	20K	Hz
Input voltage (rms)	-	1	-	Vrms

10 Frequency Response Graphs

10.1 Digital Playback for Line Output Frequency (10K Ohm Loading)

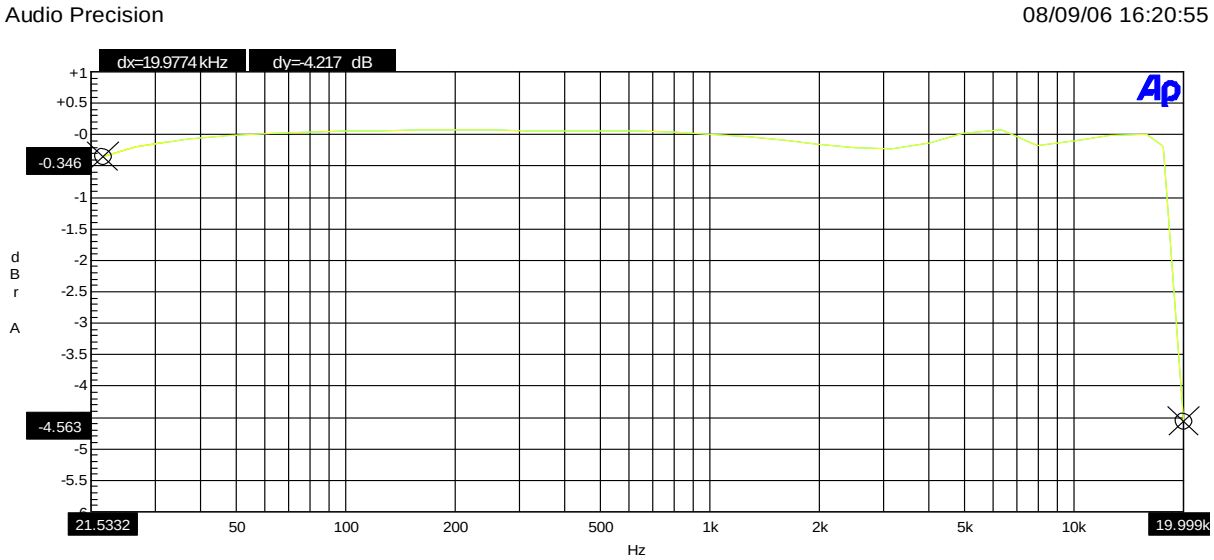
10.1.1 Frequency Response 48Ks/Sec (10K Ohm Loading)



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-0.951 dBr A	*-0.664 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-0.952 dBr A	-0.664 dBr A

Vista-Frequency Response-M48k.at27

10.1.2 Frequency Response 44.1Ks/Sec (10K Ohm Loading)



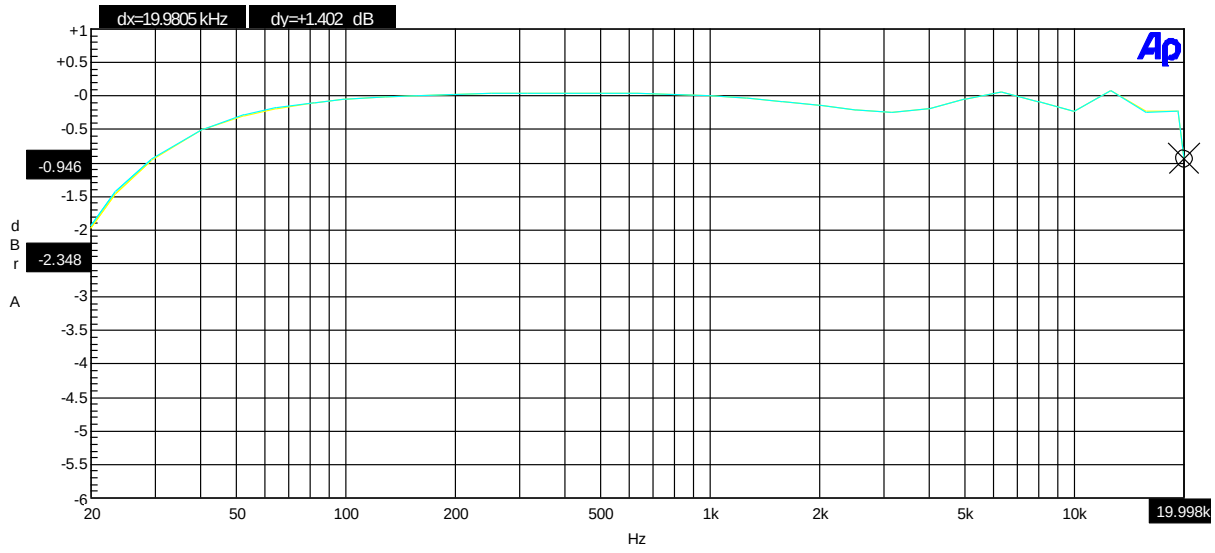
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-0.346 dBr A	*-4.563 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-0.346 dBr A	-4.564 dBr A

Vista-Frequency Response-M44k.at27

10.2 Digital Playback for Line Output Frequency (32 Ohm Loading)

10.2.1 Frequency Response 48Ks/Sec (32 Ohm Loading)

Audio Precision 08/09/06 16:30:39

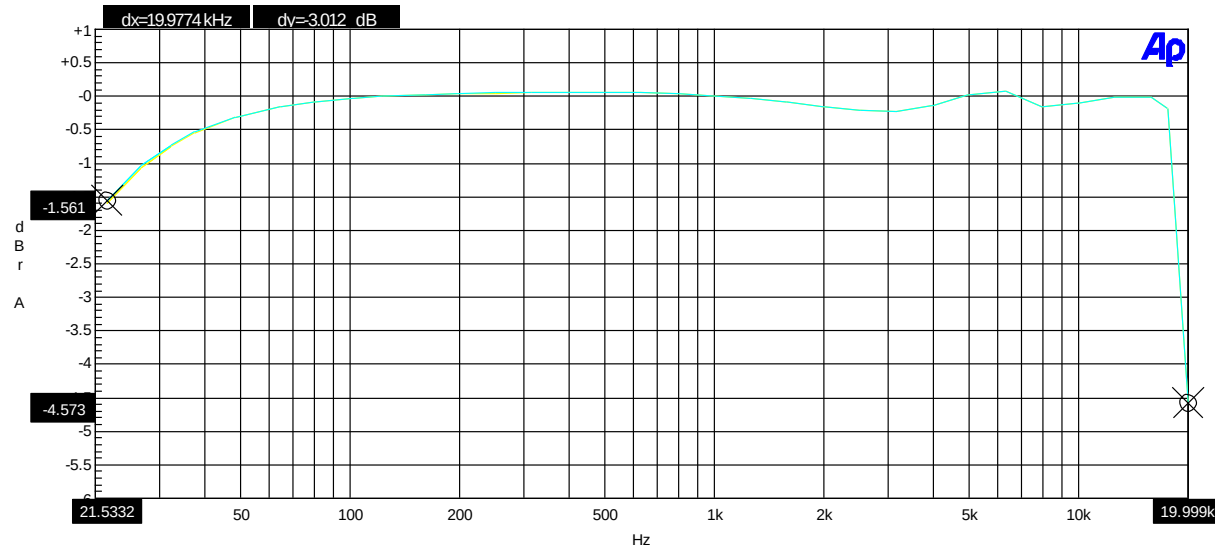


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-2.348 dBr A	*-0.946 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-2.387 dBr A	-0.946 dBr A

Vista-Frequency Response-M48k.at27

10.2.2 Frequency Response 44.1Ks/Sec (32 Ohm Loading)

Audio Precision 08/09/06 16:39:28



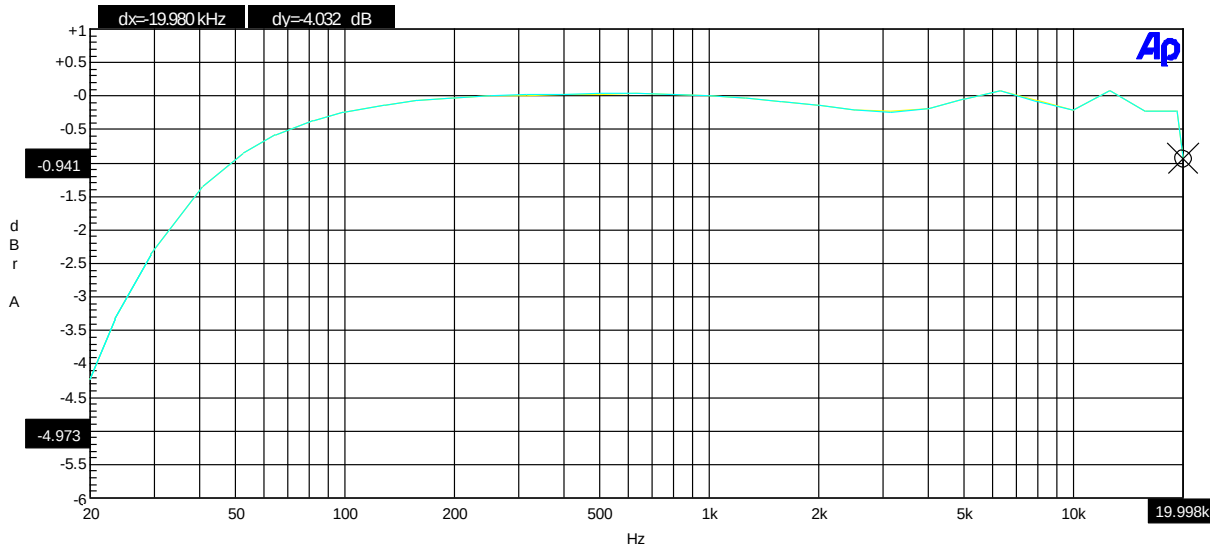
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-1.561 dBr A	*-4.573 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-1.590 dBr A	-4.572 dBr A

Vista-Frequency Response-M44k.at27

10.3 Digital Playback for Line Output Frequency (16 Ohm Loading)

10.3.1 Frequency Response 48Ks/Sec (16 Ohm Loading)

Audio Precision 08/09/06 16:56:01

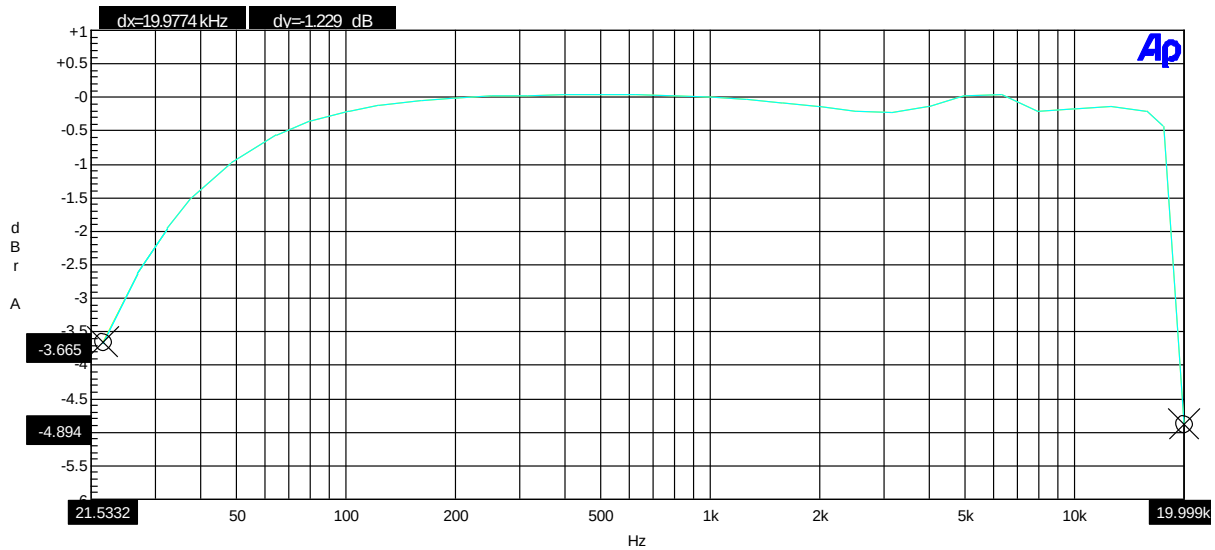


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-0.941 dBr A	*-4.973 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-0.940 dBr A	-4.962 dBr A

Vista-Frequency Response-M48k.at27

10.3.2 Frequency Response 44.1Ks/Sec (16 Ohm Loading)

Audio Precision 08/09/06 17:03:08

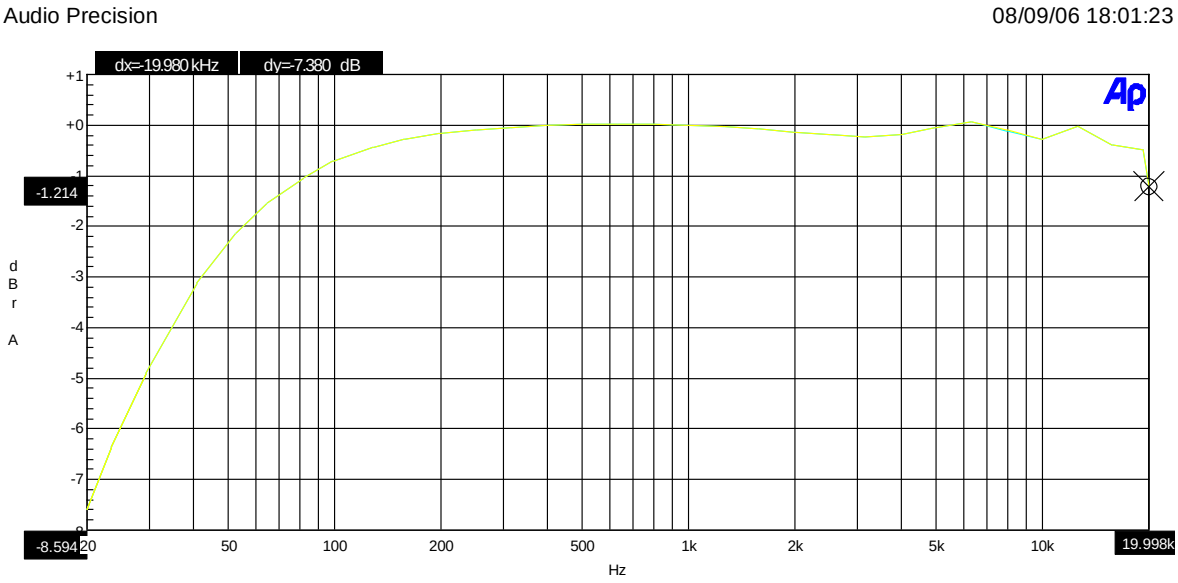


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-3.665 dBr A	*-4.894 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-3.657 dBr A	-4.893 dBr A

Vista-Frequency Response-M44k.at27

10.4 Digital Playback for Line Output Frequency (8 Ohm Loading)

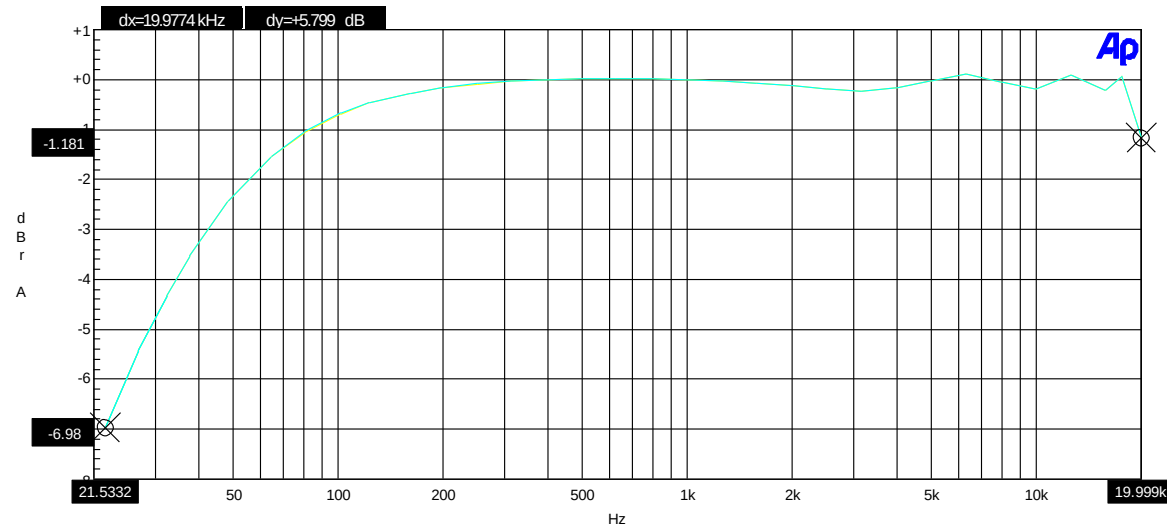
10.4.1 Frequency Response 48Ks/Sec (8 Ohm Loading)



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		-1.216 dBr A	-8.597 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		*-1.214 dBr A	*-8.594 dBr A

Vista-Frequency Response-M48k.at27

10.4.2 Frequency Response 44.1Ks/Sec (8 Ohm Loading)

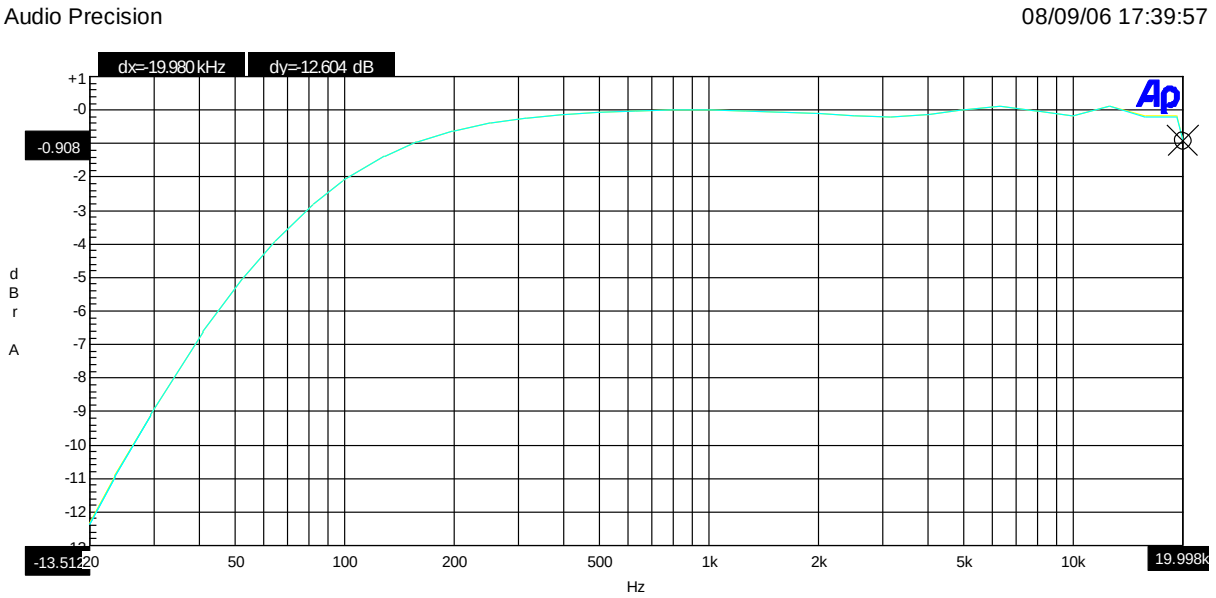


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-6.980 dBr A	*-1.181 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-6.977 dBr A	-1.179 dBr A

Vista-Frequency Response-M44k.at27

10.5 Digital Playback for Line Output Frequency (4 Ohm Loading)

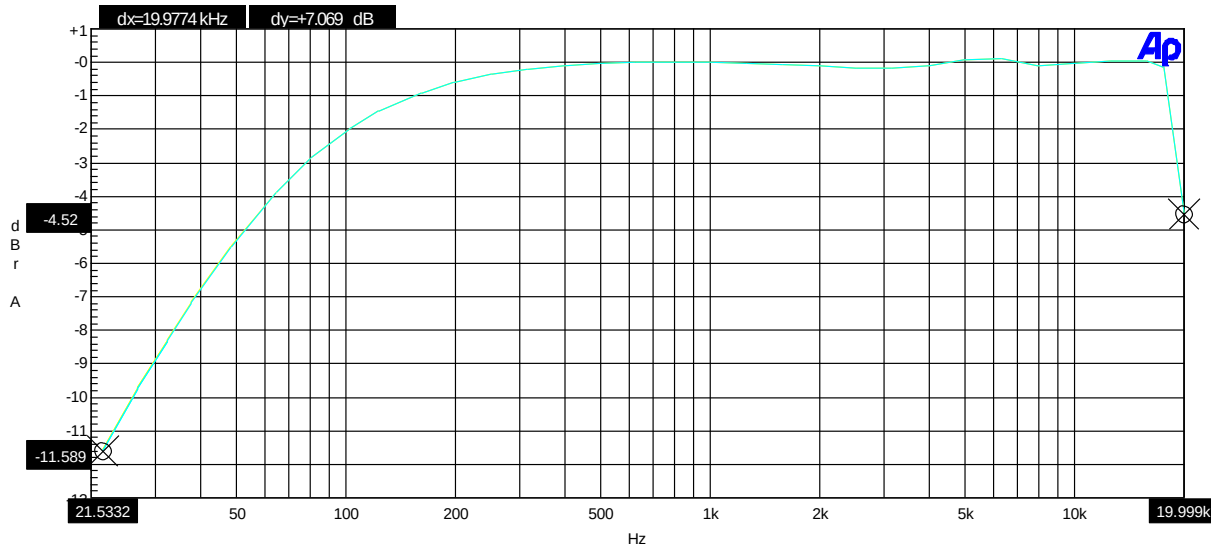
10.5.1 Frequency Response 48Ks/Sec (4 Ohm Loading)



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-0.908 dBr A	*-13.512 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-0.904 dBr A	-13.481 dBr A

Vista-Frequency Response-M48k.at27

10.5.2 Frequency Response 44.1Ks/Sec (4 Ohm Loading)

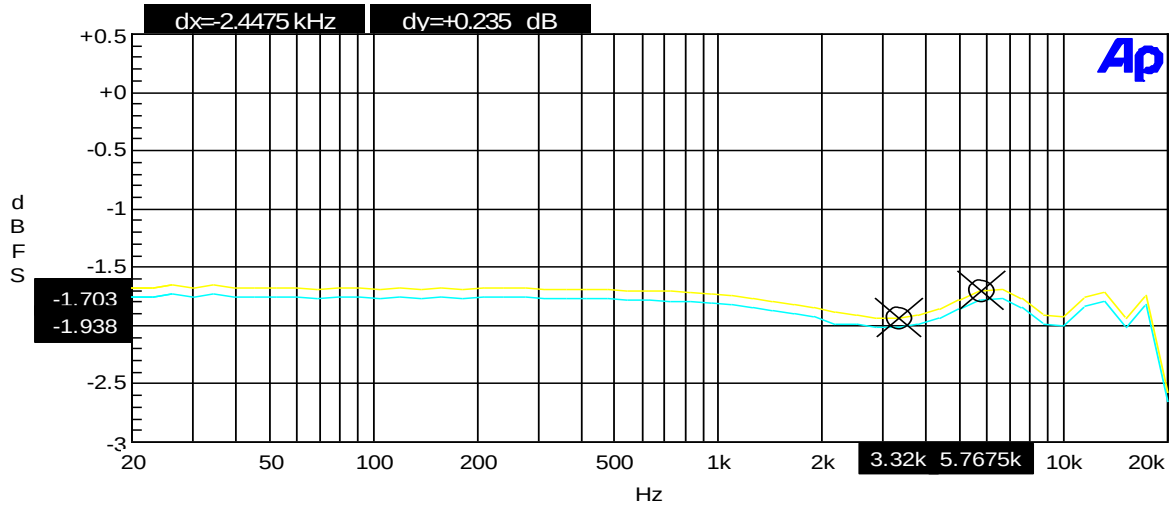


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-11.589 dBr A	*-4.520 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-11.559 dBr A	-4.516 dBr A

Vista-Frequency Response-M44k.at27

10.6 ADC (Line In) Frequency Response

Audio Precision A-D FREQUENCY RESPONSE 08/11/06 11:32:41

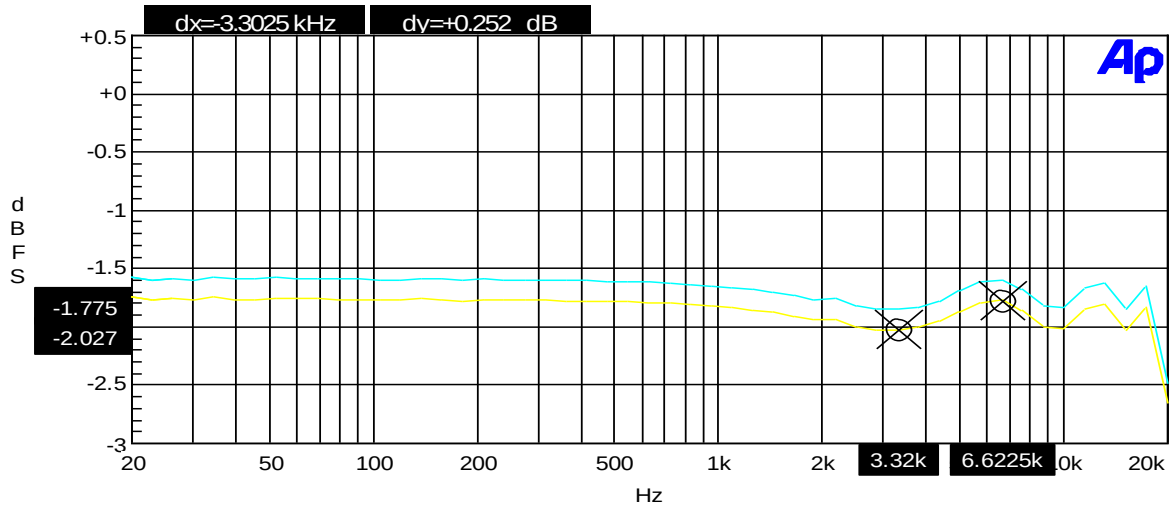


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1
1	1	Yellow	Solid	1	DSP Anlr.Level A	Left		*-1.703 dBFS
1	2	Cyan	Solid	1	DSP Anlr.Level B	Left		-1.782 dBFS

Vista-A-D Frequency Response.at2c

10.7 ADC (Mic In) Frequency Response

Audio Precision A-D FREQUENCY RESPONSE 08/11/06 11:35:01



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1
1	1	Yellow	Solid	1	DSP Anlr.Level A	Left		*-1.775 dBFS
1	2	Cyan	Solid	1	DSP Anlr.Level B	Left		-1.600 dBFS

Vista-A-D Frequency Response.at2c

Reference

- USB-IF-, USB specification 1.1/2.0-, and USB audio device class specification 1.0-compliant

—End of Datasheet—

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