CM6502 / CM6502B

USB Audio Sound Chip

DESCRIPTION

CM6502 / CM6502B are a USB 2.0 audio chip builds in 8051 for flexible applications. With internal 2-channel ADC and DAC and S/PDIF interface makes it suits for Headset, Docking, Speaker and Mic applications. The internal 8051 can be also developed to a lot of different applications, such as Lync device, iDevice docking or even Android Phone or Tablet/Slate docking device.

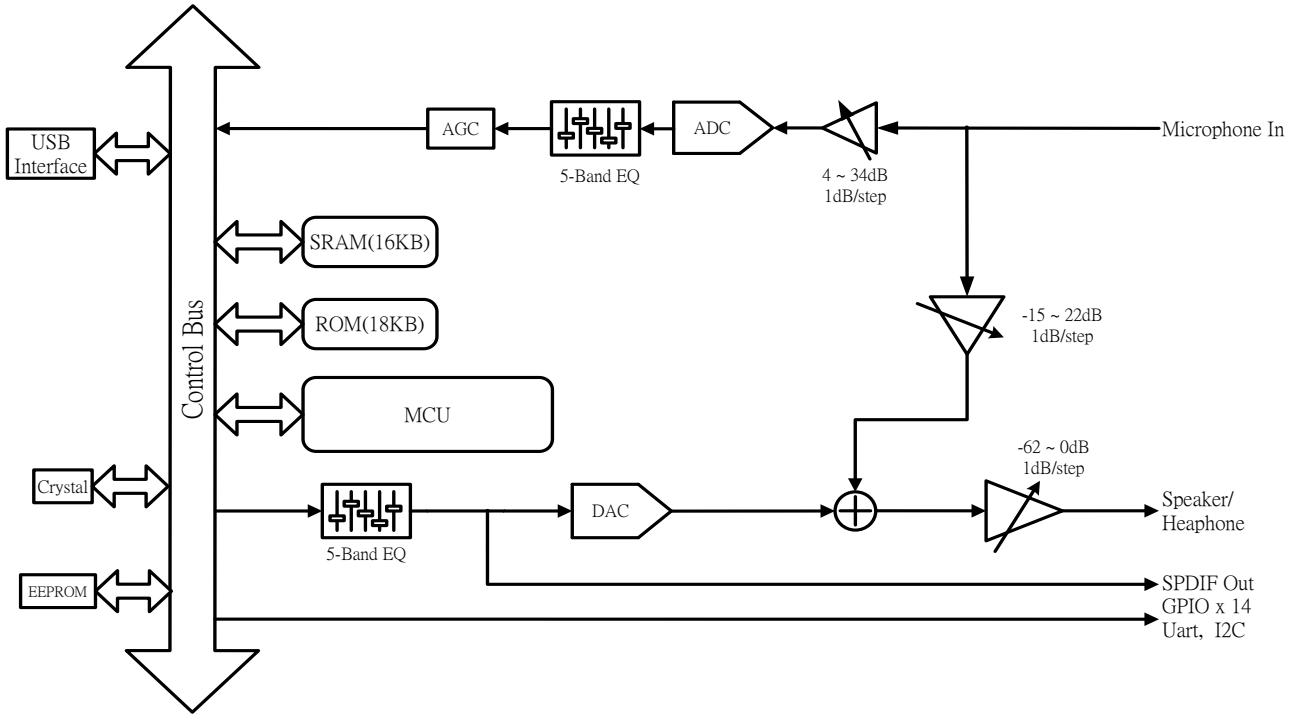
CM6502 / CM6502B is compatible with USB audio Class 1.0, thus it can plug & play without additional software installation on the major operation systems. The internal DAC/ADC and S/PDIF out interface support 48K/44.1KHz sampling rate and 16bit resolution.

CM6502 / CM6502B integrates the Equalizer on both playback and recording paths to compensate the frequency response of mic and headphone.

FEATURES

- USB 2.0 full-speed compliant
- USB Audio Class 1.0 compliant
- USB Human Interface Device (HID) Class 1.1 compliant
- 2 channel DAC for audio output interface
- 2 channel ADC for audio input interface
- Support Digital Mic interface
- Build in 48K/44.1KHz and 16bit S/PDIF transmitter
- Build in Equalizer on both playback and recording paths
- Build in AGC on recording path
- Support USB suspend/resume/reset functions
- Support control, interrupt, bulk, and isochronous data transfers
- Embedded 1T 8051
- Master I2C control interface for external audio devices or EEPROM access
- 14 GPIO pins

BLOCK DIAGRAM



Release Note

Revision	Date	Description
0.1	2011/08/15	-First release of preliminary technical information
0.2	2011/10/18	-modify some wrong wordings
0.9	2011/10/31	-Separate CM6500/CM6502 / CM6502B datasheet -update pin description
0.91	2011/11/21	-add audio quality
0.92	2012/02/23	-update GPIO default status
0.93	2012/04/02	-modify PDSW as DO -add more information in chapter 6,7
0.94	2012/04/20	-modify some wording
0.95	2012/06/21	-modify GPIO pin number, all GPIO number subtract 1
		-add microphone channel separation data -add gain value in the block diagram -add gain range and capability for playback, recording and A-A stream
1.00	2012/10/19	-Formal Release
1.01	2013/01/25	-Remove S/PDIF 32K sample rate support
1.02	2013/03/01	-add CM6502B support

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1 Description and Overview

CM6502 / CM6502B are a USB 2.0 audio chip builds in 8051 for flexible applications. With internal 2-channel ADC and DAC interface makes it suits for Headset, Docking, Speaker and Mic applications. The internal 8051 can be also developed to a lot of different applications, such as Lync device, iDevice docking or even Android Phone or Tablet/Slate docking device. CM6502 / CM6502B is compatible with USB audio Class 1.0, thus it can plug & play without additional software installation on the major operation systems. The internal DAC/ADC and S/PDIF out interface support 48 K/44.1KHz sampling rate and 16 bit resolution. CM6502 / CM6502B integrate the Equalizer on both playback and recording paths to compensate the frequency response of microphone and headphone.

2 Features

USB Compliance

- USB 2.0 full-speed compliant
- USB Audio Class 1.0 compliant
- USB Human Interface Device (HID) Class 1.1 compliant
- Supports USB suspend/resume/reset functions
- Supports control, interrupt, bulk, and isochronous data transfers

Audio I/O

- Playback Stream:
  - Stereo DAC
    - Sample Rates: 8K/11.025K/16K/22.05K/32K/44.1K/48K
    - Supports Bit Length: 16 bit
    - Gain Range is -62 ~ 0dB, 1dB/step
  - Builds in S/PDIF transmitter
    - Sample Rates: 44.1K/48K
    - Supports Bit Length: 16 bits
- Recording Stream:
  - Stereo ADC
    - Sample Rates: 8K/11.025K/16K/22.05K/32K/44.1K/48K
    - Supports Bit Length: 16 bits
    - Microphone gain range is 4 ~ 34dB, 1dB/step by default, the range can be programmed by external EEPROM from -18 ~ 49dB.

- A-A Stream:
  - Stereo A-A path playback
    - Can be programmed by external EEPROM to mono microphone input and duplicate to stereo playback
    - The Microphone playback gain range is -15 ~ 22dB, 1dB/step by default, and can be programmed by external eeprom from -14 ~ 32dB.

Integrated 8051 Micro-processor

- Embedded 8051 micro-processor to handle the comment/protocol transactions
- Connects to an external EEPROM memory for firmware codes
- HID interrupts can be implemented via firmware codes
- Provides maximum HW configuration flexibility with firmware code upgrade
- VID/PID/Product String can be customized via firmware code programming

Control Interface

- Master I2C control interface for external audio devices or EEPROM access
- Max. 14 GPIO pins can be configured via firmware programming
- GPIOs are configured as HID key and LED indicators

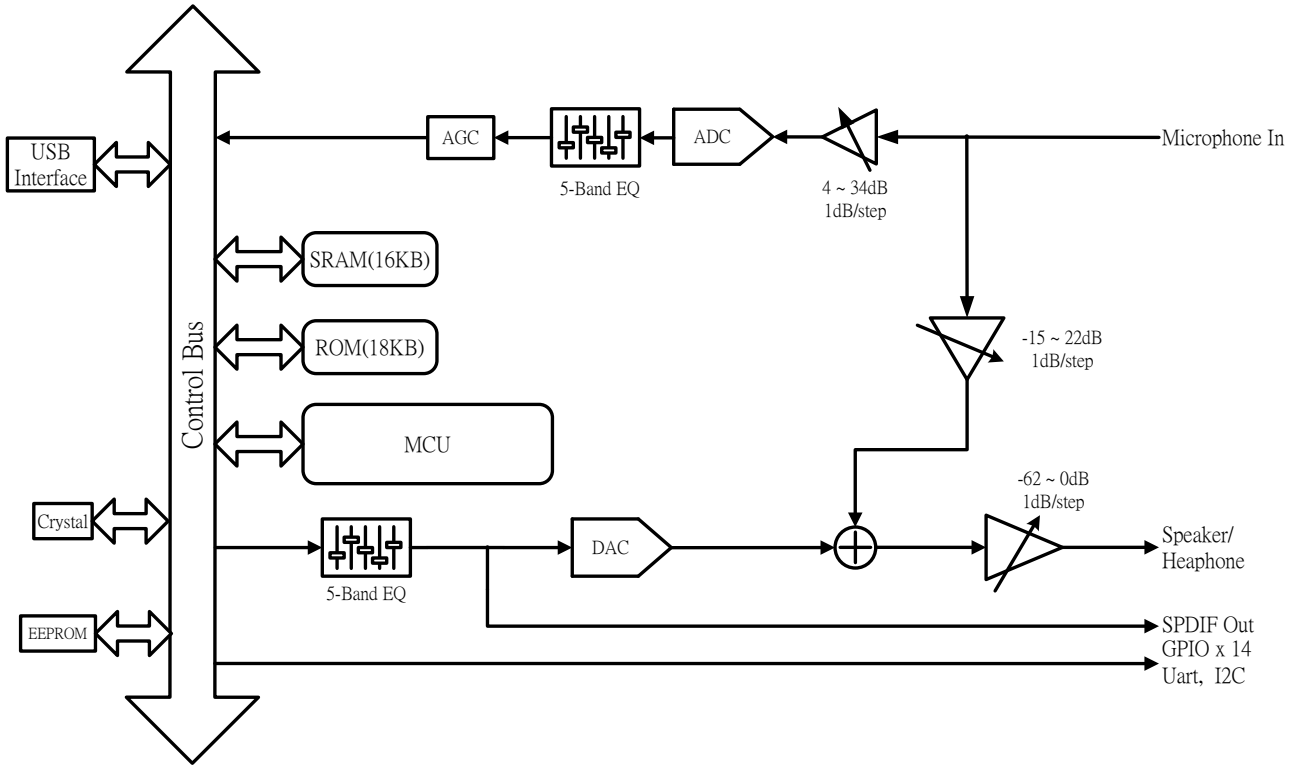
General

- Hardware pins for mode configuration including Headset, Speaker, Docking and Mic
- Hardware pin for A-A path enable/disable
- Only single 12MHz crystal input is required (embedded PLL function)
- Single 5V power supply (embedded 5V to 1.8V regulator for digital core, 5V to 3.3V regulator for digital IO, 5V to 3.5V regulator for analog codec)
- 3.3V digital I/O pads with 5V tolerance
- Industrial standard LQFP-48 package (7x7mm)

3 Applications

- USB Headset
- Lync Headset
- Notebook/Netbook Docking
- Android Phone/Slate Docking
- USB Speaker
- USB DAC
- USB Mic

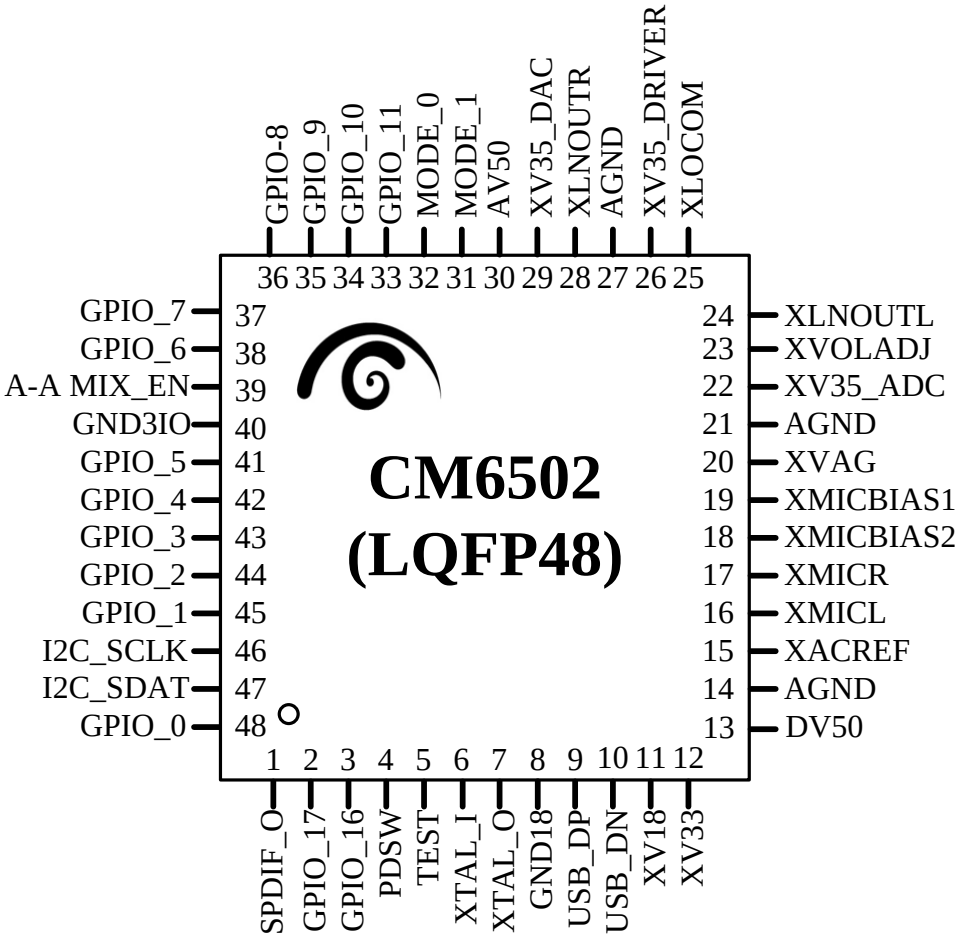
4 Block Diagram

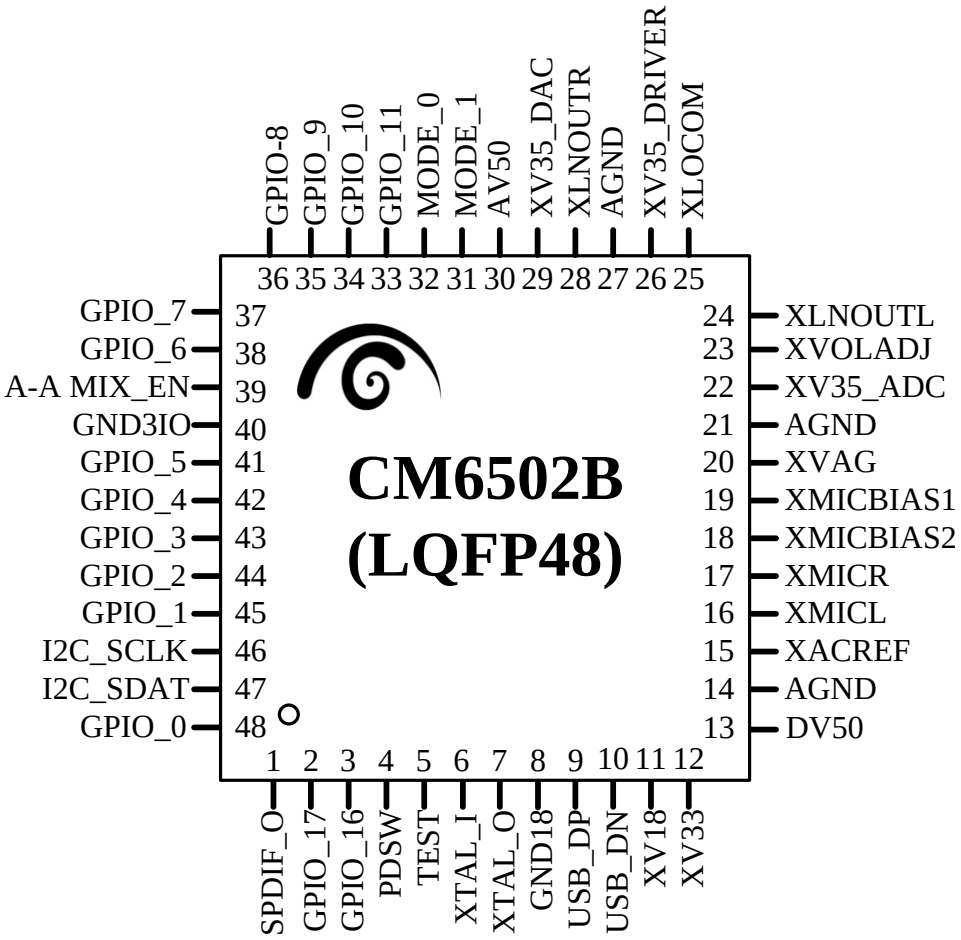


CM6502 / CM6502B Functional Block Diagram

5 Pin Assignment

5.1 Pin-Out Diagram





Pin Description

Pin #	Symbol	I/O	Description
Clock			
7	XTAL_O	AO	12MHz crystal oscillator output
6	XTAL_I	AI	12MHz crystal oscillator input
USB2.0 BUS Interface			
10	USB_DN	AIO	USB 2.0 data negative (USB D- signal)
9	USB_DP	AIO	USB 2.0 data positive (USB D+ signal)
Power/Ground			
13	DV50	PWR	5V digital power for 5/3.3 regulator
12	XV33	AO	Regulator 3.3V output, drive capacity 150mA for USB and digital I/O
40	GND3IO	GND	Digital Ground
11	XV18	AO	Regulator 1.8V output, drive capacity 100mA for digital core
8	GND18	GND	Digital Ground
30	AV50	PWR	5V analog power for 5/3.5 regulator
14	AGND	GND	Analog Ground
29	XV35_DAC	AO	Regulator 3.5V output, drive capacity 100mA for analog and amplifier
22	XV35_ADC	PWR	3.5V power for ADC and Voltage and Current Reference
21	AGND	GND	Analog Ground
26	XV35_DRIVER	PWR	3.5V power for Driver
27	AGND	GND	Analog Ground
Audio Interface			
15	XACREF	AO	Input signal common reference
16	XMICL	AI	Mic in left channel
17	XMICR	AI	Mic in right channel
18	XMICBIAS2	AO	Microphone bias
19	XMICBIAS1	AO	Microphone bias
20	XVAG	AO	Voltage reference cap filter
23	XVOLADJ	AI	Analog control voltage input for playback volume control
24	XLNOUTL	AO	Line out left channel
25	XLOCOM	AO	Line out common reference for cap-less connection
28	XLNOUTR	AO	Line out right channel
S/PDIF I/O			
1	SPDIF_O	DO	S/PDIF transmitter Programmable 3.3V output buffer

GPIO			
48	GPIO_0	DIO	General purpose input/output (default Volume Up). Programmable 3.3V/5V tolerance bidirectional buffer, pull-up
45	GPIO_1	DIO	General purpose input/output (default Volume Down). Programmable 3.3V/5V tolerance bidirectional buffer, pull-up
44	GPIO_2	DIO	General purpose input/output (default Play Mute). Programmable 3.3V/5V tolerance bidirectional buffer, pull-up
43	GPIO_3	DIO	General purpose input/output (default Rec Mute). Programmable 3.3V/5V tolerance bidirectional buffer, pull-up
42	GPIO_4	DIO	General purpose input/output (default LED Live, 2K Hz). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
41	GPIO_5	DIO	General purpose input/output (default LED Play Mute). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
38	GPIO_6	DIO	General purpose input/output (default LED Rec Mute, 1K Hz). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
37	GPIO_7	DIO	General purpose input/output (default EQ Mode Select0). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
36	GPIO_8	DIO	General purpose input/output (default EQ Mode Selet1). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
			GPIO[8:7]=0,0: Normal GPIO[8:7]=1,0: Communication GPIO[8:7]=0,1: Gaming GPIO[8:7]=1,1: Movie
35	GPIO_9	DIO	General purpose input/output (default Rec Clip Indicator). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
34	GPIO_10	DIO	General purpose input/output (default Wave Volume Up). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down Digital Mic clock, enable through external eeprom
33	GPIO_11	DIO	General purpose input/output (default Wave Volume Down). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down Digital Mic data, enable through external eeprom
3	GPIO_16	DIO	General purpose input/output (default MCU_RXD). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
2	GPIO_17	DIO	General purpose input/output (default MCU_TRX). Programmable 3.3V/5V tolerance bidirectional buffer, pull-down
2-Wire Master Serial Bus (I2C)			
47	I2C_SDAT	DIO	2-wire slave serial data Programmable 3.3V/5V tolerant bidirectional buffer, pull-down
46	I2C_SCLK	DIO	2-wire slave serial clock Programmable 3.3V/5V tolerant bidirectional buffer, pull-down
Miscellaneous			
4	PDSW	DO	Self Power used, 1:self power, 0:bus power Programmable 3.3V input buffer, Schmitt trigger, Pull-down
5	TEST	DI	For test
39	A-A MIX_EN	DI	0: A-A path disable 1: A-A path enable
32	MODE_0	DI	MODE_1= 0, MODE_0= 0 for Headset MODE_1= 0, MODE_0= 1 for Microphone MODE_1= 1, MODE_0= 0 for Speaker MODE_1= 1, MODE_0= 1 for Docking
31	MODE_1	DI	

6 USB Audio Topology

CM6502 / CM6502B support 4 types of topology by default. They are Headset, Docking, Speaker, Mic.

Different topology can be selected by pin Mode_0 and Mode_1. The combination as below.

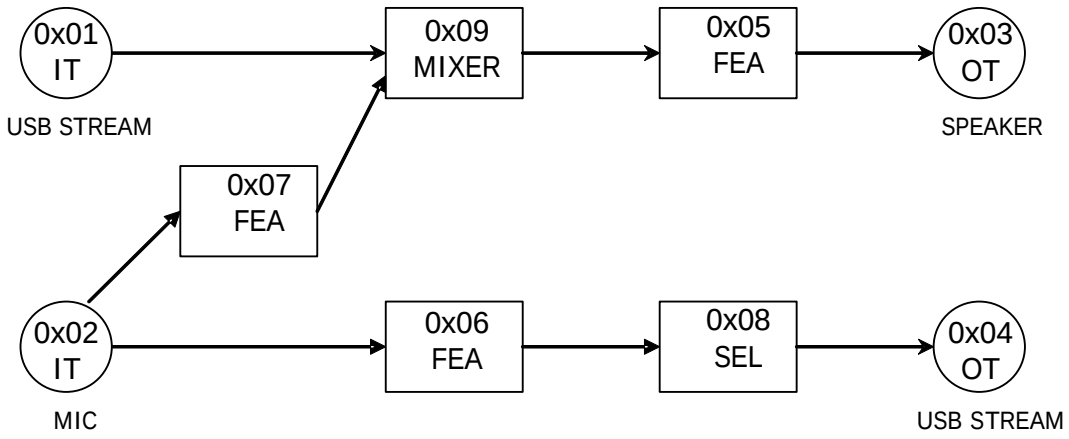
MODE_1= 0, MODE_0= 0 for Headset

MODE_1= 0, MODE_0= 1 for Microphone

MODE_1= 1, MODE_0= 0 for Speaker

MODE_1= 1, MODE_0= 1 for Docking

6.1 Headset Topology



Device Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	12	Descriptor length
1	bDescriptorType	1	01	Device Descriptor
2	bcdUSB	2	0110	USB 1.1 compliant
4	bDeviceClass	1	00	Device class specified by interface
5	bDeviceSubClass	1	00	Device subclass specified by interface
6	bDeviceProtocol	1	00	Device protocol specified by interface
7	bMaxPacketSize0	1	10	Endpoint zero packet size
8	idVendor	2	0D8C	Vendor ID
10	idProduct	2	0178~017F	Product ID
12	bcdDevice	2	0000	Device release number
14	iManufacturer	1	01	Index of string descriptor describing manufacturer
15	iProduct	1	02	Index of string descriptor describing product
16	iSerialNumber	1	00	Index of string descriptor describing serial number
17	bNumConfigurations	1	01	Number of configuration

Configuration Descriptor

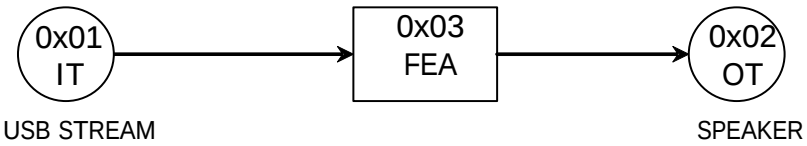
Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length

1	bDescriptorType	1	02	Configuration Descriptor
2	wTotalLength	2	011D	Total length of data returned for this configuration: 285 Bytes
4	bNumInterfaces	1	04	Number of interfaces supported by this Configuration: 00: Control 01: ISO-Out 02: ISO-In 03: INT-In (HID)
5	bConfigurationValue	1	01	Configuration value
6	iConfiguration	1	00	Index of string descriptor describing this configuration
7	bmAttributes	1	80	Attributes(Bus Powered)
8	bMaxPower	1	32	Maximum power consumption from bus = 100mA: 8'h32 (50x2 mA) (PWRSEL_2 = 1)

Audio Control Interface 0 Descriptor 0

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	04	Interface Descriptor
2	bInterfaceNumber	1	00	Interface number
3	bAlternateSetting	1	00	Alternate interface
4	bNumEndpoints	1	00	Number of endpoint used by this interface
5	bInterfaceClass	1	01	Audio Interface Class
6	bInterfaceSubClass	1	01	Subclass code: AUDIO_CONTROL
7	bInterfaceProtocol	1	00	Protocol code
8	iInterface	1	00	Index of string descriptor describing this interface

6.2 Speaker Topology



Device Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	12	Descriptor length
1	bDescriptorType	1	01	Device Descriptor
2	bcdUSB	2	0110	USB 1.1 compliant
4	bDeviceClass	1	00	Device class specified by interface
5	bDeviceSubClass	1	00	Device subclass specified by interface
6	bDeviceProtocol	1	00	Device protocol specified by interface
7	bMaxPacketSize0	1	10	Endpoint zero packet size
8	idVendor	2	0D8C	Vendor ID
10	idProduct	2	0180~018F	Product ID
12	bcdDevice	2	0000	Device release number
14	iManufacturer	1	01	Index of string descriptor describing manufacturer
15	iProduct	1	02	Index of string descriptor describing product
16	iSerialNumber	1	00	Index of string descriptor describing serial number

17	bNumConfigurations	1	01	Number of configuration

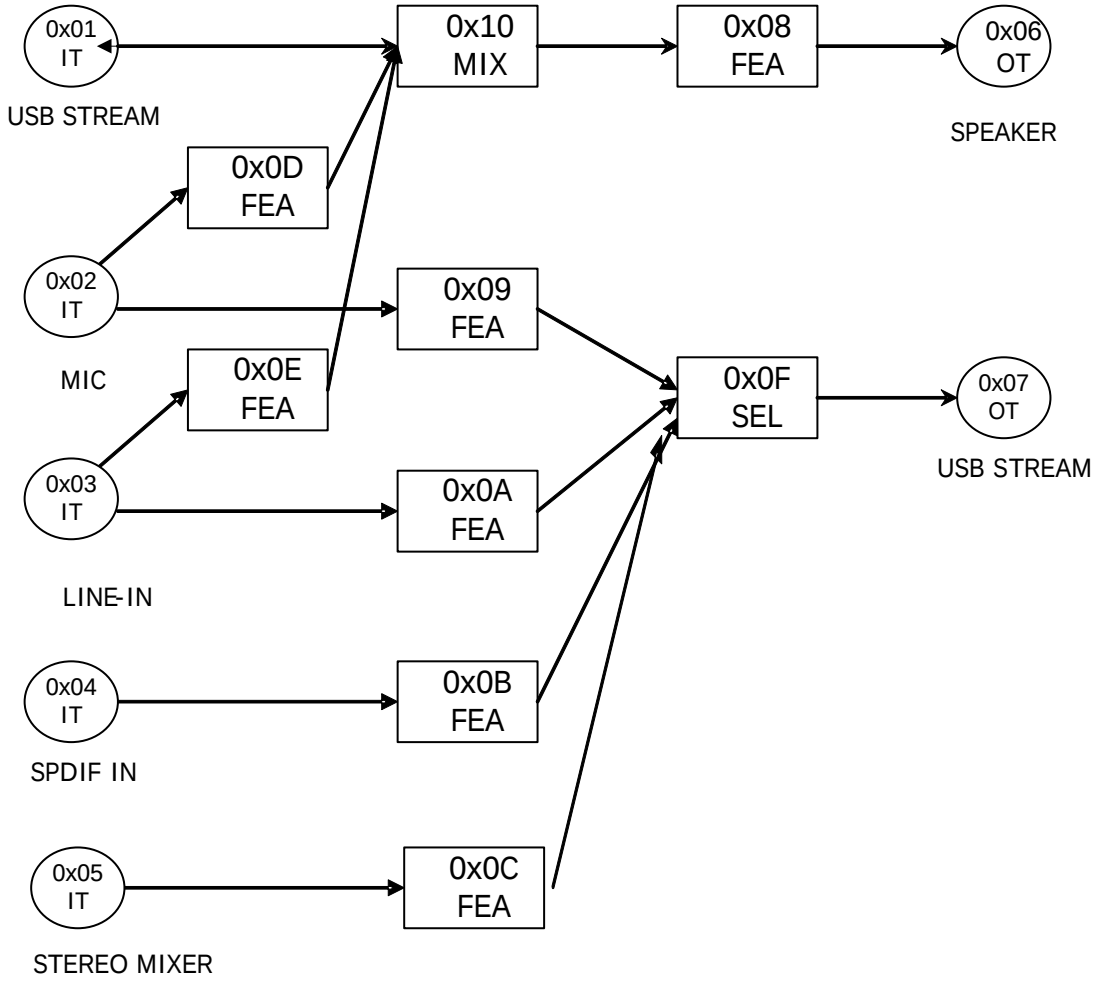
Configuration Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	02	Configuration Descriptor
2	wTotalLength	2	0099	Total length of data returned for this configuration: 153 Bytes
4	bNumInterfaces	1	03	Number of interfaces supported by this Configuration: 00: Control 01: ISO-Out 02: INT-In (HID)
5	bConfigurationValue	1	01	Configuration value
6	iConfiguration	1	00	Index of string descriptor describing this configuration
7	bmAttributes	1	80	Attributes(Bus Powered)
8	bMaxPower	1	32	Maximum power consumption from bus = 100mA: 8'h32 (50x2 mA) (PWRSEL_2 = 1)

Audio Control Interface 0 Descriptor 0

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	04	Interface Descriptor
2	bInterfaceNumber	1	00	Interface number
3	bAlternateSetting	1	00	Alternate interface
4	bNumEndpoints	1	00	Number of endpoint used by this interface
5	bInterfaceClass	1	01	Audio Interface Class
6	bInterfaceSubClass	1	01	Subclass code: AUDIO_CONTROL
7	bInterfaceProtocol	1	00	Protocol code
8	iInterface	1	00	Index of string descriptor describing this interface

6.3 Docking Topology



Device Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	12	Descriptor length
1	bDescriptorType	1	01	Device Descriptor
2	bcdUSB	2	0110	USB 1.1 compliant
4	bDeviceClass	1	00	Device class specified by interface
5	bDeviceSubClass	1	00	Device subclass specified by interface
6	bDeviceProtocol	1	00	Device protocol specified by interface
7	bMaxPacketSize0	1	10	Endpoint zero packet size
8	idVendor	2	0D8C	Vendor ID
10	idProduct	2	01A8~01AF	Product ID
12	bcdDevice	2	0000	Device release number
14	iManufacturer	1	01	Index of string descriptor describing manufacturer
15	iProduct	1	02	Index of string descriptor describing product
16	iSerialNumber	1	00	Index of string descriptor describing serial number
17	bNumConfigurations	1	01	Number of configuration

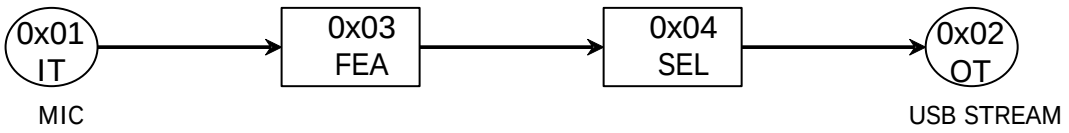
Configuration Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	02	Configuration Descriptor
2	wTotalLength	2	016D	Total length of data returned for this configuration: 365 Bytes
4	bNumInterfaces	1	04	Number of interfaces supported by this Configuration: 00: Control 01: ISO-Out 02: ISO-In 03: HID
5	bConfigurationValue	1	01	Configuration value
6	iConfiguration	1	00	Index of string descriptor describing this configuration
7	bmAttributes	1	80	Attributes(Bus Powered)
8	bMaxPower	1	32	Maximum power consumption from bus = 100mA: 8'h32 (50x2 mA) (PWRSEL_2 = 1)

Audio Control Interface 0 Descriptor 0

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	04	Interface Descriptor
2	bInterfaceNumber	1	00	Interface number
3	bAlternateSetting	1	00	Alternate interface
4	bNumEndpoints	1	00	Number of endpoint used by this interface
5	bInterfaceClass	1	01	Audio Interface Class
6	bInterfaceSubClass	1	01	Subclass code: AUDIO_CONTROL
7	bInterfaceProtocol	1	00	Protocol code
8	iInterface	1	00	Index of string descriptor describing this interface

6.4 Microphone (Stereo) Topology



Device Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	12	Descriptor length
1	bDescriptorType	1	01	Device Descriptor
2	bcdUSB	2	0110	USB 1.1 compliant
4	bDeviceClass	1	00	Device class specified by interface
5	bDeviceSubClass	1	00	Device subclass specified by interface
6	bDeviceProtocol	1	00	Device protocol specified by interface
7	bMaxPacketSize0	1	10	Endpoint zero packet size
8	idVendor	2	0D8C	Vendor ID
10	idProduct	2	0190~019F	Product ID
12	bcdDevice	2	0000	Device release number

14	iManufacturer	1	01	Index of string descriptor describing manufacturer
15	iProduct	1	02	Index of string descriptor describing product
16	iSerialNumber	1	00	Index of string descriptor describing serial number
17	bNumConfigurations	1	01	Number of configuration

Configuration Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	02	Configuration Descriptor
2	wTotalLength	2	00A0	Total length of data returned for this configuration: 160 Bytes
4	bNumInterfaces	1	03	Number of interfaces supported by this Configuration: 00: Control 01: ISO-In 03: HID
5	bConfigurationValue	1	01	Configuration value
6	iConfiguration	1	00	Index of string descriptor describing this configuration
7	bmAttributes	1	80	Attributes(Bus Powered)
8	bMaxPower	1	32	Maximum power consumption from bus = 100mA: 8'h32 (50x2 mA) (PWRSEL_2 = 1)

Audio Control Interface 0 Descriptor 0

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	04	Interface Descriptor
2	bInterfaceNumber	1	00	Interface number
3	bAlternateSetting	1	00	Alternate interface
4	bNumEndpoints	1	00	Number of endpoint used by this interface
5	bInterfaceClass	1	01	Audio Interface Class
6	bInterfaceSubClass	1	01	Subclass code: AUDIO_CONTROL
7	bInterfaceProtocol	1	00	Protocol code
8	iInterface	1	00	Index of string descriptor describing this interface

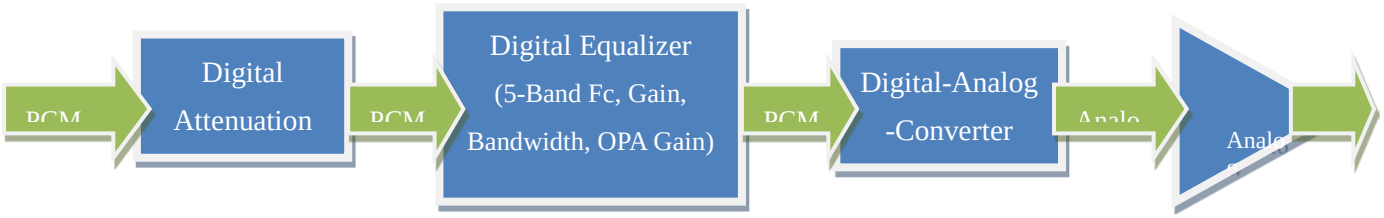
7 Function Description

7.1 Playback Equalizer

7.1.1 5-band Equalizer

CM6502 / CM6502B has integrated 5-band hardware digital equalizer (EQ) engine inside the chips to fulfill various application usages. It provides up-to-4 preset modes on customer's product design for different user scenarios including default/music, movies, Gaming and communication modes. Customers could also change the gain parameters for each of the preset application EQ mode via EEPROM coding. In addition, the EQ engine could also be utilized for compensating and fine-tuning the headphone driver for Sound Pressure Level (SPL) performance to a specific preference. In this case, customers could fully customize all EQ coefficients (center frequency, gain values, and bandwidth) to one optimized frequency response curve and setting in terms of the headphone driver and housing's acoustics characteristics, also via

EEPROM programming.



The EQ engine contains 5 frequency bands (Fc) of digital filters to conduct transfer functions of the frequency response over the audio band. It allows maximum +-12dB digital gain (Gain) for each band with 0.5dB adjustment per step. Each filter will have its bandwidth (BW) factor between 0 and 1.0.

Fc: Center Frequency, F1~F5, 20<Fc<20K (Hz)
Gain: Digital Frequency Gain, -12dB <= Gain <=+12dB, 0.5dB/step
BW: Filter Bandwidth Factor, 0<BW<1
OPA Gain: Analog Gain Compensation setting for each equalizer mode

The EQ engine already provides 4 preset modes/settings based on the same preset F1~F5 center frequencies and OPA gain:

F1 (Bass)= 100Hz
F2 = 350Hz
F3 = 1KHz
F4 = 3.5KHz
F5 (Treble) = 13KHz

With the 4 preset EQ modes, customers could use EEPROM parameters to change the gain values for each band of the center frequency and hence customize the 4-preset EQ curves based on the preset center frequencies and bandwidth. Alternatively, customers could also skip the 4 preset modes and create a customized EQ curve by changing the center frequencies, gain values and even the bandwidth factors in EEPROM parameters to make the headphone sound better or meet some frequency requirements. However, in this case, the product will always use one optimized EQ setting and could not allow users to dynamically change among different preset modes. Customer could also consider reporting Treble/Bass feature unit by EEPROM to Windows UAA driver to allow end-users to adjust Bass (F1) and Treble (F5) by

themselves. Therefore there are three usage/application scenarios as the summary table below:

3 EQ Usage/Application Scenarios

No	Scenario	Gain Value	Center Frequency / Bandwidth Factor	Number of Modes	User Control Type
1	**4 Switchable Presets**	Configurable	Fixed	4	Hardware
2	**Full-Customized EQ**	Configurable	Configurable	1	N.A.
3	**Treble/Bass Feature Unit**	Configurable	Configurable	1	Software

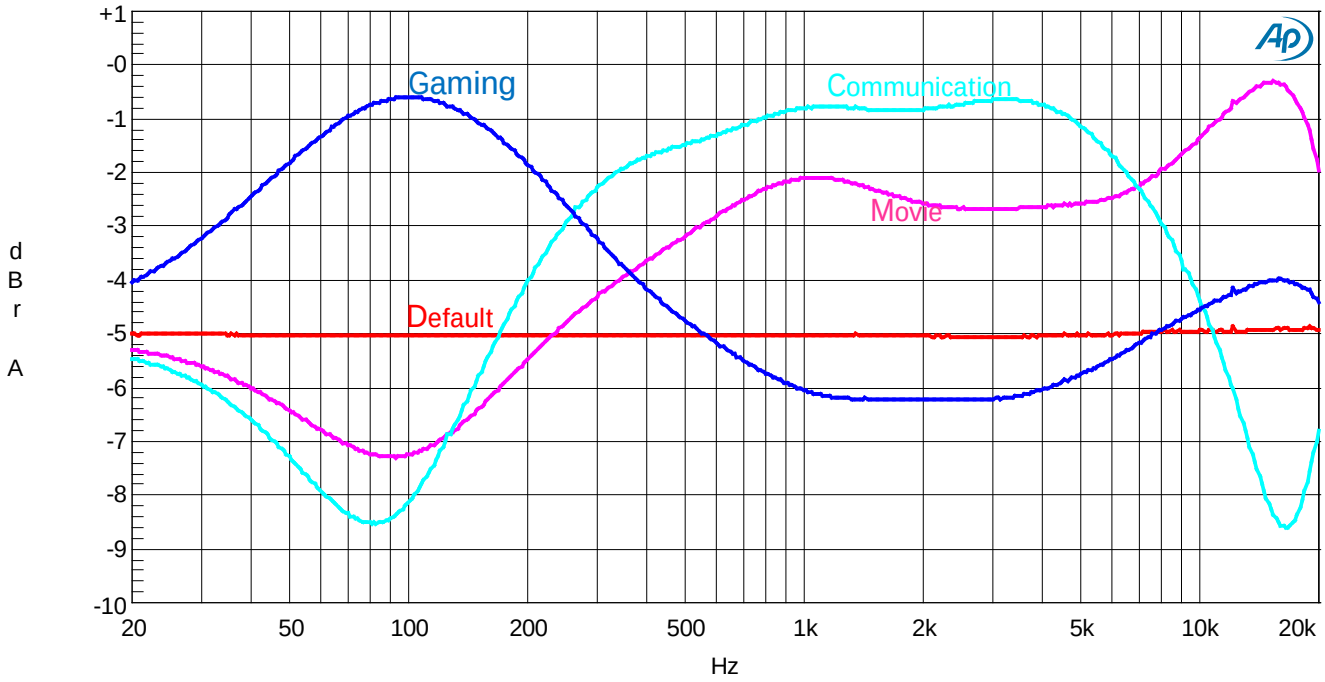
Note: Hardware user control type means end-users could select which EQ mode they're going to use by a hardware switch/button on the product; Software control means they could control the treble/bass gain values by GUI in Windows OS sound device advanced settings.

7.1.2 4 preset EQ mode

As mentioned above, EQ engine already provides 4 preset EQ modes for different user scenarios/applications. End users could use the hardware switch on the product (determined by 2 EQ configuration input pins) to dynamically change to different EQ modes. The following shows the frequency response of each mode.

Mode	GPIO8	GPIO7	Color
Default	0	0	----------
Gaming	0	1	----------
Communication	1	0	----------
Movie	1	1	----------

Audio Precision 04/20/11 15:35:35



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr.Ampl	Left	00
2	1	Magenta	Solid	2	Anlr.Ampl	Left	11
3	1	Cyan	Solid	2	Anlr.Ampl	Left	10
4	1	Blue	Solid	2	Anlr.Ampl	Left	

DA-EQ-SPDIF_In_DA_Out.at27

7.2 Recording Equalizer

CM6502 / CM6502B also provide 5-band Equalizer for the input. It can be used to compensate the frequency response of Microphone unit. Customers could fully customize all EQ coefficients (center frequency, gain values, and bandwidth) through external EEPROM.

7.3 Recording AGC

Automatic Gain Control (AGC) is an automatically controlled method to adjust with intensity of signal; AGC is closes the return circuit; that is by the negative response system too.

AGC is by way of compressing volume, Will increase Gain first when AGC is started, Set up the upper and lower limits of the signal; compress the dynamic range of sound. Usually use the occasion of AGC, should be recording and producing and speaking sound, or volume is being changed under little environment. If the lasting low voice of volume, AGC will enlarge volume, volume is sustained loudly, AGC will reduce volume.

FEATURES

Programmable AGC Parameters

Selectable Gain from –12 dB to 45 dB in 1-dB Steps

Selectable Attack, Release and Hold Times

AGC Enable/Disable Function

Limiter Enable/Disable Function

Pre-Detect Limiter Level Function

Two-Channel AGC Independent

Under input source types, to set AGC gain max/min limit

I2S rec	+12~ -16DB	0xf9= 0x1c (max)+fix gain(9db) = 0x25 0cfA= 0x00(min)
Digmic	+20 ~ -16DB	0xf9= 0x24 (max)+fix gain(9db) =0x2d 0xfA= 0x00(min)
Analog mic	+30 ~ 0DB	0xf9=0x0F+fix gain(9db) inv -> 0x39(max) 0xfA=0x2D inv -> 0x12(min)

AGC Variable Description

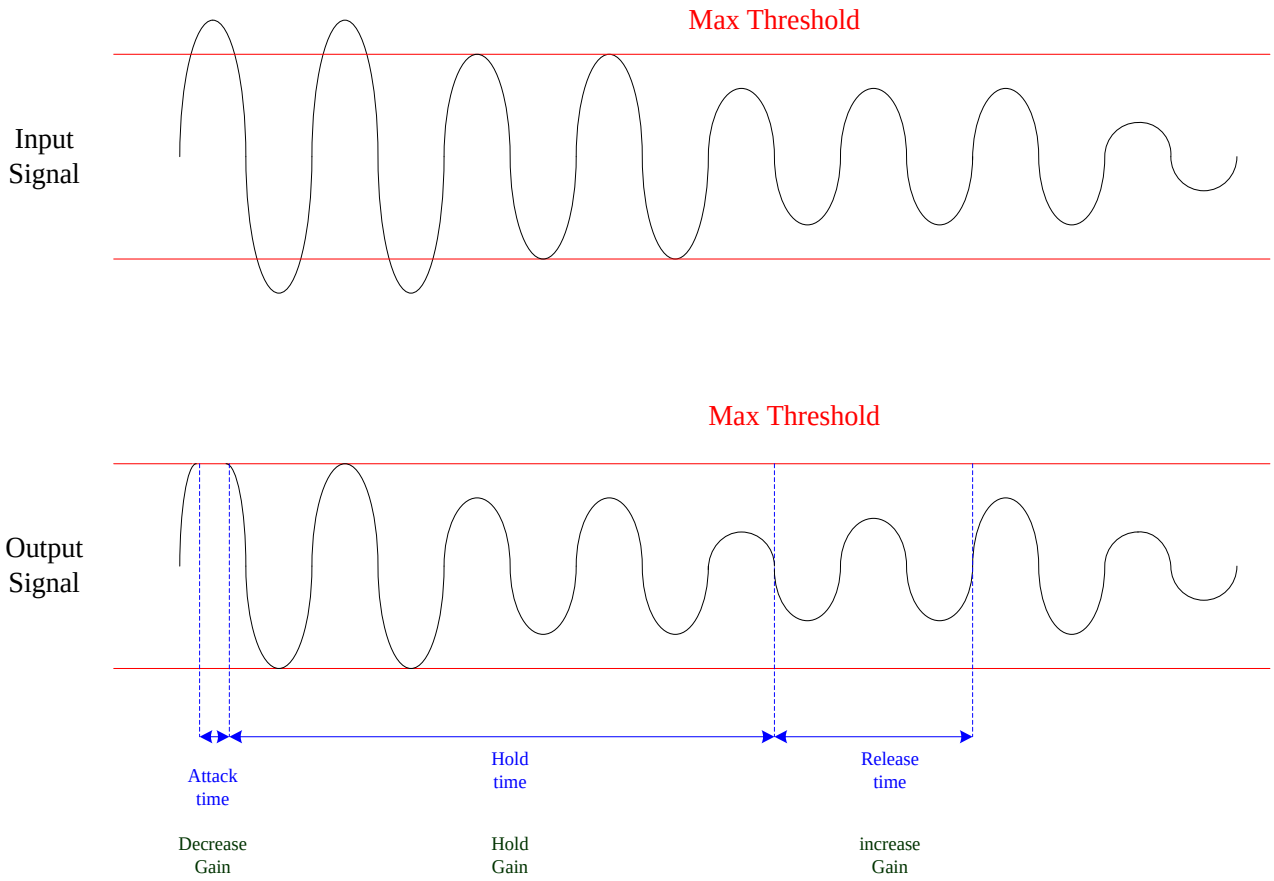
Fixed Gain: The normal gain of the device when the AGC is inactive.

Limiter Level: The value that sets the maximum allowed output amplitude.

Attack Time: The minimum time between two gain decrements.

Release Time: The minimum time between two gain increments.

Hold Time: The time it takes for the very first gain increment after the input signal amplitude decreases.



7.4 HID Function

7.4.1 HID interrupt in

Input Data Format:

byte 0	always 1 for org HID event report ID
byte1	for defined HID event, and each event occupies one bit
byte2	
byte3	start address of returned data (H-start_addr)
byte4	start address of returned data (L-start_addr)
byte5	bit7
	bit6:UART_INT
	bit5:GPI_INT
	bit4:SPIS_INT(slavemode int)
	bit3: SPIM_INT(mastermode int)
	bit2:I2CS_INT(slavemode int)
	bit1:I2CM_INT(mastermode int)
	bit0: IR_INT
byte6	read data of [start_addr]
byte7	read data of [start_addr+1]
byte8	read data of [start_addr+2]
byte9	read data of [start_addr+3]
byte10	read data of [start_addr+4]
byte11	read data of [start_addr+5]
byte12	read data of [start_addr+6]
byte13	read data of [start_addr+7]
byte14	read data of [start_addr+8]
byte15	read data of [start_addr+9]

7.4.2 HID Get_Input_report

Command Format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h A1	8'h 01	16'h 01 01	16'h 00 03	16'h 00 10	Report

	(Get_Report)	(Rpt Type + Rpt ID)	(Interface)	(16 bytes)	

*Note: The Start_Addr value in the input reported is put in the Internal Register Address 0xff. Software must set the value of Start_Addr Register to make sure Get Input Report can read the proper data you want.

Input Data Format:

byte 0	always 1 for org HID event report ID
byte1	for defined HID event, and each event occupies one bit
byte2	
byte3	start address of returned data (H-start_addr)
byte4	start address of returned data (L-start_addr)
byte5	bit7
	bit6:UART_INT
	bit5:GPI_INT
	bit4:SPIS_INT(slavemode int)
	bit3: SPIM_INT(mastermode int)
	bit2:I2CS_INT(slavemode int)
	bit1:I2CM_INT(mastermode int)
	bit0: IR_INT
byte6	read data of [start_addr]
byte7	read data of [start_addr+1]
byte8	read data of [start_addr+2]
byte9	read data of [start_addr+3]
byte10	read data of [start_addr+4]
byte11	read data of [start_addr+5]
byte12	read data of [start_addr+6]
byte13	read data of [start_addr+7]
byte14	read data of [start_addr+8]
byte15	read data of [start_addr+9]

7.4.3 HID Set_Output_report

Command Format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h 21	8'h 09 (Set_Report)	16'h 02 01 (Rpt Type + Rpt ID)	16'h 00 03 (Interface)	16'h 00 10 (16 bytes)	Report

*Note: Byte5 is the beginning address of this write sequence.

Output Data Format:

byte 0	always 1 for org HID event report ID
byte1	start address of write reg (H-start_addr)
byte2	start address of write reg (L-start_addr)
byte3	effective write/read data length (<=12)
byte4	write data to [start_addr]
byte5	write data to [start_addr+1]
byte6	write data to [start_addr+2]
byte7	write data to [start_addr+3]
byte8	write data to [start_addr+4]
byte9	write data to [start_addr+5]
byte10	write data to [start_addr+6]
byte11	write data to [start_addr+7]
byte12	write data to [start_addr+8]
byte13	write data to [start_addr+9]
byte14	write data to [start_addr+10]
byte15	write data to [start_addr+11]

7.5 Vendor Command Definition

7.5.1 Vender Command Read

Command Format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h C3	8'h 02 (Command 2)	16'h -- -- (Start Address of input Data)	16'h 00 00	16'h 00 – (<=64 bytes)	Data

Input Data Format:

Byte 0	Data of Reg[wValue]
Byte 1	Data of Reg[wValue + 1]
Byte 2	Data of Reg[wValue + 2]
…	…
Byte 63	Data of Reg[wValue + 63]

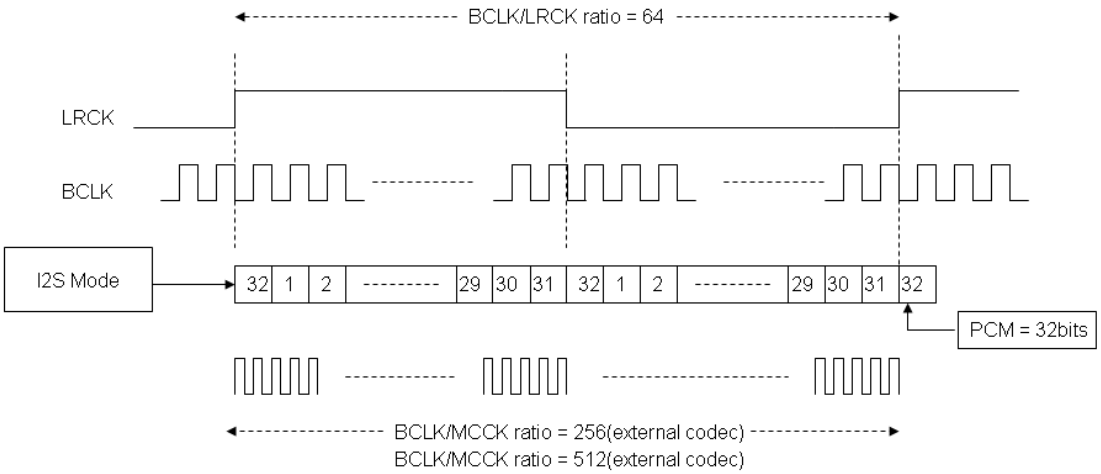
7.5.2 Vender Command Write

Command Format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h 43	8'h 01 (Command 1)	16'h -- -- (Start Address of Output Data)	16'h 00 00	16'h 00 – (<=64 bytes)	Data

Output Data Format:

Byte 0	Data of Reg[wValue]
Byte 1	Data of Reg[wValue + 1]
Byte 2	Data of Reg[wValue + 2]
…	…
Byte 63	Data of Reg[wValue + 63]



7.6 SPDIF Control Description

7.6.1 SPDIF Frame Description

- Audio format : linear 16 bit default.
- Allowed sampling frequencies (Fs) of the audio:
  - 44.1kHz from CD
  - 48 kHz from DAT
  - 32 kHz from DSR
- One way communication: from a transmitter to a receiver.
- Control information:
  - V (validity) bit : indicates if audio sample is valid.
  - U (user) bit : user free coding i.e. running time song, track number.
  - C (channel status) bit : emphasis, sampling rate and copy permit.
  - P (parity) bit : error detection bit to check for good reception.
- Coding format: biphase mark except the headers (preambles), for sync purposes.
- Bandwidth occupation : 100kHz up to 6Mhz (no DC!)
- Signal bitrate is 2.8Mhz (Fs=44.1kHz), 2Mhz (Fs=32kHz) and 3.1Mhz (Fs=48kHz).

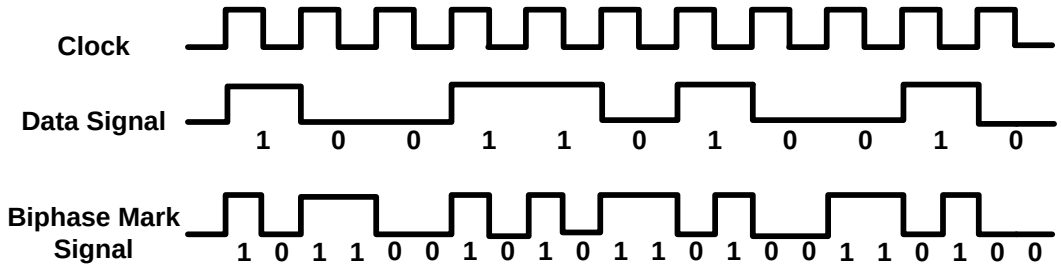


Figure -17 Biphase Mark signal of SPDIF

Preamble	cell-order (last cell "0")	cell-order (last cell "1")
"B"	11101000	00010111
"M"	11100010	00011101
"W"	11100100	00011011

Preamble B:

Marks a word containing data for channel A (left) at the start of the data-block.

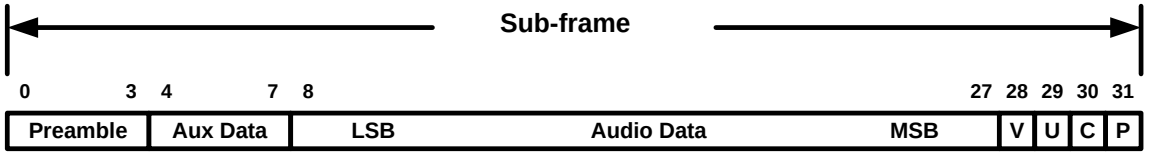
Preamble M:

Marks a word with data for channel A that isn't at the start of the data-block.

Preamble W:

Marks a word containing data for channel B. (right, for stereo). When using more than 2 channels, this could also be any other channel (except for A).

The number of subframes that are used depends on the number of channels that is transmitted. A CD-player uses Channels A and B (left/right) and so each frame contains two subframes. A block contains 192 frames and starts with a preamble "B":



V: Valid, U:User-Data, C:Channel-Status-Data, P:Parity-Bit

Figure -1 SPDIF sub-frame description

In each block, 384 bits of channel status and subcode info are transmitted. The Channel-status bits are equal for both subframes, so actually only 192 useful bits are transmitted:

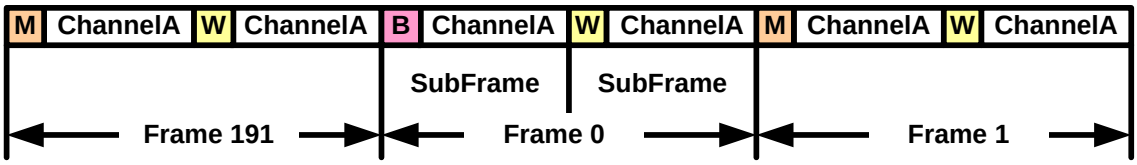


Figure -2 Preamble Description of 192 SPDIF frame

7.6.2 SPDIF Out Channel Status

	bit0	bit1	bit2	bit3	bit4	bit5	bit6	bit7
byte0	**consumer / professional**	**audio / non-audio**	**copyright**	**pre-emphasis**			**mode**	
default	0(P)	0(P)	1(P)	0(P)	0(fixed)	0(fixed)	0(fixed)	0(fixed)
byte1	**category code**							**L**
default	0(P)	0(P)	0(P)	0(P)	0(P)	0(P)	0(P)	0(P)
byte2	**source number**				**channel number**			
default	0(fixed)	0(fixed)	0(fixed)	0(fixed)	0(fixed)	0(fixed)	0(fixed)	0(fixed)
byte3	**sampling frequency**				**clock accuracy**		**reserved**	
default	0(P)	0(P)	0(P)	0(P)	0(fixed)	0(fixed)	0(fixed)	0(fixed)

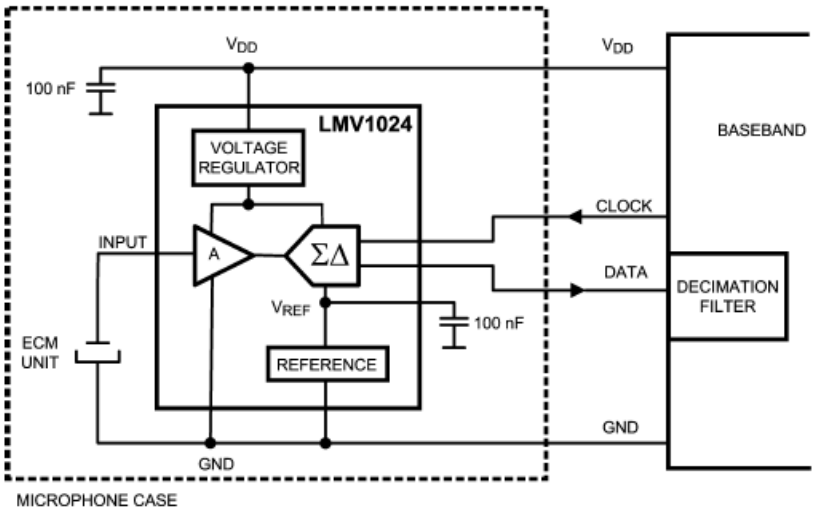
NOTE

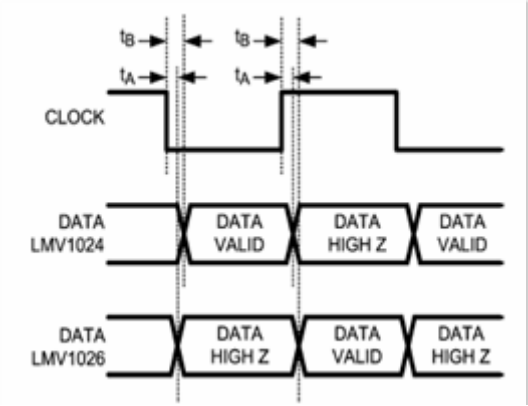
P : these bit can be programmed by USB HID or USB vendor command

7.7 Digital Mic

Digital-Mic Clock and Data Timing

Typical Application

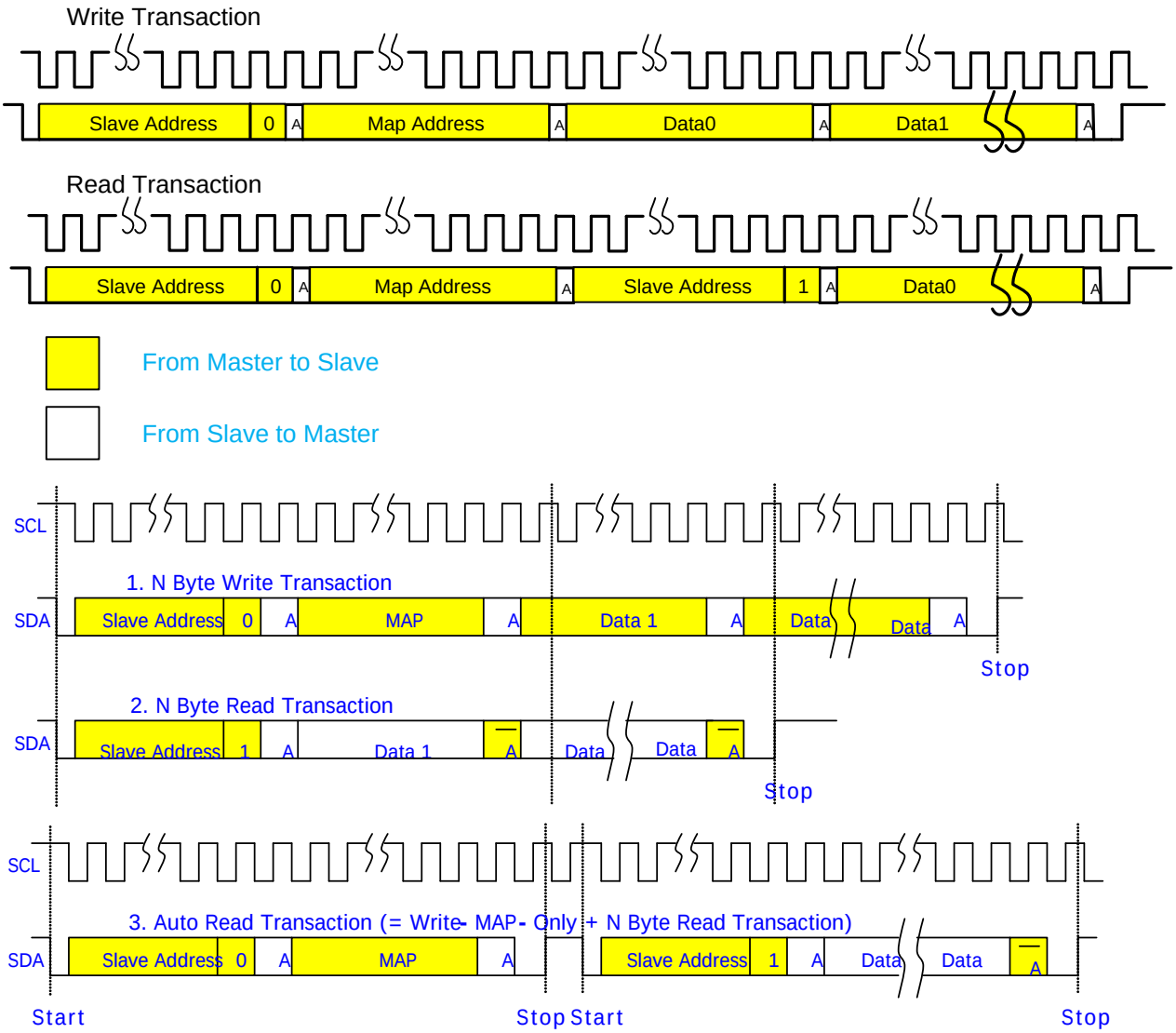




7.8 I2C Interface

7.8.1 I2C Master Mode

I2C protocol timing



from master to slave

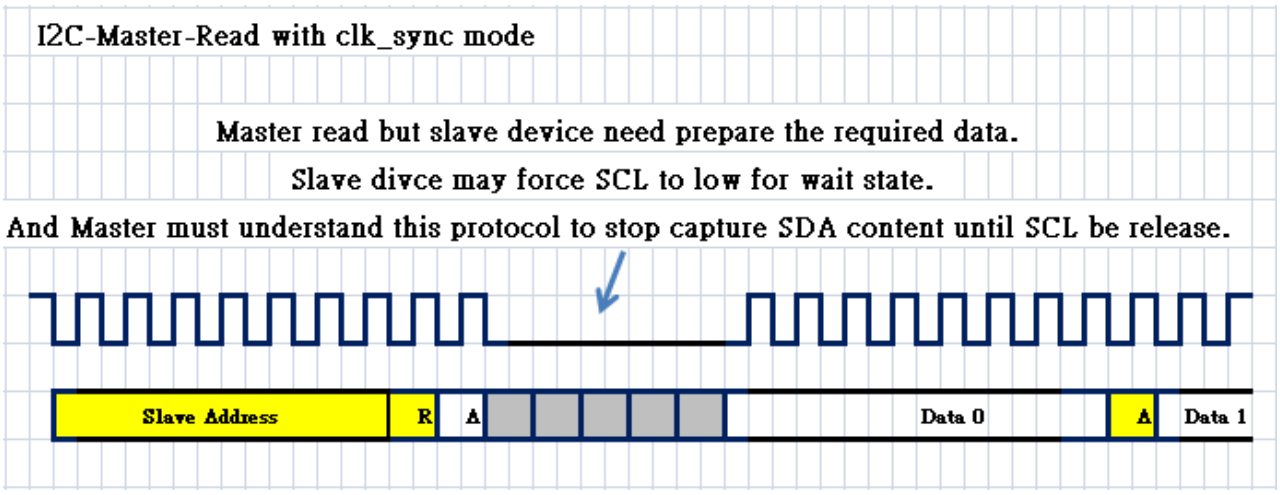
from slave to master

$A =$ *acknowledge* (*SDA Low*)

$\overline{A}$ = *not acknowledge* (*SDA High*)

MAP: Memory Address Pointer
(the target register address
in slave device)

7.8.2 I2C-Master Read with clk_sync mode



7.8.3 I2C Slave Mode

Slave Mode Architecture

"7-bit slave address = 7'b0001000 to 7'b0001011"

CM6502 / CM6502B can serves as a slave device with bit rate up to 400Kbps (fast mode). External MCU can write data to CM6502 / CM6502B or read data from CM6502 / CM6502B (No Size limitation in I2C Interface). Since host side and MCU can both access to all the internal registers.

CM6502 / CM6502B will transfer an interrupt to internal MCU until the INT bit of I2C control Register have been clean by internal MCU. The interrupt will be trigger when write transaction done or detect read-slave-address.

The main usage of 2-wire slave bus is to become the interface between the CM6502 / CM6502B and a external micro control unit (EMCU).

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

Test Conditions: DV50 = 5V, AV50 = 5V, DGND =0V, TA=+25°C

Parameter	Symbol	Min	Typ	Max	Units
Storge temperature	-	-25	-	150	°C
Operating ambient temperature	-	0	25	75	°C
Digital supply voltage(DV50)	-	4.5	5.0	5.5	V
Analog Supply Voltage(AV50)		4.5	5.0	5.5	V
I/O pin voltage	-	GND	-	V_{DD}	V
ESD(Human Body Mode)			±4000		V
ESD(Machine Mode)			±200		V

8.2 Recommended Operation Conditions

Parameter	Symbol	Min	Typ	Max	Units
Analog Supply Voltage	-		5		V
Digital Supply Voltage			5		
Operating Ambient Temperature			25		°C
Crystal Clock	-		12.000		MHz

8.3 Power Consumption

Test Conditions: DV50=5V, AV50 = 5V, DGND =0V, TA=+25°C

Sample Rate=48Khz, 16Bits, Operation: HP-Out Playback+Mic-In Recording, EQ disable, Spdif out disable

Parameter	Symbol	Min	Typ	Max	Units
Total Power Consumption (Playback+Record)	-	-	55	-	mA
Standby Power Consumption	-	-	50	-	mA
Suspend Mode Power Consumption	-	-	10	-	uA

8.4 DC Characteristics

Test Conditions: DV50=5V, V_{DD} = 3.3V, DGND =0V, TA=+25°C, V_{DD} = 3.3V

Parameter	Symbol	Min	Typ	Max	Units
Input voltage range	Vin	V_{DD}-0.3	V_{DD}	V_{DD}+0.3	V
Output voltage range	Vout	0	-	V_{DD}	V
High level input voltage	Vih	0.7V_{DD}	-	-	V
Low level input voltage	Vil	-	-	0.3V_{DD}	V
High level output voitage	Voh	2.4	-	-	V

Low level output voltage	Vol		-	0.4	V
Input leakage current	Iil	-10	-	10	uA
Output leakage current	Iol	-10	-	10	uA
Output buffer driver current	-	-	8	-	mA
SPDIF transmit output driver current	-	-	8	-	mA

8.5 Audio Performance

8.5.1 DAC Audio Quality

TA=25℃, DV50=5V, AV50=5V

Items		Test Conditions	Test Values			Unit
			Min	Typ	Max	
Full scale output voltage		10KΩ loading fs=48KHz		0.95		Vrms
		32Ω loading fs=48KHz		0.82		Vrms
THD+N @ Vout=-3dB		10KΩ loading fs=48KHz/16bits,A-Weighted	-78		-93	dB
		32Ω loading fs=48KHz/16bits,A-Weighted	-67		-92	dB
Dynamic range with signal present		10KΩ loading fs=48KHz/16bits,A-Weighted		91		dB
		32Ω loading fs=48KHz/16bits,A-Weighted		92		dB
Noise level during system activity		10KΩ loading fs=48KHz/16bits,A-Weighted		94		dB
		32Ω loading fs=48KHz/16bits,A-Weighted		96		dB
Inter channel phase delay		100Hz ~ 20KHz	+0.02		+1.05	deg
Sampling frequency accuracy		10KΩ loading fs=48KHz/16bits,A-Weighted	-0.0043		+0.0015	%
Channel separation		10KΩ loading fs=48KHz/16bits,A-Weighted	98		119	dB
		32Ω loading fs=48KHz/16bits,A-Weighted	67		78	dB
Magnitude Response	Frequency Response	10KΩ loading fs=48KHz/16bits,A-Weighted	-0.085		-0.937	dB
	Passband Ripple	10KΩ loading fs=48KHz/16bits,A-Weighted			0.291	dB

8.5.2 ADC Audio Quality

TA=25℃, DV50=5V, AV50=5V, Input test signal is 997Hz sine wave, measure bandwidth is 20Hz to 20KHz

Items	Test Conditions	Test Values			Unit
		Min	Typ	Max	
Full scale output voltage	Microphone fs=48KHz		1.11		Vrms
THD+N @ Vout=-3dB	Microphone fs=48KHz/16bits,A-Weighted	-81		-89	dB
Dynamic range with signal present	Microphone fs=48KHz/16bits,A-Weighted		90		dB
Sampling frequency accuracy	Microphone fs=48KHz/16bits,A-Weighted	+0.0001		+0.009	%
Channel separation	Microphone fs=48KHz/16bits,A-Weighted	81		91	dB
Frequency Response	Microphone fs=48KHz/16bits,A-Weighted	-0.433		-0.484	dB
Passband Ripple	Microphone fs=48KHz/16bits,A-Weighted			0.204	dB

8.5.3 A-A path Audio Quality

TA=25℃, DV50=5V, AV50=5V

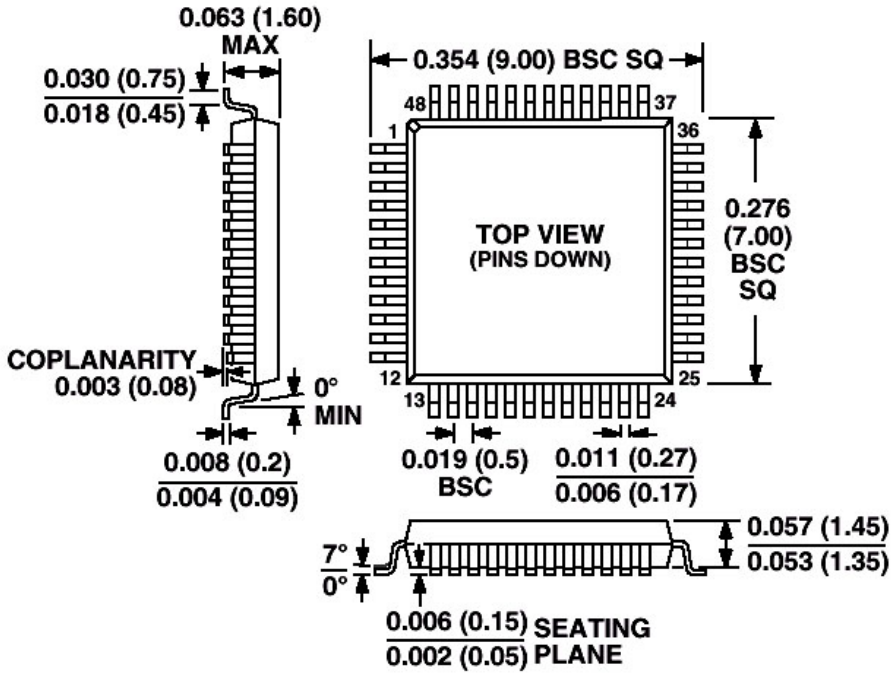
Items	Test Conditions	Test Values			Unit
		Min	Typ	Max	
Full scale output voltage	Microphone to Line out		1.09		Vrms
THD+N @ Vout=-3dB	Microphone to Line out fs=48KHz/16bits,A-Weighted	-80		-81	dB
Dynamic range with signal present	Microphone to Line out fs=48KHz/16bits,A-Weighted		92		dB
Channel separation	Microphone to Line out fs=48KHz/16bits,A-Weighted	74		119	dB
Frequency Response	Microphone to Line out fs=48KHz/16bits,A-Weighted	-0.194		+0.484	dB
Passband Ripple	Microphone fs=48KHz/16bits,A-Weighted			0.1	dB

9 Package Dimension

Model Number	Package	Operating Ambient Temperature	Supply Range
CM6502 / CM6502B	48-Pin LQFP 7mm×7mm×1.4mm (Plastic)	-15°C to +70°C	DVdd = 5V, AVdd = 5V

Outline Dimensions ***Dimensions shown in inches and (mm)**

48-Lead Thin Plastic Quad Flatpack (LQFP)



Package Dimension of CM6502 / CM6502B

—End of Specifications—

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