GENERAL DESCRIPTION

The CM6520 makes simple work out of implementing a complete control and protection scheme for a DC-DC step-down converter. Designed to drive N-channel MOSFETs in a synchronous buck topology, the CM6520 integrates the control, output adjustment, monitoring and protection functions into a single 8-Lead package.

The CM6520 provides simple, single feedback loop, voltage-mode control with fast transient response. The output voltage can be precisely regulated to as low as 0.8V, with a maximum tolerance of ±1.5% over temperature and line voltage variations. A fixed frequency oscillator reduces design complexity, while balancing typical application cost and efficiency.

The error amplifier features a 15MHz gain-bandwidth product and 8V/μs slew rate which enables high converter bandwidth for fast transient performance. The resulting PWM duty cycles range from 0% to 100%.

Protection from over current conditions is provided by monitoring the $r_{DS(ON)}$ of the lower MOSFET to inhibit PWM operation appropriately. This approach simplifies the implementation and improves efficiency by eliminating the need for a current sense resistor.

FEATURES

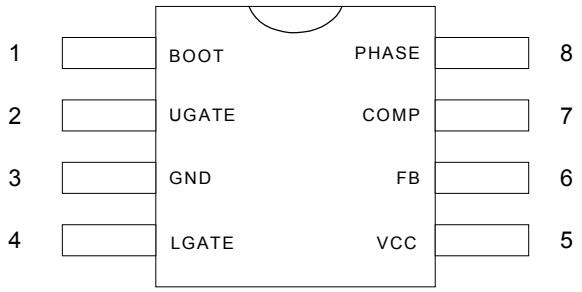
- 8-Pin SOP package
- Buck Converter VIN Operate from +3.3V input to +14V
- VCC Operate from +3.75V to +6V
- Buck Converter VIN can be greater than VCC
- 0.8V to VIN output range
- 0.8V internal reference
- ±1.5% over line voltage and temperature
- Drives N-channel MOSFETs
- Simple Single-Loop control design
- Voltage-mode PWM control
- Fast transient response
- High-Bandwidth error amplifier
- Full 0% to 100% duty cycle
- Lossless, programmable over current protection Uses lower MOSFET's rDS(ON)
- Converter can source and sink current
- Internal soft start
- 300kHz fixed frequency oscillator

APPLICATIONS

- Power Supplies for Microprocessors
- Subsystem Power Supplies
- Cable Modems, Set-Top Box, DSL Modems
- DSP and Core Communications Processor Supplies
- Memory Supplies
- Personal Computer Peripherals
- Industrial Power Supplies
- Low-Voltage Distributed Power Supplies

PIN CONFIGURATION

SOP-08
Top View



ORDERING INFORMATION

Part Number	Temperature Range	Package
CM6520IS	-40℃ to +85℃	8-Pin SOP (S08)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) ..... +6V
Absolute Boot Voltage (V_{BOOT}) ..... +20V
Upper Driver Supply Voltage, $V_{BOOT} - V_{PHASE}$ ..... +20V
Input, Output or I/O Voltage ..... GND-0.3V to VCC+0.3V

OPERATING CONDITIONS

Supply Voltage (V_{CC}) ..... +5V±10%
Operating Junction Temperature Range, T_J ..... -40℃ to +125℃
Ambient Temperature Range ..... -40℃ to +85℃
Lead Temperature (10 sec.) ..... 300℃

THERMAL INFORMATION

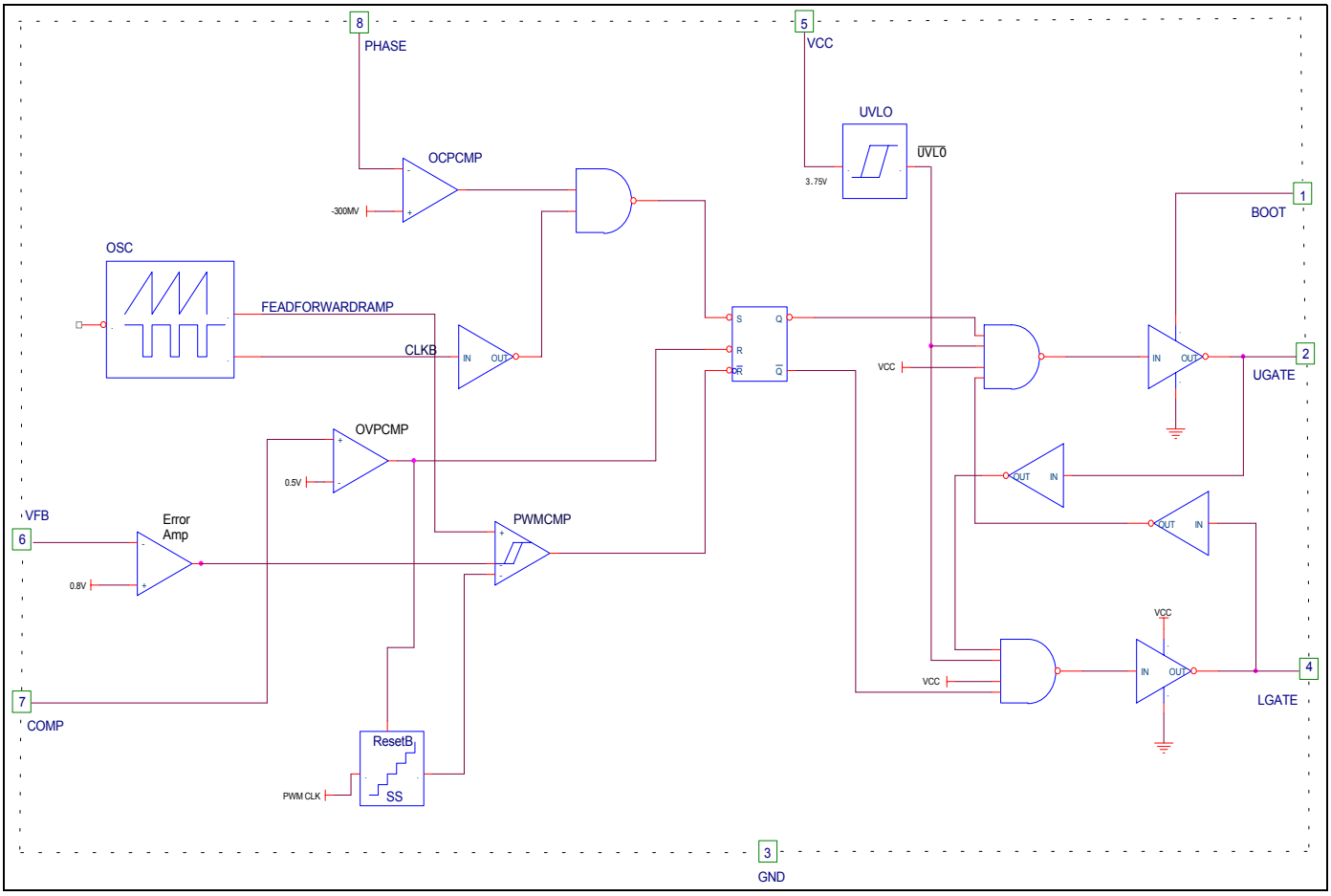
Thermal Resistance (SOP-08), θ_{JA} ..... 100℃/W
Maximum Junction Temperature Range, T_J ..... +150℃
Maximum Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (10 sec.) ..... 300℃

ELECTRICAL CHARACTERISTICS

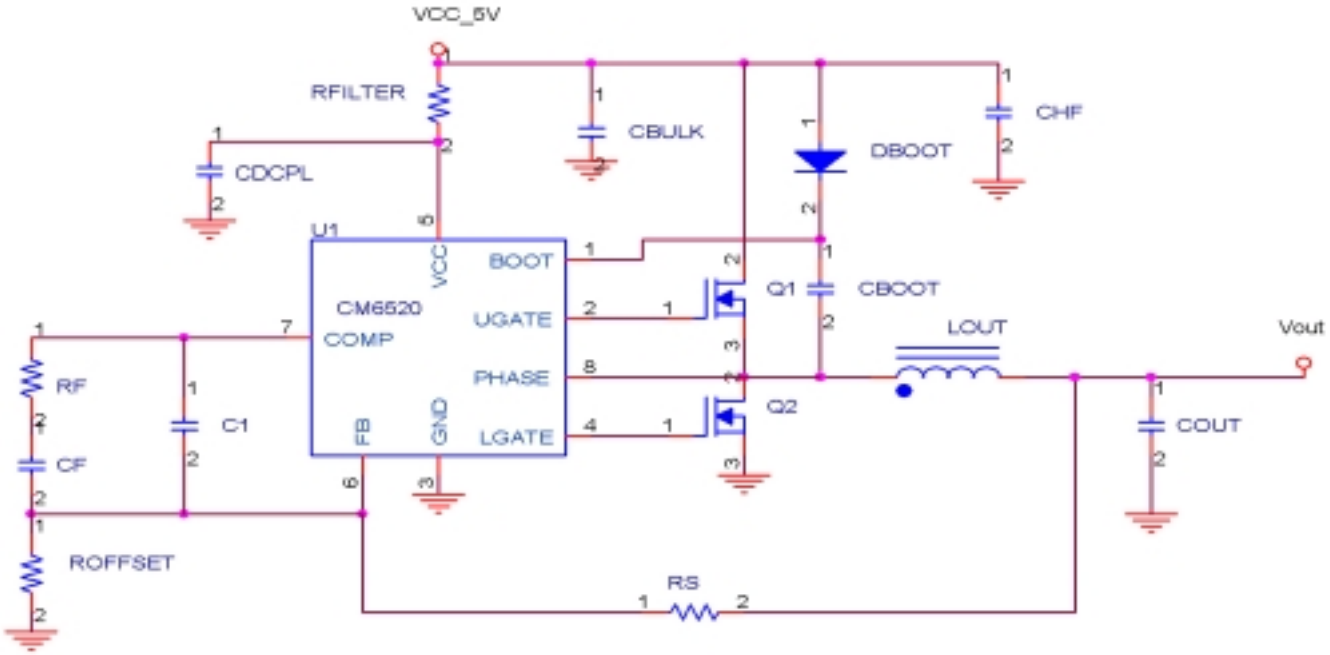
Electrical Characteristics at I_{OUT} = 0mA, and T_J = +25℃; unless otherwise noted

Symbol	Parameter	Test Conditions	CM6520			Unit
			Min.	Typ.	Max.	
VCC Supply Current						
IVCC	Nominal Supply		2.6	3.2	3.8	mA
Power-On Reset						
POR	Rising VCC POR Threshold		3.8	4.0	4.2	V
	VCC POR Threshold Hysteresis		0.24	0.25	0.30	V
Oscillator						
FOSC	Frequency	VCC = 5V	250	300	340	kHz
ΔVOSC	Ramp Amplitude			1.5		V
Reference						
VREF	Reference Voltage Tolerance				1.5	%
	Nominal Reference Voltage			0.8		V
Error Amplifier						
	DC Gain			82		dB
GBWP	Gain-Bandwidth Product		14			MHz
SR	Slew Rate	COMP = 10pF	4.65	8.0	9.2	V/μs
Gate Drivers						
$I_{UGATE-SRC}$	Upper Gate Source Driver	V_{BOOT} = 10V, I_{UGATE} = 100 mA		15		Ohm
$I_{UGATE-SNK}$	Upper Gate Sink Driver			7		Ohm
$I_{LGATE-SRC}$	Lower Gate Source Driver	V_{VCC} = 5V, I_{LGATE} = 100 mA		9.5		Ohm
$I_{LGATE-SNK}$	Lower Gate Sink Driver			3.5		Ohm
Protection / Disable						
VOCP	OCP Threshold	Vvcc=5V, Sweep Phase		-300		mV
VDISABLE	Disable Threshold	Sweep COMP		0.3		V

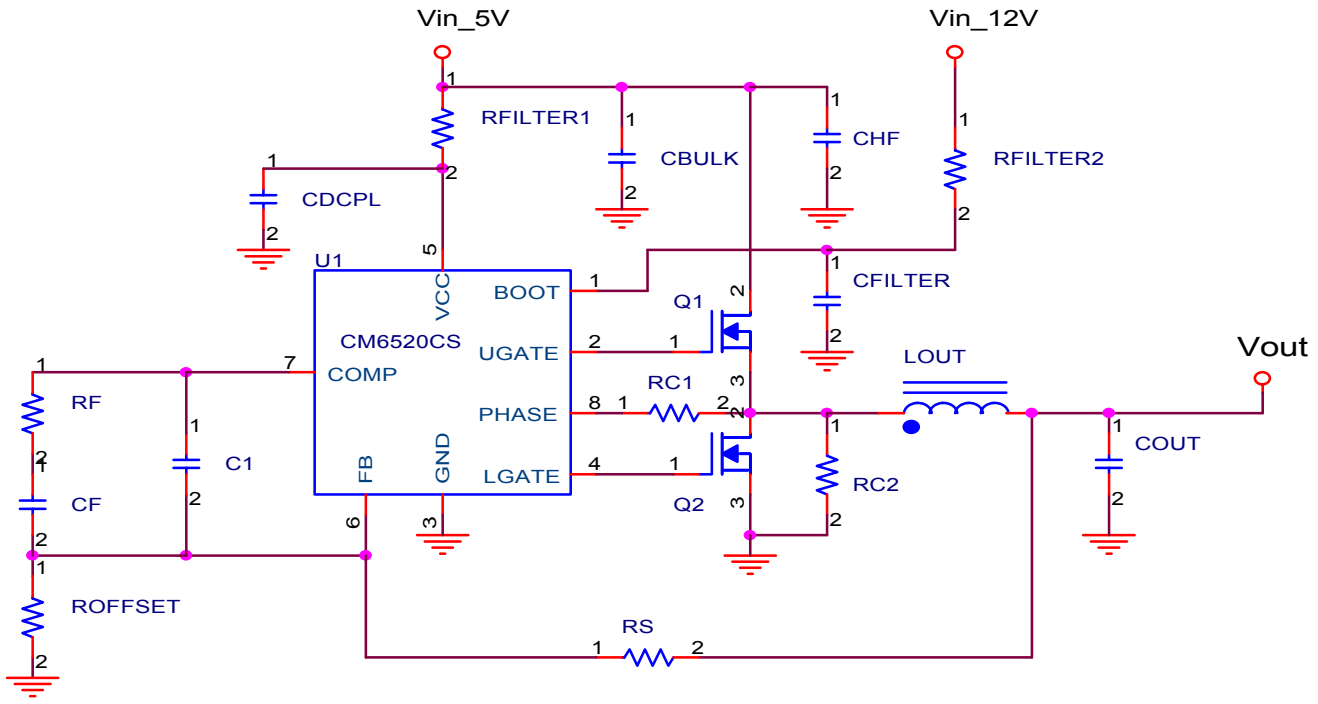
BLOCK DIAGRAM



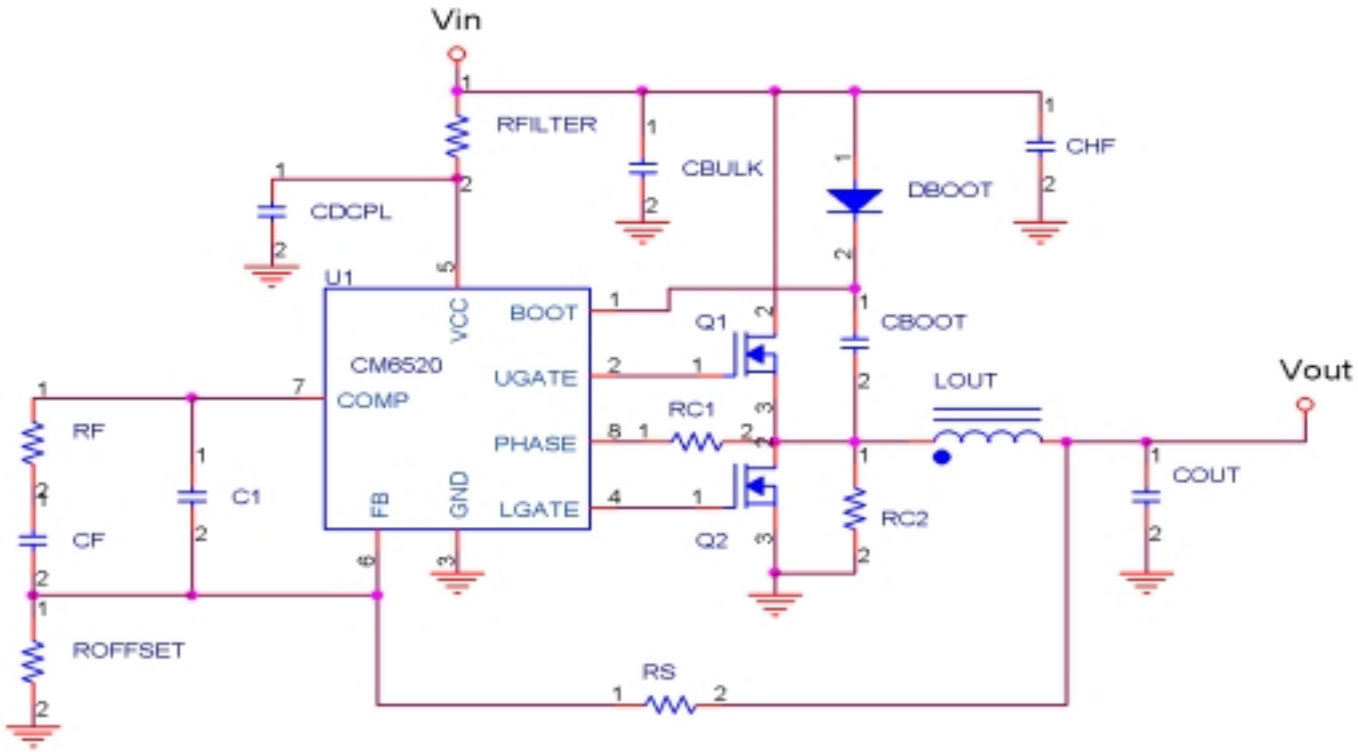
TYPICAL APPLICATION



Single Power 5V Application



Dual Power 5V and 12V Application



Adjustable OCP Point Application

Functional Pin Description

VCC (Pin 5)
This pin provides the bias supply for the CM6520, as well as the lower MOSFET's gate. Connect a well-decoupled 5V supply to this pin.

FB (Pin 6)
This pin is the inverting input of the internal error amplifier. Use this pin, in combination with the COMP pin, to compensate the voltage-control feedback loop of the converter.

GND (Pin 3)
This pin represents the signal and power ground for the IC. Tie this pin to the ground island/plane through the lowest impedance connection available.

PHASE (Pin 8)
Connect this pin to the upper MOSFET's source. This pin is used to monitor the voltage drop across the lower MOSFET for over current protection. The OCP threshold is -300mV. If Phase is less than -300mV, the upper MOSFET cannot be turned on in the next cycle.

UGATE (Pin 2)
Connect this pin to the upper MOSFET's gate. This pin provides the PWM-controlled gate drive for the upper MOSFET. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET can be turned on. The Sourcing Rdson is 15 Ohm and the sink Rdson is 7 Ohm. UGATE can handle high voltage up to maximum 20V.

BOOT (Pin 1)
This pin provides ground referenced bias voltage to the upper MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive a logic-level N-channel MOSFET. It can take 20V as the maximum voltage. It can be powered by a DC power supply or powered by a boost strap circuit.

COMP (Pin 7)
During soft-start, and all the time during normal converter operation, this pin represents the output of the error amplifier. Use this pin, in combination with the FB pin, to compensate the voltage-control feedback loop of the converter.

Pulling COMP to a level below 0.3V enables Soft Start process. The whole Soft Start process takes about 5mS.

LGATE (Pin 4)
Connect this pin to the lower MOSFET's gate. This pin provides the PWM-controlled gate drive for the lower MOSFET. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET can be turned on.

Functional Description

Start Up
The CM6520 automatically initializes upon receipt of power. The Power-on Reset (POR) function continually monitors the bias voltage at the VCC pin. The POR function initiates the Soft Start (SS) operation after the supply voltage exceeds its POR threshold.

Over Current Protection (OCP)
The over current function protects the converter from a shorted output by using the lower MOSFET's on-resistance, $r_{DS(ON)}$, to monitor the current. Therefore, even the power input voltage is greater than VCC, CM6520 still can support this. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor.

The CM6520's OCP threshold is a fixed value, -300mV. When Phase voltage is less -300mV, the next on-cycle will not be initialized.

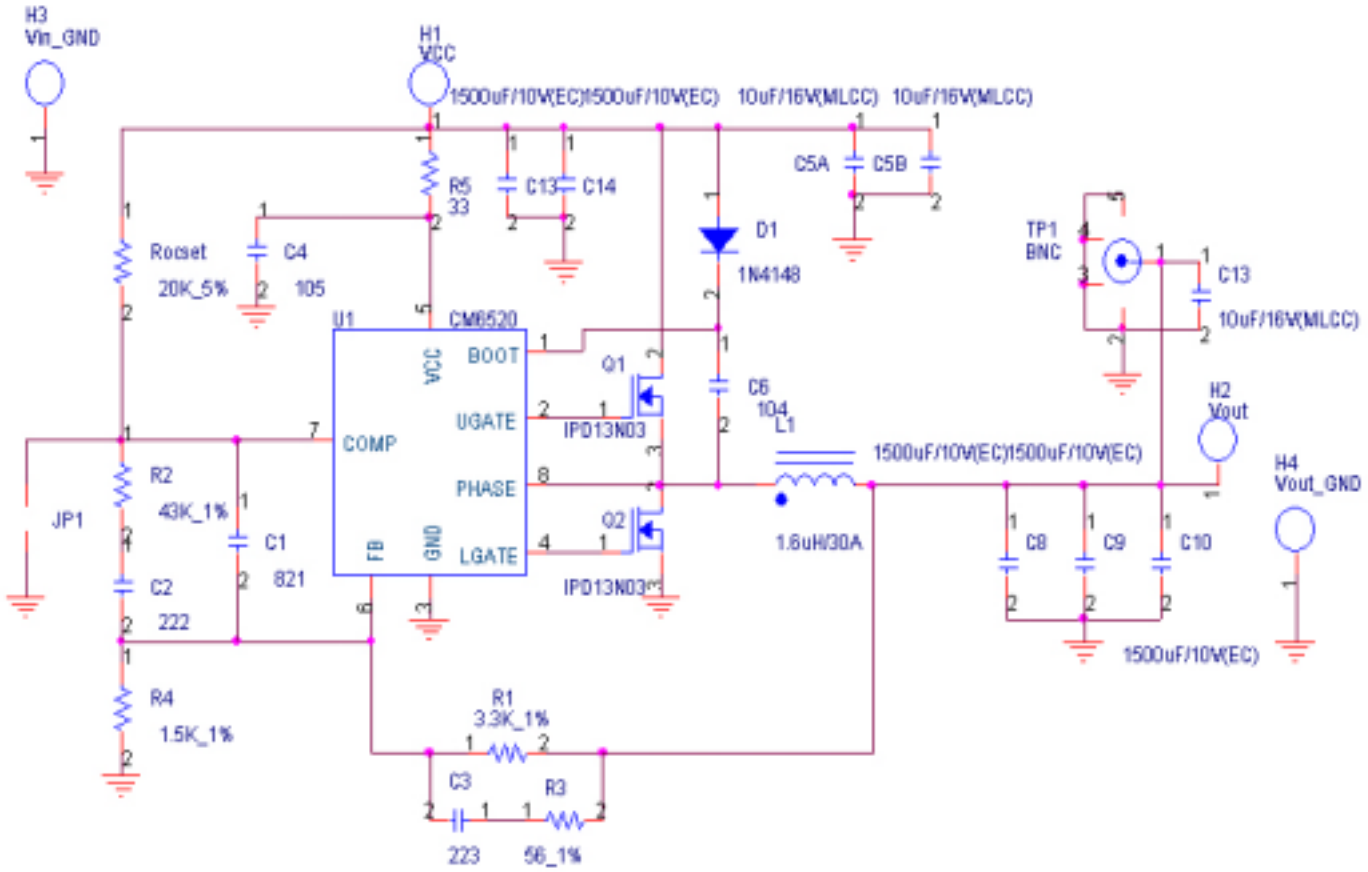
Over Voltage Protection (OVP)
An Over Voltage Protection Comparator is monitoring the COMP. When COMP voltage is less than 0.3V, the Soft Start process is initiated.

Soft Start
Both POR and OVP initiate the soft start sequence after the over current set point has been sampled. Soft Start clamps virtually the error amplifier output (COMP pin) and reference input (non-inverting terminal of the error amp) to the internally generated Soft Start voltage. The oscillator's triangular waveform is compared to the ramping error amplifier voltage. This generates PHASE pulses of increasing width that charge the output capacitor(s). When the internally generated Soft Start voltage exceeds the COMP pin voltage, the output voltage is in regulation. This method provides a rapid and controlled output voltage rise. The entire startup sequence typically takes about 5ms.

Current Sinking
The CM6520 incorporates a MOSFET shoot-through protection method which allows a converter to sink current as well as source current. Care should be exercised when designing a converter with the CM6520 when it is known that the converter may sink current.

When the converter is sinking current, it is behaving as a boost converter that is regulating its input voltage. This means that the converter is boosting current into the buck converter input power, if the buck converter input power has the same supply source which supplies the bias voltage, VCC to the CM6520. If there is nowhere for this current to go, such as to other distributed loads on the VCC rail, through a voltage limiting protection device, or other methods, the capacitance on the VCC bus will absorb the current. This situation will allow voltage level of the VCC rail to increase. If the voltage level of the rail is boosted to a level that exceeds the maximum voltage rating of the CM6520, then the IC will experience an irreversible failure and the converter will no longer be operational. Ensuring that there is a path for the current to follow other than the capacitance on the rail will prevent this failure mode.

DEMO BOARD APPLICATION CIRCUIT



Component	Reference design	Maximum load current		
		5A	10A	15A
MosFET	Q1, Q2	Rds(on)<30mΩ	Rds(on)<20mΩ	Rds(on)<10mΩ
Inductor	L1	5uF	3uF	1.6uF
No. of input capacitor	C13, C14	1	1	2
No. of output capacitor	C8,C9,C10	1	2	3
No. of decoupling capacitor	C5A, C5B	1	1	2

Reference design capacitor: 1500uF(ESR=33mΩ)
Reference design decoupling capacitor: 10uF(MLCC)

Application Guidelines
Component Selection Guidelines
Input Capacitor Selection
Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q1 and the source of Q2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

MOSFET Selection/Considerations
The CM6520 requires 2 N-Channel power MOSFETs. These should be selected based upon Rds(ON), gate supply requirements, and thermal management requirements.
In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor. The switching losses seen when sourcing current will be different from the switching losses seen when sinking current. When sourcing current, the upper MOSFET realizes most of the switching losses. The lower switch realizes most of the switching losses when the converter is sinking current (see the equations below). These equations assume linear voltage current transitions and do not adequately model power loss due the reverse-recovery of the upper and lower MOSFET's body diode. The gate-charge losses are dissipated by the CM6520 and don't heat the MOSFETs. However, large gatecharge increases the switching interval, tSW which increases the MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.
Losses while Sourcing Current

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times F_S$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D)$$

Losses while Sinking Current

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D) + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times F_S$$

Where: D is the duty cycle = VOUT / VIN,
tSW is the combined switch ON and OFF time, and
FS is the switching frequency.

Given the reduced available gate bias voltage (5V), logic-level or sub-logic-level transistors should be used for both N-MOSFETs. Caution should be exercised with devices exhibiting very low VGS(ON) characteristics. The shoot through protection present aboard the CM6520 may be circumvented by these MOSFETs if they have large parasitic impedences and/or capacitances that would inhibit the gate of the MOSFET from being discharged below it's threshold level before the complementary MOSFET is turned on.

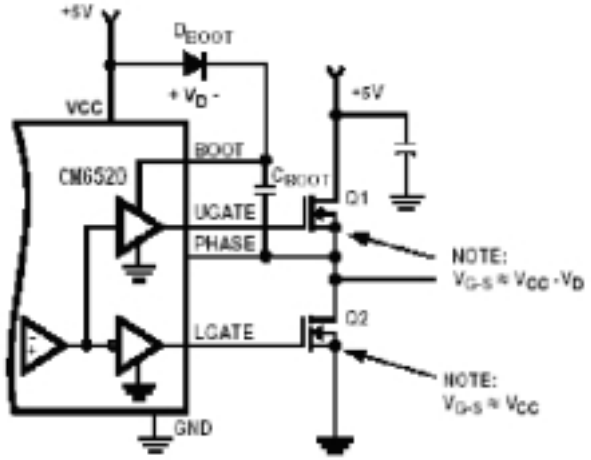


FIGURE 5. UPPER GATE DRIVE BOOTSTRAP

Figure 5 shows the upper gate drive (BOOT pin) supplied by a bootstrap circuit from VCC. The boot capacitor,CBOOT, develops a floating supply voltage referenced to the PHASE pin. The supply is refreshed to a voltage of VCC less the boot diode drop (VD) each time the lower MOSFET, Q2, turns on.

Output Inductor Selection
The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{Fs \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the CM6520 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}}$$

where: ITRAN is the transient load current step,
tRISE is the response time to the application of load, and
tFALL is the response time to the removal of load.
The worst case response time can be either at the application or removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Feedback Compensation

Figure 6 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (VOUT) is regulated to the Reference voltage level. The error amplifier (Error Amp) output (VE/A) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of VIN at the PHASE node. The PWM wave is smoothed by the output filter (LO and CO).

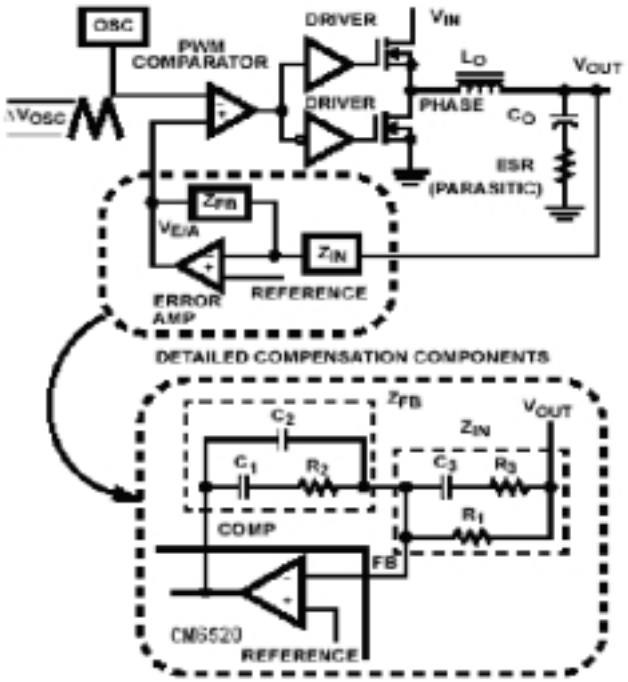


FIGURE 6. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

The modulator transfer function is the small-signal transfer function of VOUT/VE/A. This function is dominated by a DC Gain and the output filter (LO and CO), with a double pole break frequency at FLC and a zero at FESR. The DC Gain of the modulator is simply the input voltage (VIN) divided by the peak-to-peak oscillator voltage VOSC.

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad F_{ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \times R_2 \times C_1} \qquad F_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R_1 + R_3) \times C_3} \qquad F_{P2} = \frac{1}{2\pi \times R_3 \times C_3}$$

The compensation network consists of the error amplifier (internal to the CM6520) and the impedance networks ZIN and ZFB. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f0dB) and adequate phase margin. Phase margin is the difference between the closed loop phase at f0dB and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 7. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R2/R1) for desired converter bandwidth.
2. Place 1ST Zero Below Filter's Double Pole (~75% FLC).
3. Place 2ND Zero at Filter's Double Pole.
4. Place 1ST Pole at the ESR Zero.
5. Place 2ND Pole at Half the Switching Frequency.
6. Check Gain against Error Amplifier's Open-Loop Gain.
7. Estimate Phase Margin - Repeat if Necessary.

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern components and loads are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Feedback divider

The reference of CM6520 is 0.8V. The output voltage can be set by R1 and R4 as shown in Fig.4. The equation is following:
Vout = 0.8(1+R1/R4)
The R1 should be between 2kΩ to 5kΩ. Put the R1,R4 and others compensation component as close to CM6520 as possible.

Shutdown

Pulling low the COMP pin can shutdown the CM6520 PWM controller. You can use a small single transistor as switch like as JP1 shown in Fig.4.

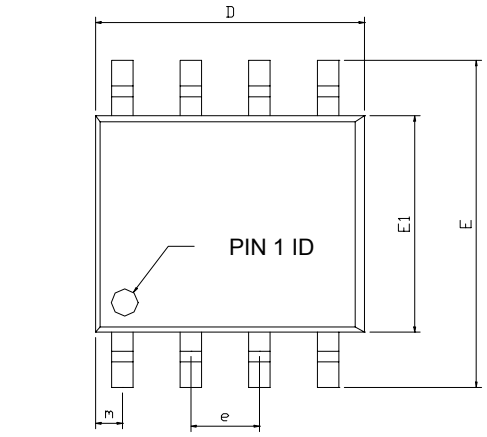
Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible, using ground plane construction or single point grounding.

To minimize the voltage overshoot, the interconnecting wires indicated by heavy lines should be part of a ground or power plane in a printed circuit board. Locate the CM6520 within 3 inches of the MOSFETs, Q1 and Q2. The circuit traces for the MOSFETs' gate and source connections from the CM6520 must be sized to handle up to 1A peak current. Provide local V_{CC} decoupling between VCC and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT and PHASE pins. All components used for feedback compensation should be located as close to the IC a practical.

PACKAGE DIMENSION

SOP-08 (S08)



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A1	0.10	---	0.25	0.004	---	0.010
A2	1.40	---	1.55	0.055	---	0.061
b	0.30	---	0.51	0.012	---	0.020
C	0.15	---	0.26	0.006	---	0.010
D	4.60	---	5.06	0.169	---	0.199
E	5.79	---	6.20	0.228	---	0.244
E1	3.76	---	4.01	0.148	---	0.158
e	---	1.27	---	---	0.050	---
L	0.38	---	0.69	0.015	---	0.035
m	0.43	---	0.69	0.017	---	0.027
θ	0°	---	8°	0°	---	8°

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