CM7104

High Speed Audio DSP with Hi-Fi Audio Codec

Rev. 1.00

Updated: 2018/12/24

REVISION HISTORY

Revision	Release Date	Summary
0.92	2015/04/09	First release for CM7104 datasheet
0.93	2015/07/31	Typo correction
0.94	2016/12/05	Function diagram correction
0.95	2016/12/08	Modify Ch 9.13
0.96	2017/04/11	Add DSP OutBound0 Ring Buffer Control Registers and PLL tracking mode
0.97	2017/05/22	Typo correction
1.00	2018/12/24	Formal release

Table of Contents

List of Tables

List of Figures

1. General Description

The CM7104 is a highly-integrated Audio DSP plus CODEC system whose high-performance and low-power consumption make it ideal for a wide range of mobile systems, such as Tablet, Smartphone and Ultra-book.

The CM7104 DSP core, Tensilica HiFi EP, with extensive memory resources provides low-power advanced digital signal processing. Given that Tensilica HiFi core is widely used by many third-party software developers, it makes CM7104 create an extensive wide software reference design ecosystem, including multi-microphone advanced voice processing (NS, AEC…etc.), low power speech trigger and recognition, and high-quality well-known branding audio post-processing. The CM7104 integrates a fully-flexible digital mixing and routing with asynchronous sample rate converter (ASRC) to support the DSP core for wide use case flexibility.

Two digital audio interfaces are provided, supporting I^2S/PCM/TDM audio formats. Two differential analog microphone inputs and up to two digital microphone inputs can accept audio signals from multiple microphone or line input sources. Two differential line outputs can provide high performance analog audio signal outputs for connecting high-quality amplification systems.

The CM7104 also combines a variety of low-power fixed-function signal processing components. The advanced multiband DRC (Dynamic Range Control) enables further digital audio processing capabilities on playback or record paths. Advanced DRC function comprises multi-section and multi-band parts, ensuring signal level maintenance, maximizes loudness, and prevents audio clipping and speaker damage.

The CM7104 can be powered from a 1.8V power supply only, and its individual blocks are all design for power efficient target, helping devices to achieve long time playback, record, voice talk…etc. cases. The CM7104 is supplied by a LQFP48 package within 7x7 mm^2.

2. Features

- Audio DSP (Tensilica Hi Fi EP)
  - Up to 300MHz DSP for audio/voice processing
  - Up to 768KByte internal memory
  - Separate power control for inbound/outbound DMA
  - Separate power control for internal RAM bank
- Parametric 10 bands equalizer (EQ) for playback path
- Advanced DRC with multi-section compressor function for playback/recording path
- Sound detection wake up technology (VAD)
- Wind noise reduction filter
- 2 24bit/8kHz ~ 192kHz I2S/PCM/TDM digital interface
- Digital asynchronous sampling rate converter (ASRC) function
- One PDM interface for external PDM Class-D amplifier
- 2 stereo digital microphone interface
- SPI control interface (Up to 28MHz clock rate)
- I2C master/slave control interface
- Haptic generator function
- Sidetone generator function
- 2 mono differential/singled-ended line output
  - -90dB THD+N (0dB gain path)
  - 100dBA SNR (0dB gain path)
- 2 mono singled-ended line input
  - -95dB THD+N (0dB gain path)
  - 102dBA SNR (0dB gain path)
- 2 analog boost pre-amplifiers (+20/24/30/35/40/44/50/52dB) and 1 low noise microphone bias
  - MIC Input to ADC with 50dB Boost, SNR>66dBA, THD+N<-65dB
- Internal PLL can receive wide range clock input
- One adjustable MICBIAS (0.9*MICVDD or 0.75*MICVDD)
- LQFP-48 (7mm x 7mm) package

3. Power/Ground Operation Conditions

POWER TYPE	DECSRIPTION	MIN	TYP	MAX	UNIT
DBVDD1	Digital power for digital I/O buffer	1.71	1.8	3.6	V
DCVDD1	Digital power for codec core (Supplied by internal LDO2 or external power)	1.1	1.2	1.3	V
DCVDD3	Digital power for DSP (Supplied by internal LDO1 or external power)	1.1	1.2	1.3	V
AVDD18	Analog core power	1.71	1.8	1.9	V
DACREF	Analog reference power	1.71	1.8	1.9	V
AVDD33	Microphone bias power	3.0	3.3	3.6	V
AVDD18_LOUT	Analog power for LOUT	1.71	1.8	1.9	V
LDO_IN	LDO power for DSP	1.2	1.8	1.9	V
DGND, AGND18, AGND18_LOUT,	Ground		0		V

*If LDO_IN=1.2V will impact DSP MIPS. The maximum DSP MIPS should be under 100MIPS.

4. System Application

- Smart Phones
- Tablet
- OTT solution
- Gaming headset

5. Function Block and Mixer Path

5.1. Function Block

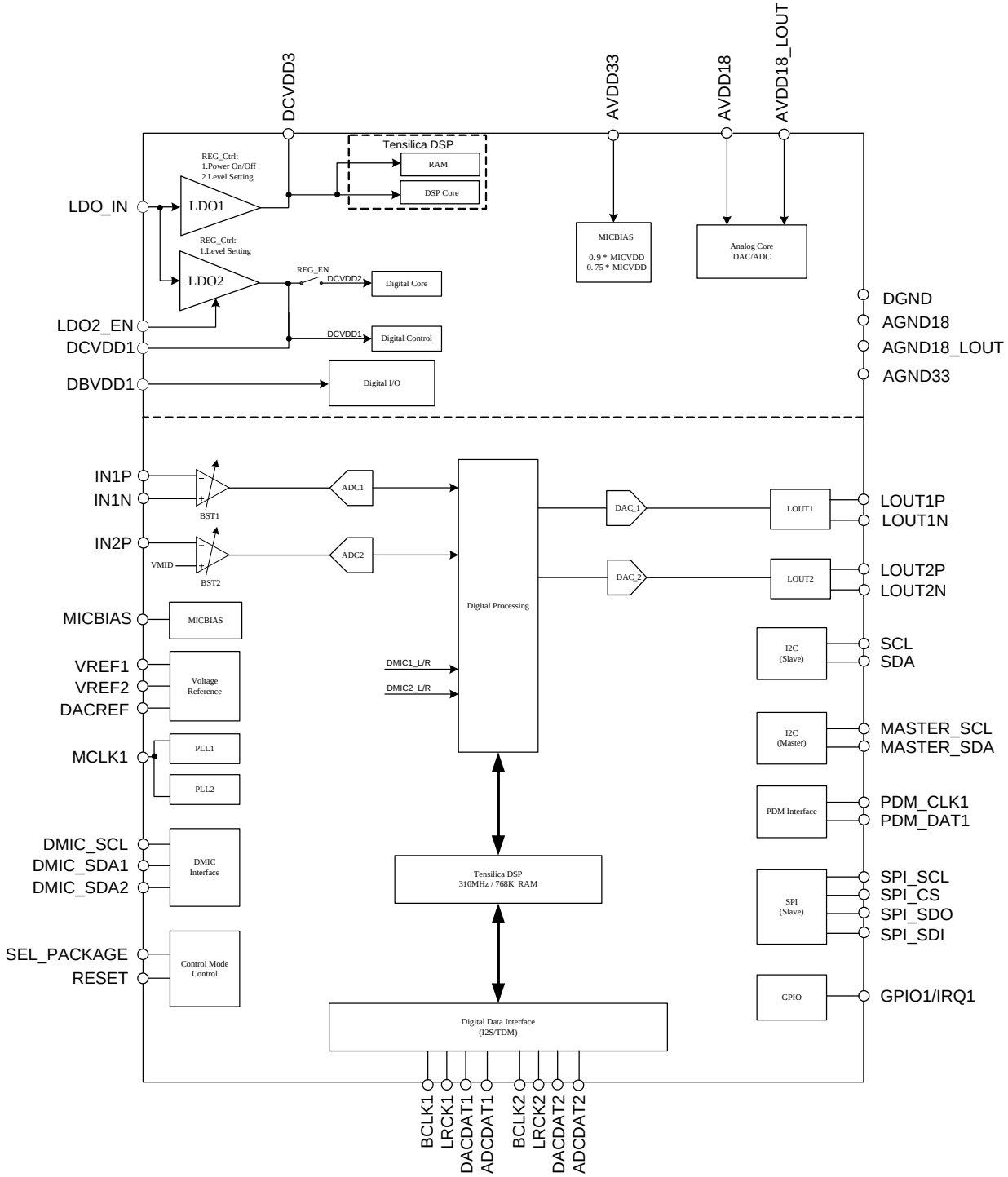


Figure 1. Block Diagram

5.2. Audio Mixer Path

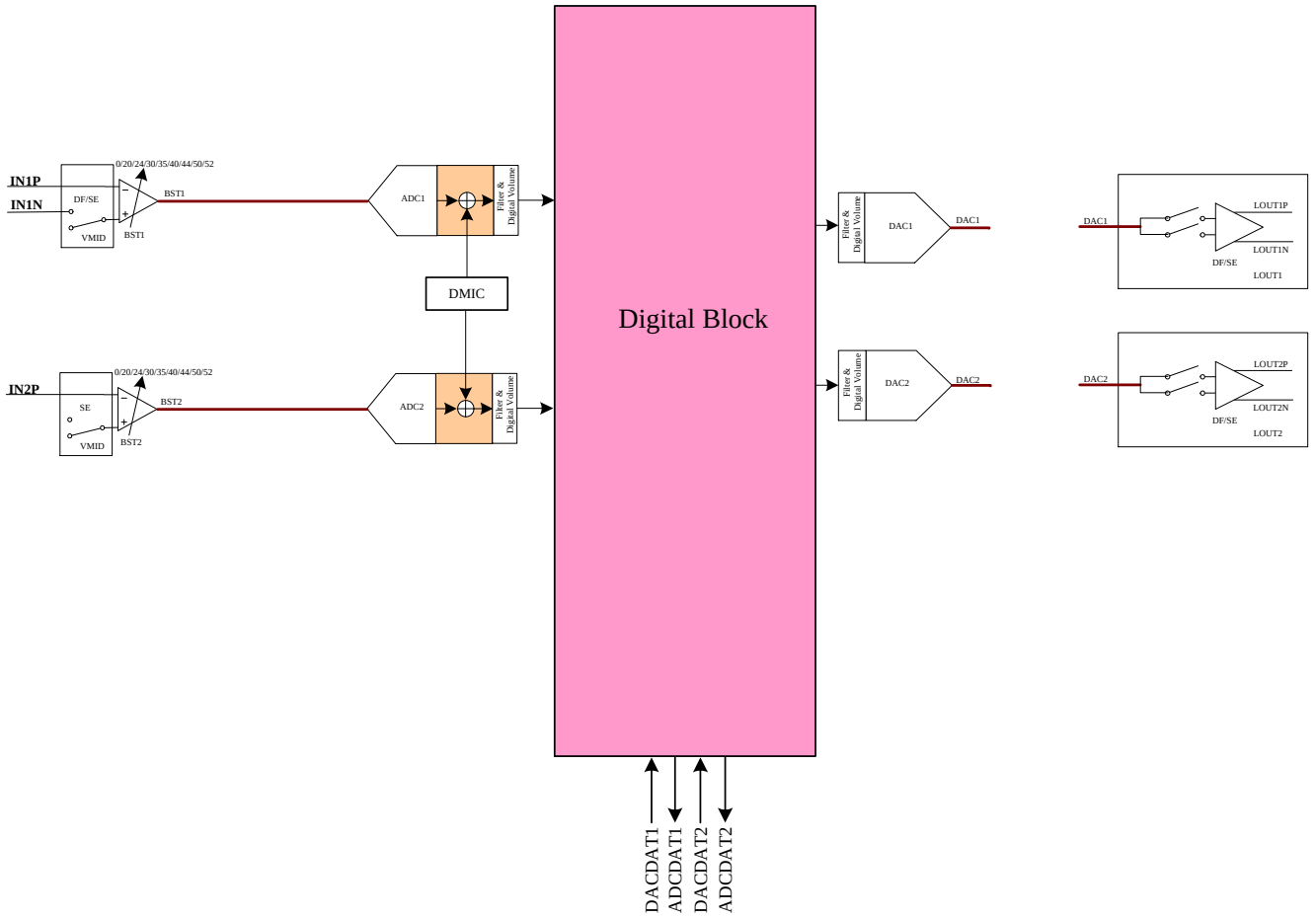


Figure 2. Digital Mixer Path

5.3. Digital Mixer Path

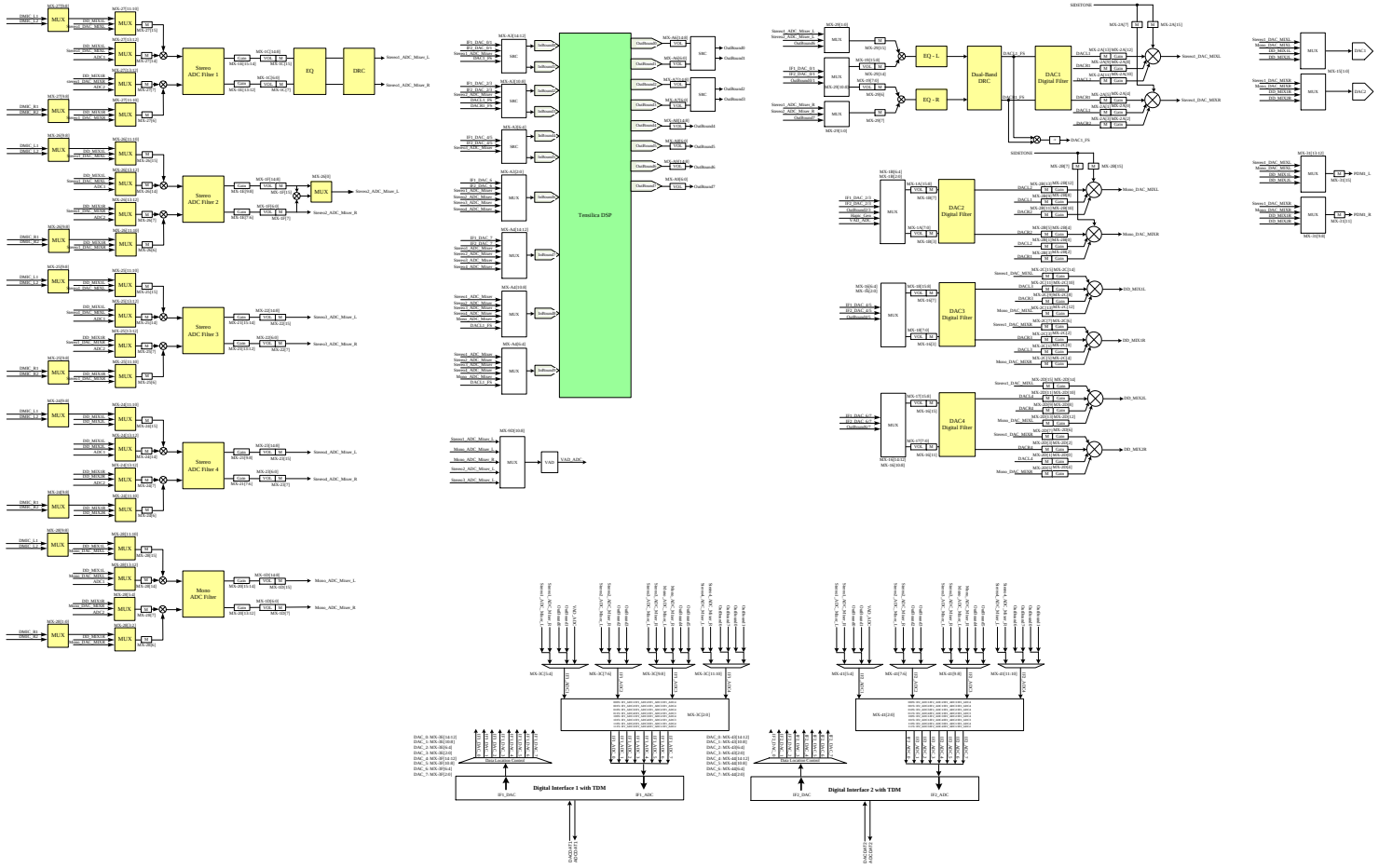


Figure 3. Digital Mixer Path

6. Pin Assignments

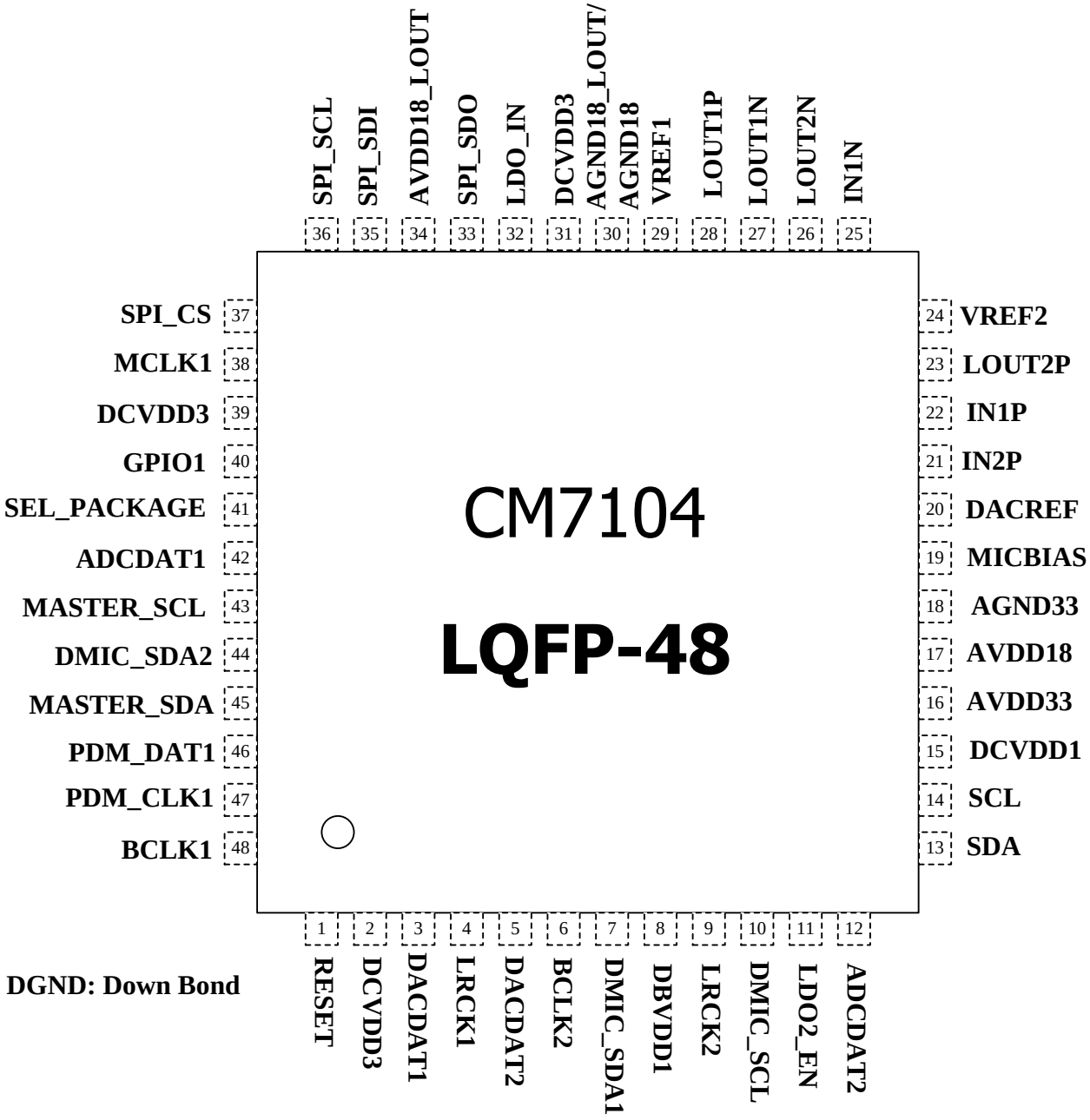


Figure 4. Pin Assignments

7. Pin Descriptions

7.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
DACDAT1	I	3	First I2S/TDM interface serial data input	Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state (PU & PD) control by REG PR-29h[15] & [14]
ADCDAT1	O	42	First I2S/TDM interface serial data output	V_{OL}=0.1*DBVDD1, V_{OH}=0.9*DBVDD1 Default status: output type (low)
BCLK1	I/O	48	First I2S/TDM interface serial bit clock	Master: V_{OL} =0.1*DBVDD1, V_{OH} =0.9*DBVDD1 Slave: Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state (PU & PD) control by REG PR-29h[15] & [14]
LRCK1	I/O	4	First I2S/TDM interface synchronous signal	Master: V_{OL} =0.1*DBVDD1, V_{OH} =0.9*DBVDD1 Slave: Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state (PU & PD) control by REG PR-29h[15] & [14]
DACDAT2	I	5	Second I2S/TDM interface serial data input	Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state (PU & PD) control by REG PR-29h[13] & [12]
ADCDAT2	O	12	Second I2S/TDM interface serial data output	V_{OL}=0.1*DBVDD1, V_{OH}=0.9*DBVDD1 Default status: output type (low)
BCLK2	I/O	6	Second I2S/TDM interface serial bit clock	Master: V_{OL} =0.1*DBVDD1, V_{OH} =0.9*DBVDD1 Slave: Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state (PU & PD) control by REG PR-29h[13] & [12]

Name	Type	Pin	Description	Characteristic Definition
LRCK2	I/O	9	Second I2S/TDM interface synchronous signal	Master: V_{OL} =0.1*DBVDD1, V_{OH} =0.9*DBVDD1 Slave: Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state (PU & PD) control by REG PR-29h[13] & [12]
SPI_SCL	I	36	SPI interface clock input	Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state (PU & PD) control by REG PR-29h[3] & [2]
SPI_CS	I	37	SPI interface chip select input	Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state (PU & PD) control by REG PR-29h[3] & [2]
SPI_SDO	O	33	SPI interface data output	Output: V_{OL} =0.1*DBVDD1, V_{OH} =0.9*DBVDD1 Default status: output type (low)
SPI_SDI	I	35	SPI interface data input	Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state (PU & PD) control by REG PR-29h[3] & [2]
MASTER_SCL	O	43	I2C interface master mode clock output	Output: V_{OL} =0.1*DBVDD1, V_{OH} =0.9*DBVDD1 Open drain structure Default status: output type (low)
MASTER_SDA	I/O	45	I2C interface master mode serial data	Output: V_{OL} =0.1*DBVDD1, V_{OH} =0.9*DBVDD1 Open drain structure (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: output type
SCL	I	14	I2C interface slave mode clock input	Input: Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state (PD) control by REG PR-29h[0]

Name	Type	Pin	Description	Characteristic Definition
SDA	I/O	13	I2C interface slave mode serial data	Open drain structure Default status: input type (floating) Initial state (PD) control by REG PR-29h[0]

Name	Type	Pin	Description	Characteristic Definition
PDM_SCL1	O	47	First PDM interface clock output	Output: V_{OL} =0.1*DBVDD1, V_{OH} =0.9*DBVDD1 Default status: output type (low)
PDM_DAT1	O	46	First PDM interface data output	Output: V_{OL} =0.1*DBVDD1, V_{OH} =0.9*DBVDD1 Default status: output type (low)
MCLK1	I	38	First reference clock input	Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state (PU & PD) control by REG PR-29h[7] & [6]
DMIC_SCL	O	10	First digital microphone clock output	Output: V_{OL} =0.1*DBVDD1, V_{OH} =0.9*DBVDD1 Default status: output type (low)
DMIC_SDA1	I	7	First digital microphone data input	Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state (PU & PD) control by REG PR-2Ah[13] & [12]
DMIC_SDA2	I	44	Second digital microphone data input	Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state (PU & PD) control by REG PR-2Ah[11] & [10]
LDO2_EN	I	11	LDO2 enable pin 0'b: disable (reset CM7104) 1'b: enable	Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state control by external pull-low or pull-down
RESET	I	1	Chip hard reset control 0'b: Reset 1'b: Normal	Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state control by external pull-low or pull-down

Name	Type	Pin	Description	Characteristic Definition
GPIO1/IRQ	I/O	40	Multi-function pin: General purpose input and output Interrupt output	Output: V_{OL} =0.1*DBVDD1, V_{OH} =0.9*DBVDD1 Input: Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state (PU & PD) control by REG PR-2Ah[3] & [2]
SEL_PACKAGE	I	41	Package identify 0'b: Normal mode 1'b: DSP auto boot mode	Schmitt trigger (V_{IL}=0.35*DBVDD1, V_{IH}=0.65*DBVDD1) Default status: input type (floating) Initial state control by external pull-low or pull-down
				Total: 26 Pins

7.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
LOUT1P	O	28	Line output type Differential output, positive channel	Analog output
LOUT1N	O	27	Line output type Differential output, negative channel	Analog output
LOUT2P	O	23	Line output type Differential output, positive channel	Analog output
LOUT2N	O	26	Line output type Differential output, negative channel	Analog output
IN1P	I	22	Analog microphone input Differential input, positive channel	Analog input
IN1N	I	25	Analog microphone input Differential input, negative channel	Analog input
IN2P	I	21	Analog microphone input Differential input, positive channel	Analog input
				Total: 7 Pins

7.3. Filter/Reference

Table 3. Filter/Reference

Name	Type	Pin	Description	Characteristic Definition
MICBIAS	O	19	Bias voltage output for analog microphone	Programmable analog DC output
VREF1	R	29	First internal reference voltage	4.7uF capacitor to analog ground
VREF2	R	24	Second internal reference voltage	4.7uF capacitor to analog ground
				Total: 3 Pins

7.4. Power/Ground

Table 4. Power/Ground

Name	Type	Pin	Description	Characteristic Definition
AVDD33	P	16	Analog power for MICBIAS	1.71V ~ 3.63V (Default 3.3V is recommended)
AGND33	P	18	Analog ground for MICBIAS	
AVDD18	P	17	First analog power	1.71V ~ 1.9V (Default 1.8V is recommended)
AGND18	P	30	Analog ground	
AVDD18_LOUT	P	34	Second analog power	1.71V ~ 1.9V (Default 1.8V is recommended)
AGND18_LOUT	P	30	Analog ground	
DCVDD3	P	31	Digital power for DSP (Internal LDO1 generated) External PCB trace short with ball-H2/H9	1.1V ~ 1.3V (Default 1.2V is recommended)
DCVDD3	P	39	Digital power for DSP (Internal LDO1 generated) External PCB trace short with ball-D1/H9	1.1V ~ 1.3V (Default 1.2V is recommended)
DCVDD3	P	2	Digital power for DSP (Internal LDO1 generated) External PCB trace short with ball-H2/D1	1.1V ~ 1.3V (Default 1.2V is recommended)
DCVDD1	P	15	Digital power for Codec core (Internal LDO2 generated)	1.1V ~ 1.3V (Default 1.2V is recommended)
DBVDD1	P	8	Digital power for digital I/O buffer	1.71V~3.63V (Default 1.8V is recommended)
DGND	P	DB	Digital ground	
LDO_IN	P	32	LDO1 input power	1.2V ~ 1.9V (Default 1.8V is recommended)
DACREF	P	20	Reference voltage	4.7uF capacitor to analog ground 1.71V ~ 1.9V (Default 1.8V is recommended)
				Total: 12 Pins

8. Power

There are different power types in CM7104. DBVDD1 is for digital I/O power, DCVDD1 is for digital core power, DCVDD3 is for DSP power, AVDD18 is for analog power, AVDD18_LOUT is for LOUT power, AVDD33 is for MICBIAS power.

Table 5. Power Supply for Best Performance

Power	DBVDD1	DCVDD1	DCVDD3	LDO_IN	AVDD18	AVDD18_LOUT	AVDD33
Setting	1.8V	1.2V	1.2V	1.8V	1.8V	1.8V	3.3V

*1.2V DCVDD1/3 is generated by internal LDO.

To prevent all power down leakage, we suggest supply power for each power pin of CM7104 or remove power for all power pin of CM7104.

Table 6. Power Supply Condition for Power Down Leakage

Power	DBVDD1	LDO_IN	AVDD18	AVDD18_LOUT	AVDD33
Condition	Supplied	Supplied	Supplied	Supplied	Supplied
Condition	Off	Off	Off	Off	Off

9. Function Description

9.1. Reset

There are 2 types of reset operation: power on reset (POR) and register reset.

Table 7. Reset Operation

Reset Type	Trigger Condition	CODEC Response
POR	Monitor digital power supply voltage reach V_{POR}	Reset all hardware logic and all registers to default values.
Register Reset	Write MX-00h	Reset all registers to default values except some specify control registers and logic.

9.1.1. Power-On Reset (POR)

When powered on, DCVDD passes through the V_{POR} band of the CM7104 (V_{POR_ON} ~V_{POR_OFF}). A power on reset (POR) will generate an internal reset signal (POR reset 'LOW') to reset the whole chip.

Table 8. Power-On Reset Voltage

Symbol	Min	Typical	Max	Unit
V_{POR_ON}	-	0.65	-	V
V_{POR_OFF}	-	0.55	-	V

Note:
1.V_{POR_OFF} must be below V_{POR_ON}
2. $T^oC = 25^oC$
3. When DCVDD is supplied 1.2V

9.1.2. Software Reset

When MX-00h is wrote, all registers become to default value.

9.2. Clocking

There are two clock systems in CM7104. One is for Codec, the other is for DSP. These two clock systems can be selected from PLL1/2, MCLK1 or internal clock.

The stereo DAC digital filter clock is from Clock_system. For other DAC/ADC stereo/mono digital filter can be selected from Clock_system ~ Clock_system8.

When enable ASRC (Asynchronous Sample Rate Converter) function, the clock sources from MCLK and BCLK1, BCLK2 are allowed to be asynchronous. The Cmedia ASRC technology can ensure data accuracy and keep audio performance under clock source asynchronous. The ASRC clock source is also can be selected from each interface (I2S1, I2S2).

When CM7104 at master mode, the clock source from Clock_system will be divided and be sent to external device. The ratio of BCLK and LRCK can set by register.

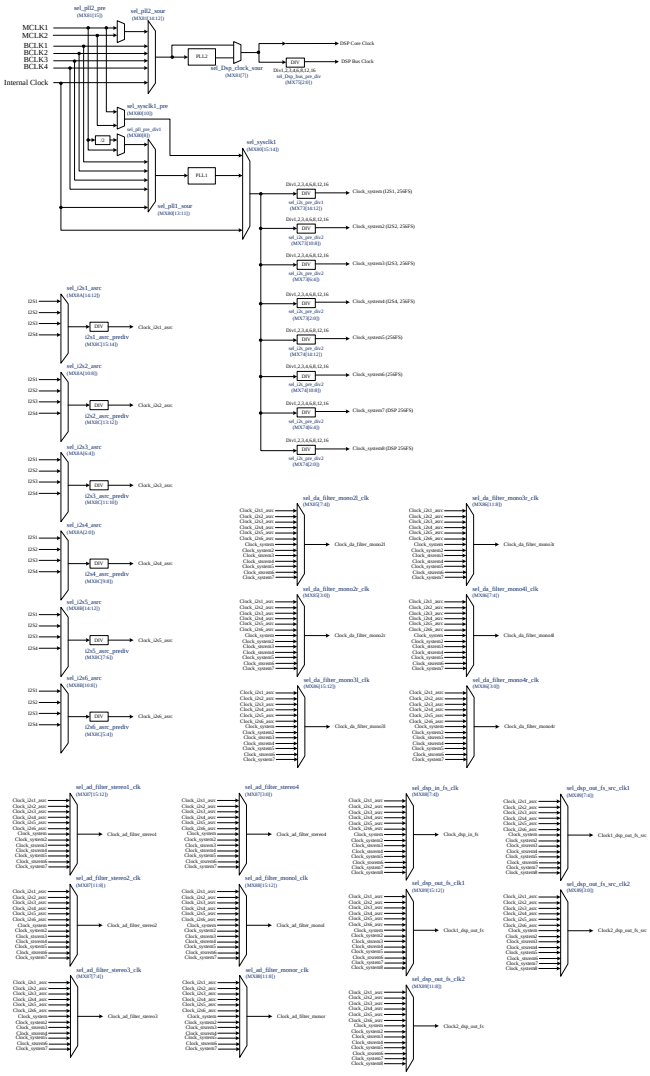


Figure 5. Audio Clock Tree

9.2.1. Phase-Locked Loop

There are two PLLs in CM7104. PLL1 dedicates for Codec (system clock, DAC clock, ADC clock or digital filter clock) used. PLL2 dedicates for DSP used. For each input of PLL1 and PLL2, please reference *Clock Tree Section* in detail.

These two PLLs can accept input frequency range is from 2MHz to 40MHz. Output frequency of PLL can depend-on PLL transmit formula to calculate:

$F_{OUT} = (F_{IN} * (N+2)) / ((M+2) * (K+2))$ {Note: M = -1 is bypass}

Table 9. PLL1 Clock Setting Table for 48K (Unit: MHz)

F_{IN} (MHz)	M	N	K	F_{OUT} (MHz)
2.048	-1	46	2	24.576
3.6864	1	78	2	24.576
4.096	-1	22	2	24.576
12	14	129	2	24.5625
13	14	119	2	24.57812
15.36	3	30	2	24.576
16	5	41	2	24.57143
19.2	15	85	2	24.5647
24	8	39	2	24.6

Table 10. PLL1 Clock Setting Table 11.1K (Unit: MHz)

F_{IN} (MHz)	M	N	K	F_{OUT} (MHz)
2.048	8	439	2	24.579
3.6864	0	47	2	22.576
4.096	15	373	2	22.588
12	15	126	2	22.588
13	15	116	2	22.558
15.36	15	98	2	22.588
16	12	77	2	22.571
19.2	15	78	2	22.588
24	15	62	2	22.588

Table 12. PLL2 Clock Setting Table (Unit: MHz)

F_{IN} (MHz)	M	N	K	F_{OUT} (MHz)
5.6448	-1	108	0	310.464
6.144	-1	99	0	310.272
11.2896	-1	53	0	310.464
12.288	0	99	0	310.272
19.2	1	95	0	310.4
22.5792	0	53	0	310.464
24.576	2	99	0	310.272
26	-1	22	0	312.0

PLL1/2 operation:

Power on sequences for PLL1/2:

1. Set PLL1/2 M/N/K code (MX-7A ~ MX-7D)
   =>Write to registers (MX-7A ~ MX-7D) for PLL parameter
2. Power on PLL1/2 (MX-64[8] & [9])
   =>Write "1" to MX-64[8] for power on PLL2
   =>Write "1" to MX-64[9] for power on PLL1
3. Check PLL1/2 ready status (MX-7B[0] & MX-7D[0])
   =>After 1ms, check MX-7B[0] is "1" or "0"? "1" means PLL1 ready for clock output
   =>After 1ms, check MX-7D[0] is "1" or "0"? "1" means PLL2 ready for clock output

Update PLL parameter sequences for PLL1/2 when PLL1/2 had power on:

1. Modify PLL1/2 M/N/K code (MX-7A ~ MX-7D)
   =>Write to registers (MX-7A ~ MX-7D) for PLL parameter
2. Update control for PLL1/2 (MX-7B[1] & MX-7D[1])
   =>Write "1" to MX-7B[1] then write "0" to MX-7B[1] for generate one trigger pulse to update PLL1 parameter
   =>Write "1" to MX-7D[1] then write "0" to MX-7D[1] for generate one trigger pulse to update PLL2 parameter
3. Check PLL1/2 ready status (MX-7B[0] & MX-7D[0])
   =>After 1ms, check MX-7B[0] is "1" or "0"? "1" means PLL1 ready for clock output
   =>After 1ms, check MX-7D[0] is "1" or "0"? "1" means PLL2 ready for clock output

9.3. Control Interface Configuration

There are three methods to control CM7104 global registers – I2C control interface and SPI control interface and DSP direct to control. When DSP power off that only I2C interface could control CM7104 global registers. If DSP power on that the CM7104 global registers could be controlled by I2C interface or SPI interface through DSP access global registers.

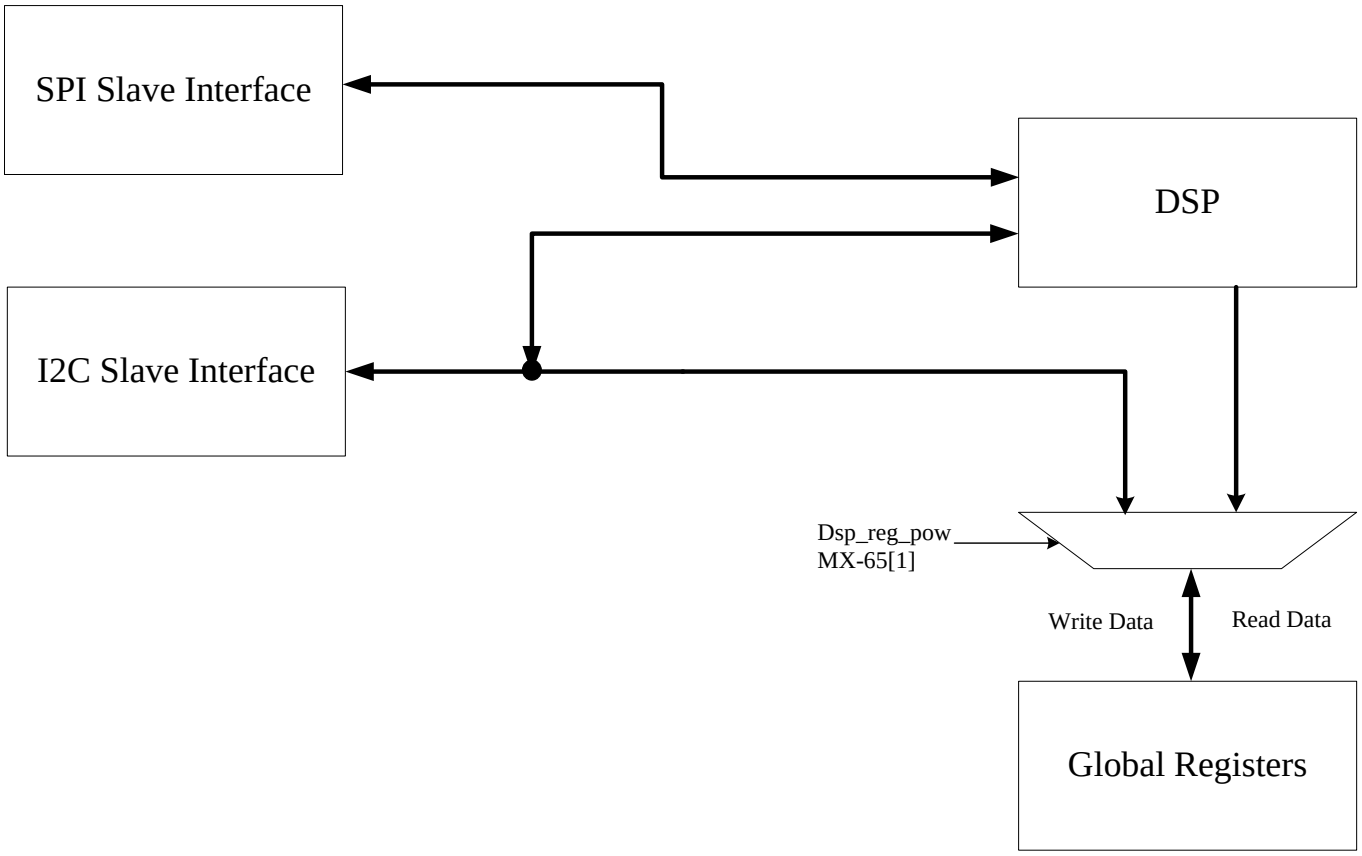


Figure 6. Control Interface Configuration

9.4. I²C and I²S/PCM/TDM Interface

The CM7104 supports I²C for the digital control interface. For digital data interface, CM7104 supports two I²S/PCM.TDM interface. These I²S/PCM audio digital interfaces are used to send data to 2 DACs or receive data from stereo ADC. These two I²S/PCM audio digital interfaces also can be configured to Master mode or Slave mode.

Master Mode

Under master mode, BCLK and LRCK are configured as output port and output clock signal base on internal system clock (SYSCLK). That has two kinds of clock can be selected, one is 32FS and the other is 64FS. For data format, CM7104 supports normal I2S, Left Justified, PCM Mode A and PCM Mode B, total four types can be supported.

The master mode clock source is selected from each I2S SYSCLK and I2S SYSCLK is selected from MCLK1 or PLL1. For each I2S SYSCLK has independent divider control, the independent divider control provides flexible clock output for each I2S interface. Refer to Figure 7. Audio Clock Tree, for details.

Table 13. The relative of SYSCLK/BCLK/LRCK

Mode	MCLK	BCLK	LRCK
32FS	256*FS=12.288MHz	32*FS=1.536MHz	FS=48KHz
64FS	256*FS=12.288MHz	64*FS=3.072MHz	FS=48KHz
32FS	256*FS=11.2896MHz	32*FS=1.4112MHz	FS=44.1KHz
64FS	256*FS=11.2896MHz	64*FS=2.8224MHz	FS=44.1KHz

Example for master mode:
Target format:
Sample Rate: 48 KHz
Channel Length: 32 bits
LRCK=48KHz
BCLK=3.072MHz (64 * 48KHz)

MCLK clock request:
MCLK=12.288MHz (256 * 48 KHz)

Register settings:
Set MX-FA[0] to “1” // For MCLK input clock getting control
Set MX-61[15] to “1” // Enable I2S-1
Set MX-70[15] to “0” // Enable Master mode
Set MX-3B[9:8] to “11” // Select 64*FS for BCLK in master mode
Set MX-73[14:12] to “000” // Select I2S-1 pre-divider

Slave Mode

Under slave mode BCLK and LRCK are configured as input port and receive clock signal. In synchronous I2S mode, MCLK and BCLK/LRCK should be synchronous. That means MCLK is equal to 256FS or 512FS, BCLK is equal to 64FS or 32FS and the clock rising edge of MCLK is aligned with BCLK.

In asynchronous I2S mode, MCLK and BCLK/LRCK are asynchronous and no any relationship. At this condition, needs to turn on internal ASRC function of CM7104. As Figure 8. In this connection, the MCLK is from external oscillator that clock is no relation (or asynchronous) with SOC and BT or 3G BaseBand. SOC (master mode) connects to I2S1 (slave mode) and BT (master mode) connects to I2S2 (slave mode). When turn on ASRC function, the SYSCLK is need to higher than 512FS clock rate. If the MCLK is lower than 512*FS, that can use internal PLL to generate higher than 512*FS clock.

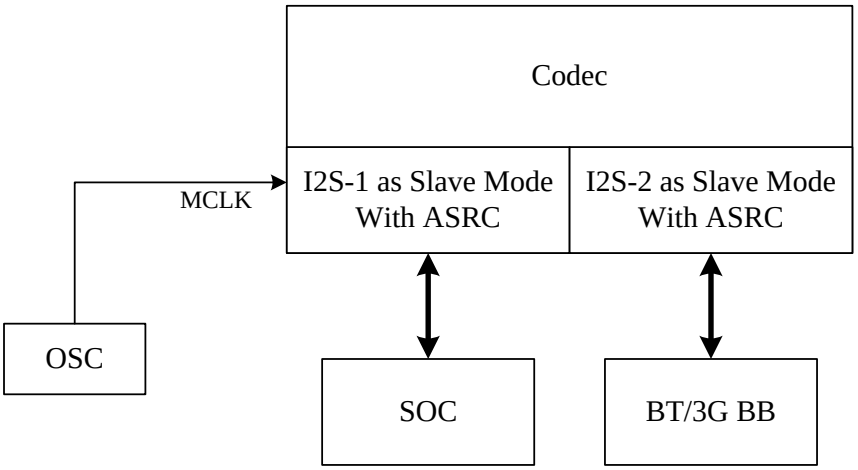


Figure 9. System Connection for ASRC Function

9.5. Digital Data Interface

9.5.1. I²S/PCM/TDM Interface

The two I2S/PCM interface can be configured as master mode or slave mode. Supported audio data formats are listed as below:

- PCM mode
  - Stereo PCM Mode A & Mode B
  - Mono PCM Mode A & Mode B
  - TDM mode-1 (Max. BCLK Rate is 12.288MHz => 48KHz * 32Bit * 8CH)
  - TDM mode-2 (Max. BCLK Rate is 9.6MHz => 48KHz * 25Bit * 8CH)
    - ✓ BCLK clock rate only support 50FS/100FS/150FS/200FS (FS is sample rate)
- I²S mode
  - Normal I2S mode
  - Left justified mode
  - TDM mode-1 (Max. BCLK Rate is 12.288MHz => 48KHz * 32Bit * 8CH)

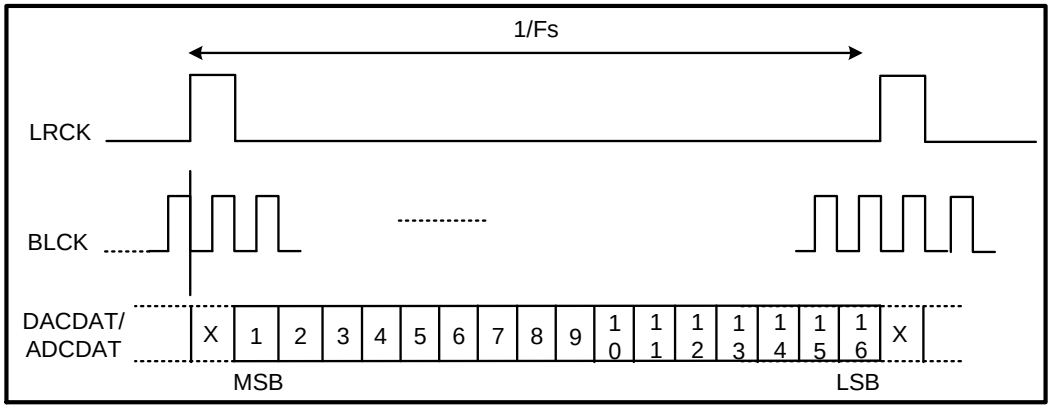


Figure 10. MONO PCM Data Mode A Format (BCLK POLARITY=0)

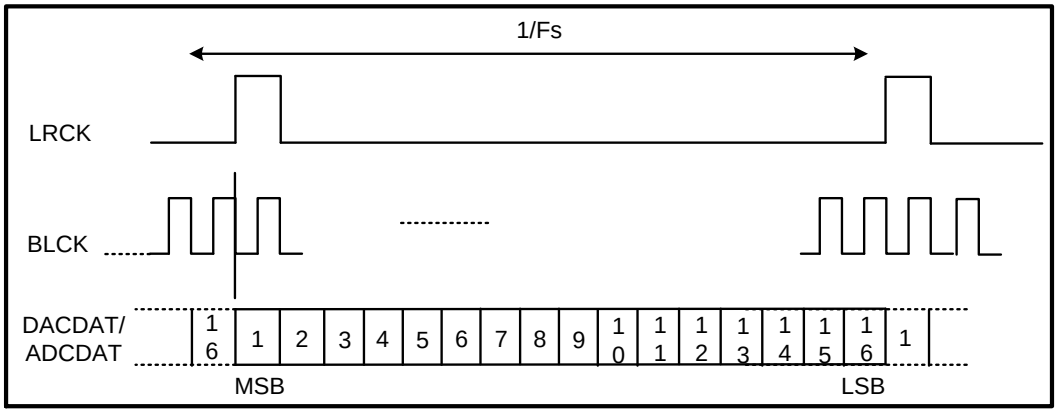


Figure 11. MONO PCM Data Mode B Format (BCLK POLARITY=0)

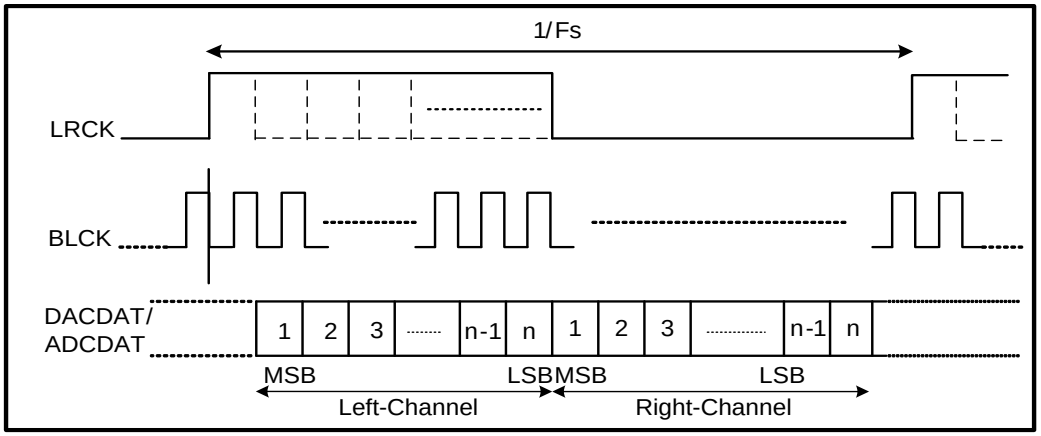


Figure 12. PCM Stereo Data Mode A Format (BCLK POLARITY=0)

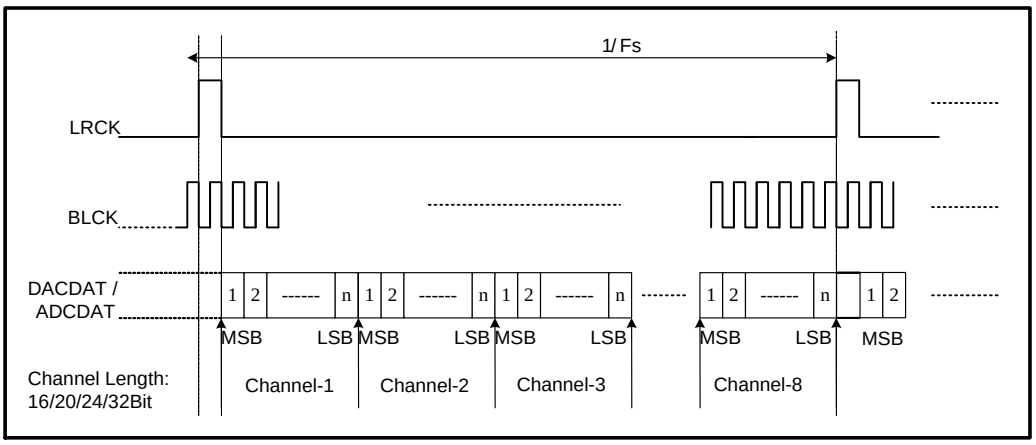


Figure 13. TDM Mode-1 PCM Data Mode A Format (BCLK POLARITY=0)

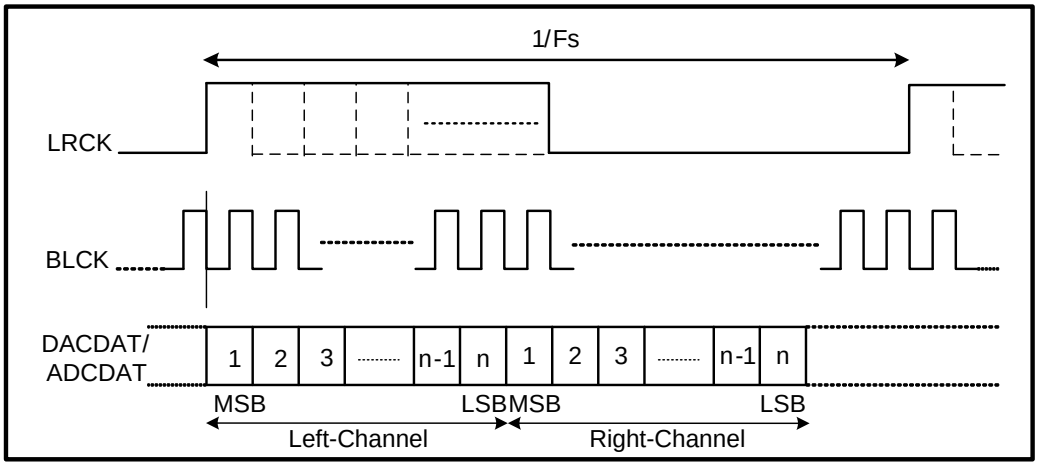


Figure 14. PCM Stereo Data Mode B Format (BCLK POLARITY=0)

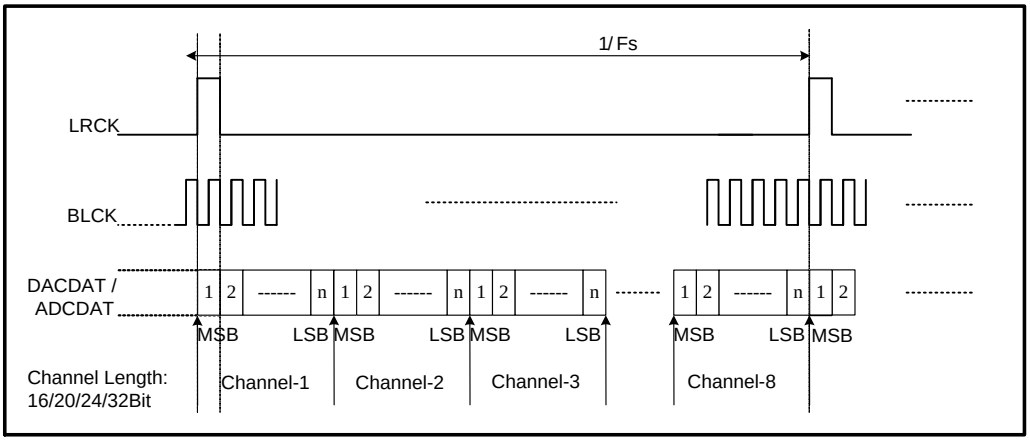


Figure 15. TDM Mode-1 PCM Data Mode B Format (BCLK POLARITY=0)

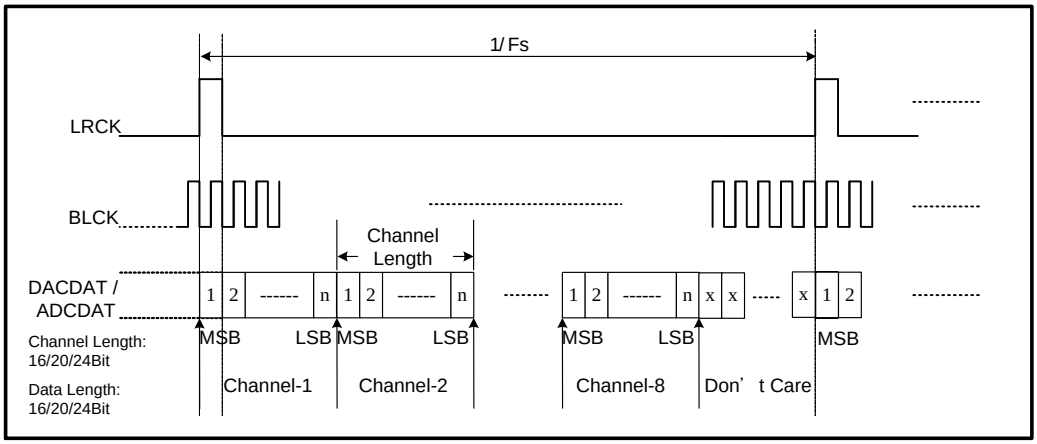


Figure 16. TDM Mode-2 PCM Data Mode B Format (BCLK POLARITY=0)

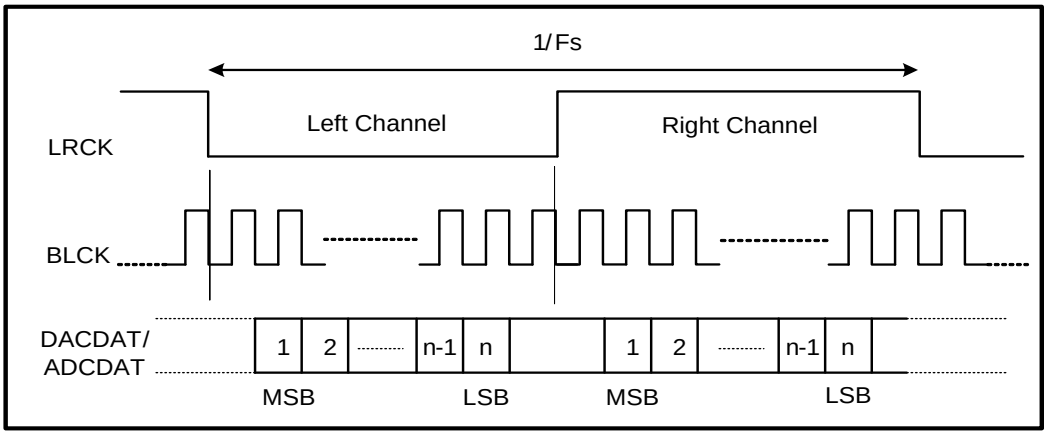


Figure 17. I²S Data Format (BCLK POLARITY=0)

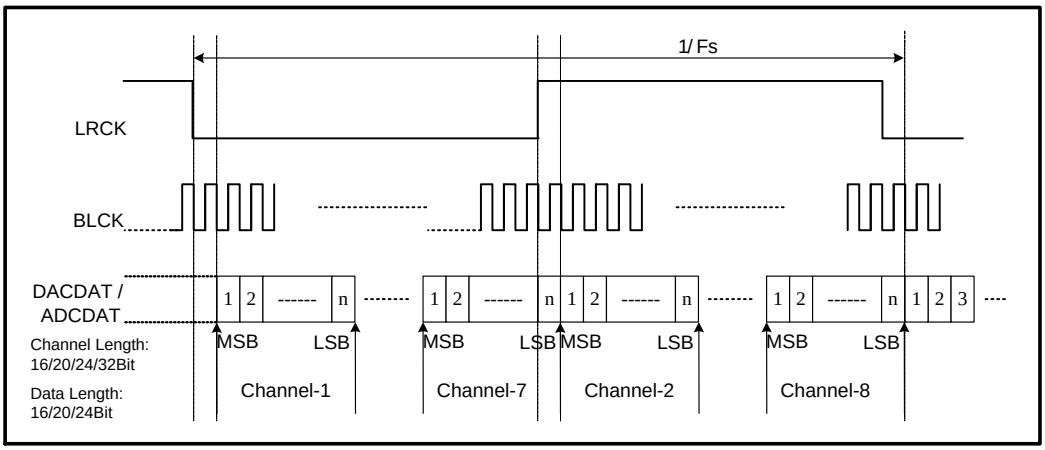


Figure 18. I²S TDM Data Format (BCLK POLARITY=0)

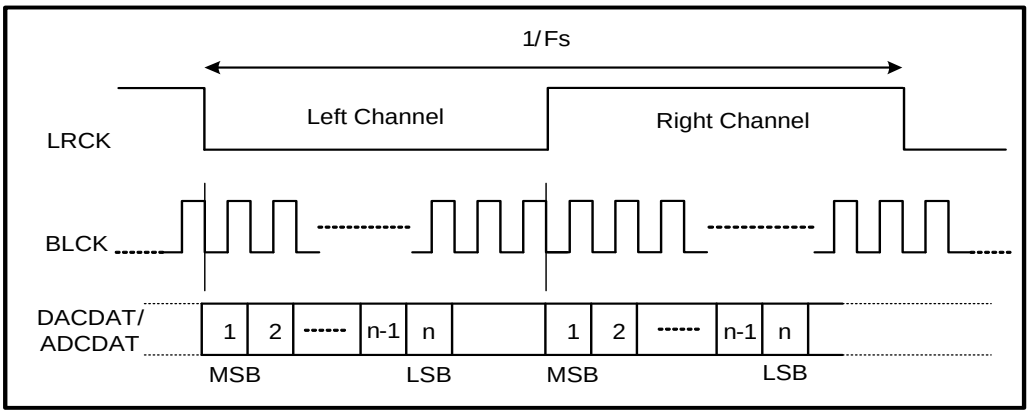


Figure 19. Left-Justified Data Format (BCLK POLARITY=0)

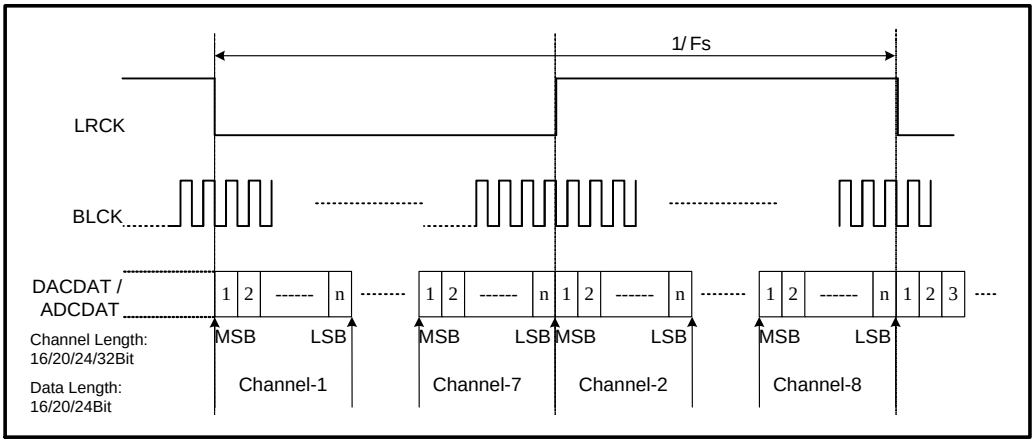


Figure 20. Left-Justified TDM Data Format (BCLK POLARITY=0)

9.6. Analog Audio Input Port

The CM7104 has two type analog input ports: microphone input and line input.

- **IN1P/IN1N**

  The port is a microphone type or line type input port. The input port can be configured as single-ended mode or differential mode by MX-03[7]. The microphone input port has its microphone bias and microphone boost. The low noise microphone bias can improve recording performance and enhance recording quality. Build-in short current detection scheme can be used for switch detection. Multi-steps microphone boost gain set by sel_bst1 (MX-03[15:12]) is easy to use for microphone application. Pow_bst1 can be used to power down the MIC1 boost and pow_micbias1 can be used to power down the microphone bias 1.

- **IN2P/IN2N**

  The IN2P/N is a dual type input port: microphone input and line input. Microphone input can be configured to differential input or single-ended input by MX-03[6]. Multi-steps microphone boost gain set by sel_bst2 (MX-03[11:8]) is easy to use for microphone application. Pow_bst2 can be used to power down the MIC2 boost.

9.7. Analog Audio Output Port

The CM7104 supports one type output port – line output:

- **Line_OUT_L/R**

  The output type is line type output. The output can configure as single ended output or differential output. The input only from DAC output.

9.8. Multi-Function Pins

GPIO1 is a multi-function pin in CM7104. For different functions of each pin are controlled by register. You need to set the right register settings for each multi-function pins on your application.

- **GPIO1/IRQ – Pin 33**

The pin default is GPIO function. It can change to IRQ function by write MX-C0[15] to 1’b.

9.9. DRC and AGC Function

The CM7104 supports multi-band DRC. It uses crossover filter to separate low frequency band and high frequency band. The low frequency band signal will pass Bass DRC block then sum with Normal DRC signal. The corner frequency of crossover filter can be adjusted by register settings. Which range is from 6KHz to 50Hz on 48KHz sample rate. The following figure shows the function block.

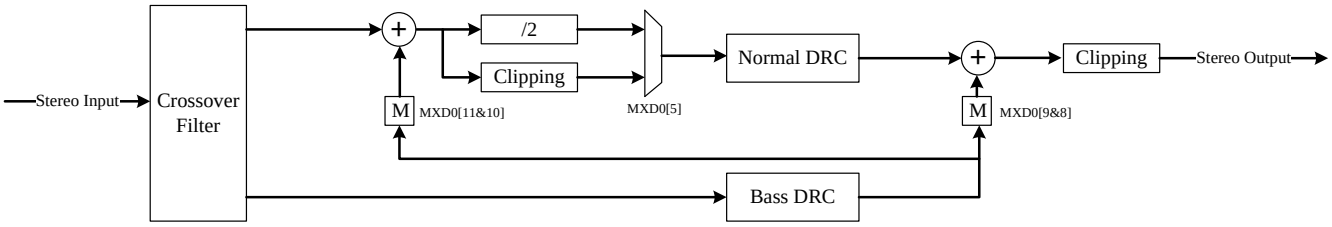


Figure 21. DAC DRC Function Block

Crossover Filter Coefficient Calculation

Corner Frequency is Fc, Sample Rate is Fs.
First order low-pass-filter:
Wp = tan ((180*Fc)/Fs)
A1 = Hex(((-)(Wp – 1) / (Wp + 1)) * (2^22))
A2 = 0
H0 = Hex((Wp / (Wp + 1)) * (2^22))

First order high-pass-filter:
Wp = tan ((180*Fc)/Fs)
A1 = Hex(((-)(Wp – 1) / (Wp + 1)) * (2^22))
A2 = 0
H0 = Hex((1 / (Wp + 1)) * (2^22))

Second order low-pass-filter:
Wp = tan ((180*Fc)/Fs)
A1 = Hex(((-)(2*(Wp^2 – 1)) / (Wp^2 + sqrt(2)*Wp + 1)) * (2^22))
A2 = Hex(((-)(Wp^2 – sqrt(2) + 1) / (Wp^2 + sqrt(2)*Wp + 1)) * (2^22))
H0 = Hex((Wp^2 / (Wp^2 + sqrt(2)*Wp + 1)) * (2^22))

Second order high-pass-filter:
Wp = tan ((180*Fc)/Fs)
A1 = Hex(((-)(2*(Wp^2 – 1)) / (Wp^2 + sqrt(2)*Wp + 1)) * (2^22))
A2 = Hex(((-)(Wp^2 – sqrt(2) + 1) / (Wp^2 + sqrt(2)*Wp + 1)) * (2^22))
H0 = Hex((1 / (Wp^2 + sqrt(2)*Wp + 1)) * (2^22))

The Dynamic Range Controller (DRC) dynamically adjusts the input signal and let the output signal achieve the target level. The CM7104 supports playback DRC for DAC path, and the DRC can also be used as AGC(Auto Gain Controller) for ADC path. The control register is at MX-D3[15:14]. The function block is shown as below. The signal input pass through the Pre-Gain first, then DRC volume and Post-Gain then output. The Pre-Gain is use to enlarge the input signal. The DRC volume is use to attenuate the signal after detected by DRC. The Post-Gain is use to fine tune the signal after pass DRC tuning.

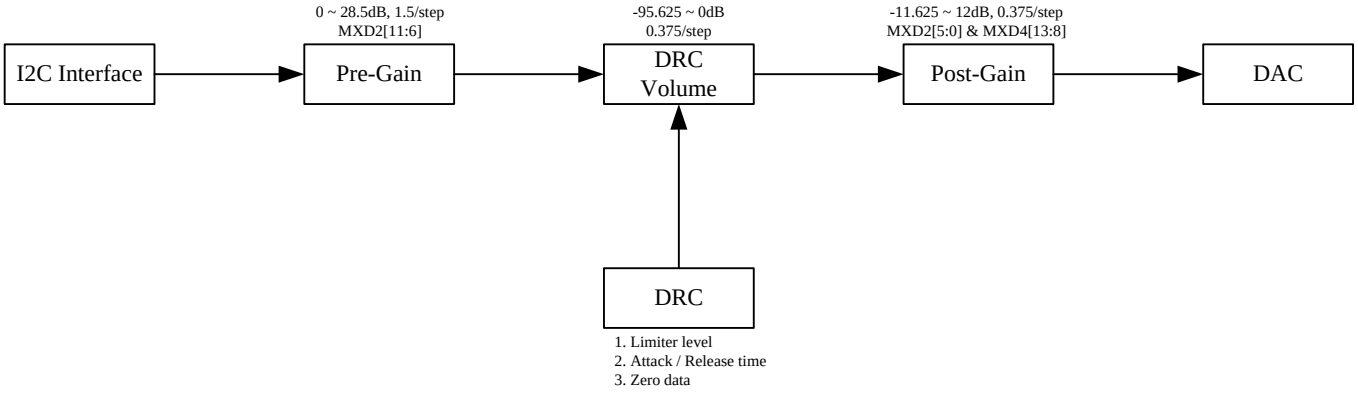


Figure 22. DAC DRC Function Block

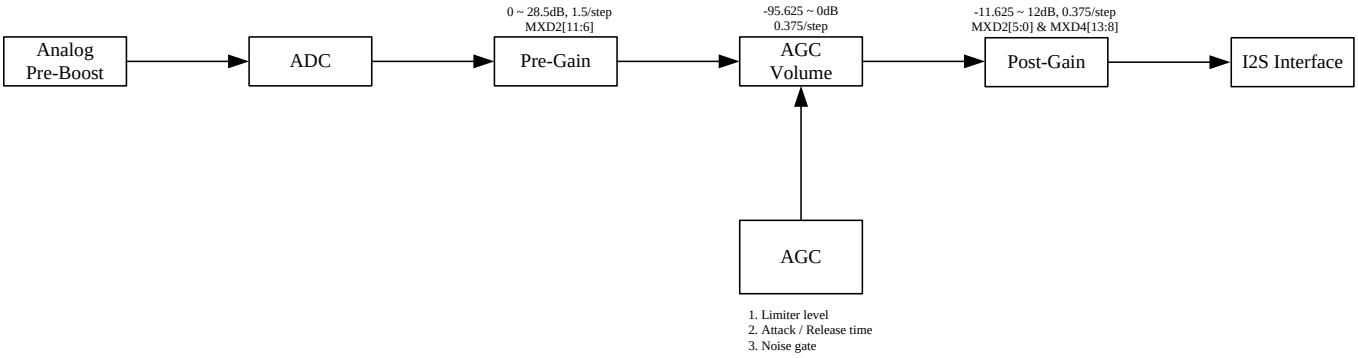


Figure 23. ADC AGC Function Block

DRC Output Curve - Playback Mode:

The Figure 28 shows DRC output curve for DAC playback application.

Alc_thmax(High frequency band: MX-D6[5:0] / Low frequency band: MX-DC[5:0]):
The parameter limits the maximum output level when 0dB full scale input. The limit range is from 0dBFS to -23.625dBFS.

Ratio_1(High frequency band: MX-D4[6:5] / Low frequency band: MX-DA[6:5]):
The parameter determines the slope begin from start point. There are 4 slopes can be selected.

Alc_thmax2(High frequency band: MX-D6[11:6] / Low frequency band: MX-DC[11:6]):
The parameter determines the first knee from ratio_1 curve. The range is from 0dBFS to -45dBFS.

Ratio_2(High frequency band: MX-D4[15:14] / Low frequency band: MX-DA[15:14]):
The parameter determines the slope begin from first knee. There are 4 slopes can be selected.
The second knee is calculated by internal circuit. It bases on ratio_2 and alc_thmin to calculate.

Alc_thmin(High frequency band: MX-D5[10:5] / Low frequency band: MX-DB[10:5]):
The parameter determines the third knee from previous curve. The range is from -60dBFS to -94.5dBFS.

Ratio_3(High frequency band: MX-D4[1:0] / Low frequency band: MX-DA[1:0]):
The slope is determined by third knee and end point. The end point is determined by boost gain on MX-D2[11:6] register.

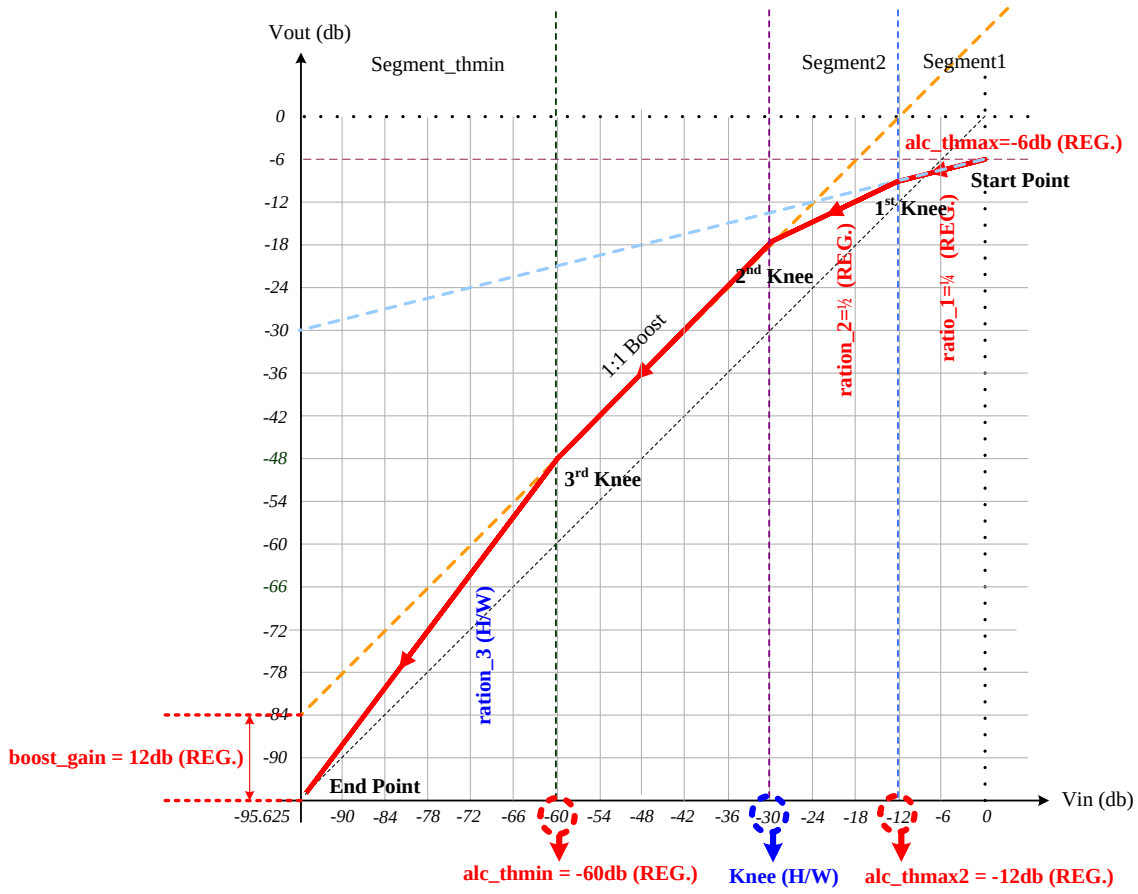


Figure 24. Playback DRC Output Curve

DRC Output Curve - Record Mode 1:

The Figure 28 shows DRC output curve for ADC record application.

Alc_thmax(MX-D6[5:0]):

The parameter limits the maximum output level when 0dB full scale input. The limit range is from 0dBFS to -23.625dBFS.

Ratio_1(MX-D4[6:5]):

The parameter determines the slope begin from start point. There are 4 slopes can be selected.

Alc_thmax2(MX-D6[11:6]):

The parameter determines the first knee from ratio_1 curve. The range is from 0dBFS to -45dBFS.

Ratio_2(MX-D4[15:14]):

The parameter determines the slope begin from first knee. There are 4 slopes can be selected.
The second knee is calculated by internal circuit. It bases on ratio_2 and alc_thnoise to calculate.

Alc_thnoise(MX-D5[4:0]):

The parameter determines the third knee from previous curve. The range is from -24dBFS to -70.5dBFS.

Noise_gate_ratio(MX-D4[1:0]):

The parameter determines the slope begin from third knee. There are 4 slopes can be selected.
The end point is determined by third knee and noise_gate_ratio.

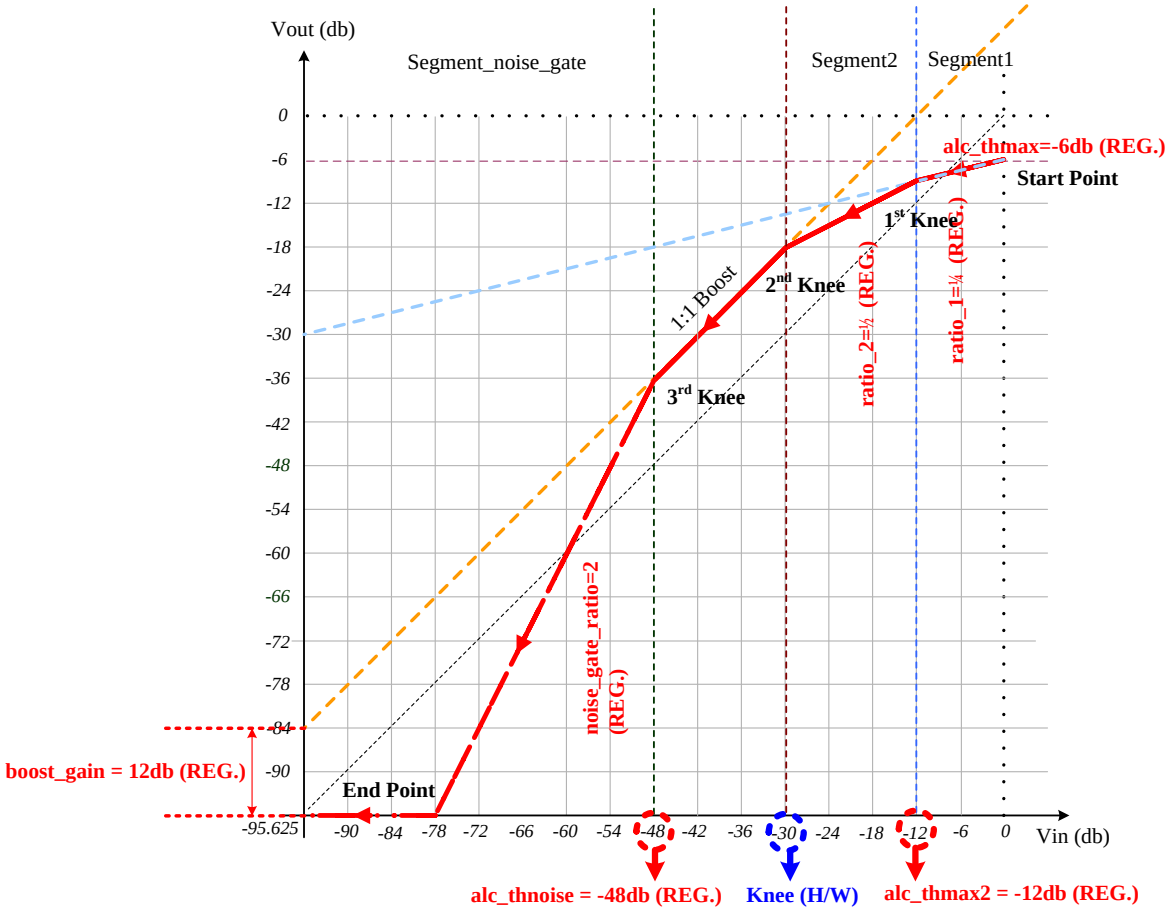


Figure 25. Record DRC Output Curve - 1

DRC Output Curve - Record Mode 2:

The Figure 29 shows another DRC output curve for ADC record application.

Alc_thmax(MX-D6[5:0]):

The parameter limits the maximum output level when 0dB full scale input. The limit range is from 0dBFS to -23.625dBFS.

Ratio_1(MX-D4[6:5]):

The parameter determines the slope begin from start point. There are 4 slopes can be selected.

Alc_thmax2(MX-D6[11:6]):

The parameter determines the first knee from ratio_1 curve. The range is from 0dBFS to -45dBFS.

Ratio_2(MX-D4[15:14]):

The parameter determines the slope begin from first knee. There are 4 slopes can be selected.
The second knee is calculated by internal circuit. It bases on ratio_2 and alc_thnoise to calculate.

Alc_thnoise(MX-D5[4:0]):

The parameter determines the third knee from previous curve. The range is from -24dBFS to -70.5dBFS. From third knee to fourth knee is a noise drop function by enable noise gate drop mode at MX-B5[4]. The drop level is determined by boost_gain (MX-D2[11:6]) and alc_noise_gate_exp (MX-D5[15:12]).

Noise_gate_ratio(MX-D5[1:0]):

The parameter determines the slope begin from fourth knee. There are 4 slopes can be selected. The end point is determined by fourth knee and noise_gate_ratio.

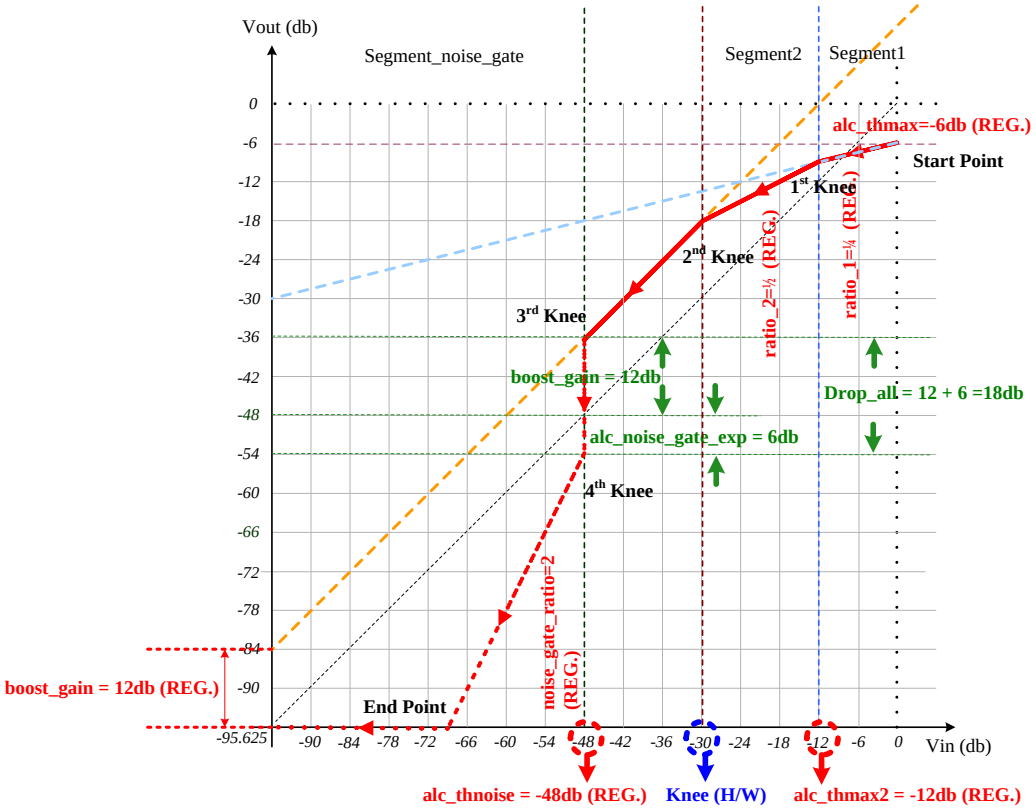


Figure 26. Record DRC Output Curve - 2

9.10. Equalizer Block

The CM7104 supports independent EQ function for DAC playback and ADC record.

For DAC playback path, the equalizer block cascades 11 bands of equalizer to each channel to tailor the frequency characteristics of embedded speaker system according to user preferences and to emulate environment sound. The 11 bands equalizer includes three high pass filters, five band pass filters, two low pass filter and one biquad filter. One high pass filter cascaded in the front end is used to drop low frequency tone, The tone has a large amplitude and may damage a mini speaker. The high pass filter can be used to adjust Treble strength with gain control. One low pass filter with gain control can adjust the Bass strength. Three bands of band pass filters are used to emulate environment sounds, e.g., 'Pub', 'Live', 'Rock',… etc.. The gain, center frequency and bandwidth of each filter are all programmable. One biquad filter can switch to high-pass, low-pass or band-pass filter by register settings.

For ADC record path, the equalizer block cascades 6 bands of equalizer to stereo channel. The equalizers can used to do microphone device frequency compensation. The 6 bands equalizer include one low-pass-filter, four band-pass-filter and one high-pass-filter. The gain, center frequency and bandwidth of filter are also all programmable.

9.11. Wind Noise Reduction Filter

The wind filter is implemented by a high pass filter equalizer. The wind filter is mainly for ADC recording used. The cut-off freqnecy of wind filter is programmable and is varied accroding to different sample rate. The filter is used to remove DC offset at normal condition, and to remove wind noise at application mode.

There are three wind filters for three ADC filters:

Stereo1 ADC Wind Filter => MX-C5 & MX-C6

Mono ADC Wind Filter => MX-C7 & MX-C8

Stereo2 ADC Wind Filter => MX-C9 & MX-CA

Stereo3 ADC Wind Filter => MX-CB & MX-CC

Stereo4 ADC Wind Filter => MX-CD & MX-CE

Wind filter setting procedure (For example: Stereo1 ADC Filter):

Step1: Disable wind filter – MX-C5[15]

Step2: Select filter coarse coefficient – MX-C5[14:12] and MX-C5[10:8]

Step3: Select filter fine coefficient – MX-C6[13:8] and MX-C6[5:0]

Step4: Enable wind filter – MX-C5[15]

The following table (Table 14.) is shown the Fc with sample rate selection.
For the formula of Fc calculation is also shown as:

$Fc = (Fs * \tan^{-1}(a/(2-a))) / \pi$

Where:
Sample rate = 8K/12K/16K (MX-C5[14:12] and [10:8]), $a = 2^{-6} + n * 2^{-6}$ (n is MX-C6[13:8] & MX-D4[5:0])
Sample rate = 24K/32K (MX-C5[14:12] and [10:8]), $a = 2^{-7} + n * 2^{-7}$ (n is MX-C6[13:8] & MX-D4[5:0])
Sample rate = 44.1K/48L (MX-C5[14:12] and [10:8]), $a = 2^{-8} + n * 2^{-8}$ (n is MX-C6[13:8] & MX-D4[5:0])
Sample rate = 88.2K/96L (MX-C5[14:12] and [10:8]), $a = 2^{-9} + n * 2^{-9}$ (n is MX-C6[13:8] & MX-D4[5:0])
Sample rate = 176.4K/192L (MX-C5[14:12] and [10:8]), $a = 2^{-10} + n * 2^{-10}$ (n is MX-C6[13:8] & MX-D4[5:0])

Table 14. Sample Rate with filter coefficient for Wind Filter

PR-6E[11:6]	L & R Channel Sample Rate Setting				
n	8K	16K	32K	44.1K	48K
000000’b, 0	20.0	40.1	39.9	27.4	29.8
000001’b, 1	40.4	80.8	80.2	55.0	59.9
000010’b, 2	61.1	122.2	120.7	82.7	90.0
000011’b, 3	82.1	164.2	161.6	110.5	120.3
000100’b, 4	103.4	206.9	202.8	138.4	150.6
000101’b, 5	125.1	250.2	244.4	166.4	181.1
000110’b, 6	147.1	294.3	286.2	194.5	211.7
000111’b, 7	169.5	339.0	328.4	222.7	242.5
001000’b, 8	192.2	384.4	371.0	251.1	273.3
001001’b, 9	215.2	430.5	413.8	279.5	304.3
001010’b, 10	238.7	477.4	457.0	308.1	335.4
001011’b, 11	262.4	524.9	500.5	336.8	366.6
001100’b, 12	286.6	573.2	544.4	365.6	397.9
001101’b, 13	311.1	622.3	588.6	394.5	429.4
001110’b, 14	336.0	672.1	633.2	423.5	460.9
001111’b, 15	361.3	722.6	678.1	452.6	492.6
010000’b, 16	386.9	773.9	723.3	481.9	524.5
010001’b, 17	413.0	826.0	768.9	511.2	556.4
010010’b, 18	439.4	878.9	814.9	540.7	588.5
010011’b, 19	466.2	932.5	861.2	570.3	620.7
010100’b, 20	493.5	987.0	907.8	600.0	653.0
010101’b, 21	521.1	1042.2	954.9	629.8	685.5
010110’b, 22	549.1	1098.2	1002.2	659.7	718.1
010111’b, 23	577.5	1155.0	1050.0	689.8	750.8

PR-6E[11:6] n	L & R Channel Sample Rate Setting				
	8K	16K	32K	44.1K	48K
011000'b, 24	606.3	1212.7	1098.1	719.9	783.6
011001'b, 25	635.5	1271.1	1146.6	750.2	816.6
011010'b, 26	665.1	1330.3	1195.5	780.6	849.6
011011'b, 27	695.2	1390.4	1244.7	811.1	882.9
011100'b, 28	725.6	1451.2	1294.3	841.8	916.2
011101'b, 29	756.4	1512.9	1344.3	872.5	949.7
011110'b, 30	787.6	1575.3	1394.7	903.4	983.3
011111'b, 31	819.3	1638.6	1445.4	934.4	1017.0
100000'b, 32	851.3	1702.7	1496.5	965.5	1050.9
100001'b, 33	883.7	1767.5	1548.0	996.8	1084.9
100010'b, 34	916.6	1822.3	1599.9	1028.1	1119.0
100011'b, 35	949.8	1899.6	1652.2	1059.6	1153.3
100100'b, 36	983.3	1966.7	1704.9	1091.2	1187.7
100101'b, 37	1017.3	2034.7	1757.9	1122.9	1222.2
100110'b, 38	1051.6	2103.3	1811.4	1154.8	1256.9
100111'b, 39	1086.3	2172.7	1865.2	1186.7	1291.7
101000'b, 40	1121.4	2242.9	1919.5	1218.8	1326.6
101001'b, 41	1156.8	2313.7	1974.1	1251.0	1361.7
101010'b, 42	1192.6	2385.2	2029.1	1283.4	1396.9
101011'b, 43	1228.7	2457.4	2084.6	1315.8	1432.2
101100'b, 44	1265.1	2530.2	2140.4	1348.4	1467.7
101101'b, 45	1301.8	2603.6	2196.6	1381.1	1503.3
101110'b, 46	1338.8	2677.7	2253.3	1414.0	1539.0
101111'b, 47	1376.1	2752.3	2310.3	1447.0	1574.9
110000'b, 48	1413.7	2827.5	2367.7	1480.0	1610.9
110001'b, 49	1451.5	2903.1	2425.5	1513.3	1647.1
110010'b, 50	1489.6	2979.3	2483.8	1546.6	1683.4
110011'b, 51	1528.0	3056.0	2542.4	1580.1	1719.8
110100'b, 52	1566.5	3133.1	2601.5	1613.7	1756.4
110101'b, 53	1605.3	3210.6	2660.9	1647.4	1793.1
110110'b, 54	1644.2	3288.4	2720.8	1681.3	1830.0
110111'b, 55	1683.3	3366.6	2781.0	1715.3	1867.0
111000'b, 56	1722.5	3445.1	2841.7	1749.4	1904.1
111001'b, 57	1761.9	3523.9	2902.7	1783.6	1941.4
111010'b, 58	1801.4	3602.9	2964.2	1818.0	1978.8
111011'b, 59	1841.0	3682.1	3026.1	1852.5	2016.3
111100'b, 60	1880.7	3761.4	3088.3	1887.1	2054.0
111101'b, 61	1920.4	3840.8	3151.0	1921.9	2091.9
111110'b, 62	1960.2	3920.4	3214.1	1956.8	2129.9
111111'b, 63	2000.0	4000.0	3277.5	1991.8	2168.0

9.12. I²C Control Interface

I²C is a 2-wire (SCL/SDA) half-duplex serial communication interface, supporting only slave mode. SCL is used for clock and SDA is for data. SCL clock supports up to 400KHz rate and SDA data is a open drain structure. The input has built-in spike filter and can remove less than 50ns spike at SCL and SDA.

9.12.1. Address Setting

Table 15. Address Setting (0x58h)

(MSB)			BIT				(LSB)
0	1	0	1	1	0	0	R/W

9.12.2. Complete Data Transfer

Data Transfer over I²C Control Interface

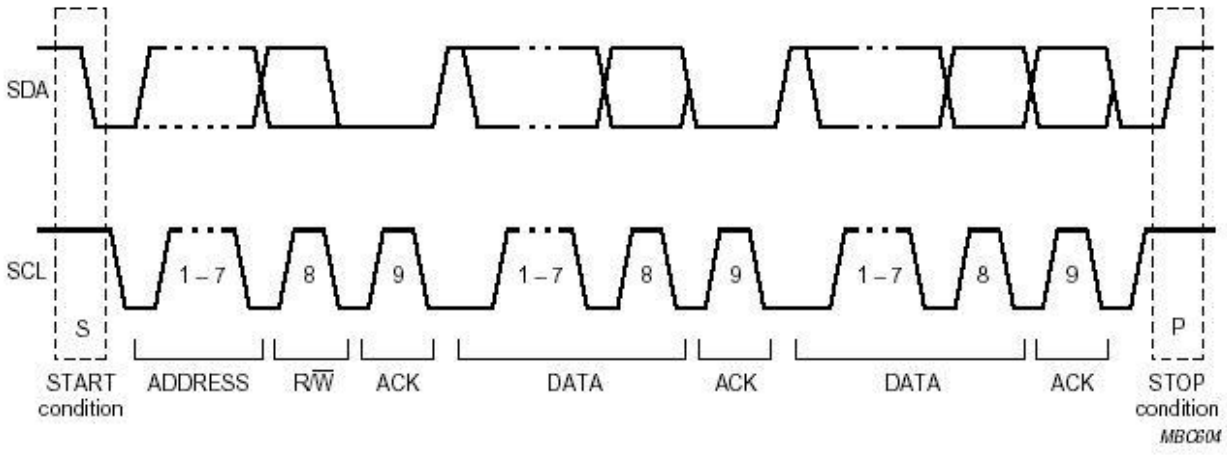
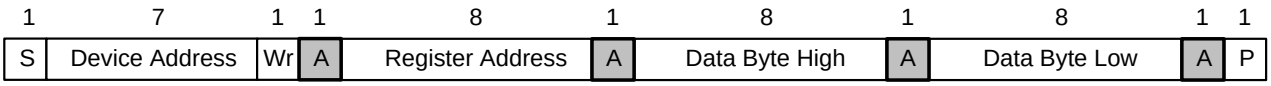


Figure 27. Data Transfer Over I²C Control Interface

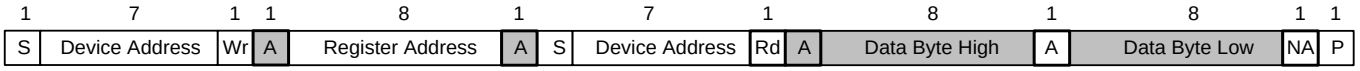
Write WORD Protocol

Table 16. Write WORD Protocol



Read WORD Protocol

Table 17. Read WORD Protocol



S: Start Condition
Slave Address: 7-bit Device Address
Wr: 0 for Write Command
Rd: 1 for Read Command
Command Code: 8-bit Register Address

A: 0 for ACK, 1 for NACK
Data Byte: 16-bit Mixer data
□: Master-to-Slave
□: Slave-to-Master

9.12.3. Memory Map Conversion for I2C Control Interface

When in DSP mode (power-on DSP), read/write registers by I2C interface needs to use memory map method to convert. For global control registers locate at 0x1802_0000 ~ 0x1802_1000. Please refer to section 8.5 for DSP APB address map.

Register: 0x00				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:2	R	0'h	Reserved
Op_code	1:0	R/W	1'h	Operation Mode Control 00'b: Reserved 01'b: 16-bit Write 10'b: 32-bit Read 11'b: 32-bit Write

Register: 0x01				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
I2c_port_address	15:0	R/W	0'h	Memory Address[15:0]

Register: 0x02				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
I2c_port_address	15:0	R/W	0'h	Memory Address[31:16]

Register: 0x03				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
I2c_port_data	15:0	R/W	0'h	Memory Address Data[15:0]

Register: 0x04				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
I2c_port_data	15:0	R/W	0'h	Memory Address Data[31:16]

9.13. SPI Slave Mode Control Interface

The SPI interface was only supported slave mode in CM7104. The transmit rate is up to 28MHz.

SPI Write Command:

CMD Phase	Address Phase	Data Phase	Dummy Phase

	CMD Phase	Address Phase	Data Phase	Dummy Phase	ACK
Single 16 bits write	0x01	32 bits	16 bits	8bits	1bit
single 32 bits write	0x03	32 bits	32 bits	8bits	1bit
Burst write	0x05	32 bits	64*4 bits	8bits	1bit per 64bits
Single 16 bits write with 8-bit address	0x09	8 bits	16 bits	8bits	1 bit

CMD PHASE: 8 bits command code
Address Phase: System bus memory space address
Data Phase: Write data
Dummy Phase: System bus write data
ACK Phase: Response ACK to spi_sdo pin

SPI Read Command:

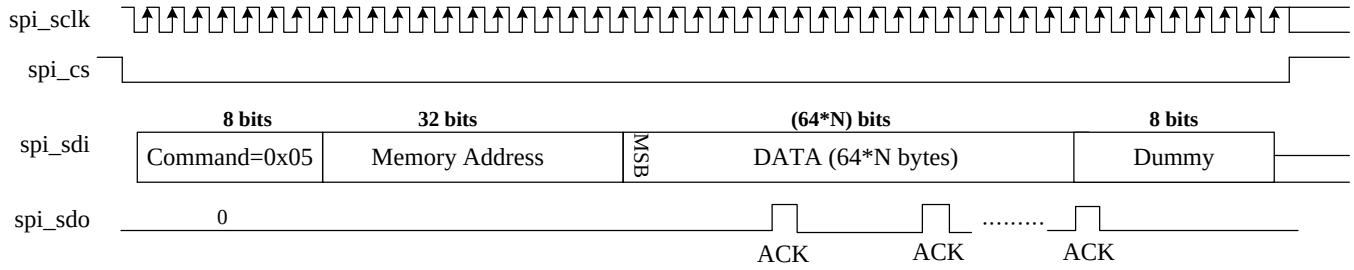
CMD Phase	Address Phase	Dummy Phase	Data Phase

	CMD Phase	Address Phase	Dummy Phase	Data Phase	ACK
Single 16 bits read	0x00	32 bits	32 bits	16 bits	0 bit
single 32 bits read	0x02	32 bits	32 bits	32 bits	0 bit
Burst read	0x04	32 bits	32 bits	64*4 bits	0 bit
Single 16 bits read with 8-bit address	0x08	8 bits	32 bits	16 bits	0 bit

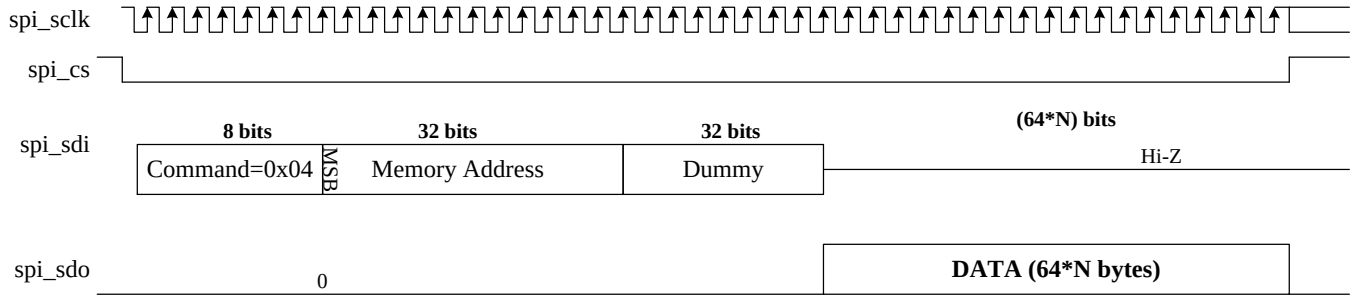
CMD PHASE: 8 bits command code
Address Phase: System bus memory space address
Dummy Phase: System bus prepare data
Data Phase: Read data

Burst Write Mode:

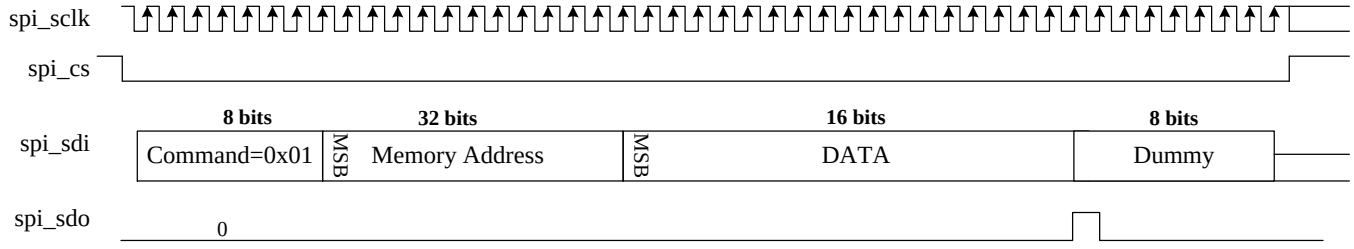
Burst Write Mode:



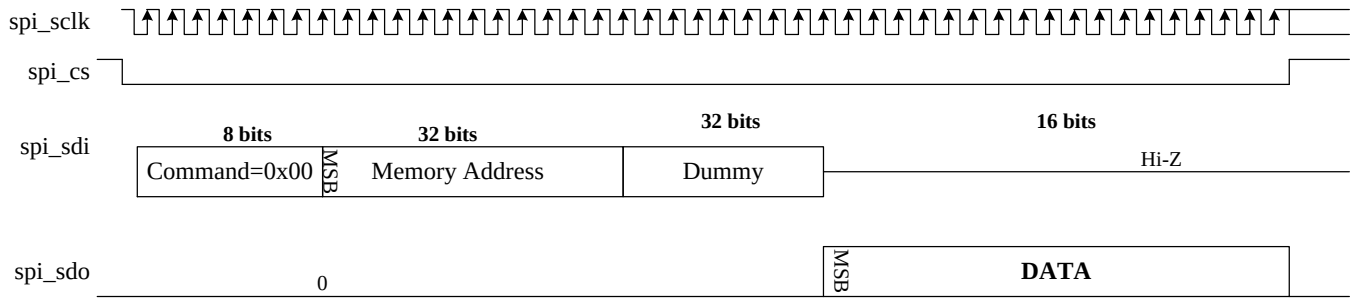
Burst Read Mode:



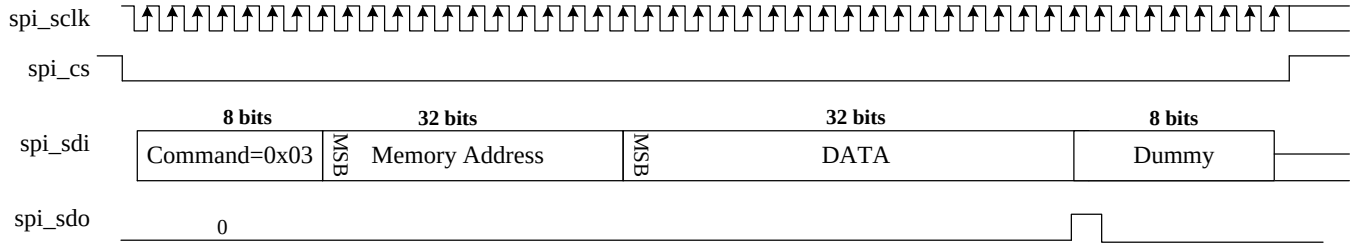
Single 16 bits Write Mode:



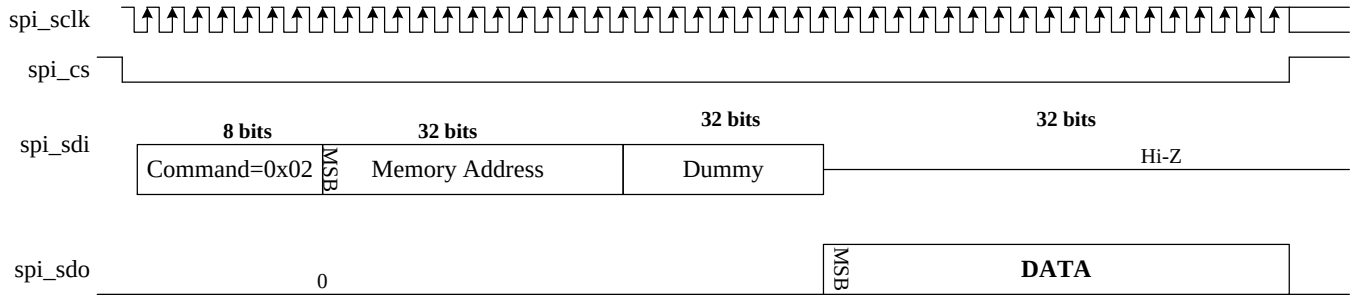
Single 16 bits Read Mode:



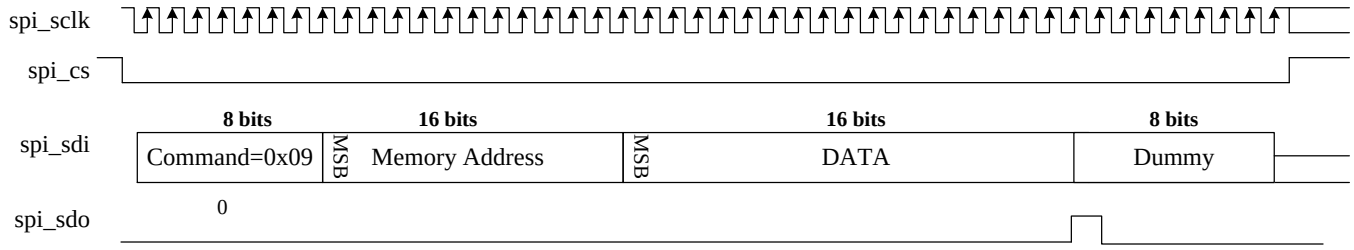
Single 32 bits Write Mode:



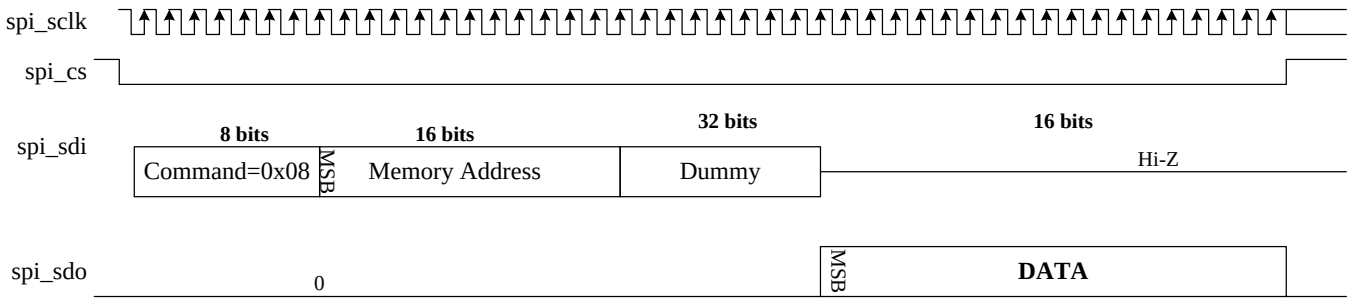
Single 32 bits Read Mode:



Single 16 bits Write Mode with 16 bits Address:



Single 16 bits Read Mode with 16 bits Address:



9.14. I2C Master Mode Control Interface

CM7104 can support a 2-wire (SCL/SDA) I^2C master serial communication interface. SCL is used for clock and SDA is for data. SCL clock supports up to 400KHz rate.

7 Bits Device ID

There are 7 bits device ID can be set. 0x0000 000x'b ~ 0x1111 111x'b

Table 18. 7-Bits Device ID

(MSB)			BIT				(LSB)
x	x	x	x	x	x	X	R/W

Register Address ID

There are up to 5 bytes register address ID can be set.

Register Data

There are up to 5 bytes register data can be set.

I2C Format

Table 19. I2C Master Mode Format

Register Write Format

1	7	1	1	8	1	8	1	8	1	8	1	8	1	8	1	8	1	8	1	8	1	1
S	Device ID	W	A	Register Address (A39 ~ A32)	A	Register Address (A31 ~ A24)	A	Register Address (A23 ~ A16)	A	Register Address (A15 ~ A8)	A	Register Address (A7 ~ A0)	A	Register Data (D31 ~ A24)	A	Register Data (D23 ~ A16)	A	Register Data (D15 ~ A8)	A	Register Data (D7 ~ A0)	A	P

Register Read Format

1	7	1	1	8	1	8	1	8	1	8	1	1	7	1	1	8	1	8	1	8	1	8	1	8	1	1
S	Device ID	W	A	Register Address (A39 ~ A32)	A	Register Address (A31 ~ A24)	A	Register Address (A23 ~ A16)	A	Register Address (A15 ~ A8)	A	Register Address (A7 ~ A0)	A	S	Device ID	R	A	Register Data (D31 ~ A24)	A	Register Data (D23 ~ A16)	A	Register Data (D15 ~ A8)	A	Register Data (D7 ~ A0)	A	P

9.15. GPIO, Interrupt

The CM7104 supports one GPIO – GPIO1. For GPIO function, the GPIO can be configured to input or output. For input type, the internal circuit can read pin status and report to register table. For output type, the internal circuit can drive this pin to high or low to control external device. In GPIO function, the pin polarity can be controlled by register at output type.

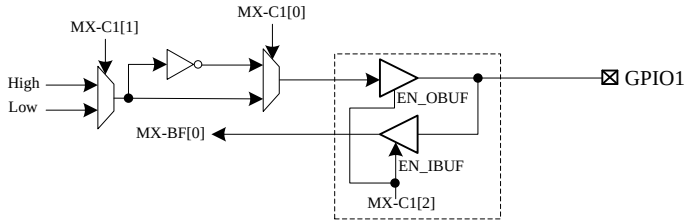


Figure 28. GPIO Function Block

For IRQ function as shown on below figure, when either status is trigged, the IRQ pin will output a change as interrupt signal. For SAD flag, it also can as an interrupt (DSP_IRQ_0) of DSP

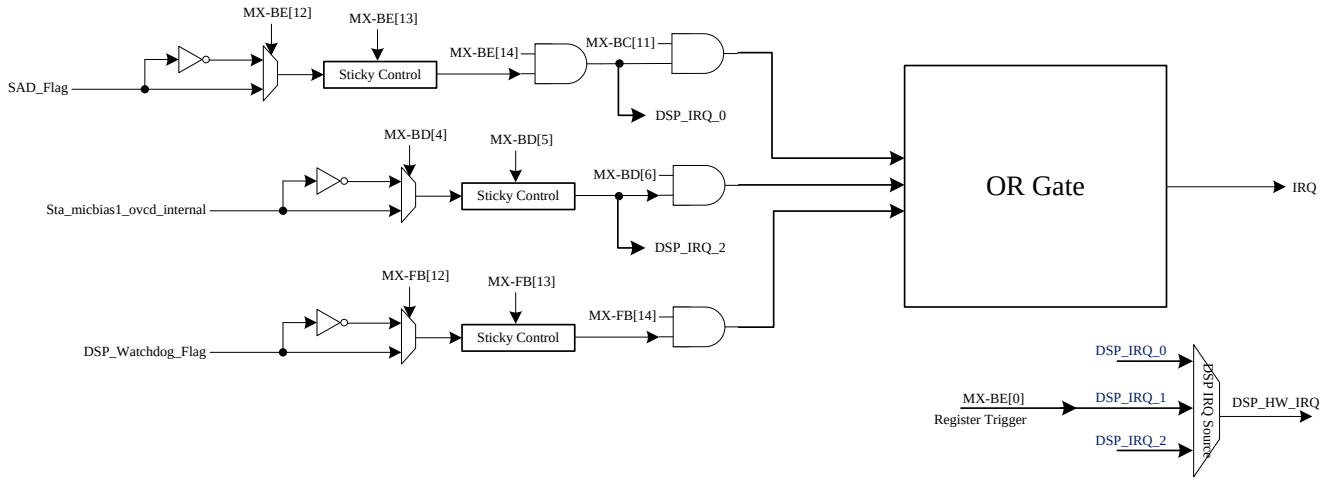
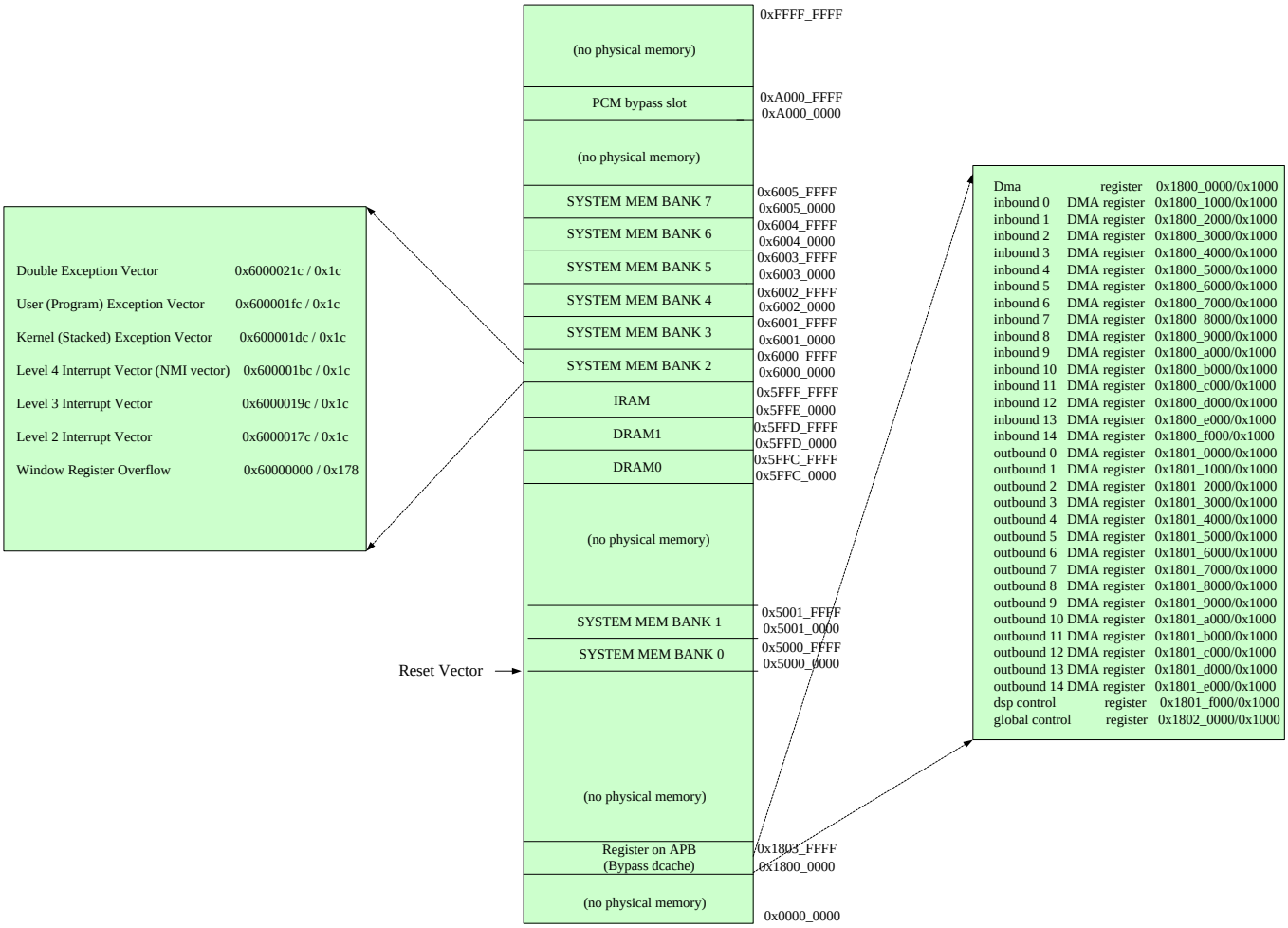


Figure 29. IRQ Function Block

9.16. DSP APB Address Map



9.17. DSP Interrupt

Int #	L1	L2	Debug	NMI	Note
Int 0	Level				Reserved for FPGA
Int 1	Level				Reserved for FPGA
Int 2	Level				Reserved for FPGA
Int 3	Level				DMA
Int 4	Level				inbound frame achieve interrupt (all ch or mode)
Int 5	Level				inbound frame achieve interrupt (all ch or mode)
Int 6	Level				outbound data level under frame size interrupt (all ch or mode)
Int 7	Level	Level			outbound data level under frame size interrupt (all ch or mode)
Int 8		Level			Reserved
Int 9		Level			ring buffer error interrupt (full/empty)
Int 10		Level			Register interrupt
Int 11		Level			Reserved
Int 12		Level			Reserved
Int 13		Level			Reserved
Int 14		Edge			Reserved
Int 15		Edge			Reserved
Int 16				NMI	NMI control by dsp_reg 0x90 [2]
Int 17	Software				Software int
Int 18		Software			Software int
Int 19	Timer0				Timer 0
Int 20		Timer1			Timer 1
Int 21		Timer2			Timer 2

10. Registers List

CM7104 register map as shown as following and accessing unimplemented registers, will return a 0.

10.1. Register Map

Table 20. Register Map

Type	Name	Description	Register Address	Reset State
Reset	S/W Reset	S/W Reset & Device ID	MX-00h	0x0000'h
Analog I/O & MICBIAS	LOUT	Line Output Volume & Mute/Un-Mute	MX-01h	0xA800'h
	IN1/2	IN1/2 Control 1	MX-03h	0x0000'h
	Micbias	MICBIAS Control	MX-04h	0x0000'h
Digital Mixer/Gain/Volume	Sidetone	Sidetone	MX-13h	0x000B'h
	DAC	Digital to Analog DAC Source Control	MX-15h	0x0000'h
	DAC	Interface/DSP to DAC Path Control	MX-16h	0x4444'h
	DAC4	DAC4 Digital Volume Control	MX-17h	0xAFAF'h
	DAC3	DAC3 Digital Volume Control	MX-18h	0xAFAF'h
	DAC1	DAC1 Digital Volume Control	MX-19h	0xAFAF'h
	DAC	DAC2 Digital Volume Control	MX-1Ah	0xAFAF'h
	DACL2/R2-2	Interface/DSP to DAC Path Control	MX-1Bh	0x0044'h
	ADC	Stereo1 ADC Digital Volume Control	MX-1Ch	0x2F2F'h
	ADC	Mono ADCL/R Digital Path Volume Control	MX-1Dh	0x2F2F'h
	ADC	Stereo1/2 ADC Digital Boost Gain Control	MX-1Eh	0x0000'h
	ADC	Stereo2 ADCL/R Digital Volume Control	MX-1Fh	0x2F2F'h
	ADC	Mono ADC Digital Boost Gain Control	MX-20h	0x0000'h
	ADC	Stereo3/4 ADC Digital Boost Gain Control	MX-21h	0x0000'h
	ADC	Stereo3 ADC Digital Volume Control	MX-22h	0x2F2F'h
	ADC	Stereo4 ADC Digital Volume Control	MX-23h	0x2F2F'h
	ADC	Stereo4 ADC Digital Mixer Control	MX-24h	0xD4C0'h
	ADC	Stereo3 ADC Digital Mixer Control	MX-25h	0xD4C0'h
	ADC	Stereo2 ADC Digital Mixer Control	MX-26h	0xD4C0'h
	ADC	Stereo1 ADC Digital Mixer Control	MX-27h	0xD4C0'h
	ADC	Mono ADC Digital Mixer Control	MX-28h	0xD4D1'h
	ADC/DAC	ADC to DAC Digital Mixer Control	MX-29h	0x8080'h
	DAC	Stereo1 DAC Digital Mixer Control	MX-2Ah	0xAAAA'h
	DAC	Mono DAC Digital Mixer Control	MX-2Bh	0xAAAA'h
	ADC/DAC	Digital to Digital Mixer Control	MX-2Ch	0xAAAA'h
	ADC/DAC	Digital to Digital Mixer Control	MX-2Dh	0xAAAA'h
I2S Interface	I2S	Interface1 Control	MX-70h	0x8000'h
	I2S	Interface2 Control	MX-71h	0x8000'h
PDM	PDM	PDM Output Control	MX-31h	0x8888'h
	PDM	PDM Output Control	MX-32h	0x0000'h
	PDM	PDM Command Control	MX-34h	0x0000'h
TDM Interface	TDM	TDM1 Interface Control	MX-3Bh	0x0300'h
	TDM	TDM1 Interface Control	MX-3Ch	0x0000'h
	TDM	TDM1 Interface Control	MX-3Dh	0x4000'h
	TDM	TDM1 Interface Control	MX-3Eh	0x0123'h
	TDM	TDM1 Interface Control	MX-3Fh	0x0123'h
	TDM	TDM2 Interface Control	MX-40h	0x0300'h
	TDM	TDM2 Interface Control	MX-41h	0x0000'h

Type	Name	Description	Register Address	Reset State
	TDM	TDM2 Interface Control	MX-42h	0x4000'h
	TDM	TDM2 Interface Control	MX-43h	0x0123'h
	TDM	TDM2 Interface Control	MX-44h	0x0123'h
Master I2C	Master I2C	Master I2C Controller	MX-47h	0x0001'h
	Master I2C	Master I2C Controller	MX-48h	0x0000'h
	Master I2C	Master I2C Controller	MX-49h	0x0000'h
	Master I2C	Master I2C Controller	MX-4Ah	0x0000'h
	Master I2C	Master I2C Controller	MX-4Bh	0x0000'h
	Master I2C	Master I2C Controller	MX-4Ch	0x0000'h
	Master I2C	Master I2C Controller	MX-4Dh	0x0000'h
	Master I2C	Master I2C Controller	MX-4Eh	0x0000'h
Digital MIC		Digital Microphone Control	MX-50h	0x1505'h
		Digital Microphone Control	MX-51h	0x0055'h
Haptic Generator	Haptic	Haptic Generator Control	MX-56h	0x0111'h
	Haptic	Haptic Generator Control	MX-57h	0x0064'h
	Haptic	Haptic Generator Control	MX-58h	0xEF0E'h
	Haptic	Haptic Generator Control	MX-59h	0xF0F0'h
	Haptic	Haptic Generator Control	MX-5Ah	0xEF0E'h
	Haptic	Haptic Generator Control	MX-5Bh	0xF0F0'h
	Haptic	Haptic Generator Control	MX-5Ch	0xEF0E'h
	Haptic	Haptic Generator Control	MX-5Dh	0xF0F0'h
	Haptic	Haptic Generator Control	MX-5Eh	0xF000'h
	Haptic	Haptic Generator Control	MX-5Fh	0x0000'h
Power Management	Management-1	I2S & DAC & ADC Power Control	MX-61h	0x0000'h
	Management-2	Digital Filter & PDM Power Control	MX-62h	0x0000'h
	Management-3	VREF & MBias & LOUTMIX & LDO Power Control	MX-63h	0x0055'h
	Management-4	MICBST & MICBIAS & PLL & LDO Power Control	MX-64h	0x0000'h
	Management-5	DSP & SRAM Power Control	MX-65h	0x0001'h
	Management-6	SRAM Power Status	MX-66h	0x0000'h
	Management-7	SRAM Power Control	MX-67h	0x0000'h
HPF	HPF	ADC/DAC HPF Control	MX-68h	0x0E00'h
PR Register	PR Index	PR Register Index	MX-6Ah	0x0000'h
	PR Data	PR Register Data	Mx-6Ch	0x0000'h
Global Clock & PLL	Clock	Clock Tree Control	MX-73h	0x1111'h
	Clock	Clock Tree Control	MX-74h	0x1111'h
	Clock	Clock Tree Control	MX-75h	0x0000'h
	PLL	PLL Control 1	MX-7Ah	0x0000'h
	PLL	PLL Control 1	MX-7Bh	0x0000'h
	PLL	PLL Control 2	MX-7Ch	0x0000'h
	PLL	PLL Control 2	MX-7Dh	0x0000'h
	Clock	Global Clock Control	MX-80h	0x0000'h
	Clock	Clock Tree Control	MX-81h	0x0000'h
	ASRC	ASRC Control	MX-83h	0x0000'h
	ASRC	ASRC Control	MX-84h	0x0000'h

Type	Name	Description	Register Address	Reset State
	ASRC	ASRC Control	MX-85h	0x0000'h
	ASRC	ASRC Control	MX-86h	0x0000'h
	ASRC	ASRC Control	MX-87h	0x0000'h
	ASRC	ASRC Control	MX-88h	0x0000'h
	ASRC	ASRC Control	MX-89h	0x0000'h
	ASRC	ASRC Control	MX-8Ah	0x0000'h
	ASRC	ASRC Control	MX-8Bh	0x0000'h
	ASRC	ASRC Control	MX-8Ch	0x0000'h
SAD	SAD	SAD Function Control	MX-9Ch	0x2184'h
	SAD	SAD Function Threshold Control	MX-9Dh	0x010A'h
	SAD	SAD Function Threshold Control	MX-9Eh	0x0AEA'h
	SAD	SAD Function Threshold Control	MX-9Fh	0x000C'h
	SAD	SAD Flag	MX-A0h	0x0000'h
DSP	InBound	DSP InBound Path Control	MX-A3h	0x0000'h
		DSP InBound Path Control	MX-A4h	0x0000'h
	SRC	DSP SRC Control	MX-A5h	0x0000'h
	SRC	DSP SRC Control	MX-E3h	0x5800'h
	SRC	DSP SRC Control	MX-E7h	0x5800'h
	SRC	DSP SRC Control	MX-EBh	0x5800'h
	SRC	DSP SRC Control	MX-EFh	0x5800'h
	SRC	DSP SRC Control	MX-F3h	0x5800'h
	OutBound	DSP OutBound0/1 Digital Volume Control	MX-A6h	0x2F2F'h
		DSP OutBound2/3 Digital Volume Control	MX-A7h	0x2F2F'h
		DSP OutBound4/5 Digital Volume Control	MX-A8h	0x2F2F'h
		DSP OutBound6/7 Digital Volume Control	MX-A9h	0x2F2F'h
SVOL	SVOL	Soft Volume and ZCD Control	MX-B3h	0x0009'h
IRQ	IRQ	IRQ Control	MX-BDh	0x0000'h
	IRQ	IRQ Control	MX-BEh	0x0000'h
GPIO	GPIO	GPIO Status	MX-BFh	0x0000'h
	GPIO	GPIO Control	MX-C0h	0x0000'h
	GPIO	GPIO Control	MX-C1h	0x0000'h
Wind Filter	Stereo1	Stereo1 ADC Adjustable HPF Control	MX-C5h	0xB320'h
	Stereo1	Stereo1 ADC Adjustable HPF Control	MX-C6h	0x0000'h
	Mono	Mono ADC Adjustable HPF Control	MX-C7h	0xB300'h
	Mono	Mono ADC Adjustable HPF Control	MX-C8h	0x0000'h
	Stereo2	Stereo2 ADC Adjustable HPF Control	MX-C9h	0xB300'h
	Stereo2	Stereo2 ADC Adjustable HPF Control	MX-CAh	0x0000'h
	Stereo3	Stereo3 ADC Adjustable HPF Control	MX-CBh	0xB300'h
	Stereo3	Stereo3 ADC Adjustable HPF Control	MX-CCh	0x0000'h
	Stereo4	Stereo4 ADC Adjustable HPF Control	MX-CDh	0xB300'h
	Stereo4	Stereo4 ADC Adjustable HPF Control	MX-CEh	0x0000'h
DRC	Multi-Band DRC2 Control	MX-DBh	0x0000'h	0x001F'h
	DRC	Multi-Band DRC1 Control	MX-D3h	0x020C'h
	DRC	Multi-Band DRC1 Control	MX-D4h	0x1F00'h
	DRC	Multi-Band DRC1 Control	MX-D5h	0x0000'h
	DRC	Multi-Band DRC1 Control	MX-D6h	0x0000'h
	DRC	Multi-Band DRC1 Control	MX-D7h	0x0000'h
	DRC	Multi-Band DRC2 Control	MX-D8h	0x001F'h
	DRC	Multi-Band DRC2 Control	MX-D9h	0x020C'h

Type	Name	Description	Register Address	Reset State
	DRC	Multi-Band DRC2 Control	MX-DAh	0x1F00'h
	DRC	Multi-Band DRC2 Control	MX-DBh	0x0000'h
	DRC	Multi-Band DRC2 Control	MX-DCh	0x0000'h
	DRC	Multi-Band DRC2 Control	MX-DDh	0x0029'h
	DRC	Multi-Band DRC1 Control	MX-DFh	0x0200'h
	DRC	Multi-Band DRC2 Control	MX-E1h	0x0000'h
General Control		General Control	MX-FAh	0x0000'h
		General Control	MX-FBh	0x0000'h
		General Control	MX-FCh	0x0000'h
		Digital Pin Initial Status	PR-29h	0x0000'h
		Digital Pin Initial Status	PR-2Ah	0x0000'h
		Digital Pin Initial Status	PR-2Bh	0x0000'h
		ADC/DAC RESET Control	PR-3Dh	0x2088'h
Vendor ID	ID	Vendor ID	MX-FEh	0x10EC'h

10.2. MX-00h: S/W Reset & Status

Default: 0000'h

Table 21. MX-00h: S/W Reset & Status

DSP Address: 0x1802_0000 I2C Address: 0x00				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:0	R	0'h	Reserved

Note: Writing **"0x10ECh"** into this register will reset all registers to their default value. The written data is ignored.

10.3. MX-01h: Line Output Control

Default: A800'h

Table 22. MX-01h: Line Output Control

DSP Address: 0x1802_0002 I2C Address: 0x01				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_lout1	15	R/W	1'h	Mute LOUT 1 Left channel Control 0'b: Unmute 1'b: Mute(-∞ dB)
En_dfo1	14	R/W	0'h	Enable Differential LOUT1 0'b: Disable 1'b: Enable
mu_lout2	13	R/W	1'h	Mute LOUT 2 Left channel Control 0'b: Unmute 1'b: Mute(-∞ dB)
En_dfo2	12	R/W	0'h	Enable Differential LOUT2 0'b: Disable 1'b: Enable
reserved	11:10	R/W	2'h	Reserved
En_lout1	9	R/W	0'h	LOUT1 Enhance Output Driving Ability 0'b: Normal 1'b: Enhance
En_lout2	8	R/W	0'h	LOUT2 Enhance Output Driving Ability 0'b: Normal 1'b: Enhance
Reserved	7:0	R	0'h	Reserved

10.4. MX-03h: Input Port Control

Default: 0000’h

Table 23. MX-03h: Input Port Control

DSP Address: 0x1802_0006 **I2C Address: 0x03**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_bst1	15:12	R/W	0’h	MIC Boost-1 Control 0000’b: Bypass 0001’b: +20dB 0010’b: +24dB 0011’b: +30dB 0100’b: +35dB 0101’b: +40dB 0110’b: +44dB 0111’b: +50dB 1000’b: +52dB Others : Reserved
sel_bst2	11:8	R/W	0’h	MIC Boost-2 Control 0000’b: Bypass 0001’b: +20dB 0010’b: +24dB 0011’b: +30dB 0100’b: +35dB 0101’b: +40dB 0110’b: +44dB 0111’b: +50dB 1000’b: +52dB Others : Reserved
en_in1_df	7	R/W	0’h	IN1 Differential input 0’b: Disable 1’b: Enable
en_in2_df	6	R/W	0’h	IN2 Differential input 0’b: Disable 1’b: Enable
reserved	5:0	R	0’h	Reserved

10.5. MX-04h: MICBIAS Control

Default: 0000'h

Table 24. MX-04h: MICBIAS Control

DSP Address: 0x1802_0008 I2C Address: 0x04				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_micbias1	15	R/W	0'h	MICBIAS1 Output Voltage Control 0'b: 82% for 1.8V, 90% for 3.3V 1'b: 69% for 1.8V, 75% for 3.3V
Selg_micbias1	14	R/W	0'h	Control of MICBIAS1 VDD 0'b: VDD=1.8V 1'b: VDD=3.3V
Reserved	13:12	R	0'h	Reserved
ovcd_micbias1	11	R/W	0'h	MICBIAS1 Short Current Detector Control 0'b: Disable 1'b: Enable
ovcd_th_sel_micbias1	10:9	R/W	0'h	MICBIAS1 Short Current Detector Threshold 00'b: 640uA 01'b: 1280uA 1x'b: 1920uA Note: tolerance is 200uA
Reserved	8:0	R	0'h	Reserved

10.6. MX-13h: Sidetone Control

Default: 000B'h

Table 25. MX-13h: Sidetone Control

DSP Address: 0x1802_0026 I2C Address: 0x13				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sidetone_hpf_sel	15:13	R/W	0'h	Sidetone HPF Fc Selection 000'b: 120Hz 001'b: 239Hz 010'b: 358Hz 011'b: 477Hz 100'b: 597Hz 101'b: 716hz 110'b: 835Hz 111'b: 955Hz
Sidetone_hpf_en	12	R/W	0'h	2nd HPF for Sidetone Path 0'b: Bypass HPF 1'b: Enable HPF

DSP Address: 0x1802_0026 I2C Address: 0x13				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_sidetone_source	11:9	R/W	0'h	Select Sidetone Source 000'b: DMIC_L1 001'b: DMIC_L2 010'b: DMIC_L3 011'b: DMIC_L4 100'b: ADC_1 101'b: ADC_2 Others: Reserved
Reserved	8:7	R	0'h	Reserved
En_sidetone	6	R/W	0'h	Sidetone Enabe Control 0'b: Disable 1'b: Enable
Gain_sidetone	5	R/W	0'h	Sidetone gain control 0'b: 0dB 1'b: +12dB
vol_sidetone	4:0	R/W	B'h	Sidetone volume in 1.5 dB step 00'h: -46.5dB 1F'h: 0dB

10.7. MX-15h: Analog DAC1/2 Source Control

Default: 0000'h

Table 26. MX-15h: Analog DAC1/2/3 Source Control

DSP Address: 0x1802_002A I2C Address: 0x15				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:2	R	0'h	Reserved
Sel_dac1_2_source	1:0	R/W	0'h	Analog DAC1/2 Source Selection 00'b: Stere1_DAC_MIXL/R 01'b: Mono_DAC_MIXL/R 10'b: DD_MIX1L/R 11'b: DD_MIX2L/R

10.8. MX-16h: Interface/DSP to DAC3/4 Digital Mixer Control

Default: 4444'h

Table 27. MX-16h: Interface/DSP to DAC3/4 Digital Mixer Control

DSP Address: 0x1802_002C **I2C Address: 0x16**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_dac4_l	15	R/W	0'h	Digital Mute DAC4 Left Volume 0: Un-Mute 1: Mute (-∞ dB)
Sel_dacl4	14:12	R/W	1'h	Select Source Data to DACL4 000'b: IF1_DAC_6 001'b: IF2_DAC_6 010'b: Reserved 011'b: Reserved 100'b: Reserved 101'b: OutBound6 Others: Reserved
mu_dac4_r	11	R/W	0'h	Digital Mute DAC4 Right Volume 0: Un-Mute 1: Mute (-∞ dB)
Sel_dacr4	10:8	R/W	1'h	Select Source Data to DACR4 000'b: IF1_DAC_7 001'b: IF2_DAC_7 010'b: Reserved 011'b: Reserved 100'b: Reserved 101'b: OutBound7 Others: Reserved
mu_dac3_l	7	R/W	0'h	Digital Mute DAC3 Left Volume 0: Un-Mute 1: Mute (-∞ dB)
Sel_dacl3	6:4	R/W	1'h	Select Source Data to DACL3 000'b: IF1_DAC_4 001'b: IF2_DAC_4 010'b: Reserved 011'b: Reserved 100'b: Reserved 101'b: OutBound4 Others: Reserved
mu_dac3_r	3	R/W	0'h	Digital Mute DAC3 Right Volume 0: Un-Mute 1: Mute (-∞ dB)

DSP Address: 0x1802_002C I2C Address: 0x16				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_dacr3	2:0	R/W	1'h	Select Source Data to DACR3 000'b: IF1_DAC_5 001'b: IF2_DAC_5 010'b: Reserved 011'b: Reserved 100'b: Reserved 101'b: OutBound5 Others: Reserved

10.9. MX-17h: DAC4 Digital Volume Control

Default: AFAF'h

Table 28. MX-17h: DAC4 Digital Volume Control

DSP Address: 0x1802_002E I2C Address: 0x17				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
vol_dac4_l	15:8	R/W	AF'h	DAC4 Left Channel Digital Volume in 0.375 dB step 00'h: -65.625dB AF'h: 0dB
vol_dac4_r	7:0	R/W	AF'h	DAC4 Right Channel Digital Volume in 0.375 dB step 00'h: -65.625dB AF'h: 0dB

10.10. MX-18h: DAC3 Digital Volume Control

Default: AFAF'h

Table 29. MX-18h: DAC3 Digital Volume Control

DSP Address: 0x1802_0030 I2C Address: 0x18				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
vol_dac3_l	15:8	R/W	AF'h	DAC3 Left Channel Digital Volume in 0.375 dB step 00'h: -65.625dB AF'h: 0dB
vol_dac3_r	7:0	R/W	AF'h	DAC3 Right Channel Digital Volume in 0.375 dB step 00'h: -65.625dB AF'h: 0dB

10.11. MX-19h: DAC1 Digital Volume Control

Default: AFAF'h

Table 30. MX-19h: DAC1 Digital Volume Control

DSP Address: 0x1802_0032 I2C Address: 0x19				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
vol_dac1_l	15:8	R/W	AF'h	DAC1 Left Channel Digital Volume in 0.375 dB step 00'h: -65.625dB AF'h: 0dB
vol_dac1_r	7:0	R/W	AF'h	DAC1 Right Channel Digital Volume in 0.375 dB step 00'h: -65.625dB AF'h: 0dB

10.12. MX-1Ah: DAC2 Digital Volume Control

Default: AFAF'h

Table 31. MX-1Ah: DAC2 Digital Volume Control

DSP Address: 0x1802_0034 I2C Address: 0x1A				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
vol_dac2_l	15:8	R/W	AF'h	DAC2 Left Channel Digital Volume in 0.375 dB step 00'h: -65.625dB AF'h: 0dB
vol_dac2_r	7:0	R/W	AF'h	DAC2 Right Channel Digital Volume in 0.375 dB step❶ 00'h: -65.625dB AF'h: 0dB

10.13. MX-1Bh: Interface/DSP to DAC2 Digital Mixer Control

Default: 0044'h

Table 32. MX-1Bh: Interface/DSP to DAC2 Digital Mixer Control

DSP Address: 0x1802_0036 I2C Address: 0x1B				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:8	R	0'h	Reserved

DSP Address: 0x1802_0036 I2C Address: 0x1B				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_dac2_l	7	R/W	0'h	Digital Mute DAC2 Left Volume 0: Un-Mute 1: Mute (-∞ dB)
Sel_dacl2	6:4	R/W	1'h	Select Source Data to DACL2 000'b: IF1_DAC_2 001'b: IF2_DAC_2 010'b: Reserved 011'b: Reserved 100'b: Reserved 101'b: OutBound2 111'b: Reserved
mu_dac2_r	3	R/W	0'h	Digital Mute DAC2 Right Volume 0: Un-Mute 1: Mute (-∞ dB)
Sel_dacr2	2:0	R/W	1'h	Select Source Data to DACR2 000'b: IF1_DAC_3 001'b: IF2_DAC_3 010'b: Reserved 011'b: Reserved 100'b: Reserved 101'b: OutBound3 110'b: Haptic_gen 111'b: VAD_ADC

10.14. MX-1Ch: Stereo1 ADC Digital Volume Control

Default: 2F2F'h

Table 33. MX-1Ch: Stereo1 ADC Digital Volume Control

DSP Address: 0x1802_0038 I2C Address: 0x1C				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_stereo1_adc_vol_l	15	R/W	0'h	Digital Mute From Stereo1 ADC Left Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_stereo1_adcl	14:8	R/W	2F'h	Stereo1 ADC Left Channel Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB
mu_stereo1_adc_vol_r	7	R/W	0'h	Digital Mute From Stereo1 ADC Right Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)

DSP Address: 0x1802_0038 I2C Address: 0x1C				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Vol_stereo1_adcr	6:0	R/W	2F'h	Stereo1 ADC Right Channel Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB

10.15. MX-1Dh: Mono ADC Digital Volume Control

Default: 2F2F'h

Table 34. MX-1Dh: Mono ADC Digital Volume Control

DSP Address: 0x1802_003A I2C Address: 0x1D				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_mono_adc_vol_l	15	R/W	0'h	Digital Mute From Mono ADC Left Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_mono_adcl	14:8	R/W	2F'h	Mono ADC Left Channel Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB
mu_mono_adc_vol_r	7	R/W	0'h	Digital Mute From Mono ADC Right Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_mono_adcr	6:0	R/W	2F'h	Mono ADC Right Channel Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB

10.16. MX-1Eh: Stereo1/2 ADC Digital Boost Gain Control

Default: 0000'h

Table 35. MX-1Eh: Stereo1/2 ADC Digital Boost Gain Control

DSP Address: 0x1802_003C I2C Address: 0x1E				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Stereo1_ad_bst_gain_l	15:14	R/W	0'h	Stereo1 ADC Left Channel Digital Boost Gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Stereo1_ad_bst_gain_r	13:12	R/W	0'h	Stereo 1 ADC Right Channel Digital Boost Gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB

DSP Address: 0x1802_003C I2C Address: 0x1E				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Stereo1_ad_comp_gain	11:10	R/W	0'h	Stereo1 ADC Compensate Gain 00'b : 0dB 01'b: 1dB 10'b : 2dB 11'b: 3dB
Stereo2_ad_bst_gain_l	9:8	R/W	0'h	Stereo2 ADC Left Channel Digital Boost Gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Stereo2_ad_bst_gain_r	7:6	R/W	0'h	Stereo 2ADC Right Channel Digital Boost Gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Stereo2_ad_comp_gain	5:4	R/W	0'h	Stereo2 ADC Compensate Gain 00'b : 0dB 01'b: 1dB 10'b : 2dB 11'b: 3dB
reserved	3:0	R	0'h	Reserved

10.17. MX-1Fh: Stereo2 ADC Digital Volume Control

Default: 2F2F'h

Table 36. MX-1Fh: Stereo2 ADC Digital Volume Control

DSP Address: 0x1802_003E I2C Address: 0x1F				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_stereo2_adc_vol_l	15	R/W	0'h	Digital Mute From Stereo2 ADC Left Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_stereo2_adcl	14:8	R/W	2F'h	Stereo2 ADC Left Channel Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB
mu_stereo2_adc_vol_r	7	R/W	0'h	Digital Mute From Stereo2 ADC Right Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_stereo2_adcr	6:0	R/W	2F'h	Stereo2 ADC Right Channel Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB

10.18. MX-20h: Mono ADC Digital Boost Gain Control

Default: 0000'h

Table 37. MX-20h: Mono ADC Digital Boost Gain Control

DSP Address: 0x1802_0040 I2C Address: 0x20				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Mono_ad_bst_gain_l	15:14	R/W	0'h	Mono ADC Left Channel Digital Boost Gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Mono_ad_bst_gain_r	13:12	R/W	0'h	Mono ADC Right Channel Digital Boost Gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Mono_ad_comp_gain	11:10	R/W	0'h	Mono ADC Compensate Gain 00'b : 0dB 01'b: 1dB 10'b : 2dB 11'b: 3dB
reserved	9:0	R	0'h	Reserved

10.19. MX-21h: Stereo3/4 ADC Digital Boost Gain Control

Default: 0000'h

Table 38. MX-21h: Stereo3/4 ADC Digital Boost Gain Control

DSP Address: 0x1802_0042 I2C Address: 0x21				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Stereo3_ad_bst_gain_l	15:14	R/W	0'h	Stereo3 ADC Left Channel Digital Boost Gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Stereo3_ad_bst_gain_r	13:12	R/W	0'h	Stereo3 ADC Right Channel Digital Boost Gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Stereo3_ad_comp_gain	11:10	R/W	0'h	Stereo3 ADC Compensate Gain 00'b : 0dB 01'b: 1dB 10'b : 2dB 11'b: 3dB
Stereo4_ad_bst_gain_l	9:8	R/W	0'h	Stereo4 ADC Left Channel Digital Boost Gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Stereo4_ad_bst_gain_r	7:6	R/W	0'h	Stereo4 ADC Right Channel Digital Boost Gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Stereo4_ad_comp_gain	5:4	R/W	0'h	Stereo4 ADC Compensate Gain 00'b : 0dB 01'b: 1dB 10'b : 2dB 11'b: 3dB
reserved	3:0	R	0'h	Reserved

10.20. MX-22h: Stereo3 ADC Digital Volume Control

Default: 2F2F'h

Table 39. MX-22h: Stereo3 ADC Digital Volume Control

DSP Address: 0x1802_0044 I2C Address: 0x22				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_stereo3_adc_vol_l	15	R/W	0'h	Digital Mute From Stereo3 ADC Left Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_stereo3_adcl	14:8	R/W	2F'h	Stereo3 ADC Left Channel Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB
mu_stereo3_adc_vol_r	7	R/W	0'h	Digital Mute From Stereo3 ADC Right Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_stereo3_adcr	6:0	R/W	2F'h	Stereo3 ADC Right Channel Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB

10.21. MX-23h: Stereo4 ADC Digital Volume Control

Default: 2F2F'h

Table 40. MX-23h: Stereo4 ADC Digital Volume Control

DSP Address: 0x1802_0046 I2C Address: 0x23				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_stereo4_adc_vol_l	15	R/W	0'h	Digital Mute From Stereo4 ADC Left Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_stereo4_adcl	14:8	R/W	2F'h	Stereo4 ADC Left Channel Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB
mu_stereo4_adc_vol_r	7	R/W	0'h	Digital Mute From Stereo4 ADC Right Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_stereo4_adcr	6:0	R/W	2F'h	Stereo4 ADC Right Channel Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB

DSP Address: 0x1802_0046 I2C Address: 0x23				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**

10.22. MX-24h: Stereo4 ADC Digital Mixer Control

Default: D4C0'h

Table 41. MX-24h: Stereo4 ADC Digital Mixer Control

DSP Address: 0x1802_0048 I2C Address: 0x24				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_stereo4_adcl2	15	R/W	1'h	Mute Source2 to Stereo4 ADC Left Channel 0'b:UnMute 1'b:Mute
mu_stereo4_adcl1	14	R/W	1'h	Mute Source1 to Stereo4 ADC Left Channel 0'b:UnMute 1'b:Mute
sel_stereo4_adc1	13:12	R/W	1'h	Select Stereo4 ADC L/R Channel Source 1 00'b: DD_MIX1L/R 01'b: ADC1/2 10'b: DD_MIX2L/R 11'b: Reserved
sel_stereo4_adc2	11:10	R/W	1'h	Select Stereo4 ADC L/R Channel Source 2 00'b: DD_MIX1L/R 01'b: DMIC1/DMIC2 10'b: DD_MIX2L/R 11'b: Reserved
Sel_stereo4_dmic	9:8	R/W	0'h	Select Stereo4 DMIC Source 00'b: DMIC1 01'b: DMIC2 10'b: Reserved 11'b: Reserved
mu_stereo4_adcr1	7	R/W	1'h	Mute Source1 to Stereo4 ADC Right Channel 0'b:UnMute 1'b:Mute
mu_stereo4_adcr2	6	R/W	1'h	Mute Source2 to Stereo4 ADC Right Channel 0'b:UnMute 1'b:Mute
Reserved	5:0	R	0'h	Reserved

10.23. MX-25h: Stereo3 ADC Digital Mixer Control

Default: DC40’h

Table 42. MX-25h: Stereo3 ADC Digital Mixer Control

DSP Address: 0x1802_004A **I2C Address: 0x25**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_stereo3_adcl2	15	R/W	1’h	Mute Source2 to Stereo3 ADC Left Channel 0’b:UnMute 1’b:Mute
mu_stereo3_adcl1	14	R/W	1’h	Mute Source1 to Stereo3 ADC Left Channel 0’b:UnMute 1’b:Mute
sel_stereo3_adc1	13:12	R/W	1’h	Select Stereo3 ADC L/R Channel Source 1 00’b: DD_MIX1L/R 01’b: ADC1/2 10’b: Stereo1_DAC_MIXL/R 11’b: Reserved
sel_stereo3_adc2	11:10	R/W	1’h	Select Stereo3 ADC L/R Channel Source 2 00’b: DD_MIX1L/R 01’b: DMIC1/DMIC2 10’b: Stereo1_DAC_MIXL/R 11’b: Reserved
Sel_stereo3_dmic	9:8	R/W	0’h	Select Stereo3 DMIC Source 00’b: DMIC1 01’b: DMIC2 10’b: Reserved 11’b: Reserved
mu_stereo3_adcr1	7	R/W	1’h	Mute Source1 to Stereo3 ADC Right Channel 0’b:UnMute 1’b:Mute
mu_stereo3_adcr2	6	R/W	1’h	Mute Source2 to Stereo3 ADC Right Channel 0’b:UnMute 1’b:Mute
Reserved	5:0	R	0’h	Reserved

10.24. MX-26h: Stereo2 ADC Digital Mixer Control

Default: DC40’h

Table 43. MX-26h: Stereo2 ADC Digital Mixer Control

DSP Address: 0x1802_004C **I2C Address: 0x26**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_stereo2_adcl2	15	R/W	1’h	Mute Source2 to Stereo2 ADC Left Channel 0’b:UnMute 1’b:Mute
mu_stereo2_adcl1	14	R/W	1’h	Mute Source1 to Stereo2 ADC Left Channel 0’b:UnMute 1’b:Mute
sel_stereo2_adc1	13:12	R/W	1’h	Select Stereo2 ADC L/R Channel Source 1 00’b: DD_MIX1L/R 01’b: ADC1/2 10’b: Stereo1_DAC_MIXL/R 11’b: Reserved
sel_stereo2_adc2	11:10	R/W	1’h	Select Stereo2 ADC L/R Channel Source 2 00’b: DD_MIX1L/R 01’b: DMIC1/DMIC2 10’b: Stereo1_DAC_MIXL/R 11’b: Reserved
Sel_stereo2_dmic	9:8	R/W	0’h	Select Stereo2 DMIC Source 00’b: DMIC1 01’b: DMIC2 10’b: Reserved 11’b: Reserved
mu_stereo2_adcr1	7	R/W	1’h	Mute Source1 to Stereo2 ADC Right Channel 0’b:UnMute 1’b:Mute
mu_stereo2_adcr2	6	R/W	1’h	Mute Source2 to Stereo2 ADC Right Channel 0’b:UnMute 1’b:Mute
reserved	5:1	R	0’h	reserved
Sel_stereo2_lr_mix	0	R/W	0’h	Mixing Control for Stereo2 ADC Left channel 0’b: L 1’b: L+R

10.25. MX-27h: Stereo1 ADC Digital Mixer Control

Default: DC40’h

Table 44. MX-27h: Stereo1 ADC Digital Mixer Control

DSP Address: 0x1802_004E **I2C Address: 0x27**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_stereo1_adcl2	15	R/W	1’h	Mute Source 2 to Stereo1 ADC Left Channel 0’b:UnMute 1’b:Mute
mu_stereo1_adcl1	14	R/W	1’h	Mute Source 1 to Stereo1 ADC Left Channel 0’b:UnMute 1’b:Mute
sel_stereo1_adc1	13:12	R/W	1’h	Select Stereo1 ADC L/R Channel Source 1 00’b: DD_MIX1L/R 01’b: ADC_1 10’b: Stereo1_DAC_MIXL/R 11’b: Reserved
sel_stereo1_adc2	11:10	R/W	1’h	Select Stereo1 ADC L/R Channel Source 2 00’b: DD_MIX1L/R 01’b: DMIC1/DMIC2 10’b: Stereo1_DAC_MIXL/R 11’b: Reserved
Sel_stereo1_dmic	9:8	R/W	0’h	Select Stereo1 DMIC Source 00’b: DMIC1 01’b: DMIC2 10’b: Reserved 11’b: Reserved
mu_stereo1_adcr1	7	R/W	1’h	Mute Source 1 to Stereo1 ADC Right Channel 0’b:UnMute 1’b:Mute
mu_stereo1_adcr2	6	R/W	1’h	Mute Source 2 to Stereo1 ADC Right Channel 0’b:UnMute 1’b:Mute
reserved	5:0	R	0’h	reserved

10.26. MX-28h: Mono ADC Digital Mixer Control

Default: D4D1'h

Table 45. MX-28h: Mono ADC Digital Mixer Control

DSP Address: 0x1802_0050 **I2C Address: 0x28**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_mono_adcl2	15	R/W	1'h	Mute Source 3 to Mono ADC Left channel 0'b:UnMute 1'b:Mute
mu_mono_adcl1	14	R/W	1'h	Mute Source 3 to Mono ADC Left channel 0'b:UnMute 1'b:Mute
sel_mono_adcl1	13:12	R/W	1'h	Select Mono ADC Left channel source 1 00'b: DD_MIX1L 01'b: ADC1 10'b: Mono_DAC_Mixer_L 11'b: Reserved
sel_mono_adcl2	11:10	R/W	1'h	Select Mono ADC Left channel source 2 00'b: DD_MIX1L 01'b: DMIC1_L or DMIC2_L 10'b: Mono_DAC_Mixer_L 11'b: Reserved
Sel_mono_dmic_l	9:8	R/W	0'h	Select Mono Left Channel DMIC Source 00'b: DMIC1_L 01'b: DMIC2_L 10'b: Reserved 11'b: Reserved
mu_mono_adcr1	7	R/W	1'h	Mute Source 1 to Mono ADC Right channel 0'b:UnMute 1'b:Mute
mu_mono_adcr2	6	R/W	1'h	Mute Source 2 to Mono ADC Right channel 0'b:UnMute 1'b:Mute
sel_mono_adcr1	5:4	R/W	1'h	Select Mono ADC Right channel source 1 00'b: DD_MIX1R 01'b: ADC2 10'b: Mono_DAC_Mixer_R 11'b: Reserved
sel_mono_adcr2	3:2	R/W	0'h	Select Mono ADC Right channel source 2 00'b: DD_MIX1R 01'b: DMIC1_R or DMIC2_R 10'b: Mono_DAC_Mixer_R 11'b: Reserved
Sel_mono_dmic_r	1:0	R/W	1'h	Select Mono Right Channel DMIC Source 00'b: DMIC1_R 01'b: DMIC2_R 10'b: Reserved 11'b: Reserved

10.27. MX-29h: ADC/Interface/DSP to DAC1 Digital Mixer Control

Default: 8080'h

Table 46. MX-29h: ADC/Interface/DSP to DAC1 Digital Mixer Control

DSP Address: 0x1802_0052 **I2C Address: 0x28**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Mu_adda_mixer1_l	15	R/W	1'h	Mute ADC Filter to DAC1 Filter Left Channel 0'b:UnMute 1'b:Mute
Mu_dac1_l	14	R/W	0'h	Mute IF1 DAC Left Channel 0'b:UnMute 1'b:Mute
Reserved	13:11	R	0'h	Reserved
Sel_dac1	10:8	R/W	0'h	DACL Source Selection 1 000'b: IF1_DAC_0 001'b: IF2_DAC_0 010'b: Reserved 011'b: Reserved 100'b: Reserved 101'b: OutBound0 Others: Reserved
Mu_adda_mixer1_r	7	R/W	1'h	Mute ADC Filter to DAC1 Filter Right Channel 0'b:UnMute 1'b:Mute
Mu_dac1_r	6	R/W	0'h	Mute IF1 DAC Right Channel 0'b:UnMute 1'b:Mute
Reserved	5:2	R	0'h	Reserved
Sel_adda1	1:0	R/W	0'h	DAC1L/R Source Selection 00'b: Stereo1_ADC_Mixer_L/R 01'b: Stereo2_ADC_Mixer_L/R 10'b: OutBound6/7 Others: Reserved

10.28. MX-2Ah: Stereo1 DAC Digital Mixer Control

Default: AAAA'h

Table 47. MX-2Ah: Stereo1 DAC Digital Mixer Control

DSP Address: 0x1802_0054 I2C Address: 0x2A				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Mu_sidetone2dacl1	15	R/W	1'h	Mute Side Tone to DAC1L 0'b: Un-Mute 1'b: Mute
Reserved	14	R	0'h	Reserved
mu_stereo_dacl1_mixl	13	R/W	1'h	Mute Stereo DAC1 Left channel 0'b:Un-Mute 1'b:Mute
gain_dacl1_to_stereo_l	12	R/W	0'h	Gain Control for DAC1L to Stereo Left Mixer 0'b: 0dB 1'b: -6dB
mu_stereo_dacl2_mixl	11	R/W	1'h	Mute Stereo DAC2 Left channel 0'b:Un-Mute 1'b:Mute
gain_dacl2_to_stereo_l	10	R/W	0'h	Gain Control for DAC2L to Stereo Left Mixer 0'b: 0dB 1'b: -6dB
mu_stereo_dacr1_mixl	9	R/W	1'h	Mute Stereo DAC1 Right channel to Left Mixer 0'b:Un-Mute 1'b:Mute
gain_dacr1_to_stereo_l	8	R/W	0'h	Gain Control for DAC1R to Stereo Left Mixer 0'b: 0dB 1'b: -6dB
Mu_sidetone2dacr1	7	R/W	1'h	Mute Side Tone to DAC1R 0'b: Un-Mute 1'b: Mute
reserved	6	R	0'h	Reserved
mu_stereo_dacr1_mixr	5	R/W	1'h	Mute Stereo DAC1 Right channel 0'b:Un-Mute 1'b:Mute
gain_dacr1_to_stereo_r	4	R/W	0'h	Gain Control for DAC1R to Stereo Right Mixer 0'b: 0dB 1'b: -6dB
mu_stereo_dacr2_mixr	3	R/W	1'h	Mute Stereo DAC2 Right channel 0'b:UnMute 1'b:Mute
gain_dacr2_to_stereo_r	2	R/W	0'h	Gain Control for DAC2R to Stereo Right Mixer 0'b: 0dB 1'b: -6dB
mu_stereo_dacl1_mixr	1	R/W	1'h	Mute Stereo DAC1 Left channel to Right Mixer 0'b:Un-Mute 1'b:Mute

DSP Address: 0x1802_0054 I2C Address: 0x2A				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
gain_dacl1_to_stereo_r	0	R/W	0'h	Gain Control for DAC1L to Stereo Right Mixer 0'b: 0dB 1'b: -6dB

10.29. MX-2Bh: Mono DAC Digital Mixer Control

Default: AAAA'h

Table 48. MX-2Bh: Mono DAC Digital Mixer Control

DSP Address: 0x1802_0056 I2C Address: 0x2B				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Mu_sidetone2dacl2	15	R/W	1'h	Mute Side Tone to DAC2L 0'b: UnMute 1'b: Mute
reserved	14	R	0'h	Reserved
mu_mono_dacl2_mixl	13	R/W	1'h	Mute DAC2 Left Channel to Mono DAC Left Mixer 0'b:UnMute 1'b:Mute
gain_mono_l_dacl2	12	R/W	0'h	Gain Control for DAC2 Left Channel to Mono DAC Left Mixer 0'b: 0dB 1'b: -6dB
mu_mono_dacr2_mixl	11	R/W	1'h	Mute DAC2 Right Channel to Mono DAC Left Mixer 0'b:UnMute 1'b:Mute
gain_mono_l_dacr2	10	R/W	0'h	Gain Control for DAC2 Right Channel to Mono DAC Left Mixer 0'b: 0dB 1'b: -6dB
mu_mono_dacl1_mixl	9	R/W	1'h	Mute DAC1 Left Channel to Mono DAC Left Mixer 0'b:UnMute 1'b:Mute
gain_mono_l_dacl1	8	R/W	0'h	Gain Control for DAC1 Left Channel to Mono DAC Left Mixer 0'b: 0dB 1'b: -6dB
Mu_sidetone2dacr2	7	R/W	1'h	Mute Side Tone to DAC2R 0'b: UnMute 1'b: Mute
Reserved	6	R	0'h	reserved
mu_mono_dacr2_mixr	5	R/W	1'h	Mute DAC2 Right Channel to Mono DAC Right Mixer 0'b:UnMute 1'b:Mute

DSP Address: 0x1802_0056 I2C Address: 0x2B				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
gain_mono_r_dacr2	4	R/W	0'h	Gain Control for DAC2 Right Channel to Mono DAC Right Mixer 0'b: 0dB 1'b: -6dB
mu_mono_dacr1_mixr	3	R/W	1'h	Mute DAC1 Right Channel to Mono DAC Right Mixer 0'b:UnMute 1'b:Mute
gain_mono_r_dacr1	2	R/W	0'h	Gain Control for DAC1 Right Channel to Mono DAC Right Mixer 0'b: 0dB 1'b: -6dB
mu_mono_dacl2_mixr	1	R/W	1'h	Mute DAC2 Left Channel to Mono DAC Right Mixer 0'b:UnMute 1'b:Mute
gain_mono_r_dacl2	0	R/W	0'h	Gain Control for DAC2 Left Channel to Mono DAC Right Mixer 0'b: 0dB 1'b: -6dB

10.30. MX-2Ch: Digital to Digital Mixer Control

Default: AAAA'h

Table 49. MX-2Ch: Digital to Digital Mixer Control

DSP Address: 0x1802_0058 I2C Address: 0x2C				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Mu_stereomixl_to_ddmix1l	15	R/W	1'h	Mute Stereo_DAC_Mixer_L to DD_MIX1L 0'b:UnMute 1'b:Mute
gain_stereomixl_to_ddmix1l	14	R/W	0'h	Gain Control for Stereo_DAC_Mixer_L to DD_MIX1L 0'b: 0dB 1'b: -6dB
Mu_monomixl_to_ddmix1l	13	R/W	1'h	Mute Mono_DAC_Mixer_L to DD_MIX1L 0'b:UnMute 1'b:Mute
gain_monomixl_to_ddmix1l	12	R/W	0'h	Gain Control for Mono_DAC_Mixer_L to DD_MIX1L 0'b: 0dB 1'b: -6dB
Mu_dacl3_to_ddmix1l	11	R/W	1'h	Mute DACL3 to DD_MIX1L 0'b:UnMute 1'b:Mute

DSP Address: 0x1802_0058 I2C Address: 0x2C				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
gain_dacl3_to_ddmix1l	10	R/W	0'h	Gain Control for DACL3 to DD_MIX1L 0'b: 0dB 1'b: -6dB
Mu_dacr3_to_ddmix1l	9	R/W	1'h	Mute DACR3 to DD_MIX1L 0'b:UnMute 1'b:Mute
gain_dacr3_to_ddmix1l	8	R/W	0'h	Gain Control for DACR3 to DD_MIX1L 0'b: 0dB 1'b: -6dB
Mu_stereomixr_to_ddmix1r	7	R/W	1'h	Mute Stereo_DAC_Mixer_R to DD_MIX1R 0'b:UnMute 1'b:Mute
gain_stereomixr_to_ddmix1r	6	R/W	0'h	Gain Control for Stereo_DAC_Mixer_R to DD_MIX1R 0'b: 0dB 1'b: -6dB
Mu_monomixr_to_ddmix1r	5	R/W	1'h	Mute Mono_DAC_Mixer_R to DD_MIX1R 0'b:UnMute 1'b:Mute
gain_monomixr_to_ddmix1r	4	R/W	0'h	Gain Control for Mono_DAC_Mixer_R to DD_MIX1R 0'b: 0dB 1'b: -6dB
Mu_dacr3_to_ddmix1r	3	R/W	1'h	Mute DACR3 to DD_MIX1R 0'b:UnMute 1'b:Mute
gain_dacr3_to_ddmix1r	2	R/W	0'h	Gain Control for DACR3 to DD_MIX1R 0'b: 0dB 1'b: -6dB
Mu_dacl3_to_ddmix1r	1	R/W	1'h	Mute DACL3 to DD_MIX1R 0'b:UnMute 1'b:Mute
gain_dacl3_to_ddmix1r	0	R/W	0'h	Gain Control for DACL3 to DD_MIX1R 0'b: 0dB 1'b: -6dB

10.31. MX-2Dh: Digital to Digital Mixer Control

Default: AAAA'h

Table 50. MX-2Dh: Digital to Digital Mixer Control

DSP Address: 0x1802_005A I2C Address: 0x2D				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Mu_stereomixl_to_ddmix2l	15	R/W	1'h	Mute Stereo_DAC_Mixer_L to DD_MIX2L 0'b:UnMute 1'b:Mute
gain_stereomixl_to_ddmix2l	14	R/W	0'h	Gain Control for Stereo_DAC_Mixer_L to DD_MIX2L 0'b: 0dB 1'b: -6dB
Mu_monomixl_to_ddmix2l	13	R/W	1'h	Mute Mono_DAC_Mixer_L to DD_MIX2L 0'b:UnMute 1'b:Mute
gain_monomixl_to_ddmix2l	12	R/W	0'h	Gain Control for Mono_DAC_Mixer_L to DD_MIX2L 0'b: 0dB 1'b: -6dB
Mu_dacl4_to_ddmix2l	11	R/W	1'h	Mute DACL4 to DD_MIX2L 0'b:UnMute 1'b:Mute
gain_dacl4_to_ddmix2l	10	R/W	0'h	Gain Control for DACL4 to DD_MIX2L 0'b: 0dB 1'b: -6dB
Mu_dacr4_to_ddmix2l	9	R/W	1'h	Mute DACR4 to DD_MIX2L 0'b:UnMute 1'b:Mute
gain_dacr4_to_ddmix2l	8	R/W	0'h	Gain Control for DACR4 to DD_MIX2L 0'b: 0dB 1'b: -6dB
Mu_stereomixr_to_ddmix2r	7	R/W	1'h	Mute Stereo_DAC_Mixer_R to DD_MIX2R 0'b:UnMute 1'b:Mute
gain_stereomixr_to_ddmix2r	6	R/W	0'h	Gain Control for Stereo_DAC_Mixer_R to DD_MIX2R 0'b: 0dB 1'b: -6dB
Mu_monomixr_to_ddmix2r	5	R/W	1'h	Mute Mono_DAC_Mixer_R to DD_MIX2R 0'b:UnMute 1'b:Mute
gain_monomixr_to_ddmix2r	4	R/W	0'h	Gain Control for Mono_DAC_Mixer_R to DD_MIX2R 0'b: 0dB 1'b: -6dB
Mu_dacr4_to_ddmix2r	3	R/W	1'h	Mute DACR4 to DD_MIX2R 0'b:UnMute 1'b:Mute
gain_dacr4_to_ddmix2r	2	R/W	0'h	Gain Control for DACR4 to DD_MIX2R 0'b: 0dB 1'b: -6dB

DSP Address: 0x1802_005A I2C Address: 0x2D				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Mu_dacl4_to_ddmix2r	1	R/W	1'h	Mute DACL4 to DD_MIX2R 0'b:UnMute 1'b:Mute
gain_dacl4_to_ddmix2r	0	R/W	0'h	Gain Control for DACL4 to DD_MIX2R 0'b: 0dB 1'b: -6dB

10.32. MX-31h: PDM Output Control

Default: 8888'h

Table 51. MX-31h: PDM Output Control

DSP Address: 0x1802_0062 I2C Address: 0x31				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_pdm1_l	15	R/W	1'h	Mute PDM 1 Left Channel Data 0'b: UnMute 1'b: Mute
Reserved	14	R	0'h	Reserved
sel_pdm1_l	13:12	R/W	0'h	Select PDM 1 Left Channel Source 00'b: Stereo1_DAC_MIXL 01'b: Mono_DAC_MIXL 10'b: DD_MIX1L 11'b: DD_MIX2L
mu_pdm1_r	11	R/W	1'h	Mute PDM 1 Right Channel Data 0'b: UnMute 1'b: Mute
Reserved	10	R	0'h	Reserved
sel_pdm1_r	9:8	R/W	0'h	Select PDM 1 Right Channel Source 00'b: Stereo1_DAC_MIXR 01'b: Mono_DAC_MIXR 10'b: DD_MIX1R 11'b: DD_MIX2R
Reserved	7:0	R/W	88'h	Reserved

10.33. MX-32h: PDM Output Control

Default: 0000'h

Table 52. MX-32h: PDM Output Control

DSP Address: 0x1802_0064 I2C Address: 0x32				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:12	R	0'h	Reserved
Pdm1_cmd_exe	11	R/W	0'h	PDM1 write 1'b1 then write 0'b1 to Execute Pattern Command
Reserved	10:5	R/W	0'h	Reserved
Pdm1_cmd_busy	4	R	0'h	PDM1 Pattern Controller Busy Flag 0'b: Normal 1'b: Busy
Sel_pdm_pattern_ctrl	3	R/W	0'h	Select Into PDM Pattern Control Repeat Count Number 0'b: Repeat 64 times 1'b: Repeat 128times
Gain_pdm_in	2	R/W	0'h	PDM Gain Selection 0'b: -6dB 1'b: 0dB
Sel_pdm_div	1:0	R/W	0'h	System Clock to PDM Filter Divider 00'b: Div 1 01'b: Div 2 10'b: Div 4 11'b: Div 3

10.34. MX-34h: PDM Command Control

Default: 0000'h

Table 53. MX-34h: PDM Command Control

DSP Address: 0x1802_0068 I2C Address: 0x34				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:8	R/W	0'h	Reserved
Pdm1_cmd_pattern	7:0	R/W	0'h	PDM1 pattern cmd

10.35. MX-3Bh: TDM1 Interface Control

Default: 0300'h

Table 54. MX-3Bh: TDM1 Interface Control

DSP Address: 0x1802_0076 **I2C Address: 0x3B**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
mode_sel_i2s1	12	R/W	0'h	I2S / TDM Mode Control 0'b: Normal I2S Mode 1'b: TDM Mode
Tdmslot_sel_i2s1	11:10	R/W	0'h	TDM Channel Number Select 00'b: 2ch 01'b: 4ch 10'b: 6ch 11'b: 8ch
Channel_length_i2s1	9:8	R/W	3'h	TDM Channel Length 00'b: 16bit (For Slave Mode and Master Mode) 01'b: 20bit (For Slave Mode) 10'b: 24bit (For Slave Mode) 11'b: 32bit (For Slave Mode and Master Mode)
sel_i2s_rx_adc1_i2s1	7:6	R/W	0'h	Data Swap for Slot0/1 in ADCDAT1 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
sel_i2s_rx_adc2_i2s1	5:4	R/W	0'h	Data Swap for Slot2/3 in ADCDAT1 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
sel_i2s_rx_adc3_i2s1	3:2	R/W	0'h	Data Swap for Slot4/5 in ADCDAT1 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
sel_i2s_rx_adc4_i2s1	1:0	R/W	0'h	Data Swap for Slot6/7 in ADCDAT1 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R

10.36. MX-3Ch: TDM1 Interface Control

Default: 0000’h

Table 55. MX-3Ch: TDM1 Interface Control

DSP Address: 0x1802_0078 **I2C Address: 0x3C**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:12	R	0’h	Reserved
Sel_i2s_rx_adc4_pre_i2s1	11:10	R/W	0’h	TDM1 IF1_ADC4 Data Selection 00’b: Stereo4_ADC_Mixer_L/R 01’b: OutBound6/7 10’b: OutBound0/1 11’b: Reserved
Sel_i2s_rx_adc3_pre_i2s1	9:8	R/W	0’h	TDM1 IF1_ADC3 Data Selection 00’b: Stereo3_ADC_Mixer_L/R 01’b: Mono_ADC_Mixer_L/R 10’b: OutBound4/5 11’b: Reserved
Sel_i2s_rx_adc2_pre_i2s1	7:6	R/W	0’h	TDM1 IF1_ADC2 Data Selection 00’b: Stereo2_ADC_Mixer_L/R 01’b: OutBound2/3 10’b: Reserved 11’b: Reserved
Sel_i2s_rx_adc1_pre_i2s1	5:4	R/W	0’h	TDM1 IF1_ADC1 Data Selection 00’b: Stereo1_ADC_Mixer_L/R 01’b: OutBound0/1 10’b: VAD_ADC 11’b: Reserved
Reserved	3	R	0’h	Reserved
Sel_i2s_rx_i2s1	2:0	R/W	0’h	TDM1 ADC Data Control 000’b: 1/2/3/4 001’b: 2/1/3/4 010’b: 2/3/1/4 011’b: 4/1/2/3 100’b: 1/3/2/4 101’b: 1/4/2/3 110’b: 3/1/2/4 111’b: 3/4/1/2

10.37. MX-3Dh: TDM1 Interface Control

Default: 4000'h

Table 56. MX-3Dh: TDM1 Interface Control

DSP Address: 0x1802_007A **I2C Address: 0x3D**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s_lrck_polarity_i2s1	15	R/W	0'h	TDM1 LRCK Polarity Inverter 0'b: Normal 1'b: Invert
Reserved	14:12	R/W	4'h	Reserved
lrck_pulse_sel_i2s1	11	R/W	0'h	TDM1 LRCK Pulse Width Select (Master Mode Only) 0'b: One BCLK width 1'b: One channel slot width
Reserved	10:8	R/W	0'h	Reserved
mute_tdm2_outl_i2s1	7	R/W	0'h	TDM1 ADC Data Slot0 Mute/Unmute Control 0'b : Un-Mute 1'b : Mute
mute_tdm2_outr_i2s1	6	R/W	0'h	TDM1 ADC Data Slot1 Mute/Unmute Control 0'b : Un-Mute 1'b : Mute
mute_tdm4_outl_i2s1	5	R/W	0'h	TDM1 ADC Data Slot2 Mute/Unmute Control 0'b : Un-Mute 1'b : Mute
mute_tdm4_outr_i2s1	4	R/W	0'h	TDM1 ADC Data Slot3 Mute/Unmute Control 0'b : Un-Mute 1'b : Mute
mute_tdm6_outl_i2s1	3	R/W	0'h	TDM1 ADC Data Slot4 Mute/Unmute Control 0'b : Un-Mute 1'b : Mute
mute_tdm6_outr_i2s1	2	R/W	0'h	TDM1 ADC Data Slot5 Mute/Unmute Control 0'b : Un-Mute 1'b : Mute
mute_tdm8_outl_i2s1	1	R/W	0'h	TDM1 ADC Data Slot6 Mute/Unmute Control 0'b : Un-Mute 1'b : Mute
mute_tdm8_outr_i2s1	0	R/W	0'h	TDM1 ADC Data Slot7 Mute/Unmute Control 0'b : Un-Mute 1'b : Mute

10.38. MX-3Eh: TDM1 Interface Control

Default: 0123'h

Table 57. MX-3Eh: TDM1 Interface Control

DSP Address: 0x1802_007C I2C Address: 0x3E				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
sel_i2s_tx_l_dac1_i2s1	14:12	R/W	0'h	IF1_DAC_0 Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
Reserved	11	R	0'h	Reserved
sel_i2s_tx_r_dac1_i2s1	10:8	R/W	1'h	IF1_DAC_1 Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
Reserved	7	R	0'h	Reserved
sel_i2s_tx_l_dac2_i2s1	6:4	R/W	2'h	IF1_DAC_2 Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
Reserved	3	R	0'h	Reserved
sel_i2s_tx_r_dac2_i2s1	2:0	R/W	3'h	IF1_DAC_3 Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7

10.39. MX-3Fh: TDM1 Interface Control

Default: 0123'h

Table 58. MX-3Fh: TDM1 Interface Control

DSP Address: 0x1802_007E I2C Address: 0x3F				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
sel_i2s_tx_l_dac3_i2s1	14:12	R/W	0'h	IF1_DAC_4 Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
Reserved	11	R	0'h	Reserved
sel_i2s_tx_r_dac3_i2s1	10:8	R/W	1'h	IF1_DAC_5 Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7

DSP Address: 0x1802_007E I2C Address: 0x3F				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	7	R	0'h	Reserved
sel_i2s_tx_l_dac4_i2s1	6:4	R/W	2'h	IF1_DAC_6 Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
Reserved	3	R	0'h	Reserved
sel_i2s_tx_r_dac4_i2s1	2:0	R/W	3'h	IF1_DAC_7 Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7

10.40. MX-40h: TDM2 Interface Control

Default: 0300'h

Table 59. MX-40h: TDM2 Interface Control

DSP Address: 0x1802_0080 I2C Address: 0x40				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
mode_sel_i2s2	12	R/W	0'h	I2S2 / TDM Mode Control 0'b: Normal I2S Mode 1'b: TDM Mode
Tdmslot_sel_i2s2	11:10	R/W	0'h	TDM2 Channel Number Select 00'b: 2ch 01'b: 4ch 10'b: 6ch 11'b: 8ch
Channel_length_i2s2	9:8	R/W	3'h	TDM2 Channel Length 00'b: 16bit (For Slave Mode and Master Mode) 01'b: 20bit (For Slave Mode) 10'b: 24bit (For Slave Mode) 11'b: 32bit (For Slave Mode and Master Mode)
sel_i2s_rx_adc1_i2s2	7:6	R/W	0'h	Data Swap for Slot0/1 in ADCDAT2 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
sel_i2s_rx_adc2_i2s2	5:4	R/W	0'h	Data Swap for Slot2/3 in ADCDAT2 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R

DSP Address: 0x1802_0080 I2C Address: 0x40				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s_rx_adc3_i2s2	3:2	R/W	0'h	Data Swap for Slot4/5 in ADCDAT2 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
sel_i2s_rx_adc4_i2s2	1:0	R/W	0'h	Data Swap for Slot6/7 in ADCDAT2 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R

10.41. MX-41h: TDM2 Interface Control

Default: 0000'h

Table 60. MX-41h: TDM2 Interface Control

DSP Address: 0x1802_0082 I2C Address: 0x41				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:12	R	0'h	Reserved
Sel_i2s_rx_adc4_pre_i2s2	11:10	R/W	0'h	TDM2 IF2_ADC4 Data Selection 00'b: Stereo4_ADC_Mixer_L/R 01'b: OutBound6/7 10'b: OutBound0/1 11'b: Reserved
Sel_i2s_rx_adc3_pre_i2s2	9:8	R/W	0'h	TDM2 IF2_ADC3 Data Selection 00'b: Stereo3_ADC_Mixer_L/R 01'b: Mono_ADC_Mixer_L/R 10'b: OutBound4/5 11'b: Reserved
Sel_i2s_rx_adc2_pre_i2s2	7:6	R/W	0'h	TDM2 IF2_ADC2 Data Selection 00'b: Stereo2_ADC_Mixer_L/R 01'b: OutBound2/3 10'b: Reserved 11'b: Reserved
Sel_i2s_rx_adc1_pre_i2s2	5:4	R/W	0'h	TDM2 IF2_ADC1 Data Selection 00'b: Stereo1_ADC_Mixer_L/R 01'b: OutBound0/1 10'b: VAD_ADC 11'b: Reserved
Reserved	3	R	0'h	Reserved

DSP Address: 0x1802_0082 I2C Address: 0x41				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_i2s_rx_i2s2	2:0	R/W	0'h	TDM2 ADC Data Control 000'b: 1/2/3/4 001'b: 2/1/3/4 010'b: 3/1/2/4 011'b: 4/1/2/3 100'b: 1/3/2/4 101'b: 1/4/2/3 110'b: 2/3/1/4 111'b: 3/4/1/2

10.42. MX-42h: TDM2 Interface Control

Default: 4000'h

Table 61. MX-42h: TDM2 Interface Control

DSP Address: 0x1802_0084 I2C Address: 0x42				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s_lrck_polarity_i2s2	15	R/W	0'h	TDM2 LRCK2 Polarity Inverter 0'b: Normal 1'b: Invert
Reserved	14:12	R/W	4'h	Reserved
lrck_pulse_sel_i2s2	11	R/W	0'h	TDM2 LRCK2 Pulse Width Select (Master Mode Only) 0'b: One BCLK width 1'b: One channel slot width
Reserved	10:8	R/W	0'h	Reserved
mute_tdm2_outl_i2s2	7	R/W	0'h	TDM2 ADC Data Slot0 Mute/Unmute Control 0'b : Un-Mute 1'b : Mute
mute_tdm2_outr_i2s2	6	R/W	0'h	TDM2 ADC Data Slot1 Mute/Unmute Control 0'b : Un-Mute 1'b : Mute
mute_tdm4_outl_i2s2	5	R/W	0'h	TDM2 ADC Data Slot2 Mute/Unmute Control 0'b : Un-Mute 1'b : Mute
mute_tdm4_outr_i2s2	4	R/W	0'h	TDM2 ADC Data Slot3 Mute/Unmute Control 0'b : Un-Mute 1'b : Mute
mute_tdm6_outl_i2s2	3	R/W	0'h	TDM2 ADC Data Slot4 Mute/Unmute Control 0'b : Un-Mute 1'b : Mute
mute_tdm6_outr_i2s2	2	R/W	0'h	TDM2 ADC Data Slot5 Mute/Unmute Control 0'b : Un-Mute 1'b : Mute

DSP Address: 0x1802_0084 I2C Address: 0x42				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mute_tdm8_outl_i2s2	1	R/W	0'h	TDM2 ADC Data Slot6 Mute/Unmute Control 0'b : Un-Mute 1'b : Mute
mute_tdm8_outr_i2s2	0	R/W	0'h	TDM2 ADC Data Slot7 Mute/Unmute Control 0'b : Un-Mute 1'b : Mute

10.43. MX-43h: TDM2 Interface Control

Default: 0123'h

Table 62. MX-43h: TDM2 Interface Control

DSP Address: 0x1802_0086 I2C Address: 0x43				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
sel_i2s_tx_l_dac1_i2s2	14:12	R/W	0'h	IF2_DAC_0 Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
Reserved	11	R	0'h	Reserved
sel_i2s_tx_r_dac1_i2s2	10:8	R/W	1'h	IF2_DAC_1 Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
Reserved	7	R	0'h	Reserved
sel_i2s_tx_l_dac2_i2s2	6:4	R/W	2'h	IF2_DAC_2 Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
Reserved	3	R	0'h	Reserved
sel_i2s_tx_r_dac2_i2s2	2:0	R/W	3'h	IF2_DAC_3 Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7

10.44. MX-44h: TDM2 Interface Control

Default: 0123'h

Table 63. MX-44h: TDM2 Interface Control

DSP Address: 0x1802_0088 I2C Address: 0x44				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
sel_i2s_tx_l_dac3_i2s2	14:12	R/W	0'h	IF2_DAC_4 Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
Reserved	11	R	0'h	Reserved
sel_i2s_tx_r_dac3_i2s2	10:8	R/W	1'h	IF2_DAC_5 Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
Reserved	7	R	0'h	Reserved
sel_i2s_tx_l_dac4_i2s2	6:4	R/W	2'h	IF2_DAC_6 Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
Reserved	3	R	0'h	Reserved
sel_i2s_tx_r_dac4_i2s2	2:0	R/W	3'h	IF2_DAC_7 Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7

10.45. MX-47h: I2C Master Controller Control

Default: 0001'h

Table 64. MX-47h: I2C Master Controller Control

DSP Address: 0x1802_008E I2C Address: 0x47				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_i2c_cmd	15	R/W	0'h	I2C Master Controller Read/Write Command 0'b: Write 1'b: Read
Sel_i2c_data_len	14:12	R/W	0'h	I2C Master Controller Data Length 000'b: 0 byte 001'b: 1 byte 010'b: 2 byte 011'b: 3 byte 100'b: 4 byte Others: Reserved

DSP Address: 0x1802_008E I2C Address: 0x47				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Aec_cmd_start	11	R	0'h	Write "1" to Start Comtroller I2C Command
Sel_i2c_addr_len	10:8	R/W	0'h	I2C Master Controller Address Length 000'b: 1byte 001'b: 2 byte 010'b: 3 byte 011'b: 4 byte 100'b: 5 byte Others: Reserved
Aec_busy	7	R	0'h	I2C Controller R/W Busy 0'b: Normal 1'b: Busy
Reserved	6:2	R	0'h	Reserved
I2c_clk_sel	1:0	R/W	1'h	I2C Clock Rate Selection 00'b: 768kHz 01'b: 384kHz 10'b: 192kHz 11'b: 96kHz

10.46. MX-48h: I2C Master Controller Control

Default: 0000'h

Table 65. MX-48h: I2C Master Controller Control

DSP Address: 0x1802_0090 I2C Address: 0x48				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Aec_addr_1byte	15:8	R/W	0'h	I2C Master Controller Address Command (1byte)
Aec_addr_2byte	7:0	R/W	0'h	I2C Master Controller Address Command (2byte)

10.47. MX-49h: I2C Master Controller Control

Default: 0000'h

Table 66. MX-49h: I2C Master Controller Control

DSP Address: 0x1802_0092 I2C Address: 0x49				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Aec_addr_3byte	15:8	R/W	0'h	I2C Master Controller Address Command (3byte)
Aec_addr_4byte	7:0	R/W	0'h	I2C Master Controller Address Command (4byte)

10.48. MX-4Ah: I2C Master Controller Control

Default: 0000'h

Table 67. MX-4Ah: I2C Master Controller Control

DSP Address: 0x1802_0094 I2C Address: 0x4A				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Aec_addr_5byte	15:8	R/W	0'h	I2C Master Controller Address Command (5byte)
reserved	7	R	0'h	Reserved
I2c_device_addr	6:0	R/W	0'h	Device ID

10.49. MX-4Bh: I2C Master Controller Control

Default: 0000'h

Table 68. MX-4Bh: I2C Master Controller Control

DSP Address: 0x1802_0096 I2C Address: 0x4B				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Aec_write_data_1byte	15:8	R/W	0'h	I2C Master Controller Write Data Command (1byte)
Aec_write_data_2byte	7:0	R/W	0'h	I2C Master Controller Write Data Command (2byte)

10.50. MX-4Ch: I2C Master Controller Control

Default: 0000'h

Table 69. MX-4Ch: I2C Master Controller Control

DSP Address: 0x1802_0098 I2C Address: 0x4C				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Aec_write_data_3byte	15:8	R/W	0'h	I2C Master Controller Write Data Command (3byte)
Aec_write_data_4byte	7:0	R/W	0'h	I2C Master Controller Write Data Command (4byte)

10.51. MX-4Dh: I2C Master Controller Control

Default: 0000'h

Table 70. MX-4Dh: I2C Master Controller Control

DSP Address: 0x1802_009A I2C Address: 0x4D				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
read_data_aec	15:0	R	0'h	I2C Master Controller Read Data Command

10.52. MX-4Eh: I2C Master Controller Control

Default: 0000'h

Table 71. MX-4Eh: I2C Master Controller Control

DSP Address: 0x1802_009C I2C Address: 0x4E				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
read_data_aec2	15:0	R	0'h	I2C Master Controller Read Data Command

10.53. MX-50h: Digital Microphone Control

Default: 1505'h

Table 72. MX-50h: Digital Microphone Control

DSP Address: 0x1802_00A0 I2C Address: 0x50				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_dmic1	15	R/W	0'h	Enable DMIC1 Interface 0'b: Disable 1'b: Enable (Output DMIC clock)
reserved	14	R	0'h	Reserved
sel_dmic_l_edge_stereo1	13	R/W	0'h	DMIC ADC Left Channel to Stereo1 Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_r_edge_stere1	12	R/W	1'h	DMIC ADC Right Channel to Stereo1 Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge

DSP Address: 0x1802_00A0 I2C Address: 0x50				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_dmic_l_edge_stereo3	11	R/W	0'h	DMIC ADC Left Channel to Stereo3 Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_r_edge_stereo3	10	R/W	1'h	DMIC ADC Right Channel to Stereo3 Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_l_edge_stereo2	9	R/W	0'h	DMIC ADC Left Channel to Stereo2 Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_r_edge_stereo2	8	R/W	1'h	DMIC ADC Right Channel to Stereo2 Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_clk	7:5	R/W	0'h	DMIC clock type Control 000'b: 256*fs/2 001'b: 256*fs/3 010'b: 256*fs/4 011'b: 256*fs/6 100'b: 256*fs/8 101'b: 256*fs/12
Reserved	4	R/W	0'h	Reserved
sel_dmic_l_edge_mono	3	R/W	0'h	DMIC ADC Left Channel to Mono Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_r_edge_mono	2	R/W	1'h	DMIC ADC Right Channel to Mono Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_l_edge_stereo4	1	R/W	0'h	DMIC ADC Left Channel to Stereo4 Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_r_edge_stereo4	0	R/W	1'h	DMIC ADC Right Channel to Stereo4 Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge

10.54. MX-51h: Digital Microphone Control

Default: 0055'h

Table 73. MX-51h: Digital Microphone Control

DSP Address: 0x1802_00A2 I2C Address: 0x51				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:4	R	0'h	Reserved
sel_dmic2_lpf_l_edge	3	R/W	0'h	DMIC2 ADC Left Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic2_lpf_r_edge	2	R/W	1'h	DMIC2 ADC Right Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic1_lpf_l_edge	1	R/W	0'h	DMIC1 ADC Left Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic1_lpf_r_edge	0	R/W	1'h	DMIC1 ADC Right Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge

10.55. MX-56h: Haptic Generator Control

Default: 0111'h

Table 74. MX-56h: Haptic Generator Control

DSP Address: 0x1802_00AC I2C Address: 0x56				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Haptic_Act_trigger	15	R	0'h	Actuator Trigger Write "1" to trigger actuator
Haptic_Act_type	14	R/W	0'h	Actuator Type 0'b: Linear Resonant Actuator (AC) 1'b: Eccentric Rotating Mass (DC)
Haptic_Act_mode	13:12	R/W	0'h	Actuator Signal Control 00'b: Disable 01'b: One-shot 10'b: Continuous 11'b: Programmable

DSP Address: 0x1802_00AC I2C Address: 0x56				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Haptic_Act_freq	11:0	R/W	111'h	Actuator Resonant Frequency in 2Hz per Step 111'h: 100Hz … 888'h: 800Hz

10.56. MX-57h: Haptic Generator Control

Default: 0064'h

Table 75. MX-57h: Haptic Generator Control

DSP Address: 0x1802_00AE I2C Address: 0x57				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Haptic_Act_inv	15	R/W	0'h	Actuator Output Invert 0'b: Normal 1'b: Output invert
Haptic_Act_busy	14	R	0'h	Actuator Status (Valid for one-shot and Programmable mode) 0'b: Available and awaiting trigger 1'b: Actuator in progress, ignores any trigger
Reserved	13:12	R	0'h	Reserved
Haptic_Act_duration	11:0	R/W	64'h	Actuator Duration for One-Shot and Programmable Mode in 0.625ms steps 000'h: 0ms 001'h: 0.625ms … FFF'h: 2559.375ms

10.57. MX-58h: Haptic Generator Control

Default: EF0E'h

Table 76. MX-58h: Haptic Generator Control

DSP Address: 0x1802_00B0 I2C Address: 0x58				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Haptic_Act_prog_1	15:0	R/W	EF0E'h	Actuator Programmable Sequence Part 1 (Start of Programmable Sequence) Sequence starts at MSB (Bit 15) Each bit represents a time frame specified by act_duration "1" enables the signal generator

DSP Address: 0x1802_00B0 I2C Address: 0x58				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**

10.58. MX-59h: Haptic Generator Control

Default: F0F0'h

Table 77. MX-59h: Haptic Generator Control

DSP Address: 0x1802_00B2 I2C Address: 0x59				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Haptic_Act_prog_2	15:0	R/W	F0F0'h	Actuator Programmable Sequence Part 2 (Continuation from part 1)

10.59. MX-5Ah: Haptic Generator Control

Default: EF0E'h

Table 78. MX-5Ah: Haptic Generator Control

DSP Address: 0x1802_00B4 I2C Address: 0x5A				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Haptic_Act_prog_3	15:0	R/W	EF0E'h	Actuator Programmable Sequence Part 3 (Continuation from part 2)

10.60. MX-5Bh: Haptic Generator Control

Default: F0F0'h

Table 79. MX-5Bh: Haptic Generator Control

DSP Address: 0x1802_00B6 I2C Address: 0x5B				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Haptic_Act_prog_4	15:0	R/W	F0F0'h	Actuator Programmable Sequence Part 4 (Continuation from part 3)

10.61. MX-5Ch: Haptic Generator Control

Default: EF0E'h

Table 80. MX-5Ch: Haptic Generator Control

DSP Address: 0x1802_00B8 I2C Address: 0x5C				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Haptic_Act_prog_5	15:0	R/W	EF0E'h	Actuator Programmable Sequence Part 5 (Continuation from part 4)

10.62. MX-5Dh: Haptic Generator Control

Default: F0F0'h

Table 81. MX-5Dh: Haptic Generator Control

DSP Address: 0x1802_00BA I2C Address: 0x5D				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Haptic_Act_prog_6	15:0	R/W	F0F0'h	Actuator Programmable Sequence Part 6 (Continuation from part 5)

10.63. MX-5Eh: Haptic Generator Control

Default: F000'h

Table 82. MX-5Eh: Haptic Generator Control

DSP Address: 0x1802_00BC I2C Address: 0x5E				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Haptic_Act_prog_7	15:0	R/W	F000'h	Actuator Programmable Sequence Part 7 (Continuation from part 6)

10.64. MX-5Fh: Haptic Generator Control

Default: 0000'h

Table 83. MX-5Fh: Haptic Generator Control

DSP Address: 0x1802_00BE I2C Address: 0x5F				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Haptic_Act_prog_8	15:0	R/W	0'h	Actuator Programmable Sequence Part 8 (Continuation from part 7)

10.65. MX-61h: Power Management Control 1

Default: 0000'h

Table 84. MX-61h: Power Management Control 1

DSP Address: 0x1802_00C2 I2C Address: 0x61				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_i2s1	15	R/W	0'h	I2S1 Digital interface enable 0'b: Power Down 1'b: Power On
en_i2s2	14	R/W	0'h	I2S2 Digital interface enable 0'b: Power Down 1'b: Power On
reserved	13	R/W	0'h	reserved
pow_dac1	12	R/W	0'h	Analog DAC1 Power Down Control 0'b: Power Down 1'b: Power On
pow_dac2	11	R/W	0'h	Analog DAC2 Power Down Control 0'b: Power Down 1'b: Power On
reserved	10:5	R/W	0'h	Reserved
Pow_adcfed1	4	R/W	0'h	Analog ADC Front-End Left Channel Power Control 0'b: Power down 1'b: Power on
Pow_adcfed2	3	R/W	0'h	Analog ADC Front-End Right Channel Power Control 0'b: Power down 1'b: Power on
pow_adc_l	2	R/W	0'h	Analog ADC_L Power Down Control 0'b: Power Down 1'b: Power On left STEREO ADC
pow_adc_r	1	R/W	0'h	Analog ADC_R Power Down Control 0'b: Power Down 1'b: Power On right STEREO ADC

DSP Address: 0x1802_00C2 I2C Address: 0x61				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
En_i2c_master	0	R/W	0'h	Enable I2C Master Mode 0'b: Disable (stop clock) 1'b: Enable (will also enable RC clock as clock source)

10.66. MX-62h: Power Management Control 2

Default: 0000'h

Table 85. MX-62h: Power Management Control 2

DSP Address: 0x1802_00C4 I2C Address: 0x62				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
pow_adc_stereo1_filter	15	R/W	0'h	Power on ADC Stereo1 Filter 0'b: Power Down 1'b: Power On
pow_adc_monol_filter	14	R/W	0'h	Power on ADC Mono Left Filter 0'b: Power Down 1'b: Power On
pow_adc_monor_filter	13	R/W	0'h	Power on ADC Mono Right Filter 0'b: Power Down 1'b: Power On
pow_dac_stereo1_filter	12	R/W	0'h	Power on DAC Stereo1 Filter 0'b: Power Down 1'b: Power On
pow_dac_mono2l_filter	11	R/W	0'h	Power on DAC Mono 2 Left Filter 0'b: Power Down 1'b: Power On
pow_dac_mono2r_filter	10	R/W	0'h	Power on DAC Mono 2 Right Filter 0'b: Power Down 1'b: Power On
pow_dac_mono3l_filter	9	R/W	0'h	Power on DAC Mono 3 Left Filter 0'b: Power Down 1'b: Power On
pow_dac_mono3r_filter	8	R/W	0'h	Power on DAC Mono 3 Right Filter 0'b: Power Down 1'b: Power On
pow_dac_mono4l_filter	7	R/W	0'h	Power on DAC Mono 4 Left Filter 0'b: Power Down 1'b: Power On
pow_dac_mono4r_filter	6	R/W	0'h	Power on DAC Mono 4 Right Filter 0'b: Power Down 1'b: Power On

DSP Address: 0x1802_00C4 I2C Address: 0x62				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
pow_adc_stereo2_filter	5	R/W	0'h	Power on ADC Stereo2 Filter 0'b: Power Down 1'b: Power On
pow_adc_stereo3_filter	4	R/W	0'h	Power on ADC Stereo3 Filter 0'b: Power Down 1'b: Power On
pow_adc_stereo4_filter	3	R/W	0'h	Power on ADC Stereo4 Filter 0'b: Power Down 1'b: Power On
Pow_pdm1	2	R/W	0'h	Power on PDM1 Interface 0'b: Power down 1'b: Power on
Reserved	1:0	R	0'h	Reserved

10.67. MX-63h: Power Management Control 3

Default: 0055'h

Table 86. MX-63h: Power Management Control 3

DSP Address: 0x1802_00C6 I2C Address: 0x63				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
pow_vref1	15	R/W	0'h	Enable VREF1 Voltage 0'b: Power down 1'b: Power on
en_fastb1	14	R/W	0'h	Fast Charge for VREF1 0'b: Fast VREF1 1'b: Slow VREF1 for good performance
pow_main_bias	13	R/W	0'h	Enable All Analog Circuit Bias 0'b: Power down 1'b: Power on
pow_lout1	12	R/W	0'h	LOUT1 Power Control 0'b: Power down 1'b: Power on
pow_bg_mbias	11	R/W	0'h	MBIAS Bandgap Power Control 0'b: Power down 1'b: Power on
pow_lout2	10	R/W	0'h	LOUT2 Power Control 0'b: Power down 1'b: Power on
reserved	9	R/W	0'h	reserved
pow_vref2	8	R/W	0'h	Enable VREF2 Voltage 0'b: Power down 1'b: Power on

DSP Address: 0x1802_00C6 I2C Address: 0x63				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_fastb2	7	R/W	0'h	Fast Charge for VREF2 0'b: Fast VREF2 1'b: Slow VREF2 for good performance
Dvo_ldo2	6:4	R/W	5'h	Selection of The LDO2 Output 000'b: 0.7V 001'b: 0.8V 010'b: 0.9V 011'b: 1.0V 100'b: 1.1V 101'b: 1.2V 110'b: 1.3V 111'b: 1.4V
Reserved	3	R	0'h	Reserved
Dvo_ldo1	2:0	R/W	5'h	Selection of The LDO1 Output LDO_IN=1.8V LDO_IN=1.2V 000'b: 1.74V 1.16V 001'b: 0.8V 0.53V 010'b: 0.9V 0.60V 011'b: 1.0V 0.67V 100'b: 1.1V 0.73V 101'b: 1.2V 0.80V 110'b: 1.3V 0.87V 111'b: 1.4V 0.93V

10.68. MX-64h: Power Management Control 4

Default: 0000'h

Table 87. MX-64h: Power Management Control 4

DSP Address: 0x1802_00C8 I2C Address: 0x64				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
pow_bst1	15	R/W	0'h	MIC Boost 1 Power Control – VON 0'b: Power down 1'b: Power on
pow_bst2	14	R/W	0'h	MIC Boost 2 Power Control – VON 0'b: Power down 1'b: Power on
Pow_clk_micbias1	13	R/W	0'h	MICBIAS1 Clock Power Control 0'b: Power down 1'b: Power on
reserved	12	R/W	0'h	reserved
pow_micbias1	11	R/W	0'h	MICBIAS1 Power Control 0'b: Power down 1'b: Power on

DSP Address: 0x1802_00C8 I2C Address: 0x64				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
pow_pump_micbias1	10	R/W	0'h	MICBIAS1 VREFP Pump Power Control (Added at next chip version) 0'b: Power down 1'b: Power on
pow_pll1	9	R/W	0'h	PLL1 Power/Reset Control 0'b: Power down and reset 1'b: Power on PLL
pow_pll2	8	R/W	0'h	PLL2 Power/Reset Control 0'b: Power down and reset 1'b: Power on PLL
Pow_dcvdd2	7	R/W	0'h	Codec Core Power Power Control 0'b: Power down 1'b: Power on
Reserved	6	R/W	0'h	Reserved
Pow2_bst1	5	R/W	0'h	MIC Boost 1 Power Control – VOP 0'b: Power down 1'b: Power on
Pow2_bst2	4	R/W	0'h	MIC Boost 2 Power Control – VOP 0'b: Power down 1'b: Power on
Reserved	3:2	R/W	0'h	Reserved
pow_clk25m	1	R/W	0'h	Internal Clock Power 0'b: Power down 1'b: Power on
Pow_ldo1	0	R/W	0'h	LDO1 Power Control 0'b: Power off 1'b: Power on

10.69. MX-65h: Power Management Control 5

Default: 0001'h

Table 88. MX-65h: Power Management Control 5

DSP Address: 0x1802_00CA I2C Address: 0x65				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:11	R	0'h	Reserved
Sram_reg_pow_7	10	R/W	0'h	Power Down System Band7 0'b: Power down 1'b: Power on
Sram_reg_pow_6	9	R/W	0'h	Power Down System Band6 0'b: Power down 1'b: Power on
Sram_reg_pow_5	8	R/W	0'h	Power Down System Band5 0'b: Power down 1'b: Power on

DSP Address: 0x1802_00CA I2C Address: 0x65				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sram_reg_pow_4	7	R/W	0'h	Power Down System Band4 0'b: Power down 1'b: Power on
Sram_reg_pow_3	6	R/W	0'h	Power Down System Band3 0'b: Power down 1'b: Power on
Sram_reg_pow_2	5	R/W	0'h	Power Down System Band2 0'b: Power down 1'b: Power on
Sram_reg_pow_1	4	R/W	0'h	Power Down System Band1 0'b: Power down 1'b: Power on
Sram_reg_pow_0	3	R/W	0'h	Power Down System Band0 0'b: Power down 1'b: Power on
Multi_ch_reg_pow	2	R/W	0'h	Power Down InBound4 ~ 10 and OutBound4 ~ 10 0'b: Power down 1'b: Power on
Dsp_reg_pow	1	R/W	0'h	Power Down All DSP 0'b: Power down 1'b: Power on
Cpu_runstall	0	R/W	1'h	DSP CPU Control 0'b: Run 1'b: Stop

10.70. MX-66h: Power Management Control 6

Default: 0000'h

Table 89. MX-66h: Power Management Control 6

DSP Address: 0x1802_00CC I2C Address: 0x66				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:10	R	0'h	Reserved
Sram_reg_pow_7_rdy	9	R	0'h	System Band7 Ready Status 0'b: Off or Busy 1'b: Ready
Sram_reg_pow_6_rdy	8	R	0'h	System Band6 Ready Status 0'b: Off or Busy 1'b: Ready
Sram_reg_pow_5_rdy	7	R	0'h	System Band5 Ready Status 0'b: Off or Busy 1'b: Ready
Sram_reg_pow_4_rdy	6	R	0'h	System Band4 Ready Status 0'b: Off or Busy 1'b: Ready

DSP Address: 0x1802_00CC I2C Address: 0x66				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sram_reg_pow_3_rdy	5	R	0'h	System Band3 Ready Status 0'b: Off or Busy 1'b: Ready
Sram_reg_pow_2_rdy	4	R	0'h	System Band2 Ready Status 0'b: Off or Busy 1'b: Ready
Sram_reg_pow_1_rdy	3	R	0'h	System Band1 Ready Status 0'b: Off or Busy 1'b: Ready
Sram_reg_pow_0_rdy	2	R	0'h	System Band0 Ready Status 0'b: Off or Busy 1'b: Ready
Multi_ch_reg_pow_rdy	1	R	0'h	DSP InBound4 ~ 10 and OutBound4 ~ 10 Ready Status 0'b: Off or Busy 1'b: Ready
Dsp_reg_rdy	0	R	0'h	DSP Ready Status 0'b: Off or Busy 1'b: Ready

10.71. MX-67h: Power Management Control 7

Default: 0000'h

Table 90. MX-67h: Power Management Control 7

DSP Address: 0x1802_00CE I2C Address: 0x67				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:11	R	0'h	Reserved
Pow_dcvdd2_iso	10	R/W	0'h	Enable Isolation for DCVDD2 0'b: Isolation 1'b: Normal
Pow_dsp_iso	9	R/W	0'h	Enable Isolation for DSP 0'b: Isolation 1'b: Normal
Sram_reg_pow_iso_7	8	R/W	0'h	Enable Isolation for Band7 0'b: Enable 1'b: Disable
Sram_reg_pow_iso_6	7	R/W	0'h	Enable Isolation for Band6 0'b: Enable 1'b: Disable
Sram_reg_pow_iso_5	6	R/W	0'h	Enable Isolation for Band5 0'b: Enable 1'b: Disable
Sram_reg_pow_iso_4	5	R/W	0'h	Enable Isolation for Band4 0'b: Enable 1'b: Disable

DSP Address: 0x1802_00CE I2C Address: 0x67				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sram_reg_pow_iso_3	4	R/W	0'h	Enable Isolation for Band3 0'b: Enable 1'b: Disable
Sram_reg_pow_iso_2	3	R/W	0'h	Enable Isolation for Band2 0'b: Enable 1'b: Disable
Sram_reg_pow_iso_1	2	R/W	0'h	Enable Isolation for Band1 0'b: Enable 1'b: Disable
Sram_reg_pow_iso_0	1	R/W	0'h	Enable Isolation for Band0 0'b: Enable 1'b: Disable
Multi_ch_reg_pow_iso	0	R/W	0'h	Enable Isolation for InBound4 ~ 10 and OutBound4 ~ 10 0'b: Enable 1'b: Disable

10.72. MX-68h: ADC/DAC HPF Control

Default: 0E00'h

Table 91. MX-68h: ADC/DAC HPF Control

DSP Address: 0x1802_00D0 I2C Address: 0x68				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:12	R	0'h	Reserved
dahpf_en	11	R/W	1'h	Enable Stereo/Mono/DD1/DD2 DAC High Pass Filter 0'b: Disable 1'b: Enable
adhpf_en	10	R/W	1'h	Enable Stereo1/2/3/4 ADC High Pass Filter 0'b: Disable 1'b: Enable
mono_adhpf_en	9	R/W	1'h	Enable Mono ADC High Pass Filter 0'b: Disable 1'b: Enable
Dahpf_coef	8:3	R/W	0'h	Stereo/Mono/DD1/DD2 DAC HPF Coefficient
Da_sample_rate	2:0	R/W	0'h	Stereo/Mono/DD1/DD2 DAC HPF Sample Rate

10.73. MX-6Ah: Private Register Index

Default: 0000'h

Table 92. MX-6Ah: Private Register Index

Name	Bits	Read/Write	Reset State	Description
reserved	15:8	R	0'h	reserved
Pr_index	7:0	R/W	0'h	PR Register Index

10.74. MX-6Ch: Private Register Data

Default: 0000'h

Table 93. MX-6Ch: Private Register Data

Name	Bits	Read/Write	Reset State	Description
Pr_data	15:0	R/W	0'h	PR Register Data

10.75. MX-70h: I2S1 Digital Interface Control

Default: 8000'h

Table61. MX-70h: I2S1 Digital Interface Control

DSP Address: 0x1802_00E0 **I2C Address: 0x70**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s1_ms	15	R/W	1'h	I2S1 Serial Data Port Mode Selection 0'b: Master 1'b: Slave
reserved	14:12	R	0'h	Reserved
En_i2s1_out_comp	11:10	R/W	0'h	I2S1 Output Data Compress (For ADCDAT1 Output) 00'b: OFF 01'b: μ law 10'b: A law 11'b: Reserved
en_i2s1_in_comp	9:8	R/W	0'h	I2S1 Input Compress (For DACDAT1 Input) 00'b: OFF 01'b: μ law 10'b: A law 11'b: Reserved
Inv_i2s1_bclk	7	R/W	0'h	I2S1 BCLK Polarity Control 0'b: Normal 1'b: Invert *I2S master mode don't support polarity control, fix at normal mode
reserved	6:4	R	0'h	Reserved

DSP Address: 0x1802_00E0 I2C Address: 0x70				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s1_len	3:2	R/W	0'h	I2S1 Data Length Selection 00'b: 16 bits 01'b: 20 bits 10'b: 24 bits 11'b: 8 bits
sel_i2s1_format	1:0	R/W	0'h	I2S1 PCM Data Format Selection 00'b: I^2S format 01'b: Left justified 10'b: PCM Mode A (LRCK One Plus at Master Mode) 11'b: PCM Mode B (LRCK One Plus at Master Mode)

10.76. MX-71h: I2S2 Digital Interface Control

Default: 8000'h

Table 94. MX-71h: I2S2 Digital Interface Control

DSP Address: 0x1802_00E2 I2C Address: 0x71				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s2_ms	15	R/W	1'h	I2S2 Serial Data Port Mode Selection 0'b: Master 1'b: Slave
reserved	14:12	R	0'h	Reserved
en_i2s2_out_comp	11:10	R/W	0'h	I2S2 Output Compress (For ADCDAT2 Output) 00'b: OFF 01'b: μ law 10'b: A law 11'b: Reserved
en_i2s2_in_comp	9:8	R/W	0'h	I2S2 Input Compress (For DACDAT2 Input) 00'b: OFF 01'b: μ law 10'b: A law 11'b: Reserved
inv_i2s2_bclk	7	R/W	0'h	I2S2 BCLK Polarity Control 0'b: Normal 1'b: Invert *I2S master mode don't support polarity control, fix at normal mode
reserved	6:4	R	0'h	Reserved
sel_i2s2_len	3:2	R/W	0'h	I2S2 Data Length Selection 00'b: 16 bits 01'b: 20 bits 10'b: 24 bits 11'b: 8bits

DSP Address: 0x1802_00E2 I2C Address: 0x71				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s2_format	1:0	R/W	0'h	I2S2 PCM Data Format Selection 00'b: I^2S format 01'b: Left justified 10'b: PCM Mode A (LRCK One Plus at Master Mode) 11'b: PCM Mode B (LRCK One Plus at Master Mode)

10.77. MX-73h: Clock Tree Control

Default: 1111'h

Table 95. MX-73h: Clock Tree Control

DSP Address: 0x1802_00E6 I2C Address: 0x73				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15	R	0'h	Reserved
sel_i2s_pre_div1	14:12	R/W	1'h	I2S_Pre_Div1 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16
Reserved	11	R	0'h	Reserved
sel_i2s_pre_div2	10:8	R/W	1'h	I2S_Pre_Div2 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16
reserved	7	R/W	0'h	reserved
sel_i2s_pre_div3	6:4	R/W	1'h	I2S_Pre_Div3 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16
reserved	3	R/W	0'h	reserved

DSP Address: 0x1802_00E6 I2C Address: 0x73				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s_pre_div4	2:0	R/W	1'h	I2S_Pre_Div4 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16

10.78. MX-74h: Clock Tree Control

Default: 1111'h

Table 96. MX-74h: Clock Tree Control

DSP Address: 0x1802_00E8 I2C Address: 0x74				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15	R	0'h	Reserved
sel_i2s_pre_div5	14:12	R/W	1'h	I2S_Pre_Div5 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16
reserved	11	R	0'h	Reserved
sel_i2s_pre_div6	10:8	R/W	1'h	I2S_Pre_Div6 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16
reserved	7	R	0'h	Reserved

DSP Address: 0x1802_00E8 I2C Address: 0x74				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s_pre_div7	6:4	R/W	1'h	I2S_Pre_Div7 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16
reserved	3	R	0'h	Reserved
sel_i2s_pre_div8	2:0	R/W	1'h	I2S_Pre_Div8 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16

10.79. MX-75h: Clock Tree Control

Default: 0000'h

Table 97. MX-75h: Clock Tree Control

DSP Address: 0x1802_00EA I2C Address: 0x75				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:8	R	0'h	Reserved
Sel_dsp_asrcout_div	7:6	R/W	0'h	DSP ASRCOUT Divider 00b: ÷ 1 01b: ÷ 1.5 10b: ÷ 2 11b: ÷ 3
Sel_dsp_asrcin_div	5:4	R/W	0'h	DSP ASRCIN Divider 00b: ÷ 1 01b: ÷ 1.5 10b: ÷ 2 11b: ÷ 3
Reserved	3	R	0'h	Reserved

DSP Address: 0x1802_00EA I2C Address: 0x75				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_dsp_bus_pre_div	2:0	R/W	0'h	DSP Bus Pre-Divider 000b: ÷ 2 001b: ÷ 4 010b: ÷ 8 011b: ÷ 16 100b: ÷ 32 101b: ÷ 64 110b: ÷ 128 111b: ÷ 1

10.80. MX-7Ah: PLL1 M/N/K Code Control

Default: 0000'h

Table 98. MX-7Ah: PLL1 M/N/K Code Control

DSP Address: 0x1802_00F4 I2C Address: 0x7A				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Pll1_n_code	15:7	R/W	0'h	N[8:0] Code for Analog PLL1 000000000'b: Div 2 000000001'b: Div 3 …….. 111111111'b: Div 513
reserved	6	R	0'h	Reserved
Pll1_k_bypass	5	R/W	0'h	Bypass PLL1 K Code 0'b : No bypass 1'b : Bypass
Pll1_k_code	4:0	R/W	0'h	K[4:0] Code for Analog PLL1 00000'b: Div 2 00001'b: Div 3 …… 11111'b: Div 33

10.81. MX-7Bh: PLL M/N/K Code Control

Default: 0000'h

Table 99. MX-7Bh: PLL M/N/K Code Control

DSP Address: 0x1802_00F6 I2C Address: 0x7B				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Pll1_m_code	15:12	R/W	0'h	M[3:0] Code for Analog PLL1 0000'b: Div 2 0001'b: Div 3 …….. 1111'b: Div 17
Pll1_m_bypass	11	R/W	0'h	Bypass PLL1 M Code 0'b : No bypass 1'b : Bypass
reserved	10:2	R	0'h	Reserved
Update_pll1	1	R/W	0'h	Update PLL1 0'b: No update PLL1 parameter 1'b: Update PLL1 parameter
Sta_pll1_ready	0	R	0'h	PLL1 Ready Status 0'b: Not ready (or power off) 1'b: Ready

10.82. MX-7Ch: PLL2 M/N/K Code Control

Default: 0000'h

Table 100. MX-7Ch: PLL2 M/N/K Code Control

DSP Address: 0x1802_00F8 I2C Address: 0x7C				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Pll2_n_code	15:6	R/W	31'h	N[9:0] Code for Analog PLL2 000000000'b: Div 2 000000001'b: Div 3 …….. 111111111'b: Div 513
Pll2_k_bypass	5	R/W	1'h	Bypass PLL2 K Code 0'b : No bypass 1'b : Bypass
Pll2_k_code	4:0	R/W	0'h	K[4:0] Code for Analog PLL2 00000'b: Div 2 00001'b: Div 3 …… 11111'b: Div 33

10.83. MX-7Dh: PLL2 M/N/K Code Control

Default: 2000'h

Table 101. MX-7Dh: PLL2 M/N/K Code Control

DSP Address: 0x1802_00FA I2C Address: 0x7D				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Pll2_m_code	15:12	R/W	2'h	M[3:0] Code for Analog PLL2 0000'b: Div 2 0001'b: Div 3 …….. 1111'b: Div 17
Pll2_m_bypass	11	R/W	0'h	Bypass PLL2 M Code 0'b : No bypass 1'b : Bypass
reserved	10:2	R	0'h	Reserved
Update_pll2	1	R/W	0'h	Update PLL2 0'b: No update PLL2 parameter 1'b: Update PLL2 parameter
Sta_pll2_ready	0	R	0'h	PLL2 Ready Status 0'b: Not ready (or power off) 1'b: Ready

10.84. MX-80h: Clock Tree Control

Default: 0000'h

Table 102. MX-80h: Clock Tree Control

DSP Address: 0x1802_0100 I2C Address: 0x80				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_sysclk1	15:14	R/W	0'h	System Clock Source MUX Control 00'b: MCLK 01'b: PLL1 10'b: Internal Clock 11'b: Reserved

DSP Address: 0x1802_0100 I2C Address: 0x80				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_pll1_sour	13:11	R/W	0'h	PLL1 Source Select 000'b: From MCLK 001'b: From BCLK1 010'b: From BCLK2 011'b: Reserved 100'b: Reserved 101'b: From RC Clock 110'b: Reserved Others: Reserved
Reserved	10:9	R	0'h	Reserved
sel_pll_pre_div1	8	R/W	0'h	Pll-1 pre_divider 0'b: ÷ 1 1'b: ÷ 2
sel_dac_osr	7:6	R/W	0'h	Stereo DAC Over Sample Rate Select 00'b:128Fs 01'b:64Fs 10'b:32Fs 11'b:Reserved
sel_adc_osr	5:4	R/W	0'h	Stereo1 ADC Over Sample Rate Select 00'b:128Fs 01'b:64Fs 10'b:32Fs 11'b:Reserved
Reserved	3:0	R	0'h	Reserved

10.85. MX-81h: Clock Tree Control

Default: 0000'h

Table 103. MX-81h: Clock Tree Control

DSP Address: 0x1802_0102 I2C Address: 0x81				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15	R/W	0'h	reserved
sel_pll2_sour	14:12	R/W	0'h	PLL2 Source Select 000'b: From MCLK 001'b: From BCLK1 010'b: From BCLK2 011'b: Reserved 100'b: Reserved 101'b: From RC Clock 110'b: Reserved Others: Reserved

DSP Address: 0x1802_0102 I2C Address: 0x81				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_dsp_asrcout_sour	11:10	R/W	0'h	DSP ASRCOUT Clock Source Select 00'b: From MCLK 01'b: From PLL1 10'b: Reserved 11'b: From RC clock
Sel_dsp_asrcin_sour	9:8	R/W	0'h	DSP ASRCIN Clock Source Select 00'b: From MCLK 01'b: From PLL1 10'b: Reserved 11'b: From RC clock
Sel_dsp_clock_sour	7	R/W	0'h	Select DSP Clock Source 0'b: From PLL2 1'b: Bypass PLL2
Reserved	6:0	R	0'h	Reserved

10.86. MX-83h: ASRC Control

Default: 0000'h

Table 104. MX-83h: ASRC Control

DSP Address: 0x1802_0106 I2C Address: 0x83				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_mono_da_3l_mode	15	R/W	0'h	Enable DAC ASRC for DD1_L 0'b : Disable 1'b : Enable
Sel_mono_da_3r_mode	14	R/W	0'h	Enable DAC ASRC for DD1_R 0'b : Disable 1'b : Enable
Sel_mono_da_4l_mode	13	R/W	0'h	Enable DAC ASRC for DD2_L 0'b : Disable 1'b : Enable
Sel_mono_da_4r_mode	12	R/W	0'h	Enable DAC ASRC for DD2_R 0'b : Disable 1'b : Enable
Reserved	11:6	R	0'h	Reserved
En_i2s6_asrc	5	R/W	0'h	Enable I2S6 ASRC Function 0'b: Disable 1'b: Enable
En_i2s5_asrc	4	R/W	0'h	Enable I2S5 ASRC Function 0'b: Disable 1'b: Enable

DSP Address: 0x1802_0106 I2C Address: 0x83				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
En_i2s4_asrc	3	R/W	0'h	Enable I2S4 ASRC Function 0'b: Disable 1'b: Enable
En_i2s3_asrc	2	R/W	0'h	Enable I2S3 ASRC Function 0'b: Disable 1'b: Enable
En_i2s2_asrc	1	R/W	0'h	Enable I2S2 ASRC Function 0'b: Disable 1'b: Enable
En_i2s1_asrc	0	R/W	0'h	Enable I2S1 ASRC Function 0'b: Disable 1'b: Enable

10.87. MX-84h: ASRC Control

Default: 0000'h

Table 105. MX-84h: ASRC Control

DSP Address: 0x1802_0108 I2C Address: 0x84				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
Sel_stereo_dac_mode	14	R/W	0'h	Enable DAC ASRC for Stereo DAC 0'b : Disable 1'b : Enable
Sel_mono_dac_l_mode	13	R/W	0'h	Enable DAC ASRC for Mono_L 0'b : Disable 1'b : Enable
Sel_mono_dac_r_mode	12	R/W	0'h	Enable DAC ASRC for Mono_R 0'b : Disable 1'b : Enable
en_dmic_asrc_stereo1	11	R/W	0'h	Enable DMIC ASRC for Stereo1 ADC 0'b : Disable 1'b : Enable
en_dmic_asrc_stereo2	10	R/W	0'h	Enable DMIC ASRC for Stereo2 ADC 0'b : Disable 1'b : Enable
en_dmic_asrc_stereo3	9	R/W	0'h	Enable DMIC ASRC for Stereo3 ADC 0'b : Disable 1'b : Enable
en_dmic_asrc_stereo4	8	R/W	0'h	Enable DMIC ASRC for Stereo4 ADC 0'b : Disable 1'b : Enable

DSP Address: 0x1802_0108 I2C Address: 0x84				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_dmic_asrc_monol	7	R/W	0'h	Enable DMIC ASRC for Mono_L ADC 0'b : Disable 1'b : Enable
en_dmic_asrc_monor	6	R/W	0'h	Enable DMIC ASRC for Mono_R ADC 0'b : Disable 1'b : Enable
en_adc_asrc_stereo1	5	R/W	0'h	Enable ADC ASRC for Stereo1 0'b : Disable 1'b : Enable
en_adc_asrc_stereo2	4	R/W	0'h	Enable ADC ASRC for Stereo2 0'b : Disable 1'b : Enable
en_adc_asrc_stereo3	3	R/W	0'h	Enable ADC ASRC for Stereo3 0'b : Disable 1'b : Enable
en_adc_asrc_stereo4	2	R/W	0'h	Enable ADC ASRC for Stereo4 0'b : Disable 1'b : Enable
en_adc_asrc_monol	1	R/W	0'h	Enable ADC ASRC for Mono 0'b : Disable 1'b : Enable
en_adc_asrc_monor	0	R/W	0'h	Enable ADC ASRC for Mono 0'b : Disable 1'b : Enable

10.88. MX-85h: ASRC Control

Default: 0000'h

Table 106. MX-85h: ASRC Control

DSP Address: 0x1802_010A I2C Address: 0x85				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_da_filter_stereo_asrc	15:12	R/W	0'h	Select the ASRC Clock Source for Stereo DAC 0000'b: CLK_sys 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: clk_i2s3_asrc 0100'b: clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_sys2 1000'b: clk_sys3 1001'b: clk_sys4 1010'b: clk_sys5 1011'b: clk_sys6 1100'b: clk_sys7 Others: Reserved
Reserved	11	R	0'h	Reserved
sys_div_stereo_da_filter	10:8	R/W	0'h	Set the System Clock Division for Stereo DAC 000'b: div1 001'b: div2 010'b: div3 011'b: div4 100'b: div6 101'b: div8 110'b: div12 111'b: div16
sel_da_filter_mono2l_asrc	7:4	R/W	0'h	Select the ASRC Clock Source for Mono2_L DAC 0000'b: CLK_sys 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: clk_i2s3_asrc 0100'b: clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_sys2 1000'b: clk_sys3 1001'b: clk_sys4 1010'b: clk_sys5 1011'b: clk_sys6 1100'b: clk_sys7 Others: Reserved

DSP Address: 0x1802_010A I2C Address: 0x85				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_da_filter_mono2r_asrc	3:0	R/W	0'h	Select the ASRC Clock Source for Mono2_R DAC 0000'b: CLK_sys 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: clk_i2s3_asrc 0100'b: clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_sys2 1000'b: clk_sys3 1001'b: clk_sys4 1010'b: clk_sys5 1011'b: clk_sys6 1100'b: clk_sys7 Others: Reserved

10.89. MX-86h: ASRC Control

Default: 0000'h

Table 107. MX-86h: ASRC Control

DSP Address: 0x1802_010C I2C Address: 0x86				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_da_filter_mono3l_asrc	15:12	R/W	0'h	Select the ASRC Clock Source for Mono3_L DAC 0000'b: CLK_sys 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: clk_i2s3_asrc 0100'b: clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_sys2 1000'b: clk_sys3 1001'b: clk_sys4 1010'b: clk_sys5 1011'b: clk_sys6 1100'b: clk_sys7 Others: Reserved

DSP Address: 0x1802_010C I2C Address: 0x86				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_da_filter_mono 3r_asrc	11:8	R/W	0'h	Select the ASRC Clock Source for Mono3_R DAC 0000'b: CLK_sys 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: clk_i2s3_asrc 0100'b: clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_sys2 1000'b: clk_sys3 1001'b: clk_sys4 1010'b: clk_sys5 1011'b: clk_sys6 1100'b: clk_sys7 Others: Reserved
sel_da_filter_mono 4l_asrc	7:4	R/W	0'h	Select the ASRC Clock Source for Mono4_L DAC 0000'b: CLK_sys 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: clk_i2s3_asrc 0100'b: clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_sys2 1000'b: clk_sys3 1001'b: clk_sys4 1010'b: clk_sys5 1011'b: clk_sys6 1100'b: clk_sys7 Others: Reserved
sel_da_filter_mono 4r_asrc	3:0	R/W	0'h	Select the ASRC Clock Source for Mono4_R DAC 0000'b: CLK_sys 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: clk_i2s3_asrc 0100'b: clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_sys2 1000'b: clk_sys3 1001'b: clk_sys4 1010'b: clk_sys5 1011'b: clk_sys6 1100'b: clk_sys7 Others: Reserved

10.90. MX-87h: ASRC Control

Default: 0000’h

Table 108. MX-87h: ASRC Control

DSP Address: 0x1802_010E **I2C Address: 0x87**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_ad_filter_stereo1_asrc	15:12	R/W	0’h	Select the ASRC Clock Source for Stereo1 ADC 0000’b: CLK_sys 0001’b: clk_i2s1_asrc 0010’b: clk_i2s2_asrc 0011’b: clk_i2s3_asrc 0100’b: clk_i2s4_asrc 0101’b: clk_i2s5_asrc 0110’b: clk_i2s6_asrc 0111’b: clk_sys2 1000’b: clk_sys3 1001’b: clk_sys4 1010’b: clk_sys5 1011’b: clk_sys6 1100’b: clk_sys7 Others: Reserved

DSP Address: 0x1802_010E I2C Address: 0x87				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_ad_filter_stereo2_asrc	11:8	R/W	0'h	Select the ASRC Clock Source for Stereo2 ADC 0000'b: CLK_sys 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: clk_i2s3_asrc 0100'b: clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_sys2 1000'b: clk_sys3 1001'b: clk_sys4 1010'b: clk_sys5 1011'b: clk_sys6 1100'b: clk_sys7 Others: Reserved
sel_ad_filter_stereo3_asrc	7:4	R/W	0'h	Select the ASRC Clock Source for Stereo3 ADC 0000'b: CLK_sys 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: clk_i2s3_asrc 0100'b: clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_sys2 1000'b: clk_sys3 1001'b: clk_sys4 1010'b: clk_sys5 1011'b: clk_sys6 1100'b: clk_sys7 Others: Reserved
sel_ad_filter_stereo4_asrc	3:0	R/W	0'h	Select the ASRC Clock Source for stereo4 ADC 0000'b: CLK_sys 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: clk_i2s3_asrc 0100'b: clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_sys2 1000'b: clk_sys3 1001'b: clk_sys4 1010'b: clk_sys5 1011'b: clk_sys6 1100'b: clk_sys7 Others: Reserved

10.91. MX-88h: ASRC Control

Default: 0000’h

Table 109. MX-88h: ASRC Control

DSP Address: 0x1802_0110 **I2C Address: 0x88**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_ad_filter_mono l_asrc	15:12	R/W	0’h	Select the ASRC Clock Source for Mono_L ADC 0000’b: CLK_sys 0001’b: clk_i2s1_asrc 0010’b: clk_i2s2_asrc 0011’b: clk_i2s3_asrc 0100’b: clk_i2s4_asrc 0101’b: clk_i2s5_asrc 0110’b: clk_i2s6_asrc 0111’b: clk_sys2 1000’b: clk_sys3 1001’b: clk_sys4 1010’b: clk_sys5 1011’b: clk_sys6 1100’b: clk_sys7 Others: Reserved

DSP Address: 0x1802_0110 **I2C Address: 0x88**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_ad_filter_monor_asrc	11:8	R/W	0'h	Select the ASRC Clock Source for Mono_R ADC 0000'b: CLK_sys 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: clk_i2s3_asrc 0100'b: clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_sys2 1000'b: clk_sys3 1001'b: clk_sys4 1010'b: clk_sys5 1011'b: clk_sys6 1100'b: clk_sys7 Others: Reserved
Reserved	7:0	R	0'h	Reserved

10.92. MX-89h: ASRC Control

Default: 0000'h

Table 110. MX-89h: ASRC Control

DSP Address: 0x1802_0112 **I2C Address: 0x89**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_dsp_out_fs_sec1	15:12	R/W	0'h	Select the ASRC Clock Source for DSP OutBound0 ~ 3 0000'b: clk_sys_div_out 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: clk_i2s3_asrc 0100'b: clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_sys2 1000'b: clk_sys3 1001'b: clk_sys4 1010'b: clk_sys5 1011'b: clk_sys6 1100'b: clk_sys7 1101'b: clk_sys8 Others: Reserved
sel_dsp_out_fs_sec2	11:8	R/W	0'h	Select the ASRC Clock Source for DSP OutBound4 ~ 7 0000'b: clk_sys_div_out 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: clk_i2s3_asrc 0100'b: clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_sys2 1000'b: clk_sys3 1001'b: clk_sys4 1010'b: clk_sys5 1011'b: clk_sys6 1100'b: clk_sys7 1101'b: clk_sys8 Others: Reserved
sel_dsp_out_fs_src_sec1	7:4	R/W	0'h	Select the ASRC Clock Source for DSP OutBound0 ~ 1 SRC Output 0000'b: Stereo DA Filter 0001'b: I2S1_ADC1 0010'b: I2S2_ADC1 0011'b: Reserved 0100'b: Reserved 0101'b: Reserved 0110'b: I2S1_ADC4 0111'b: I2S2_ADC4 1000'b: Reserved Others: Reserved
Reserved	3	R	0'h	Reserved

DSP Address: 0x1802_0112 I2C Address: 0x89				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_dsp_out_fs_src_sec2	2:0	R/W	0'h	Select the ASRC Clock Source for DSP OutBound2 ~ 3 SRC Output 000'b: Mono DA Filter 001'b: I2S1_ADC2 010'b: I2S2_ADC2 011'b: Reserved 100'b: Reserved 101'b: Reserved Others: Reserved

10.93. MX-8Ah: ASRC Control

Default: 0000'h

Table 111. MX-8Ah: ASRC Control

DSP Address: 0x1802_0114 I2C Address: 0x8A				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
sel_i2s1_asrc	14:12	R/W	0'h	Select the ASRC Source of I2S1 000'b: I2S1 001'b: I2S2 010'b: Reserved 011'b: Reserved 100'b: Reserved 101'b: Reserved Others: Reserved
Reserved	11	R	0'h	Reserved
sel_i2s2_asrc	10:8	R/W	0'h	Select the ASRC Source of I2S2 000'b: I2S1 001'b: I2S2 010'b: Reserved 011'b: Reserved 100'b: Reserved 101'b: Reserved Others: Reserved
Reserved	7	R	0'h	Reserved
sel_i2s3_asrc	6:4	R/W	0'h	Select the ASRC Source of I2S3 000'b: I2S1 001'b: I2S2 010'b: Reserved 011'b: Reserved 100'b: Reserved 101'b: Reserved Others: Reserved

DSP Address: 0x1802_0114 I2C Address: 0x8A				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	3	R	0'h	Reserved
sel_i2s4_asrc	2:0	R/W	0'h	Select the ASRC Source of I2S4 000'b: I2S1 001'b: I2S2 010'b: Reserved 011'b: Reserved 100'b: Reserved 101'b: Reserved Others: Reserved

10.94. MX-8Bh: ASRC Control

Default: 0000'h

Table 112. MX-8Bh: ASRC Control

DSP Address: 0x1802_0116 I2C Address: 0x8B				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
sel_i2s5_asrc	14:12	R/W	0'h	Select the ASRC Source of I2S5 000'b: I2S1 001'b: I2S2 010'b: Reserved 011'b: Reserved 100'b: Reserved 101'b: Reserved Others: Reserved
Reserved	11	R	0'h	Reserved
sel_i2s6_asrc	10:8	R/W	0'h	Select the ASRC Source of I2S6 000'b: I2S1 001'b: I2S2 010'b: Reserved 011'b: Reserved 100'b: Reserved 101'b: Reserved Others: Reserved
Reserved	7:0	R	0'h	Reserved

10.95. MX-8Ch: ASRC Control

Default: 0000'h

Table 113. MX-8Ch: ASRC Control

DSP Address: 0x1802_0118 I2C Address: 0x8C				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
i2s1_asrc_prediv	15:14	R/W	0'h	Set the I2S1 Clock Division for ASRC mode 00'b: div1 01'b: div2 10'b: div3 11'b: reserved
i2s2_asrc_prediv	13:12	R/W	0'h	Set the I2S2 Clock Division for ASRC mode 00'b: div1 01'b: div2 10'b: div3 11'b: reserved
i2s3_asrc_prediv	11:10	R/W	0'h	Set the I2S3 Clock Division for ASRC mode 00'b: div1 01'b: div2 10'b: div3 11'b: reserved
i2s4_asrc_prediv	9:8	R/W	0'h	Set the I2S4 Clock Division for ASRC mode 00'b: div1 01'b: div2 10'b: div3 11'b: reserved
i2s5_asrc_prediv	7:6	R/W	0'h	Set the I2S5 Clock Division for ASRC mode 00'b: div1 01'b: div2 10'b: div3 11'b: reserved
i2s6_asrc_prediv	5:4	R/W	0'h	Set the I2S6 Clock Division for ASRC mode 00'b: div1 01'b: div2 10'b: div3 11'b: reserved
Reserved	3:0	R	0'h	Reserved

10.96. MX-8Eh: PLL tracking mode 4

I2C Address: 0x8E				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserve	15:12	R/W	0'h	Reserve
Reserve	11:8	R/W	0'h	Reserve
Reserve	7:5	R	0'h	Reserve

I2C Address: 0x8E				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Se1_asrcin_clkout	4	R/W	0'h	0'b: ref off, clock off 1'b: refoff, clock keep
Se1_asrcin_ftk_loop_gain	3:2	R/W	2'h	Select the loop filter gain 00'b: 2^-8 01'b: 2^-14 10'b: 2^-18 11'b: 2^-20
Sel_ftk_phase_det	1:0	R/W	0'h	00: clock div1 01: clock div2 10: clock div4 11: clock div8

10.97. MX-9Ch: SAD Function Control

Default: 2184'h

Table 114. MX-9Ch: SAD Function Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R/W	0'h	Reserved
Sel_sad_min_dur	14:13	R/W	1'h	Minimum frame level within a pre-determined duration 00'b: 16 frames 01'b: 32 frames 10'b: 64 frames 11'b: 128 frames 80 samples/frame
Reserved	12:11	R/W	0'h	Reserved
En_sad_adpcm_bypass	10	R/W	0'h	Bypass ADPCM Encoder/Decoder 0'b: Pass ADPCM 1'b: Bypass ADPCM
En_sad_fg2enc	9	R/W	0'h	Automatic Push Data to SAD Buffer Once SAD Flag is Triggered (Only for en_sad_enc=0) 0'b: Disable 1'b: Enable
En_sad_buf_ow	8	R/W	1'h	SAD Buffer Over-Writing Control 0'b: Disable 1'b: Enable
En_sad_clr	7	R/W	1'h	Clear SAD Flag Write "1" then write "0" to clear flag
En_sad_dec	6	R/W	0'h	SAD Buffer Pop Mode Control 0'b: Disable 1'b: Enable
En_sad_enc	5	R/W	0'h	SAD Buffer Push Mode Control 0'b: Disable 1'b: Enable

Name	Bits	Read/Write	Reset State	Description
En_sad_det	4	R/W	0'h	SAD Detector Control 0'b: Disable 1'b: Enable
En_sad_sys	3	R/W	0'h	SAD Function Control 0'b: Disable 1'b: Enable
En_sad_reset	2	R/W	1'h	SAD Function Reset 0'b: Reset 1'b: Normal
Reserved	1:0	R	0'h	Reserved

10.98. MX-9Dh: SAD Function Threshold Control

Default: 010A'h

Table 115. MX-9Dh: SAD Function Threshold Control

Name	Bits	Read/Write	Reset State	Description
reserved	15:8	R/W	1'h	Reserved
Sel_sad_samll_lv	7:0	R/W	A'h	SAD Threshold1 Control 1 (Signed value) Higher threshold leads to more false alarm. Lower threshold leads to more miss.

10.99. MX-9Eh: SAD Function Threshold Control

Default: 0AEA'h

Table 116. MX-9Eh: SAD Function Threshold Control

Name	Bits	Read/Write	Reset State	Description
reserved	15:8	R/W	A'h	Reserved
Sel_sad_lv_var	7:0	R/W	EA'h	SAD Threshold2 Control (Signed value) Higher threshold leads to more miss. Lower threshold leads to more false alarm.

10.100. MX-9Fh: SAD Function Threshold Control

Default: 000C'h

Table 117. MX-9Fh: SAD Function Threshold Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:12	R	0'h	Reserved
Sad_mode_16k	11	R/W	0'h	SAD Sample Rate Converter 0'b: Up 6 (8K to 48K) 1'b: Up 3 (16K to 48K)
Sel_sad_out_wreq	10	R/W	0'h	SAD Output Sample Rate Control 0'b: Same as I2S 1'b: Use sample rate converter
Sel_sad_source	9:8	R/W	0'h	Select SAD Source 00'b: Stereo1_ADC_Mixer_L 01'b: Mono_ADC_Mixer_L 10'b: Mono_ADC_Mixer_R 11'b: Stereo2_ADC_Mixer_L
Sel_sad_lv_diff	7:0	R/W	C'h	SAD Threshold3 Control (Unsigned value) Higher threshold leads to more false alarm. Lower threshold leads to more miss.

10.101. MX-A0h: SAD Flag

Default: 0000'h

Table 118. MX-A0h: SAD Flag

Name	Bits	Read/Write	Reset State	Description
Reserved	15:12	R	0'h	Reserved
Fg_sad_hold	11	R	0'h	SAD Flag 0'b: Sound inative 1'b: Sound active
Sad_indicator	10:0	R	0'h	SAD Indicator (Unsigned value)

10.102. MX-A3h: DSP InBound Path Control

Default: 0000'h

Table 119. MX-A3h: DSP InBound Path Control

DSP Address: 0x1802_0146 I2C Address: 0xA3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved

DSP Address: 0x1802_0146 I2C Address: 0xA3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_ib01	14:12	R/W	0'h	Select InBound0/1 Source 000'b: IF1_DAC_0/1 001'b: IF2_DAC_0/1 010'b: Reserved 011'b: Stereo1_ADC_Mixer_L/R 100'b: VAD_ADC/DAC1_FS Others: Reserved
Reserved	11	R	0'h	Reserved
Sel_ib23	10:8	R/W	0'h	Select InBound2/3 Source 000'b: IF1_DAC_2/3 001'b: IF2_DAC_2/3 010'b: Reserved 011'b: Stereo2_ADC_Mixer_L/R 100'b: DACL1_FS/DACR1_FS 101'b: Reserved Others: Reserved
Reserved	7	R	0'h	Reserved
Sel_ib45	6:4	R/W	0'h	Select InBound4/5 Source 000'b: IF1_DAC_4/5 001'b: IF2_DAC_4/5 010'b: Reserved 011'b: Stereo3_ADC_Mixer_L/R 100'b: Reserved Others: Reserved
Reserved	3	R	0'h	Reserved
Sel_ib6	2:0	R/W	0'h	Select InBound6 Source 000'b: IF1_DAC_6 001'b: IF2_DAC_6 010'b: Reserved 011'b: Stereo4_ADC_Mixer_L 100'b: Reserved 101'b: Stereo1_ADC_Mixer_L 110'b: Stereo2_ADC_Mixer_L 111'b: Stereo3_ADC_Mixer_L

10.103. MX-A4h: DSP InBound Path Control

Default: 0000'h

Table 120. MX-A4h: DSP InBound Path Control

DSP Address: 0x1802_0148 I2C Address: 0xA4				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved

DSP Address: 0x1802_0148 I2C Address: 0xA4				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_ib7	14:12	R/W	0'h	Select InBound7 Source 000'b: IF1_DAC_7 001'b: IF2_DAC_7 010'b: Reserved 011'b: Stereo4_ADC_Mixer_R 100'b: Reserved 101'b: Stereo1_ADC_Mixer_R 110'b: Stereo2_ADC_Mixer_R 111'b: Stereo3_ADC_Mixer_R
Reserved	11	R	0'h	Reserved
Sel_ib8	10:8	R/W	0'h	Select InBound8 Source 000'b: Stereo1_ADC_Mixer_L 001'b: Stereo2_ADC_Mixer_L 010'b: Stereo3_ADC_Mixer_L 011'b: Stereo4_ADC_Mixer_L 100'b: Mono_ADC_Mixer_L 101'b: DACL1_FS Others: Reserved
Reserved	7	R	0'h	Reserved
Sel_ib9	6:4	R/W	0'h	Select InBound9 Source 000'b: Stereo1_ADC_Mixer_R 001'b: Stereo2_ADC_Mixer_R 010'b: Stereo3_ADC_Mixer_R 011'b: Stereo4_ADC_Mixer_R 100'b: Mono_ADC_Mixer_R 101'b: DACR1_FS 110'b: DAC1_FS Others: Reserved
Reserved	3:0	R	0'h	Reserved

10.104. MX-A5h: DSP SRC Path Control

Default: 0000'h

Table 121. MX-A5h: DSP SRC Path Control

DSP Address: 0x1802_014A I2C Address: 0xA5				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:5	R	0'h	Reserved
Sel_src_ob23	4	R/W	0'h	Select OutBound2/3 Source Pass SRC Control 0'b: Bypass 1'b: Pass SRC

DSP Address: 0x1802_014A I2C Address: 0xA5				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_src_ob01	3	R/W	0'h	Select OutBound0/1 Source Pass SRC Control 0'b: Bypass 1'b: Pass SRC
Sel_src_ib45	2	R/W	0'h	Select InBound4/5 Source Pass SRC Control 0'b: Bypass 1'b: Pass SRC
Sel_src_ib23	1	R/W	0'h	Select InBound2/3 Source Pass SRC Control 0'b: Bypass 1'b: Pass SRC
Sel_src_ib01	0	R/W	0'h	Select InBound0/1 Source Pass SRC Control 0'b: Bypass 1'b: Pass SRC

10.105. MX-A6h: DSP OutBound0/1 Digital Volume Control

Default: 2F2F'h

Table 122. MX-A6h: DSP OutBound0/1 Digital Volume Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R	0'h	Reserved
Vol_ob0	14:8	R/W	2F'h	DSP OutBound0 Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB
Reserved	7	R	0'h	Reserved
Vol_ob1	6:0	R/W	2F'h	DSP OutBound1 Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB

10.106. MX- A7h: DSP OutBound2/3 Digital Volume Control

Default: 2F2F'h

Table 123. MX-A7h: DSP OutBound2/3 Digital Volume Control

DSP Address: 0x1802_014E I2C Address: 0xA7				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
Vol_ob2	14:8	R/W	2F'h	DSP OutBound2 Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB

DSP Address: 0x1802_014E I2C Address: 0xA7				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	7	R	0'h	Reserved
Vol_ob3	6:0	R/W	2F'h	DSP OutBound3 Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB

10.107. MX-A8h: DSP OutBound4/5 Digital Volume Control

Default: 2F2F'h

Table 124. MX-A8h: DSP OutBound4/5 Digital Volume Control

DSP Address: 0x1802_0150 I2C Address: 0xA8				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
Vol_ob4	14:8	R/W	2F'h	DSP OutBound4 Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB
Reserved	7	R	0'h	Reserved
Vol_ob5	6:0	R/W	2F'h	DSP OutBound5 Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB

10.108. MX-A9h: DSP OutBound6/7 Digital Volume Control

Default: 2F2F'h

Table 125. MX-A9h: DSP OutBound6/7 Digital Volume Control

DSP Address: 0x1802_0152 I2C Address: 0xA9				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
Vol_ob6	14:8	R/W	2F'h	DSP OutBound6 Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB
Reserved	7	R	0'h	Reserved

DSP Address: 0x1802_0152 I2C Address: 0xA9				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Vol_ob7	6:0	R/W	2F'h	DSP OutBound7 Digital Volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB

10.109. MX-AEh: ADC EQ Control

Default: 6000'h

Table 126. MX-AEh: ADC EQ Control

DSP Address: 0x1802_015C I2C Address: 0xAE				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
ad_eq_param_update	14	R/W	1'h	ADC Path EQ parameter update control 0'b: Busy (Waiting for cross) 1'b: Stand-by Write "1" to update parameter
reserved	13:6	R/W	80'h	Reserved
Ad_eq_hpf1_status	5	R	0'h	ADC Path EQ High Pass Filter (HPF1) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Ad_eq_bpf4_status	4	R	0'h	ADC Path EQ Band-4 (BP4) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Ad_eq_bpf3_status	3	R	0'h	ADC Path EQ Band-3 (BP3) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Ad_eq_bpf2_status	2	R	0'h	ADC Path EQ Band-2 (BP2) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Ad_eq_bpf1_status	1	R	0'h	ADC Path EQ Band-1 (BP1) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.

DSP Address: 0x1802_015C I2C Address: 0xAE				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Ad_eq_lpf_status	0	R	0'h	ADC Path EQ Low Pass Filter (LPF) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.

10.110. MX-AFh: ADC EQ Control

Default: 0000'h

Table 127. MX-AFh: ADC EQ Control

DSP Address: 0x1802_015E I2C Address: 0xAF				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:9	R	0'h	Reserved
ad_eq_lpf_tpy	8	R/W	0'h	ADC Path 1st EQ Low Pass Filter Mode Control (LPF) 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)
ad_eq_hpf1_tpy	7	R/W	0'h	ADC Path 1st EQ High Pass Filter1 Mode Control (HPF1) 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)
Reserved	6	R	0'h	Reserved
ad_eq_hpf1_en	5	R/W	0'h	ADC Path EQ 1st High Pass Filter (HPF1) Control. 0'b: Disabled (bypass) and reset 1'b: Enabled
ad_eq_bpf4_en	4	R/W	0'h	ADC Path 2nd EQ Band-4 (BP4) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Ad_eq_bpf3_en	3	R/W	0'h	ADC Path 2nd EQ Band-3 (BP3) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Ad_eq_bpf2_en	2	R/W	0'h	ADC Path 2nd EQ Band-2 (BP2) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Ad_eq_bpf1_en	1	R/W	0'h	ADC Path 2nd EQ Band-1 (BP1) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Ad_eq_lpf_en	0	R/W	0'h	ADC Path 1st EQ Low Pass Filter (LPF) Filter Control. 0'b: Disabled and reset 1'b: Enabled.

10.111. MX-B0h: DAC EQ Control

Default: C000'h

Table 128. MX-B0h: DAC EQ Control

DSP Address: 0x1802_0160 **I2C Address: 0xB0**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_param_update	15	R/W	1'h	DAC Path EQ parameter update control 0'b: Busy (Waiting for cross) 1'b: Stand-by Write "1" to update parameter
Reserved	14:11	R/W	8'h	Reserved
Da_eq_lpf1_status	10	R	0'h	DAC Path EQ Low Pass Filter (LPF1) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Da_eq_lpf2_status	9	R	0'h	DAC Path EQ Low Pass Filter (LPF2) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Da_eq_hpf1_status	8	R	0'h	DAC Path EQ High Pass Filter (HPF1) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Da_eq_hpf2_status	7	R	0'h	DAC Path EQ High Pass Filter (HPF2) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Da_eq_hpf3_status	6	R	0'h	DAC Path EQ High Pass Filter (HPF3) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Da_eq_bpf1_status	5	R	0'h	DAC Path EQ Band-1 (BP1) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Da_eq_bpf2_status	4	R	0'h	DAC Path EQ Band-2 (BP2) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.

DSP Address: 0x1802_0160 I2C Address: 0xB0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf3_status	3	R	0'h	DAC Path EQ Band-3 (BP3) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Da_eq_bpf4_status	2	R	0'h	DAC Path EQ Band-4 (BP4) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Da_eq_bpf5_status	1	R	0'h	DAC Path EQ Band-5 (BP5) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Eq_biquad_status	0	R	0'h	DAC Path EQ Band-1 (Biquad Type) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.

10.112. MX-B1h: DAC EQ Control

Default: 0000'h

Table 129. MX-B1h: DAC EQ Control

DSP Address: 0x1802_0162 I2C Address: 0xB1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_lpf1_tpy_r	15	R/W	0'h	DAC Path Right Channel 1st EQ Low Pass Filter Mode Control (LPF1) 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)
Da_eq_lpf1_tpy_l	14	R/W	0'h	DAC Path Left Channel 1st EQ Low Pass Filter Mode Control (LPF1) 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)
Da_eq_lpf2_tpy_r	13	R/W	0'h	DAC Path Right Channel 1st EQ Low Pass Filter Mode Control (LPF2) 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)

DSP Address: 0x1802_0162 I2C Address: 0xB1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_lpf2_tpy_l	12	R/W	0'h	DAC Path Left Channel 1st EQ Low Pass Filter Mode Control (LPF2) 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)
Da_eq_hpf1_tpy_r	11	R/W	0'h	DAC Path Right Channel 1st EQ High Pass Filter1 Mode Control 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)
Da_eq_hpf1_tpy_l	10	R/W	0'h	DAC Path Left Channel 1st EQ High Pass Filter1 Mode Control 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)
Da_eq_hpf3_tpy_r	9	R/W	0'h	DAC Path Right Channel 1st EQ High Pass Filter3 Mode Control 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)
Da_eq_hpf3_tpy_l	8	R/W	0'h	DAC Path Left Channel 1st EQ High Pass Filter3 Mode Control 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)
Da_eq_lpf1_en	7	R/W	0'h	DAC Path 1st EQ Low Pass Filter (LPF1) Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Da_eq_lpf2_en	6	R/W	0'h	DAC Path 1st EQ Low Pass Filter (LPF2) Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Da_eq_hpf1_en	5	R/W	0'h	DAC Path EQ 1st High Pass Filter (HPF1) Control. 0'b: Disabled (bypass) and reset 1'b: Enabled
Da_eq_hpf2_en	4	R/W	0'h	DAC Path EQ 2nd High Pass Filter (HPF2) Control. 0'b: Disabled (bypass) and reset 1'b: Enabled
Da_eq_hpf3_en	3	R/W	0'h	DAC Path EQ 1st High Pass Butterworth Filter (HPF3) Control. 0'b: Disabled (bypass) and reset 1'b: Enabled
Reserved	2:0	R	0'h	Reserved

10.113. MX-B2h: DAC EQ Control

Default: 0000'h

Table 130. MX-B2h: DAC EQ Control

DSP Address: 0x1802_0164 I2C Address: 0xB2				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf5_en	15	R/W	0'h	DAC Path 2nd EQ Band-4 (BP5) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Da_eq_bpf4_en	14	R/W	0'h	DAC Path 2nd EQ Band-3 (BP4) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Da_eq_bpf3_en	13	R/W	0'h	DAC Path 2nd EQ Band-2 (BP3) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Da_eq_bpf2_en	12	R/W	0'h	DAC Path 2nd EQ Band-2 (BP2) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Da_eq_bpf1_en	11	R/W	0'h	DAC Path 2nd EQ Band-2 (BP1) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Eq_biquad_en	10	R/W	0'h	DAC Path 2nd EQ Band-1 (Biquad Type) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Reserved	9:0	R	0'h	Reserved

10.114. MX-B3h: Soft Volume Control

Default: 0009'h

Table 131. MX-B3h: Soft Volume Control

DSP Address: 0x1802_0166 I2C Address: 0xB3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_softvol	15	R/W	0'h	Enable Digital Volume Soft Volume Delay 0: Disable 1: Enable
Reserved	14:4	R	0'h	Reserved

DSP Address: 0x1802_0166 I2C Address: 0xB3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_svol	3:0	R/W	9'h	Soft Volume Change Delay Time (Default=1001b) 0000: 1 SVSYNC 0001: 2 SVSYNC 0010: 4 SVSYNC 0011: 8 SVSYNC 0100: 16 SVSYNC 0101: 32 SVSYNC 0110: 64 SVSYNC 0111: 128 SVSYNC 1000: 256 SVSYNC 1001: 512 SVSYNC 1010: 1024 SVSYNC Others: Reserved Note: SVSYNC=1/Fs

10.115. MX-BDh: IRQ Control

Default: 0000'h

Table 132. MX-BDh: IRQ Control

DSP Address: 0x1802_017A I2C Address: 0xBD				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:8	R	0'h	Reserved
Sta_micbias1_ovcd	7	R	0'h	MICBIAS1 Over Current Status Read: return status of each status pin Write: Write '0' to clear stick bit
en_irq_micbias1_ovcd	6	R/W	0'h	IRQ Output Source Configure of MICBIAS1 Over Current Status 0'b: Bypass 1'b: Enable
en_micbias1_ovcd_sticky	5	R/W	0'h	Sticky Control for MICBIAS1 Over Current 0'b: Disable 1'b: Enable
inv_micbias1_ovcd	4	R/W	0'h	MICBIAS1 Over Current status polarity 0'b: Normal 1'b: Output Invert
reserved	3:0	R	0'h	Reserved

10.116. MX-BEh: IRQ Control

Default: 0000'h

Table 133. MX-BEh: IRQ Control

DSP Address: 0x1802_017C I2C Address: 0xBE				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sta_vad_fg_hold	15	R	0'h	Status of VAD Flag Read: Return status of Jack Detect Select output Write: Write '0' to clear stick bit
en_irq_vad_fg_hold	14	R/W	0'h	IRQ Output Source Configure of VAD Flag Jack Detection Status 0'b: Bypass 1'b: Enable
en_vad_fg_hold_sticky	13	R/W	0'h	Sticky Control for VAD Flag Jack Detect 0'b: Disable 1'b: Enable
inv_vad_fg_hold	12	R/W	0'h	VAD Flag Status Polarity 0'b: Normal 1'b: Output Invert
Reserved	11:1	R	0'h	Reserved
Reg_tri_dsp_irq_in2	0	R/W	0'h	Register Trigger for DSP IRQ Input2 0'b: Output low to DSP IRQ input2 1'b: Output high to DSP IRQ input2

10.117. MX-BFh: GPIO Status

Default: 0000'h

Table 134. MX-BFh: GPIO Status

DSP Address: 0x1802_017E I2C Address: 0xBF				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:1	R	0'h	Reserved
sta_gpio1	0	R	0'h	GPIO1 Pin Status Read: return status of each GPIO pin

10.118. MX-C0h: GPIO Control

Default: 0000'h

Table 135. MX-C0h: GPIO Control

DSP Address: 0x1802_0180 I2C Address: 0xC0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_gpio1_type	15	R/W	0'h	GPIO1 Pin Function Select 0'b: GPIO1 1'b: IRQ1 output
Reserved	14:0	R	0'h	Reserved

10.119. MX-C1h: GPIO Control

Default: 0000'h

Table 136. MX-C1h: GPIO Control

DSP Address: 0x1802_0182 I2C Address: 0xC1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:3	R	0'h	Reserved
sel_gpio1	2	R/W	0'h	GPIO1 Pin Configuration 0'b: Input 1'b: Output
sel_gpio1_logic	1	R/W	0'h	GPIO1 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio1	0	R/W	0'h	GPIO1 Pin Polarity 0'b: Normal 1'b: Output Invert

10.120. MX-C5: Stereo1 ADC Adjustable HPF Control

Default: B320'h

Table 137. MX-C5h: Stereo1 ADC Adjustable HPF Control

DSP Address: 0x1802_018A I2C Address: 0xC5				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
adj_hpf_2nd_en_stereo1	15	R/W	1'h	Enable Adjustable 2nd High Pass Filter for Stereo1 ADC Filter 0'b : Bypass 1'b : Enable
adj_hpf_coef_l_sel_stereo1	14:12	R/W	3'h	Left Channel Coefficient Coarse Select for Stereo1 ADC Filter (If fs = 48kHz) 000'b : fc = 1017~6414Hz 001'b : fc = 492.6~5598.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 120.3~1136.2Hz 100'b : fc = 59.9~548.4Hz 101'b : fc = 29.8~269.4Hz 110'b : fc = 14.9~133.5Hz 111'b : fc = 7.4~66.4Hz
Reserved	11	R	0'h	Reserved
adj_hpf_coef_r_sel_stereo1	10:8	R/W	3'h	Right Channel Coefficient Coarse Select for Stereo1 ADC Filter (If fs = 48kHz) 000'b : fc = 1017~6414Hz 001'b : fc = 492.6~5598.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 120.3~1136.2Hz 100'b : fc = 59.9~548.4Hz 101'b : fc = 29.8~269.4Hz 110'b : fc = 14.9~133.5Hz 111'b : fc = 7.4~66.4Hz
reserved	7:0	R	20'h	Reserved

10.121. MX-C6: Stereo1 ADC Adjustable HPF Control

Default: 0000'h

Table 138. MX-C6h: Stereo1 ADC Adjustable HPF Control

DSP Address: 0x1802_018C I2C Address: 0xC6				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:14	R	0'h	Reserved
adj_hpf_coef_l_num_stereo1	13:8	R/W	0'h	Left Channel Coefficient Fine Select for Stereo1 ADC Filter (0~63)
reserved	7:6	R	0'h	Reserved
adj_hpf_coef_r_num_stereo1	5:0	R/W	0'h	Right Channel Coefficient Fine Select for Stereo1 ADC Filter (0~63)

10.122. MX-C7h: Mono ADC Adjustable HPF Control

Default: B300'h

Table 139. MX-C7h: Mono ADC Adjustable HPF Control

DSP Address: 0x1802_018E I2C Address: 0xC7				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
adj_hpf_2nd_en_mono	15	R/W	1'h	Enable Adjustable 2nd High Pass Filter for Mono ADC Filter 0'b : Bypass 1'b : Enable
adj_hpf_coef_l_sel_mono	14:12	R/W	3'h	Left Channel Coefficient Coarse Select for Mono ADC Filter (If fs = 48kHz) 000'b : fc = 1017~6414Hz 001'b : fc = 492.6~5598.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 120.3~1136.2Hz 100'b : fc = 59.9~548.4Hz 101'b : fc = 29.8~269.4Hz 110'b : fc = 14.9~133.5Hz 111'b : fc = 7.4~66.4Hz
Reserved	11	R	0'h	Reserved
adj_hpf_coef_r_sel_mono	10:8	R/W	3'h	Right Channel Coefficient Coarse Select for Mono ADC Filter (If fs = 48kHz) 000'b : fc = 1017~6414Hz 001'b : fc = 492.6~5598.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 120.3~1136.2Hz 100'b : fc = 59.9~548.4Hz 101'b : fc = 29.8~269.4Hz 110'b : fc = 14.9~133.5Hz 111'b : fc = 7.4~66.4Hz
reserved	7:0	R	20'h	Reserved

10.123. MX-C8h: Mono ADC Adjustable HPF Control

Default: 0000'h

Table 140. MX-C8h: Mono ADC Adjustable HPF Control

DSP Address: 0x1802_0190 I2C Address: 0xC8				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:14	R	0'h	Reserved
adj_hpf_coef_l_num_mono	13:8	R/W	0'h	Left Channel Coefficient Fine Select for Mono ADC Filter (0~63)

DSP Address: 0x1802_0190 I2C Address: 0xC8				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	7:6	R	0'h	Reserved
adj_hpf_coef_r_num_mono	5:0	R/W	0'h	Right Channel Coefficient Fine Select for Mono ADC Filter (0~63)

10.124. MX- C9h: Stereo2 ADC Adjustable HPF Control

Default: B300'h

Table 141. MX-C9h: Stereo2 ADC Adjustable HPF Control

DSP Address: 0x1802_0192 I2C Address: 0xC9				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
adj_hpf_2nd_en_stereo2	15	R/W	1'h	Enable Adjustable 2nd High Pass Filter for Stereo2 ADC Filter 0'b : Bypass 1'b : Enable
adj_hpf_coef_l_sel_stereo2	14:12	R/W	3'h	Left Channel Coefficient Coarse Select for Stereo2 ADC Filter (If fs = 48kHz) 000'b : fc = 1017~6414Hz 001'b : fc = 492.6~5598.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 120.3~1136.2Hz 100'b : fc = 59.9~548.4Hz 101'b : fc = 29.8~269.4Hz 110'b : fc = 14.9~133.5Hz 111'b : fc = 7.4~66.4Hz
Reserved	11	R	0'h	Reserved
adj_hpf_coef_r_sel_stereo2	10:8	R/W	3'h	Right Channel Coefficient Coarse Select for Stereo2 ADC Filter (If fs = 48kHz) 000'b : fc = 1017~6414Hz 001'b : fc = 492.6~5598.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 120.3~1136.2Hz 100'b : fc = 59.9~548.4Hz 101'b : fc = 29.8~269.4Hz 110'b : fc = 14.9~133.5Hz 111'b : fc = 7.4~66.4Hz
reserved	7:0	R	0'h	Reserved

10.125. MX- CAh: Stereo2 ADC Adjustable HPF Control

Default: 0000'h

Table 142. MX-CAh: Stereo2 ADC Adjustable HPF Control

DSP Address: 0x1802_0194 I2C Address: 0xCA				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:14	R	0'h	Reserved
adj_hpf_coef_l_num_stereo2	13:8	R/W	0'h	Left Channel Coefficient Fine Select for Stereo2 ADC Filter (0~63)
reserved	7:6	R	0'h	Reserved
adj_hpf_coef_r_num_stereo2	5:0	R/W	0'h	Right Channel Coefficient Fine Select for Stereo2 ADC Filter (0~63)

10.126. MX-CBh: Stereo3 ADC Adjustable HPF Control

Default: B300'h

Table 143. MX-CBh: Stereo3 ADC Adjustable HPF Control

DSP Address: 0x1802_0196 I2C Address: 0xCB				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
adj_hpf_2nd_en_stereo3	15	R/W	1'h	Enable Adjustable 2nd High Pass Filter for Stereo3 ADC Filter 0'b : Bypass 1'b : Enable
adj_hpf_coef_l_sel_stereo3	14:12	R/W	3'h	Left Channel Coefficient Coarse Select for Stereo3 ADC Filter (If fs = 48kHz) 000'b : fc = 1017~6414Hz 001'b : fc = 492.6~5598.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 120.3~1136.2Hz 100'b : fc = 59.9~548.4Hz 101'b : fc = 29.8~269.4Hz 110'b : fc = 14.9~133.5Hz 111'b : fc = 7.4~66.4Hz
Reserved	11	R	0'h	Reserved

DSP Address: 0x1802_0196 I2C Address: 0xCB				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
adj_hpf_coef_r_sel_stereo3	10:8	R/W	3'h	Right Channel Coefficient Coarse Select for Stereo3 ADC Filter (If fs = 48kHz) 000'b : fc = 1017~6414Hz 001'b : fc = 492.6~5598.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 120.3~1136.2Hz 100'b : fc = 59.9~548.4Hz 101'b : fc = 29.8~269.4Hz 110'b : fc = 14.9~133.5Hz 111'b : fc = 7.4~66.4Hz
reserved	7:0	R	0'h	Reserved

10.127. MX-CCh: Stereo3 ADC Adjustable HPF Control

Default: 0000'h

Table 144. MX-CCh: Stereo3 ADC Adjustable HPF Control

DSP Address: 0x1802_0198 I2C Address: 0xCC				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:14	R	0'h	Reserved
adj_hpf_coef_l_num_stereo3	13:8	R/W	0'h	Left Channel Coefficient Fine Select for Stereo3 ADC Filter (0~63)
reserved	7:6	R	0'h	Reserved
adj_hpf_coef_r_num_stereo3	5:0	R/W	0'h	Right Channel Coefficient Fine Select for Stereo3 ADC Filter (0~63)

10.128. MX- CDh: Stereo4 ADC Adjustable HPF Control

Default: B300'h

Table 145. MX-CDh: Stereo4 ADC Adjustable HPF Control

DSP Address: 0x1802_019A I2C Address: 0xCD				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
adj_hpf_2nd_en_stereo4	15	R/W	1'h	Enable Adjustable 2nd High Pass Filter for Stereo4 ADC Filter 0'b : Bypass 1'b : Enable

DSP Address: 0x1802_019A I2C Address: 0xCD				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
adj_hpf_coef_l_sel_stereo4	14:12	R/W	3'h	Left Channel Coefficient Coarse Select for Stereo4 ADC Filter (If fs = 48kHz) 000'b : fc = 1017~6414Hz 001'b : fc = 492.6~5598.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 120.3~1136.2Hz 100'b : fc = 59.9~548.4Hz 101'b : fc = 29.8~269.4Hz 110'b : fc = 14.9~133.5Hz 111'b : fc = 7.4~66.4Hz
Reserved	11	R	0'h	Reserved
adj_hpf_coef_r_sel_stereo4	10:8	R/W	3'h	Right Channel Coefficient Coarse Select for Stereo4 ADC Filter (If fs = 48kHz) 000'b : fc = 1017~6414Hz 001'b : fc = 492.6~5598.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 120.3~1136.2Hz 100'b : fc = 59.9~548.4Hz 101'b : fc = 29.8~269.4Hz 110'b : fc = 14.9~133.5Hz 111'b : fc = 7.4~66.4Hz
reserved	7:0	R	0'h	Reserved

10.129. MX- CEh: Stereo4 ADC Adjustable HPF Control

Default: 0000'h

Table 146. MX-CEh: Stereo4 ADC Adjustable HPF Control

DSP Address: 0x1802_019C I2C Address: 0xCE				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:14	R	0'h	Reserved
adj_hpf_coef_l_num_stereo4	13:8	R/W	0'h	Left Channel Coefficient Fine Select for Stereo4 ADC Filter (0~63)
reserved	7:6	R	0'h	Reserved
adj_hpf_coef_r_num_stereo4	5:0	R/W	0'h	Right Channel Coefficient Fine Select for Stereo4 ADC Filter (0~63)

10.130. MX-D2h: Multi-Band DRC1 Control

Default: 001F'h

Table 147. MX-D2h: Multi-band DRC1 Control

DSP Address: 0x1802_01A4 I2C Address: 0xD2				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15	R	0'h	Reserved
Alc_noise_gate_ht	14:12	R/W	0'h	ALC Noise Gate Hold Time Control 000'b: 0 sample 001'b: 128 samples 010'b: 256 samples … 111'b: 896 samples
alc_ft_boost	11:6	R/W	0'h	ALC Digital Pre-BOOST (0.75dB/step) 00'h= 0dB 01'h= 0.75dB 02'h= 1.5dB 03'h= 2.25dB …….. 27'h= 29.25dBFS Others: Reserved
alc_bk_gain_r	5:0	R/W	1f'h	ALC Right Channel Digital Post-BOOST (0.375dB/step) 00'h= -11.625dB …….. 3F'h= 12dB

10.131. MX- D3h: Multi-Band DRC1 Control

Default: 020C'h

Table 148. MX-D3h: Multi-Band DRC1 Control

DSP Address: 0x1802_01A6 I2C Address: 0xD3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_alc	15:14	R/W	0'h	ALC Enable (default:00b) 00'b: Disable 01'b: Enable ALC to DAC Path 10'b: Disable ALC 11'b: Enable ALC to ADC Path
Reserved	13	R	0'h	Reserved
alc_atk_rate	12:8	R/W	2'h	Select ALC attack rate (0.375dB/TU) 00'h: 83 uSec 01'h: 0.167 mSec …….. 1f'h: 5.46 Sec

DSP Address: 0x1802_01A6 I2C Address: 0xD3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_alc_rate	7:5	R/W	0'h	ALC Rate Control for Sample Rate Change 001'b: 48kHz 010'b: 96kHz 011'b: 192kHz 101'b: 44.1kHz 110'b: 88.2kHz 111'b: 176.4kHz
alc_rc_slow_rate	4:0	R/W	C'h	Select ALCC recovery rate (0.375dB/TU) 00'h: 83 uSec 01'h: 0.167 mSec …….. 1F'h: 5.46 Sec

10.132. MX- D4h: Multi-Band DRC1 Control

Default: 1F00'h

Table 149. MX-D4h: Multi-Band DRC1 Control

DSP Address: 0x1802_01A8 I2C Address: 0xD4				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Alc_drc_ratio_sel2	15:14	R/W	0'h	DRC Compression-2 Ratio Selection 00'b: 1:1 01'b: 1:2 10'b: 1:4 11'b: 1:8
alc_bk_gain_l	13:8	R/W	1F'h	DRC Left Channel Digital Post-BOOST (0.375dB/step) 00'h= -11.625dB …….. 3F'h= 12dB
Alc_drc_en	7	R/W	0'h	DRC Function Control 0'b: Disable 1'b: Enable
Alc_drc_ratio_sel	6:5	R/W	0'h	DRC Compression-1 Ratio Selection 00'b: 1:1 01'b: 1:2 10'b: 1:4 11'b: 1:8
Alc_noise_gate_drop_en	4	R/W	0'h	ALC Noise Gate Drop Mode Control 0'b: Disable 1'b: Enable
Reserved	3:2	R	0'h	Reserved

DSP Address: 0x1802_01A8 I2C Address: 0xD4				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
noise_gate_ratio_sel	1:0	R/W	0'h	ALC DRC Expansion Ratio Control when Noise Gate is Enabled 00'b: 1:1 01'b: 2:1 10'b: 4:1 11'b: 8:1

10.133. MX- D5h: Multi-Band DRC1 Control

Default: 0000'h

Table 150. MX-D5h: Multi-Band DRC1 Control

DSP Address: 0x1802_01AA I2C Address: 0xD5				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Alc_noise_gate_exp	15:12	R/W	0'h	Select Boost Compensation Gain when Signal is at Noise Gate Level. 0'h: 0dB 1'h: 3dB 2'h: 6dB …….. E'h: 42dB F'h: 45dB
Reserved	11	R	0'h	Reserved
Alc_thmin	10:5	R/W	0'h	DRC Threshold Level Control 00'h: -60dB 01'h: -60.75dB 02'h: -61.5dB … 2E'h: -94.5dB, 0.75dB/Step
alc_thnoise	4:0	R/W	0'h	Noise Gate Threshold (-1.5dB/step) 00'h: -24dBFS 01'h: -25.5dBFS …….. 1F'h: -70.5 dBFS

10.134. MX- D6h: Multi-Band DRC1 Control

Default: 0000'h

Table 151. MX-D6h: Multi-Band DRC1 Control

DSP Address: 0x1802_01AC I2C Address: 0xD6				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
Alc_thmin_fast_rc_en	14	R/W	0'h	ALC thmin Mode Fast Recover Control 0'b: Disable fast recover 1'b: Enable fast recover
alc_noise_gate_en	13	R/W	0'h	Enable Noise Gate function 0'b: Diaable 1'b: Enable
alc_noise_gain_hd	12	R/W	0'h	ALC Hold Gain when Noise Gate Mode 0'b: Disable, don't hold gain when noise gate mode (depend on noise gate threshold to do noise gate's AGC) 1'b: Enable, hold gain when noise gate mode
alc_thmax2	11:6	R/W	0'h	ALC Limiter Threshold 2 Control (0.75dB/step) 00'h= 0dBFS 01'h= -0.75dBFS 02'h= -1.5dBFS 03'h= -2.25dBFS …….. 1F'h= -45dBFS
alc_thmax	5:0	R/W	0'h	ALC Limiter Threshold Control (0.375dB/step) 00'h= 0dBFS 01'h= -0.375dBFS 02'h= -0.75dBFS 03'h= -1.125dBFS …….. 1F'h= -23.625dBFS

10.135. MX- D7h: Multi-Band DRC1 Control

Default: 0029'h

Table 152. MX-D7h: Multi-Band DRC1 Control

DSP Address: 0x1802_01AE I2C Address: 0xD7				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:3	R/W	5'h	Reserved

DSP Address: 0x1802_01AE I2C Address: 0xD7				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Alc_zero_data_lsb_sel	2:0	R/W	1'h	Threshold for ALC Zero Data Mode with Amplitude detection 000'b: -84dB 001'b: -90dB 010'b: -96dB 011'b: -108dB 100'b: -114dB 101'b: -120dB 110'b: -132dB 111'b: -138dB

10.136. MX- D8h: Multi-Band DRC2 Control

Default: 001F'h

Table 153. MX-D8h: Multi-Band DRC2 Control

DSP Address: 0x1802_01B0 I2C Address: 0xD8				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
Alc_bass_noise_gate_ht	14:12	R/W	0'h	ALC Noise Gate Hold Time Control 000'b: 0 sample 001'b: 128 samples 010'b: 256 samples … 111'b: 896 samples
Alc_bass_ft_boost	11:6	R/W	0'h	ALC Digital Pre-BOOST (0.75dB/step) 00'h= 0dB 01'h= 0.75dB 02'h= 1.5dB 03'h= 2.25dB …….. 27'h= 29.25dBFS Others: Reserved
Alc_bass_bk_gain_r	5:0	R/W	1F'h	ALC Right Channel Digital Post-BOOST (0.375dB/step) 00'h= -11.625dB …….. 3F'h= 12dB

10.137. MX- D9h: Multi-Band DRC2 Control

Default: 020C'h

Table 154. MX-D9h: Multi-Band DRC2 Control

DSP Address: 0x1802_01B2 I2C Address: 0xD9				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_alc_bass	15	R/W	0'h	ALC Enable (default:0b) 0'b: Disable ALC_Bass 1'b: Enable ALC_Bass
Reserved	14:13	R	0'h	Reserved
Alc_bass_atk_rate	12:8	R/W	2'h	Select ALC attack rate (0.375dB/TU) 00'h: 83 uSec 01'h: 0.167 mSec …….. 1f'h: 5.46 Sec
alc_bass_rate_sel	7:5	R/W	0'h	ALC Rate Control for Sample Rate Change 001'b: 48kHz 010'b: 96kHz 011'b: 192kHz 101'b: 44.1kHz 110'b: 88.2kHz 111'b: 176.4kHz
Alc_bass_rc_slow_rate	4:0	R/W	C'h	Select ALC recovery rate (0.375dB/TU) 00'h: 83 uSec 01'h: 0.167 mSec …….. 1F'h: 5.46 Sec

10.138. MX- DAh: Multi-Band DRC2 Control

Default: 1F00'h

Table 155. MX-DAh: Multi-Band DRC2 Control

DSP Address: 0x1802_01B4 I2C Address: 0xDA				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Alc_bass_drc_ratio_sel2	15:14	R/W	0'h	DRC Compression-2 Ratio Selection 00'b: 1:1 01'b: 1:2 10'b: 1:4 11'b: 1:8
Alc_bass_bk_gain_l	13:8	R/W	1f'h	ALC Left Channel Digital Post-BOOST (0.375dB/step) 00'h= -11.625dB …….. 3F'h= 12dB

DSP Address: 0x1802_01B4 I2C Address: 0xDA				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Alc_bass_drc_en	7	R/W	0'h	DRC Function Control 0'b: Disable 1'b: Enable
Alc_bass_drc_ratio_sel	6:5	R/W	0'h	DRC Compression-1 Ratio Selection 00'b: 1:1 01'b: 1:2 10'b: 1:4 11'b: 1:8
Alc_bass_noise_gate_drop_en	4	R/W	0'h	ALC Noise Gate Drop Mode Control 0'b: Disable 1'b: Enable
Reserved	3:2	R	0'h	Reserved
Alc_bass_noise_gate_ratio_sel	1:0	R/W	0'h	ALC DRC Expansion Ratio Control when Noise Gate is Enabled 00'b: 1:1 01'b: 2:1 10'b: 4:1 11'b: 8:1

10.139. MX- DBh: Multi-Band DRC2 Control

Default: 0000'h

Table 156. MX-DBh: Multi-Band DRC2 Control

DSP Address: 0x1802_01B6 I2C Address: 0xDB				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Alc_bass_noise_gate_exp	15:12	R/W	0'h	Select Boost Compensation gain when signal is at Noise Gate Level. 0'h: 0dB 1'h: 3dB 2'h: 6dB …….. E'h: 42dB F'h: 45dB
Reserved	11	R	0'h	Reserved
Alc_bass_thmin	10:5	R/W	0'h	DRC Threshold Level Control 00'h: -60dB 01'h: -60.75dB 02'h: -61.5dB … 2E'h: -94.5dB, 0.75dB/Step

DSP Address: 0x1802_01B6 I2C Address: 0xDB				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Alc_bass_thnoise	4:0	R/W	0'h	Noise Gate Threshold (-1.5dB/step) 00'h: -24dBFS 01'h: -25.5dBFS …….. 1F'h: -70.5 dBFS

10.140. MX- DCh: Multi-Band DRC2 Control

Default: 0000'h

Table 157. MX-DCh: Multi-Band DRC2 Control

DSP Address: 0x1802_01B8 I2C Address: 0xDC				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
Alc_bass_thmin_fast_rc_en	14	R/W	0'h	ALC thmin Mode Fast Recover Control 0'b: Disable fast recover 1'b: Enable fast recover
Alc_bass_noise_gate_en	13	R/W	0'h	Enable Noise Gate function 0'b: Diaable 1'b: Enable
Alc_bass_noise_gain_hd	12	R/W	0'h	ALC Hold Gain when Noise Gate Mode 0'b: Disable, don't hold gain when noise gate mode (depend on noise gate threshold to do noise gate's AGC) 1'b: Enable, hold gain when noise gate mode
Alc_bass_thmax2	11:6	R/W	0'h	ALC Limiter Threshold 2 Control (0.75dB/step) 00'h= 0dBFS 01'h= -0.75dBFS 02'h= -1.5dBFS 03'h= -2.25dBFS …….. 1F'h= -45dBFS
Alc_bass_thmax	5:0	R/W	0'h	ALC Limiter Threshold Control (0.375dB/step) 00'h= 0dBFS 01'h= -0.375dBFS 02'h= -0.75dBFS 03'h= -1.125dBFS …….. 1F'h= -23.625dBFS

10.141. MX- DDh: Multi-Band DRC2 Control

Default: 0029'h

Table 158. MX-DDh: Multi-Band DRC2 Control

DSP Address: 0x1802_01BA I2C Address: 0xDD				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:3	R	5'h	Reserved
Alc_bass_zero_data_lsb_sel	2:0	R/W	1'h	Threshold for ALC Zero Data Mode with Amplitude detection 000'b: -84dB 001'b: -90dB 010'b: -96dB 011'b: -108dB 100'b: -114dB 101'b: -120dB 110'b: -132dB 111'b: -138dB

10.142. MX- DFh: Multi-Band DRC1 Control

Default: 0200'h

Table 159. MX-DFh: Multi-Band DRC1 Control

DSP Address: 0x1802_01BE I2C Address: 0xDF				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:11	R	0'h	Reserved
Alc_limiter_ratio	10:8	R/W	2'h	ALC Limiter Ratio Control 000'b: 1/4 001'b: 1/8 010'b: 1/16 011'b: 1/32 100'b: 1/64 101'b: 1/128 110'b: 1/256 111'b: Hard Limiter
Reserved	7:0	R/W	0'h	Reserved

10.143. MX- E1h: Multi-Band DRC2 Control

Default: 0200'h

Table 160. MX-E1h: Multi-Band DRC2 Control

DSP Address: 0x1802_01C2 I2C Address: 0xE1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:11	R	0'h	Reserved
Alc_bass_limiter_ratio	10:8	R/W	2'h	ALC Limiter Ratio Control 000'b: 1/4 001'b: 1/8 010'b: 1/16 011'b: 1/32 100'b: 1/64 101'b: 1/128 110'b: 1/256 111'b: Hard Limiter
Reserved	7:0	R/W	0'h	Reserved

10.144. MX-E3h: DSP InBound1 SRC Control

Default: 5800'h

Table 161. MX-E3h: DSP InBound1 SRC Control

DSP Address: 0x1802_01C2 I2C Address: 0xE1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Ib1_Srcin_en	15	R/W	0'h	DSP InBound1 SRC Enable Control 0'b: Disable 1'b: Enable
Reserved	14	R/W	B'h	Reserved
Ib1_srcin_syn_mode	10	R/W	0'h	DSP InBound1 SRC Mode 0'b: Asynchronous 1'b: Synchronous
Reserved	9:0	R/W	0'h	Reserved

10.145. MX- E7h: DSP InBound2 SRC Control

Default: 5800'h

Table 162. MX-E7h: DSP InBound2 SRC Control

DSP Address: 0x1802_01CE I2C Address: 0xE7				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Ib2_Srcin_en	15	R/W	0'h	DSP InBound2 SRC Enable Control 0'b: Disable 1'b: Enable
Reserved	14	R/W	B'h	Reserved
Ib2_srcin_syn_mode	10	R/W	0'h	DSP InBound2 SRC Mode 0'b: Asynchronous 1'b: Synchronous
Reserved	9:0	R/W	0'h	Reserved

10.146. MX- EBh: DSP InBound3 SRC Control

Default: 5800'h

Table 163. MX-EBh: DSP InBound3 SRC Control

DSP Address: 0x1802_01D6 I2C Address: 0xEB				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Ib3_Srcin_en	15	R/W	0'h	DSP InBound3 SRC Enable Control 0'b: Disable 1'b: Enable
Reserved	14	R/W	B'h	Reserved
Ib3_srcin_syn_mode	10	R/W	0'h	DSP InBound3 SRC Mode 0'b: Asynchronous 1'b: Synchronous
Reserved	9:0	R/W	0'h	Reserved

10.147. MX- EFh: DSP OutBound1 SRC Control

Default: 5800'h

Table 164. MX-EFh: DSP OutBound1 SRC Control

DSP Address: 0x1802_01DE I2C Address: 0xEF				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Ob1_Srcout_en	15	R/W	0'h	DSP OutBound1 SRC Enable Control 0'b: Disable 1'b: Enable
Reserved	14	R/W	B'h	Reserved

DSP Address: 0x1802_01DE I2C Address: 0xEF				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ob1_srcout_syn_mode	10	R/W	0'h	DSP OutBound1 SRC Mode 0'b: Asynchronous 1'b: Synchronous
Reserved	9:0	R/W	0'h	Reserved

10.148. MX- F3h: DSP OutBound2 SRC Control

Default: 5800'h

Table 165. MX-F3h: DSP OutBound2 SRC Control

DSP Address: 0x1802_01E6 I2C Address: 0xF3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Ob2_Srcout_en	15	R/W	0'h	DSP OutBound2 SRC Enable Control 0'b: Disable 1'b: Enable
Reserved	14	R/W	B'h	Reserved
Ob2_srcout_syn_mode	10	R/W	0'h	DSP OutBound2 SRC Mode 0'b: Asynchronous 1'b: Synchronous
Reserved	9:0	R/W	0'h	Reserved

10.149. MX-FAh: General Control

Default: 0000'h

Table 166. MX-FAh: General Control

DSP Address: 0x1802_01F4 I2C Address: 0xFA				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
En_rx_tdm1_pcmb	15	R/W	0'h	Enable TDM1 Mode-2 PCM Mode B Control 0'b: Disable 1'b: Enable
Reserved	14:13	R/W	0'h	Reserved
En_spi_sdo_type	12	R/W	0'h	SPI SDO Pin Type Control 0'b: Output 1'b: Input
I2s1_adcdat	11	R/W	0'h	I2S1 ADCDAT Pin Type Control 0'b: Output 1'b: Input

DSP Address: 0x1802_01F4 I2C Address: 0xFA				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
I2s2_adcdat	10	R/W	0'h	I2S2 ADCDAT Pin Type Control 0'b: Output 1'b: Input
reserved	9:8	R/W	0'h	Reserved
En_rx_tdm2_pcmb	7	R/W	0'h	Enable TDM2 Mode-2 PCM Mode B Control 0'b: Disable 1'b: Enable
Reserved	6:5	R/W	0'h	Reserved
sel_irq_debounce	4:3	R/W	0'h	Select the De-bounce Clock of IRQ 00'b: from MCLK 01'b: from RC clock 10'b: Reserved 11'b: Reserved
Reserved	2	R/W	0'h	Reserved
En_detect_clk_sys	1	R/W	0'h	Enable MCLK Detection 0'b: Disable 1'b: Enable
digital_gate_ctrl	0	R/W	0'h	Enable Gating Mode with MCLK 0'b: Disable 1'b: Enable

10.150. MX-FBh: General Control

Default: 0000'h

Table 167. MX-FBh: General Control

DSP Address: 0x1802_01F6 I2C Address: 0xFB				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sta_dsp_watchdog_fg	15	R	0'h	Status of DSP Watch Dog Flag 0'b: Normal 1'b: Error flag
en_irq_dsp_watchdog_fg	14	R/W	0'h	IRQ Output Source Configure of DSP Watch Dog Flag 0'b: bypass 1'b: Normal
en_dsp_watchdog_fg_sticky	13	R/W	0'h	Sticky Control for DSP Watch Dog 0'b: Disable 1'b: Enable
inv_dsp_watchdog_fg	12	R/W	0'h	DSP Watch Dog Flag Status Polarity 0'b: Normal 1'b: Output Invert

DSP Address: 0x1802_01F6 I2C Address: 0xFB				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Th_dsp_watchdog	11:10	R/W	0'h	DSP Watch Dog Time Threshold 00'b: 1 sec 01'b: 2 sec 10'b: 3 sec 11'b: 4 sec
En_dsp_watchdog	9	R/W	0'h	Enable DSP Watch Dog 0'b: Disable 1'b: Enable
Reserved	8:0	R/W	0'h	Reserved

10.151. MX-FCh: General Control

Default: 0000'h

Table 168. MX-FCh: General Control

DSP Address: 0x1802_01F8 I2C Address: 0xFC				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_i2s1_mono	15	R/W	0'b	Enable I2S1 Mono mode 1'b: Enable 0'b: Disable
en_i2s2_mono	14	R/W	0'b	Enable I2S2 Mono mode 1'b: Enable 0'b: Disable
reserved	13:12	R/W	0'b	Reserved
En_irq_vad_IRQ_out	11	R/W	0'b	Enable VAD Trigger IRQ 1'b: Enable 0'b: Disable
Reserved	10:9	R/W	0'h	Reserved
En_auto_dsp_bclk	8	R/W	0'h	Enable DSP BCLK Auto Mode 0'b: Disable (Manual mode) Bus clock determined by sel_dsp_bus_pre_div. 1'b: Enable (Auto mode) When DSP accesses ext. RAM, bus clock determined by sel_dsp_bus_pre_div_auto. When DSP doesn't access ext. RAM, bus clock determined by sel_dsp_bus_pre_div.

DSP Address: 0x1802_01F8 I2C Address: 0xFC				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_dsp_bus_pre_div_auto	7:4	R/W	0'h	Select DSP BCLK Rate at Auto Mode 0000b: ÷ 2 0001b: ÷ 4 0010b: ÷ 8 0011b: ÷ 16 0100b: ÷ 32 0101b: ÷ 64 0110b: ÷ 128 0111b: ÷ 256 1000b: ÷ 512 1001b: Reserved 1010b: ÷ 1024 1011b: Reserved 1100b: Reserved 1101b: Reserved 1110b: Reserved 1111b: Reserved
Sel_dsp_bus_pre_div	3:0	R/W	0'h	Select DSP BCLK Rate 0000b: ÷ 2 0001b: ÷ 4 0010b: ÷ 8 0011b: ÷ 16 0100b: ÷ 32 0101b: ÷ 64 0110b: ÷ 128 0111b: ÷ 256 1000b: ÷ 512 1001b: Reserved 1010b: ÷ 1024 1011b: Reserved 1100b: Reserved 1101b: Reserved 1110b: Reserved 1111b: Reserved

10.152. MX-FEh: Device ID

Default: 10EC'h

Table 169. MX-FEh: Device ID

DSP Address: 0x1802_01FC I2C Address: 0xFE				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
vender_id	15:0	R	10EC'h	Vender ID "10EC"

10.153. PR-29h: Digital Pin Initial Status Control

Default: 0000'h

Table 170. PR-29h: Digital Pin Initial Status Control

Address: PR29				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Pu_i2s1	15	R/W	0'h	I2S1 (LRCK1/BCLK1/DACDAT1) Input Status Control 0'b: Floating 1'b: Pull-up
Pd_i2s1	14	R/W	0'h	I2S1 (LRCK1/BCLK1/DACDAT1) Input Status Control 0'b: Floating 1'b: Pull-down
Pu_i2s2	13	R/W	0'h	I2S2 (LRCK2/BCLK2/DACDAT2) Input Status Control 0'b: Floating 1'b: Pull-up
Pd_i2s2	12	R/W	0'h	I2S2 (LRCK2/BCLK2/DACDAT2) Input Status Control 0'b: Floating 1'b: Pull-down
reserved	11:8	R/W	0'h	Reserved
Pu_mclk1	7	R/W	0'h	MCLK1 Input Status Control 0'b: Floating 1'b: Pull-up
Pd_mclk1	6	R/W	0'h	MCLK1 Input Status Control 0'b: Floating 1'b: Pull-down
reserved	5:4	R/W	0'h	Reserved
Pu_spi	3	R/W	0'h	SPI(SPI_SCL/SPI_CS/SPI_SDI) Input Status Control 0'b: Floating 1'b: Pull-up
Pd_spi	2	R/W	0'h	SPI(SPI_SCL/SPI_CS/SPI_SDI) Input Status Control 0'b: Floating 1'b: Pull-down

Address: PR29				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Pd_i2c_m	1	R/W	0'h	Master I2C (SDA_M) Input Status Control 0'b: Floating 1'b: Pull-down
Pd_i2c_s	0	R/W	0'h	Slave I2C(SCL_S/SDA_S) Input Status Control 0'b: Floating 1'b: Pull-down

10.154. PR-2Ah: Digital Pin Initial Status Control

Default: 0000'h

Table 171. PR-2Ah: Digital Pin Initial Status Control

Address: PR2A				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:14	R/W	0'h	Reserved
Pu_dmic1	13	R/W	0'h	DMIC_SDA1 Input Status Control 0'b: Floating 1'b: Pull-up
Pd_dmic1	12	R/W	0'h	DMIC_SDA1 Input Status Control 0'b: Floating 1'b: Pull-down
Pu_dmic2	11	R/W	0'h	DMIC_SDA2 Input Status Control 0'b: Floating 1'b: Pull-up
Pd_dmic2	10	R/W	0'h	DMIC_SDA2 Input Status Control 0'b: Floating 1'b: Pull-down
reserved	9:4	R/W	0'h	Reserved
Pu_gpio1	3	R/W	0'h	GPIO1 Input Status Control 0'b: Floating 1'b: Pull-up
Pd_gpio1	2	R/W	0'h	GPIO1 Input Status Control 0'b: Floating 1'b: Pull-down
reserved	1:0	R/W	0'h	Reserved

10.155. PR-3Dh: ADC/DAC RESET Control

Default: 2088'h

Table 172. PR-3Dh: ADC/DAC RESET Control

Address: PR3D				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R/W	1'h	Reserved
en_ckgen_adc	12	R/W	0'h	ADC Reset Control 0'b: Reset 1'b: Normal
Reserved	11:10	R/W	0'h	Reserved
en_ckgen_dac	9	R/W	0'h	DAC Reset Control 0'b: Reset 1'b: Normal
Reserved	8:0	R/W	88'h	Reserved

10.156. PR-A0h: DAC_L EQ (LPF1:a1)

Default: 1C10'h

Table 173. PR-A0h: DAC_L EQ (LPF1:a1)

Address: PRA0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_lpf1_a1_l	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.157. PR-A1h: DAC_L EQ (LPF1:H0)

Default: 01F4'h

Table 174. PR-A1h: DAC_L EQ (LPF1:H0)

Address: PRA1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_lpf1_h0_l	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.158. PR-A2h: DAC_R EQ (LPF1:a1)

Default: 1C10’h

Table 175. PR-A2h: DAC_R EQ (LPF1:a1)

Address: PRA2				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_lpf1_a1_r	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.159. PR-A3h: DAC_R EQ (LPF1:H0)

Default: 01F4’h

Table 176. PR-A3h: DAC_R EQ (LPF1:H0)

Address: PRA3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_lpf1_h0_r	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.160. PR-A4h: DAC_L EQ (LPF2:a1)

Default: 1C10’h

Table 177. PR-A4h: DAC_L EQ (LPF2:a1)

Address: PRA4				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_lpf2_a1_l	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.161. PR-A5h: DAC_L EQ (LPF2:H0)

Default: 01F4'h

Table 178. PR-A5h: DAC_L EQ (LPF2:H0)

Address: PRA5				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_lpf2_h0_l	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.162. PR-A6h: DAC_R EQ (LPF2:a1)

Default: 1C10'h

Table 179. PR-A6h: DAC_R EQ (LPF2:a1)

Address: PRA6				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_lpf2_a1_r	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.163. PR-A7h: DAC_R EQ (LPF2:H0)

Default: 01F4'h

Table 180. PR-A7h: DAC_R EQ (LPF2:H0)

Address: PRA6				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_lpf2_a1_r	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.164. PR-A8h: DAC_L EQ (BPF1:a1)

Default: C882'h

Table 181. PR-A8h: DAC_L EQ (BPF1:a1)

Address: PRA8				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf1_a1_l	15:0	R/W	C882'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.165. PR-A9h: DAC_L EQ (BPF1:a2)

Default: 1C10'h

Table 182. PR-A9h: DAC_L EQ (BPF1:a2)

Address: PRA9				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf1_a2_l	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

10.166. PR-AAh: DAC_L EQ (BPF1:H0)

Default: 01F4'h

Table 183. PR-AAh: DAC_L EQ (BPF1:H0)

Address: PRAA				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf1_h0_l	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.167. PR-ABh: DAC_R EQ (BPF1:a1)

Default: C882'h

Table 184. PR-ABh: DAC_R EQ (BPF1:a1)

Address: PRAB				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf1_a1_r	15:0	R/W	C882'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.168. PR-ACh: DAC_R EQ (BPF1:a2)

Default: 1C10'h

Table 185. PR-ACh: DAC_R EQ (BPF1:a2)

Address: PRAC				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf1_a2_r	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

10.169. PR-ADh: DAC_R EQ (BPF1:H0)

Default: 01F4'h

Table 186. PR-ADh: DAC_R EQ (BPF1:H0)

Address: PRAD				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf1_h0_r	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.170. PR-AEh: DAC_L EQ (BPF2:a1)

Default: C882'h

Table 187. PR-AEh: DAC_L EQ (BPF2:a1)

Address: PRAE				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf2_a1_l	15:0	R/W	C882'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.171. PR-AFh: DAC_L EQ (BPF2:a2)

Default: 1C10'h

Table 188. PR-AFh: DAC_L EQ (BPF2:a2)

Address: PRAF				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf2_a2_l	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

10.172. PR-B0h: DAC_L EQ (BPF2:H0)

Default: 01F4'h

Table 189. PR-B0h: DAC_L EQ (BPF2:H0)

Address: PRB0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf2_h0_l	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.173. PR-B1h: DAC_R EQ (BPF2:a1)

Default: C882'h

Table 190. PR-B1h: DAC_R EQ (BPF2:a1)

Address: PRB1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf2_a1_r	15:0	R/W	C882'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.174. PR-B2h: DAC_R EQ (BPF2:a2)

Default: 1C10'h

Table 191. PR-B2h: DAC_R EQ (BPF2:a2)

Address: PRB2				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf2_a2_r	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

10.175. PR-B3h: DAC_R EQ (BPF2:H0)

Default: 01F4'h

Table 192. PR-B3h: DAC_R EQ (BPF2:H0)

Address: PRB3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf2_h0_r	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.176. PR-B4h: DAC_L EQ (BPF3:a1)

Default: C882'h

Table 193. PR-B4h: DAC_L EQ (BPF3:a1)

Address: PRB4				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf3_a1_l	15:0	R/W	C882'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.177. PR-B5h: DAC_L EQ (BPF3:a2)

Default: 1C10'h

Table 194. PR-B5h: DAC_L EQ (BPF3:a2)

Address: PRB5				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf5_a2_l	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

10.178. PR-B6h: DAC_L EQ (BPF3:H0)

Default: 01F4'h

Table 195. PR-B6h: DAC_L EQ (BPF3:H0)

Address: PRB6				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf3_h0_l	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.179. PR-B7h: DAC_R EQ (BPF3:a1)

Default: C882'h

Table 196. PR-B7h: DAC_R EQ (BPF3:a1)

Address: PRB7				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf3_a1_r	15:0	R/W	C882'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.180. PR-B8h: DAC_R EQ (BPF3:a2)

Default: 1C10'h

Table 197. PR-B8h: DAC_R EQ (BPF3:a2)

Address: PRB8				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf3_a2_r	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

10.181. PR-B9h: DAC_R EQ (BPF3:H0)

Default: 01F4'h

Table 198. PR-B9h: DAC_R EQ (BPF3:H0)

Address: PRB9				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf3_h0_r	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.182. PR-BAh: DAC_L EQ (BPF4:a1)

Default: C882'h

Table 199. PR-BAh: DAC_L EQ (BPF4:a1)

Address: PRBA				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf4_a1_l	15:0	R/W	C882'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.183. PR-BBh: DAC_L EQ (BPF4:a2)

Default: 1C10'h

Table 200. PR-BBh: DAC_L EQ (BPF4:a2)

Address: PRBB				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf4_a2_l	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

10.184. PR-BCh: DAC_L EQ (BPF4:H0)

Default: 01F4'h

Table 201. PR-BCh: DAC_L EQ (BPF4:H0)

Address: PRBC				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf4_h0_l	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.185. PR-BDh: DAC_R EQ (BPF4:a1)

Default: C882'h

Table 202. PR-BDh: DAC_R EQ (BPF4:a1)

Address: PRBD				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf4_a1_r	15:0	R/W	C882'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.186. PR-BEh: DAC_R EQ (BPF4:a2)

Default: 1C10'h

Table 203. PR-BEh: DAC_R EQ (BPF4:a2)

Address: PRBE				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf4_a2_r	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

10.187. PR-BFh: DAC_R EQ (BPF4:H0)

Default: 1C10'h

Table 204. PR-BFh: DAC_R EQ (BPF4:H0)

Address: PRBF				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf4_h0_r	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

Address: PRBF				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**

10.188. PR-C0h: DAC_L EQ (BPF5:a1)

Default: C882'h

Table 205. PR-C0h: DAC_L EQ (BPF5:a1)

Address: PRC0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf5_a1_l	15:0	R/W	C882'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.189. PR-C1h: DAC_L EQ (BPF5:a2)

Default: 1C10'h

Table 206. PR-C1h: DAC_L EQ (BPF5:a2)

Address: PRC1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf5_a2_l	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

10.190. PR-C2h: DAC_L EQ (BPF5:H0)

Default: 01F4'h

Table 207. PR-C2h: DAC_L EQ (BPF5:H0)

Address: PRC2				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf5_h0_l	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.191. PR-C3h: DAC_R EQ (BPF5:a1)

Default: C882'h

Table 208. PR-C3h: DAC_R EQ (BPF5:a1)

Address: PRC3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf5_a1_r	15:0	R/W	C882'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.192. PR-C4h: DAC_R EQ (BPF5:a2)

Default: 1C10'h

Table 209. PR-C4h: DAC_R EQ (BPF5:a2)

Address: PRC4				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf5_a2_r	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

10.193. PR-C5h: DAC_R EQ (BPF5:H0)

Default: 01F4'h

Table 210. PR-C5h: DAC_R EQ (BPF5:H0)

Address: PRC5				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_bpf5_h0_r	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.194. PR-C6h: DAC_L EQ (HPF1:a1)

Default: 1C10'h

Table 211. PR-C6h: DAC_L EQ (HPF1:a1)

Address: PRC6				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_hpf1_a1_l	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.195. PR-C7h: DAC_L EQ (HPF1:H0)

Default: 01F4'h

Table 212. PR-C7h: DAC_L EQ (HPF1:H0)

Address: PRC7				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_hpf1_h0_l	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.196. PR-C8h: DAC_R EQ (HPF1:a1)

Default: 1C10'h

Table 213. PR-C8h: DAC_R EQ (HPF1:a1)

Address: PRC8				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_hpf1_a1_r	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.197. PR-C9h: DAC_R EQ (HPF1:H0)

Default: 01F4'h

Table 214. PR-C9h: DAC_R EQ (HPF1:H0)

Address: PRC9				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_hpf1_h0_r	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.198. PR-CAh: DAC_L EQ (HPF3:a1)

Default: 1C10'h

Table 215. PR-CAh: DAC_L EQ (HPF3:a1)

Address: PRCA				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_hpf3_a1_l	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.199. PR-CBh: DAC_L EQ (HPF3:H0)

Default: 01F4'h

Table 216. PR-CBh: DAC_L EQ (HPF3:H0)

Address: PRCB				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_hpf3_h0_l	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.200. PR-CCh: DAC_R EQ (HPF3:a1)

Default: 1C10'h

Table 217. PR-CCh: DAC_R EQ (HPF3:a1)

Address: PRCC				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_hpf3_a1_r	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.201. PR-CDh: DAC_R EQ (HPF3:H0)

Default: 01F4'h

Table 218. PR-CDh: DAC_R EQ (HPF3:H0)

Address: PRCD				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_hpf3_h0_r	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

Address: PRCD				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**

10.202. PR-CEh: DAC_L EQ (HPF2:a1)

Default: 2000'h

Table 219. PR-CEh: DAC_L EQ (HPF2:a1)

Address: PRCE				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_hpf2_a1_l	15:0	R/W	2000'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.203. PR-CFh: DAC_L EQ (HPF2:a2)

Default: 0000'h

Table 220. PR-CFh: DAC_L EQ (HPF2:a2)

Address: PRCF				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_hpf2_a2_l	15:0	R/W	0000'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.204. PR-D0h: DAC_L EQ (HPF2:H0)

Default: 2000'h

Table 221. PR-D0h: DAC_L EQ (HPF2:H0)

Address: PRD0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_hpf2_h0_l	15:0	R/W	2000'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.205. PR-D1h: DAC_R EQ (HPF2:a1)

Default: 2000'h

Table 222. PR-D1h: DAC_R EQ (HPF2:a1)

Address: PRD1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_hpf2_a1_r	15:0	R/W	2000'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.206. PR-D2h: DAC_R EQ (HPF2:a2)

Default: 0000'h

Table 223. PR-D2h: DAC_R EQ (HPF2:a2)

Address: PRD2				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_hpf2_a2_r	15:0	R/W	0000'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.207. PR-D3h: DAC_R EQ (HPF2:H0)

Default: 2000'h

Table 224. PR-D3h: DAC_R EQ (HPF2:H0)

Address: PRD3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_hpf2_h0_r	15:0	R/W	2000'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.208. PR-D4h: DAC_L EQ Pre-Volume Control

Default: 0800'h

Table 225. PR-D4h: DAC_L EQ Pre-Volume Control

Address: PRD4				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_pre_vol_l	15:0	R/W	0800'h	DAC Left Channel EQ Pre-Volume Control 2's Complement in 5.11 Format. (Default is 0dB) The range is from -16 ~ 15.99, pre-gain should be in 0 ~ 15.99 [+24dB ~ -66dB]

10.209. PR-D5h: DAC_R EQ Pre-Volume Control

Default: 0800'h

Table 226. PR-D5h: DAC_R EQ Pre-Volume Control

Address: PRD5				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_pre_vol_r	15:0	R/W	0800'h	DAC Right Channel EQ Pre-Volume Control 2's Complement in 5.11 Format. (Default is 0dB) The range is from -16 ~ 15.99, pre-gain should be in 0 ~ 15.99 [+24dB ~ -66dB]

10.210. PR-D6h: DAC_L EQ Post-Volume Control

Default: 0800'h

Table 227. PR-D6h: DAC_L EQ Post-Volume Control

Address: PRD6				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_post_vol_l	15:0	R/W	0800'h	DAC Left Channel EQ Post-Volume Control 2's Complement in 5.11 Format. (Default is 0dB) The range is from -16 ~ 15.99, pre-gain should be in 0 ~ 15.99 [+24dB ~ -66dB]

10.211. PR-D7h: DAC_R EQ Post-Volume Control

Default: 0800'h

Table 228. PR-D7h: DAC_R EQ Post-Volume Control

Address: PRD7				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_post_vol_r	15:0	R/W	0800'h	DAC Right Channel EQ Post-Volume Control 2's Complement in 5.11 Format. (Default is 0dB) The range is from -16 ~ 15.99, pre-gain should be in 0 ~ 15.99 [+24dB ~ -66dB]

10.212. PR-D8h: ADC EQ (LPF:a1)

Default: 1C10'h

Table 229. PR-D8h: ADC EQ (LPF:a1)

Address: PRD8				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ad_eq_lpf_a1	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.213. PR-D9h: ADC EQ (LPF:H0)

Default: 01F4'h

Table 230. PR-D9h: ADC EQ (LPF:H0)

Address: PRD9				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ad_eq_lpf_h0	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.214. PR-DAh: ADC EQ (BPF1:a1)

Default: E904'h

Table 231. PR-DAh: ADC EQ (BPF1:a1)

Address: PRDA				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ad_eq_Bpf1_a1	15:0	R/W	E904'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.215. PR-DBh: ADC EQ (BPF1:a2)

Default: 1C10'h

Table 232. PR-DBh: ADC EQ (BPF1:a2)

Address: PRDB				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Ad_eq_Bpf1_a2	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

10.216. PR-DCh: ADC EQ (BPF1:H0)

Default: 01F4'h

Table 233. PR-DCh: ADC EQ (BPF1:H0)

Address: PRDC				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ad_eq_Bpf1_h0	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.217. PR-DDh: ADC EQ (BPF2:a1)

Default: E904'h

Table 234. PR-DDh: ADC EQ (BPF2:a1)

Address: PRDD				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ad_eq_Bpf2_a1	15:0	R/W	E904'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.218. PR-DEh: ADC EQ (BPF2:a2)

Default: 1C10'h

Table 235. PR-DEh: ADC EQ (BPF2:a2)

Address: PRDB				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Ad_eq_Bpf2_a2	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

10.219. PR-DFh: ADC EQ (BPF2:H0)

Default: 01F4'h

Table 236. PR-DFh: ADC EQ (BPF2:H0)

Address: PRDF				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ad_eq_Bpf2_h0	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.220. PR-E0h: ADC EQ (BPF3:a1)

Default: E904'h

Table 237. PR-E0h: ADC EQ (BPF3:a1)

Address: PRE0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ad_eq_Bpf3_a1	15:0	R/W	E904'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.221. PR-E1h: ADC EQ (BPF3:a2)

Default: 1C10'h

Table 238. PR-E1h: ADC EQ (BPF3:a2)

Address: PRE1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Ad_eq_Bpf3_a2	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

10.222. PR-E2h: ADC EQ (BPF3:H0)

Default: 01F4'h

Table 239. PR-E2h: ADC EQ (BPF3:H0)

Address: PRE2				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ad_eq_Bpf3_h0	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.223. PR-E3h: ADC EQ (BPF4:a1)

Default: E904'h

Table 240. PR-E3h: ADC EQ (BPF4:a1)

Address: PRE3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ad_eq_Bpf4_a1	15:0	R/W	E904'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.224. PR-E4h: ADC EQ (BPF4:a2)

Default: 1C10'h

Table 241. PR-E4h: ADC EQ (BPF4:a2)

Address: PRE4				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Ad_eq_Bpf4_a2	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

10.225. PR-E5h: ADC EQ (BPF4:H0)

Default: 01F4'h

Table 242. PR-E5h: ADC EQ (BPF4:H0)

Address: PRE5				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ad_eq_Bpf4_h0	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.226. PR-E6h: ADC EQ (HPF1:a1)

Default: 1C10'h

Table 243. PR-E6h: ADC EQ (HPF1:a1)

Address: PRE6				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Ad_eq_hpf1_a1	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

10.227. PR-E7h: ADC EQ (HPF1:H0)

Default: 01F4'h

Table 244. PR-E7h: ADC EQ (HPF1:H0)

Address: PRE7				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ad_eq_hpf1_h0	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

10.228. PR-E8h: ADC EQ Pre-Volume Control

Default: 0800'h

Table 245. PR-E8h: ADC EQ Pre-Volume Control

Address: PRE8				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ad_eq_pre_vol	15:0	R/W	0800'h	ADC Left Channel EQ Pre-Volume Control 2's Complement in 5.11 Format. (Default is 0dB) The range is from -16 ~ 15.99, pre-gain should be in 0 ~ 15.99 [+24dB ~ -66dB]

10.229. PR-E9h: ADC EQ Post-Volume Control

Default: 0800'h

Table 246. PR-E9h: ADC EQ Post-Volume Control

Address: PRE9				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Ad_eq_post_vol	15:0	R/W	0800'h	ADC Left Channel EQ Post-Volume Control 2's Complement in 5.11 Format. (Default is 0dB) The range is from -16 ~ 15.99, pre-gain should be in 0 ~ 15.99 [+24dB ~ -66dB]

10.230. PR-EAh: DAC_L Biquad EQ (BPF1:h0-1)

Default: 0200'h

Table 247. PR-EAh: DAC_L Biquad EQ (BPF1:h0-1)

Address: PREA				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
Eq_biquad_h0_l_msb	12:0	R/W	0200'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.231. PR-EBh: DAC_L Biquad EQ (BPF1:h0-2)

Default: 0000'h

Table 248. PR-E6h: DAC_L Biquad EQ (BPF1:h0-2)

Address: PREB				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Eq_biquad_h0_l_lsb	15:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.232. PR-ECh: DAC_L Biquad EQ (BPF1:b1-1)

Default: 0000'h

Table 249. PR-ECh: DAC_L Biquad EQ (BPF1:b1-1)

Address: PREC				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
Eq_biquad_b1_l_msb	12:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.233. PR-EDh: DAC_L Biquad EQ (BPF1:b1-2)

Default: 0000'h

Table 250. PR-EDh: DAC_L Biquad EQ (BPF1:b1-2)

Address: PRED				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Eq_biquad_b1_l_lsb	15:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.234. PR-EEh: DAC_L Biquad EQ (BPF1:b2-1)

Default: 0000'h

Table 251. PR-EEh: DAC_L Biquad EQ (BPF1:b2-1)

Address: PREE				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
Eq_biquad_b2_l_msb	12:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.235. PR-EFh: DAC_L Biquad EQ (BPF1:b2-2)

Default: 0000'h

Table 252. PR-EFh: DAC_L Biquad EQ (BPF1:b2-2)

Address: PREF				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Eq_biquad_b2_l_lsb	15:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.236. PR-F0h: DAC_L Biquad EQ (BPF1:a1-1)

Default: 0000'h

Table 253. PR-F0h: DAC_L Biquad EQ (BPF1:a1-1)

Address: PRF0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
Eq_biquad_a1_l_msb	12:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.237. PR-F1h: DAC_L Biquad EQ (BPF1:a1-2)

Default: 0000'h

Table 254. PR-F1h: DAC_L Biquad EQ (BPF1:a1-2)

Address: PRF1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Eq_biquad_a1_1_lsb	15:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.238. PR-F2h: DAC_L Biquad EQ (BPF1:a2-1)

Default: 0000'h

Table 255. PR-F2h: DAC_L Biquad EQ (BPF1:a2-1)

Address: PRF2				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
Eq_biquad_a2_l_msb	12:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.239. PR-F3h: DAC_L Biquad EQ (BPF1:a2-2)

Default: 0000'h

Table 256. PR-F3h: DAC_L Biquad EQ (BPF1:a2-2)

Address: PRF3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Eq_biquad_a2_l_lsb	15:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.240. PR-F4h: DAC_R Biquad EQ (BPF1:h0-1)

Default: 0200'h

Table 257. PR-F4h: DAC_R Biquad EQ (BPF1:h0-1)

Address: PRF4				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
Eq_biquad_h0_r_msb	12:0	R/W	0200'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.241. PR-F5h: DAC_R Biquad EQ (BPF1:h0-2)

Default: 0000'h

Table 258. PR-F5h: DAC_R Biquad EQ (BPF1:h0-2)

Address: PRF5				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Eq_biquad_h0_r_lsb	15:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.242. PR-F6h: DAC_R Biquad EQ (BPF1:b1-1)

Default: 0000'h

Table 259. PR-F6h: DAC_R Biquad EQ (BPF1:b1-1)

Address: PRF6				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
Eq_biquad_b1_r_msb	12:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.243. PR-F7h: DAC_R Biquad EQ (BPF1:b1-2)

Default: 0000'h

Table 260. PR-F7h: DAC_R Biquad EQ (BPF1:b1-2)

Address: PRF7				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Eq_biquad_b1_r_lsb	15:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.244. PR-F8h: DAC_R Biquad EQ (BPF1:b2-1)

Default: 0000'h

Table 261. PR-F8h: DAC_R Biquad EQ (BPF1:b2-1)

Address: PRF8				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
Eq_biquad_b2_r_msb	12:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.245. PR-F9h: DAC_R Biquad EQ (BPF1:b2-2)

Default: 0000'h

Table 262. PR-F9h: DAC_R Biquad EQ (BPF1:b2-2)

Address: PRF9				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Eq_biquad_b2_r_lsb	15:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.246. PR-FAh: DAC_R Biquad EQ (BPF1:a1-1)

Default: 0000'h

Table 263. PR-FAh: DAC_R Biquad EQ (BPF1:a1-1)

Address: PRFA				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
Eq_biquad_a1_r_msb	12:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.247. PR-FBh: DAC_R Biquad EQ (BPF1:a1-2)

Default: 0000'h

Table 264. PR-FBh: DAC_R Biquad EQ (BPF1:a1-2)

Address: PRFB				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Eq_biquad_a1_r_lsb	15:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.248. PR-FCh: DAC_R Biquad EQ (BPF1:a2-1)

Default: 0000'h

Table 265. PR-FCh: DAC_R Biquad EQ (BPF1:a2-1)

Address: PRFC				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
Eq_biquad_a2_r_msb	12:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

10.249. PR-FDh: DAC_R Biquad EQ (BPF1:a2-2)

Default: 0000’h

Table 266. PR-FDh: DAC_R Biquad EQ (BPF1:a2-2)

Address: PRFD				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Eq_biquad_a2_r_lsb	15:0	R/W	0’h	2’s complement in 4.25 format. (The range is from –8~7.99)

10.250. DSP DMA Control Registers

DSP Address: 0x1800_0000				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Src_0	31:3	R/W	Undefined	DSP DMA Source Address Offset Address: 0x00
Src_1	31:3	R/W	Undefined	DSP DMA Source Address Offset Address: 0x04
Src_2	31:3	R/W	Undefined	DSP DMA Source Address Offset Address: 0x08
Src_3	31:3	R/W	Undefined	DSP DMA Source Address Offset Address: 0x0C
Src_4	31:3	R/W	Undefined	DSP DMA Source Address Offset Address: 0x10
Src_5	31:3	R/W	Undefined	DSP DMA Source Address Offset Address: 0x14
Src_6	31:3	R/W	Undefined	DSP DMA Source Address Offset Address: 0x18
Src_7	31:3	R/W	Undefined	DSP DMA Source Address Offset Address: 0x1C
Dts_0	31:3	R/W	Undefined	DSP DMA Destination Address Offset Address: 0x20
Dts_1	31:3	R/W	Undefined	DSP DMA Destination Address Offset Address: 0x24
Dts_2	31:3	R/W	Undefined	DSP DMA Destination Address Offset Address: 0x28
Dts_3	31:3	R/W	Undefined	DSP DMA Destination Address Offset Address: 0x2C
Dts_4	31:3	R/W	Undefined	DSP DMA Destination Address Offset Address: 0x30
Dts_5	31:3	R/W	Undefined	DSP DMA Destination Address Offset Address: 0x34
Dts_6	31:3	R/W	Undefined	DSP DMA Destination Address Offset Address: 0x38
Dts_7	31:3	R/W	Undefined	DSP DMA Destination Address Offset Address: 0x3C

DSP Address: 0x1800_0000				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
size_0_valid	15	R/W	0'h	DSP DMA Valid Bit for This Entry Offset Address: 0x40
Size_0_size	13:3	R/W	Undefined	DSP DMA Size in 8 Bytes (Up to 8KB) Offset Address: 0x40
size_1_valid	15	R/W	0'h	DSP DMA Valid Bit for This Entry Offset Address: 0x44
Size_1_size	13:3	R/W	Undefined	DSP DMA Size in 8 Bytes (Up to 8KB) Offset Address: 0x44
size_2_valid	15	R/W	0'h	DSP DMA Valid Bit for This Entry Offset Address: 0x48

DSP Address: 0x1800_0000				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Size_2_size	13:3	R/W	Undefined	DSP DMA Size in 8 Bytes (Up to 8KB) Offset Address: 0x48
size_3_valid	15	R/W	0'h	DSP DMA Valid Bit for This Entry Offset Address: 0x4C
Size_3_size	13:3	R/W	Undefined	DSP DMA Size in 8 Bytes (Up to 8KB) Offset Address: 0x4C
size_4_valid	15	R/W	0'h	DSP DMA Valid Bit for This Entry Offset Address: 0x50
Size_4_size	13:3	R/W	Undefined	DSP DMA Size in 8 Bytes (Up to 8KB) Offset Address: 0x50
size_5_valid	15	R/W	0'h	DSP DMA Valid Bit for This Entry Offset Address: 0x54
Size_5_size	13:3	R/W	Undefined	DSP DMA Size in 8 Bytes (Up to 8KB) Offset Address: 0x54
size_6_valid	15	R/W	0'h	DSP DMA Valid Bit for This Entry Offset Address: 0x58
Size_6_size	13:3	R/W	Undefined	DSP DMA Size in 8 Bytes (Up to 8KB) Offset Address: 0x58
size_7_valid	15	R/W	0'h	DSP DMA Valid Bit for This Entry Offset Address: 0x5C
Size_7_size	13:3	R/W	Undefined	DSP DMA Size in 8 Bytes (Up to 8KB) Offset Address: 0x5C

DSP Address: 0x1800_0060				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
status_done_7	7	R/W	1'h	DSP DMA Done for This Entry
status_done_6	6	R/W	1'h	DSP DMA Done for This Entry
status_done_5	5	R/W	1'h	DSP DMA Done for This Entry
status_done_4	4	R/W	1'h	DSP DMA Done for This Entry
status_done_3	3	R/W	1'h	DSP DMA Done for This Entry
status_done_2	2	R/W	1'h	DSP DMA Done for This Entry
status_done_1	1	R/W	1'h	DSP DMA Done for This Entry
status_done_0	0	R/W	1'h	DSP DMA Done for This Entry

DSP Address: 0x1800_0000				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
cntl_rst	6	R/W	0'h	Hard Reset for DSP DMA Engine & Audio Engine as Power-On Reset Offset Address: 0x64
Cntl_go	0	R/W	0'h	DMA Go. Write "1" to Start DMA. Reset to "0" When All The DMA is Done or Has Been Stopped or Error is Encountered Offset Address: 0x64

DSP Address: 0x1800_0000				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
int	0	R/W	0'h	DMA Done Interrupt. Software Can Clear but Should not Set Offset Address: 0x68
Int_en	0	R/W	0'h	Interrupt Enable Offset Address: 0x6C
busy	31:0	R/W	Undefined	Count the cycles that DAM cannot access DMEM due to CPU is using it. It will stop accumulating when it is saturated. Software should reset the value. Hardware will not reset it. Offset Address: 0x74

10.251. DSP Control Registers

DSP Address: 0x1801_F000				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Interrupt_enable	10	R/W	0'h	DSP InBound Ring Buffer DMA 10 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	9	R/W	0'h	DSP InBound Ring Buffer DMA 9 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	8	R/W	0'h	DSP InBound Ring Buffer DMA 8 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	7	R/W	0'h	DSP InBound Ring Buffer DMA 7 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	6	R/W	0'h	DSP InBound Ring Buffer DMA 6 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	5	R/W	0'h	DSP InBound Ring Buffer DMA 5 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	4	R/W	0'h	DSP InBound Ring Buffer DMA 4 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	3	R/W	0'h	DSP InBound Ring Buffer DMA 3 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	2	R/W	0'h	DSP InBound Ring Buffer DMA 2 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	1	R/W	0'h	DSP InBound Ring Buffer DMA 1 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	0	R/W	0'h	DSP InBound Ring Buffer DMA 0 Frame Interrupt Enable 0'b: Disable 1'b: Enable

DSP Address: 0x1801_F008				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Interrupt_indicate	10	R	0'h	DSP InBound Ring Buffer DMA 10 Frame Interrupt Indicator
Interrupt_indicate	9	R	0'h	DSP InBound Ring Buffer DMA 9 Frame Interrupt Indicator
Interrupt_indicate	8	R	0'h	DSP InBound Ring Buffer DMA 8 Frame Interrupt Indicator
Interrupt_indicate	7	R	0'h	DSP InBound Ring Buffer DMA 7 Frame Interrupt Indicator
Interrupt_indicate	6	R	0'h	DSP InBound Ring Buffer DMA 6 Frame Interrupt Indicator
Interrupt_indicate	5	R	0'h	DSP InBound Ring Buffer DMA 5 Frame Interrupt Indicator
Interrupt_indicate	4	R	0'h	DSP InBound Ring Buffer DMA 4 Frame Interrupt Indicator
Interrupt_indicate	3	R	0'h	DSP InBound Ring Buffer DMA 3 Frame Interrupt Indicator
Interrupt_indicate	2	R	0'h	DSP InBound Ring Buffer DMA 2 Frame Interrupt Indicator
Interrupt_indicate	1	R	0'h	DSP InBound Ring Buffer DMA 1 Frame Interrupt Indicator
Interrupt_indicate	0	R	0'h	DSP InBound Ring Buffer DMA 0 Frame Interrupt Indicator

DSP Address: 0x1801_F00C				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
error_indicator	30	R	0'h	DSP OutBound Ring Buffer DMA 14 Error Indicator
error_indicator	29	R	0'h	DSP OutBound Ring Buffer DMA 13 Error Indicator
error_indicator	28	R	0'h	DSP OutBound Ring Buffer DMA 12 Error Indicator
error_indicator	27	R	0'h	DSP OutBound Ring Buffer DMA 11 Error Indicator
error_indicator	26	R	0'h	DSP OutBound Ring Buffer DMA 10 Error Indicator
error_indicator	25	R	0'h	DSP OutBound Ring Buffer DMA 9 Error Indicator
error_indicator	24	R	0'h	DSP OutBound Ring Buffer DMA 8 Error Indicator
error_indicator	23	R	0'h	DSP OutBound Ring Buffer DMA 7 Error Indicator
error_indicator	22	R	0'h	DSP OutBound Ring Buffer DMA 6 Error Indicator
error_indicator	21	R	0'h	DSP OutBound Ring Buffer DMA 5 Error Indicator
error_indicator	20	R	0'h	DSP OutBound Ring Buffer DMA 4 Error Indicator
error_indicator	19	R	0'h	DSP OutBound Ring Buffer DMA 3 Error Indicator
error_indicator	18	R	0'h	DSP OutBound Ring Buffer DMA 2 Error Indicator
error_indicator	17	R	0'h	DSP OutBound Ring Buffer DMA 1 Error Indicator
error_indicator	16	R	0'h	DSP OutBound Ring Buffer DMA 0 Error Indicator
error_indicator	14	R	0'h	DSP InBound Ring Buffer DMA 14 Error Indicator
error_indicator	13	R	0'h	DSP InBound Ring Buffer DMA 13 Error Indicator
error_indicator	12	R	0'h	DSP InBound Ring Buffer DMA 12 Error Indicator
error_indicator	11	R	0'h	DSP InBound Ring Buffer DMA 11 Error Indicator
error_indicator	10	R	0'h	DSP InBound Ring Buffer DMA 10 Error Indicator
error_indicator	9	R	0'h	DSP InBound Ring Buffer DMA 9 Error Indicator
error_indicator	8	R	0'h	DSP InBound Ring Buffer DMA 8 Error Indicator
error_indicator	7	R	0'h	DSP InBound Ring Buffer DMA 7 Error Indicator
error_indicator	6	R	0'h	DSP InBound Ring Buffer DMA 6 Error Indicator
error_indicator	5	R	0'h	DSP InBound Ring Buffer DMA 5 Error Indicator
error_indicator	4	R	0'h	DSP InBound Ring Buffer DMA 4 Error Indicator
error_indicator	3	R	0'h	DSP InBound Ring Buffer DMA 3 Error Indicator
error_indicator	2	R	0'h	DSP InBound Ring Buffer DMA 2 Error Indicator
error_indicator	1	R	0'h	DSP InBound Ring Buffer DMA 1 Error Indicator
error_indicator	0	R	0'h	DSP InBound Ring Buffer DMA 0 Error Indicator

DSP Address: 0x1801_F090				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Dsp_ctrl	2	R/W	0'h	NMI Enable 0'b: Disable 1'b: Enable
Dsp_ctrl	1	R/W	0'h	Trace Debug Enable 0'b: Disable 1'b: Enable
Dsp_ctrl	0	R/W	0'h	Boot Vector Selection 0'b: Boot on 0x5000_0000 1'b: Boot on IRAM

DSP Address: 0x1801_F094				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Interrupt_enable	10	R/W	0'h	DSP OutBound Ring Buffer DMA 10 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	9	R/W	0'h	DSP OutBound Ring Buffer DMA 9 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	8	R/W	0'h	DSP OutBound Ring Buffer DMA 8 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	7	R/W	0'h	DSP OutBound Ring Buffer DMA 7 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	6	R/W	0'h	DSP OutBound Ring Buffer DMA 6 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	5	R/W	0'h	DSP OutBound Ring Buffer DMA 5 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	4	R/W	0'h	DSP OutBound Ring Buffer DMA 4 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	3	R/W	0'h	DSP OutBound Ring Buffer DMA 3 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	2	R/W	0'h	DSP OutBound Ring Buffer DMA 2 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	1	R/W	0'h	DSP OutBound Ring Buffer DMA 1 Frame Interrupt Enable 0'b: Disable 1'b: Enable
Interrupt_enable	0	R/W	0'h	DSP OutBound Ring Buffer DMA 0 Frame Interrupt Enable 0'b: Disable 1'b: Enable

DSP Address: 0x1801_F098				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Interrupt_indicator	10	R/W	0'h	DSP OutBound Ring Buffer DMA 10 Frame Interrupt Indicator
Interrupt_indicator	9	R/W	0'h	DSP OutBound Ring Buffer DMA 9 Frame Interrupt Indicator
Interrupt_indicator	8	R/W	0'h	DSP OutBound Ring Buffer DMA 8 Frame Interrupt Indicator
Interrupt_indicator	7	R/W	0'h	DSP OutBound Ring Buffer DMA 7 Frame Interrupt Indicator
Interrupt_indicator	6	R/W	0'h	DSP OutBound Ring Buffer DMA 6 Frame Interrupt Indicator
Interrupt_indicator	5	R/W	0'h	DSP OutBound Ring Buffer DMA 5 Frame Interrupt Indicator
Interrupt_indicator	4	R/W	0'h	DSP OutBound Ring Buffer DMA 4 Frame Interrupt Indicator
Interrupt_indicator	3	R/W	0'h	DSP OutBound Ring Buffer DMA 3 Frame Interrupt Indicator
Interrupt_indicator	2	R/W	0'h	DSP OutBound Ring Buffer DMA 2 Frame Interrupt Indicator
Interrupt_indicator	1	R/W	0'h	DSP OutBound Ring Buffer DMA 1 Frame Interrupt Indicator
Interrupt_indicator	0	R/W	0'h	DSP OutBound Ring Buffer DMA 0 Frame Interrupt Indicator

10.252. DSP InBound0 Ring Buffer Control Registers

DSP Address: 0x1800_1000				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
str	31:0	R/W	Undefined	DSP InBound Ring Buffer Queue Start Address Offset Address: 0x00
end	31:0	R/W	Undefined	DSP InBound Ring Buffer Queue End Address Offset Address: 0x04
rp	31:0	R/W	Undefined	DSP InBound Ring Buffer Read Pointer (Update by F/W) Offset Address: 0x08
wp	31:0	R	Undefined	DSP InBound Ring Buffer Write Pointer (Update by H/W) Offset Address: 0x0C
Ringbuffer_en	0	R/W	0'h	DSP InBound Ring Buffer Enable Control Write "1" to start ring buffer Offset Address: 0x10
Format_sel	1	R/W	0'h	DSP InBound Ring Buffer Format 0'b: 32 bits zero padding mode 1'b: 16 bits truncate mode Offset Address: 0x10
Queue_mode_en	2	R/W	0'h	DSP InBound Ring Buffer Mode Control 0'b: Normal mode 1'b: InBound's rp will be OutBound's rp. F/W will not update InBound's rp Offset Address: 0x10

DSP Address: 0x1800_1000				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Bypass_en	3	R/W	0'h	DSP InBound Ring Buffer Bypass Control 0'b: Write data to wp 1'b: Write data to PCM bypass hub with wp disabled Offset Address: 0x10
Bypass_sel	8:4	R/W	Undefined	Write FIFO data to specified address of bypass hub (0x1801_0000 ~ 0x1801_007F) Offset Address: 0x10
Fifo_hw_rst_en	9	R/W	0'h	0'b: F/W need to assert fifo_rst=1 to flush FIFO 1'b: H/W flush FIFO itself Offset Address: 0x10
Aa_en	10	R/W	1'h	0'b: Disable 1'b: Enable auto alignment. If enabled, both start address and buffer size muse be multiples of 0x20 bytes Offset Address: 0x10
Mono_en	11	R/W	0'h	0'b: Default is stereo 1'b: Ring buffer is specified as mono operation Offset Address: 0x10
Tag_id	19:16	R/W	0'h	InBound ring buffer owns unique ID Offset Address: 0x10
Tag_conjugation	23:20	R/W	0'h	TBD Offset Address: 0x10
Fifo_rst	0	R/W	0'h	H/W and F/W write "1" to reset FIFO. IF int_fifo_full=1, F/W must assert fifo_rst and then deassert it Offset Address: 0x14
Int_buf_empty	0	R/W	0'h	Ring buffer empty interrupt. F/W can clear but should not set. Offset Address: 0x18
Int_buf_empty_en	0	R/W	0'h	Ring Buffer Empty Interrupt Enable 0'b: Disable 1'b: Enable Offset Address: 0x1C
Int_fifo_full	0	R/W	0'h	FIFO Full Interrupt. Assert only if fifo_hw_rst_en=1. F/W can clear but can not set. Offset Address: 0x20
Int_fifo_full_en	0	R/W	0'h	FIFO Full Interrupt Enable. Assert only if fifo_hw_rst_en=1 0'b: Disable 1'b: Enable Offset Address: 0x24
Rst_fw	0	R/W	0'h	F/W reset all ring buffer registers Offset Address: 0x28
Buf_thr	31:0	R/W	0'h	Parameter for inbound frame buffer level threshold. Note that (1)buf_thr cannot be set larger than buffer's own size. (2) unit:per sample of data, independent of format_sel Offset Address: 0x30
Fg_exceed_buf_thr	0	R/W	0'h	While level exceeds buf_thr, fg_exceed_buf_thr is asserted. Offset Address: 0x34

10.253. DSP OutBound0 Ring Buffer Control Registers

DSP Address: 0x1801_0000				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
str	31:0	R/W	Undefined	DSP OutBound Ring Buffer Queue Start Address Offset Address: 0x00
end	31:0	R/W	Undefined	DSP OutBound Ring Buffer Queue End Address Offset Address: 0x04
rp	31:0	R/W	Undefined	DSP OutBound Ring Buffer Read Pointer (Update by F/W) Offset Address: 0x08
wp	31:0	R	Undefined	DSP OutBound Ring Buffer Write Pointer (Update by H/W) Offset Address: 0x0C
Ringbuffer_en	0	R/W	0'h	DSP OutBound Ring Buffer Enable Control Write "1" to start ring buffer Offset Address: 0x10
Format_sel	1	R/W	0'h	DSP OutBound Ring Buffer Format 0'b: 32 bits zero padding mode 1'b: 16 bits truncate mode Offset Address: 0x10
Queue_mode_en	2	R/W	0'h	DSP OutBound Ring Buffer Mode Control 0'b: Normal mode 1'b: InBound's rp will be OutBound's rp. F/W will not update InBound's rp Offset Address: 0x10
Bypass_en	3	R/W	0'h	DSP OutBound Ring Buffer Bypass Control 0'b: Write data to wp 1'b: Write data to PCM bypass hub with wp disabled Offset Address: 0x10
Bypass_sel	8:4	R/W	Undefined	Write FIFO data to specified address of bypass hub (0x1801_0000 ~ 0x1801_007F) Offset Address: 0x10
Aa_en	10	R/W	1'h	0'b: Disable 1'b: Enable auto alignment. If enabled, both start address and buffer size muse be multiples of 0x20 bytes Offset Address: 0x10
Mono_en	11	R/W	0'h	0'b: Default is stereo 1'b: Ring buffer is specified as mono operation Offset Address: 0x10
Tag_id	19:16	R/W	0'h	InBound ring buffer owns unique ID Offset Address: 0x10
Tag_conjugation	23:20	R/W	0'h	TBD Offset Address: 0x10
threshold	31:0	R/W	100'h	Outbond buffer threshold. Fifo operation begins after the outbond buffer level exceeds threshold. Offset Address: 0x14
Int_buf_full	0	R/W	0'h	Ring buffer full interrupt. F/W can clear but should not set. Offset Address: 0x18
Int_buf_full_en	0	R/W	0'h	Ring Buffer Full Interrupt Enable 0'b: Disable 1'b: Enable Offset Address: 0x1C

DSP Address: 0x1801_0000				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Int_fifo_empty	0	R/W	0'h	FIFO Empty Interrupt. Assert only if fifo_hw_rst_en=1. F/W can clear but can not set. Offset Address: 0x20
Int_fifo_empty_en	0	R/W	0'h	FIFO Empty Interrupt Enable. Assert only if fifo_hw_rst_en=1 0'b: Disable 1'b: Enable Offset Address: 0x24
Rst_fw	0	R/W	0'h	F/W reset all ring buffer registers Offset Address: 0x28
Buf_thr	31:0	R/W	0'h	Parameter for inbound frame buffer level threshold. Note that (1)buf_thr cannot be set larger than buffer's own size. (2) unit:per sample of data, independent of format_sel Offset Address: 0x30
Fg_under_buf_thr	0	R/W	0'h	While level is under buf_thr, fg_exceed_buf_thr is asserted. Offset Address: 0x34
str	31:0	R/W	Undefined	DSP InBound Ring Buffer Queue Start Address Offset Address: 0x00
end	31:0	R/W	Undefined	DSP InBound Ring Buffer Queue End Address Offset Address: 0x04
rp	31:0	R/W	Undefined	DSP InBound Ring Buffer Read Pointer (Update by F/W) Offset Address: 0x08
wp	31:0	R	Undefined	DSP InBound Ring Buffer Write Pointer (Update by H/W) Offset Address: 0x0C

11. Electrical Characteristics

11.1. DC Characteristics

11.1.1. Absolute Maximum Ratings

Table 267. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies					
Digital IO Buffer	DBVDD1	-0.3	-	3.63	V
Digital Core (Codec)	DCVDD1	-0.3	-	1.4	V
Digital Core (DSP)	DCVDD3	-0.3	-	1.4	V
LDO Input	LDO_IN	-0.3	-	1.98	V
Analog	AVDD18	-0.3	-	1.98	V
Analog	AVDD18_LOUT	-0.3	-	1.98	V
Analog	DACREF	-0.3	-	1.98	V
Micbias	AVDD33	-0.3	-	3.63	V
Operating Ambient Temperature	Ta	-25	-	+85	°C
Storage Temperature	Ts	-55	-	+125	°C

11.1.2. Recommended Operating Conditions

Table 268. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Digital IO Buffer	DBVDD1	1.71	1.8	3.6	V
Digital Core (Codec)	DCVDD1	1.05	1.2	1.3	V
Digital Core (DSP)	DCVDD3	1.05	1.2	1.3	V
LDO Input	LDO_IN	1.2	1.8	1.9	V
Analog	AVDD18	1.71	1.8	1.9	V
Analog	AVDD18_LOUT	1.71	1.8	1.9	V
Analog	DACREF	1.71	1.8	1.9	V
Micbias	AVDD33	1.71	3.3	3.6	V

11.1.3. Static Characteristics

Table 269. Static Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage Range	V_{IN}	-0.30	-	DBVDD+0.30	V
Low Level Input Voltage	V_{IL}	-	-	0.35DBVDD	V
High Level Input Voltage	V_{IH}	0.65DBVDD	-	-	V
High Level Output Voltage	V_{OH}	0.9DBVDD	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.1DBVDD	V
Output Buffer High Drive Current	-	-	15	-	mA
Output Buffer Low Drive Current	-	-	14.7	-	mA
Input Buffer Pull-Up Resistor	-	125	148	180	KΩ
Input Buffer Pull-Down Resistor	-	193	225	266	KΩ

Parameter	Symbol	Min	Typ	Max	Units

Note: DBVDD=1.8V, DCVDD1=1.2V, $T_{ambient}$=40°C.

11.2. Analog Performance Characteristics

Table 270. Analog Performance Characteristics

Parameter	Min	Typ	Max	Units
Full Scale Input Voltage				
MIC Inputs (Single-ended)		0.55		Vrms
MIC Inputs (Differential)		1.2		Vrms
Full Scale Output Voltage				
Line Outputs (Single-ended)		0.55		Vrms
Line Outputs (Differential)		1.0		Vrms
S/N Ratio				
DAC to Line_Out (Single-Ended, -60dBFS)		100		dBA
DAC to Line_Out (Single-Ended, -60dBFS, 16-Bit Data Length)		98		dBA
DAC to Line_Out (Differential, -60dBFS)		100		dBA
DAC to Line_Out (Differential, -60dBFS, 16-Bit Data Length)		97		dBA
MIC_In to ADC with 0dB Gain (Differential, -60dBFS)		102		dBA
MIC_In to ADC with 0dB Gain (Differential, -60dBFS, 16-Bit Data Length))		101		dBA
MIC_In to ADC with 20dB Gain (Differential, -80dBFS)		95		dBA
MIC_In to ADC with 40dB Gain (Differential, -100dBFS)		78		dBA
Total Harmonic Distortion + Noise				
DAC to Line-Out (Single-Ended, -3dBFS)	-86	-91	-93	dB
DAC to Line-Out (Single-Ended, -1dBFS)	-86	-90	-92	dB
DAC to Line-Out (Differential, -3dBFS)	-86	-90	-92	dB
DAC to Line-Out (Differential, -1dBFS)	-86	-88	-90	dB
MIC_In to ADC with 0dB Gain (Differential, -3dBFS)		-95		dB
MIC_In to ADC with 0dB Gain (Differential, -1dBFS)		-94		dB
MIC_In to ADC with 20dB Gain (Differential, -23dBFS)		-91		dB
MIC_In to ADC with 20dB Gain (Differential, -21dBFS)		-91		dB
MIC_In to ADC with 40dB Gain (Differential, -43dBFS)		-77		dB
MIC_In to ADC with 40dB Gain (Differential, -41dBFS)		-76		dB
Cross Talk				
DAC to Line-Out (Differential, -3dBFS)		87		dB
MIC_In to ADC (Differential, -3dBFS)		81		dB
Noise Floor				
DAC to Line-Out (Differential, A-weighted)		12		uVrms
DAC to Line-Out (Single-Ended, A-weighted)		6.1		uVrms
MIC_In to ADC (Differential)		15		uVrms
PSRR				
DAC to Line-Out (100mVp-p, 217Hz)		73		dB

Parameter	Min	Typ	Max	Units
DAC to Line-Out (100mVp-p, 10kHz)		74		dB
MIC_In to ADC (100mVp-p, 217Hz, 0dB Boost Gain)		70		dB
MIC_In to ADC (100mVp-p, 217Hz, 20dB Boost Gain)		60		dB
MIC_In to ADC (100mVp-p, 1KHz, 20dB Boost Gain)		60		dB
MIC_In to ADC (100mVp-p, 10KHz, 20dB Boost Gain)		65		dB
Power Leakage (Chip All Power Down)				
1.8V			20	uA
3.3V			10	uA
MICBIAS1 Output Voltage				
Setting 1	-	0.9*AVDD33	-	V
Setting 2	-	0.75*AVDD33	-	V
MICBIAS1 Drive Current				
MICBIAS = 0.9*MICVDD	-	4	-	mA
Input Impedance				
IN1/IN2				
0dB		20K		Ohm
20dB		7.3K		Ohm
30dB		2.5K		Ohm
40dB		0.8K		Ohm
52dB		0.2K		Ohm

Note: Standard test conditions:
$T_{ambient}$=25°C
DBVDD1=1.8V
LDO_IN=1.8V
AVDD18=AVDD18_LOUT=1.8V
AVDD33=3.3V
DVDDD1=1.2V
LOUT Load is 10KOhm
1kHz input sine wave; PCM Sampling frequency=48kHz; 24-bit data length; Codec as slave mode; SYSCLK=256 * FS
Test bench Characterization BW: 20Hz~20kHz, 0dB attenuation

11.3. Signal Timing

11.3.1. I²C Control Interface

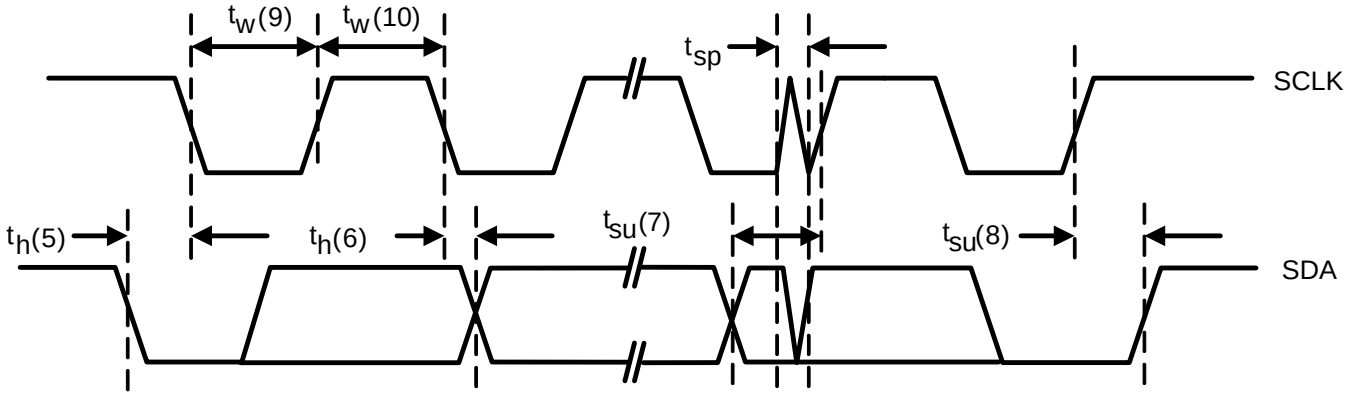


Figure 30. I²C Control Interface

Table 271. I²C Timing

Parameter	Symbol	Min	Typ	Max	Units
Clock Pulse Duration	$t_w(9)$	1.3	-	-	µs
Clock Pulse Duration	$t_w(10)$	600	-	-	ns
Clock Frequency	F	0	-	400K	Hz
Start Hold Time	$t_h(5)$	600	-	-	ns
Data Setup Time	$t_{su}(7)$	100	-	-	ns
Data Hold Time	$t_h(6)$	-	-	900	ns
Rising Time	t_r	-	-	300	ns
Falling Time	t_f	-	-	300	ns
Stop Setup Time	$t_{su}(8)$	600	-	-	ns
Pulse Width of Spikes Suppressed Input Filter	t_{sp}	0	-	50	ns

11.3.2. I²S/PCM Interface Master Mode

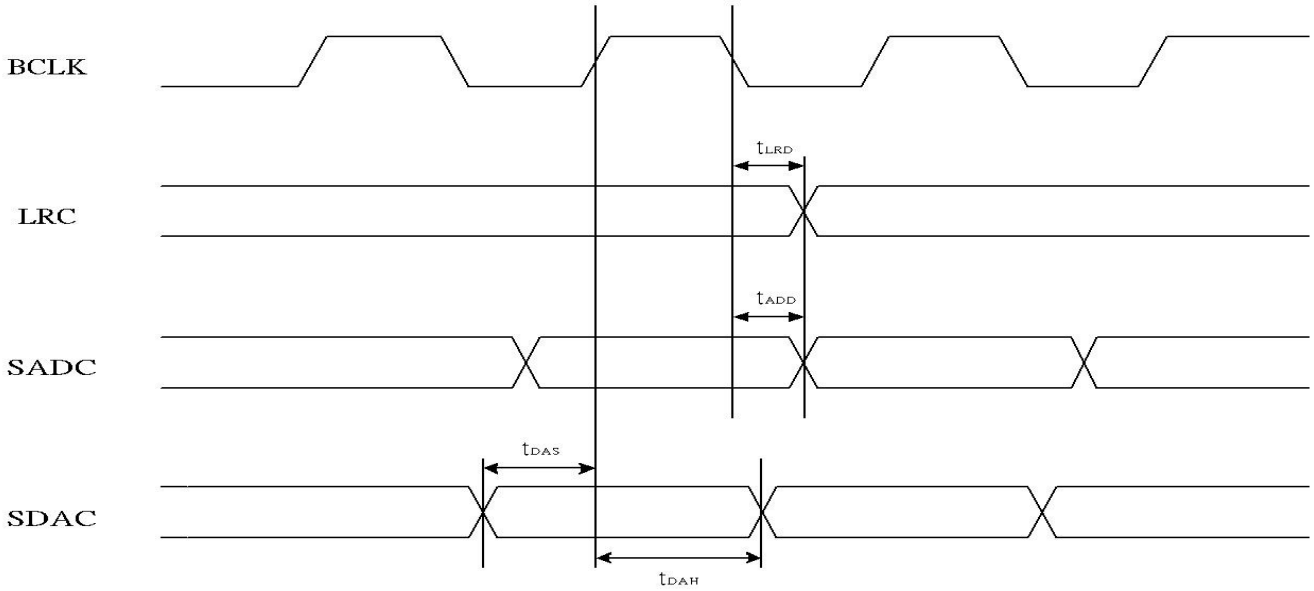


Figure 31. Timing of I²S/PCM Master Mode

Table 272. Timing of I²S/PCM Master Mode

Parameter	Symbol	Min	Typ	Max	Units
LRCK Output to BCLK Delay	t_{LRD}	-	-	30	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

11.3.3. I²S/PCM Interface Slave Mode

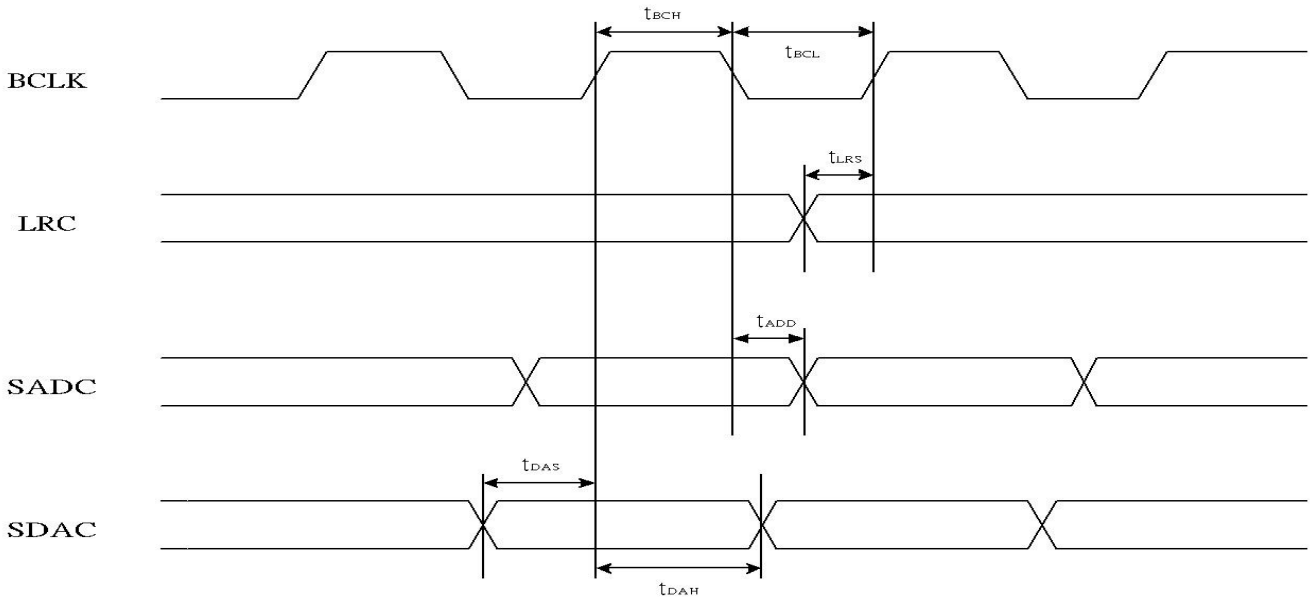


Figure 32. I²S/PCM Slave Mode Timing

Table 273. I²S/PCM Slave Mode Timing

Parameter	Symbol	Min	Typ	Max	Units
BCLK High Pulse Width	t_{BCH}	20	-	-	ns
BCLK Low Pulse Width	t_{BCL}	20	-	-	ns
LRCK Input Setup Time	t_{LRS}	30	-	-	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

11.3.4. Digital Microphone Interface

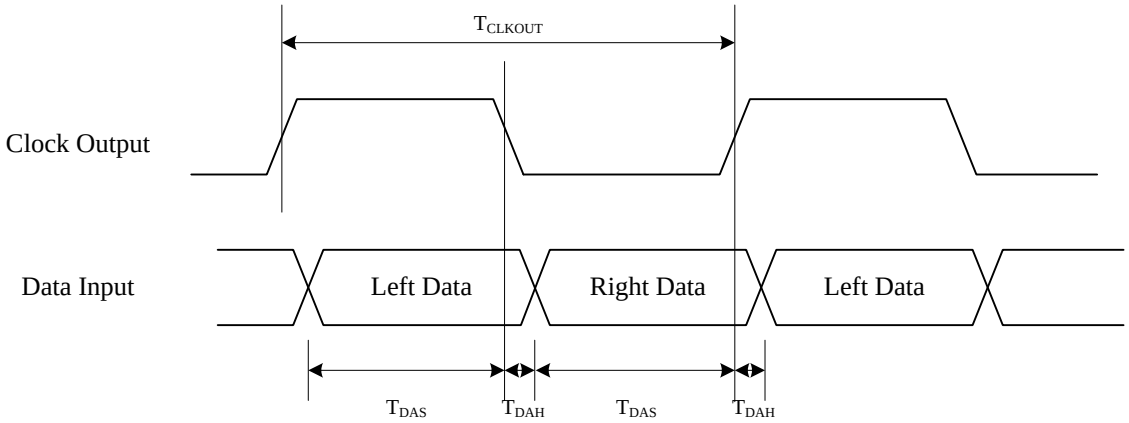


Figure 33. Digital Microphone Interface Timing

Table 274. Digital Microphone Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
Clock Output Rate	T_{CLKOUT}	150	-	-	ns
Clock Duty Cycle		45:55		55:45	
Data Input Setup Time	T_{DAS}	30	-	-	ns
Data Input Hold Time	T_{DAH}	30	-	-	ns

11.3.5. SPI Interface (Slave Mode)

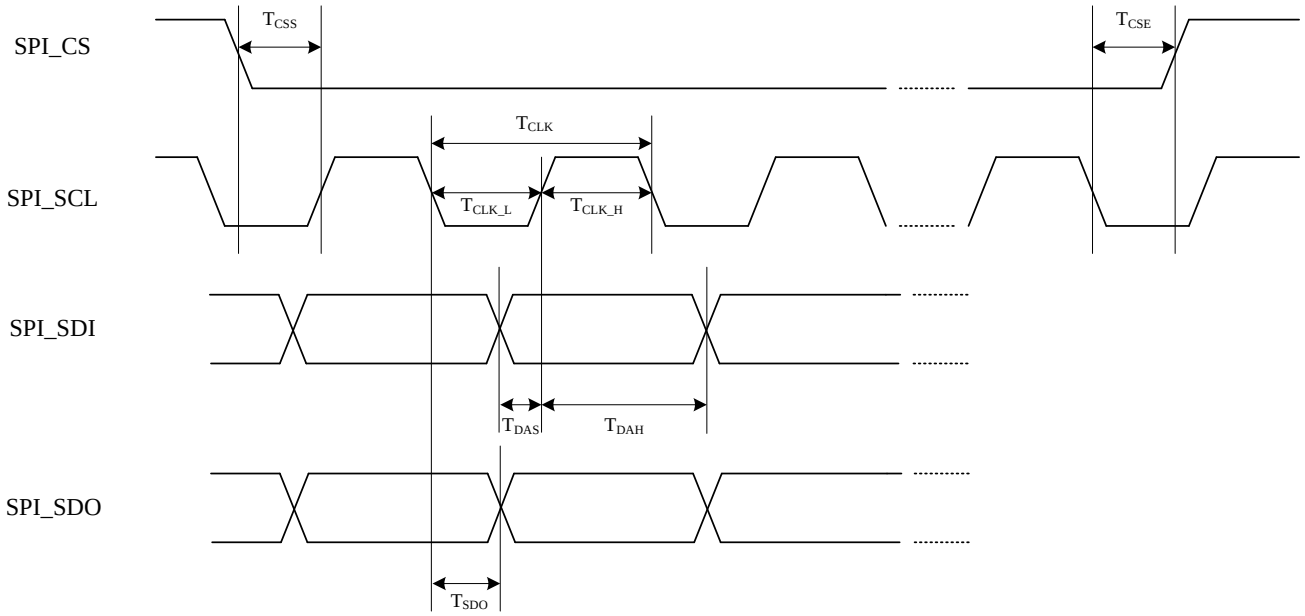
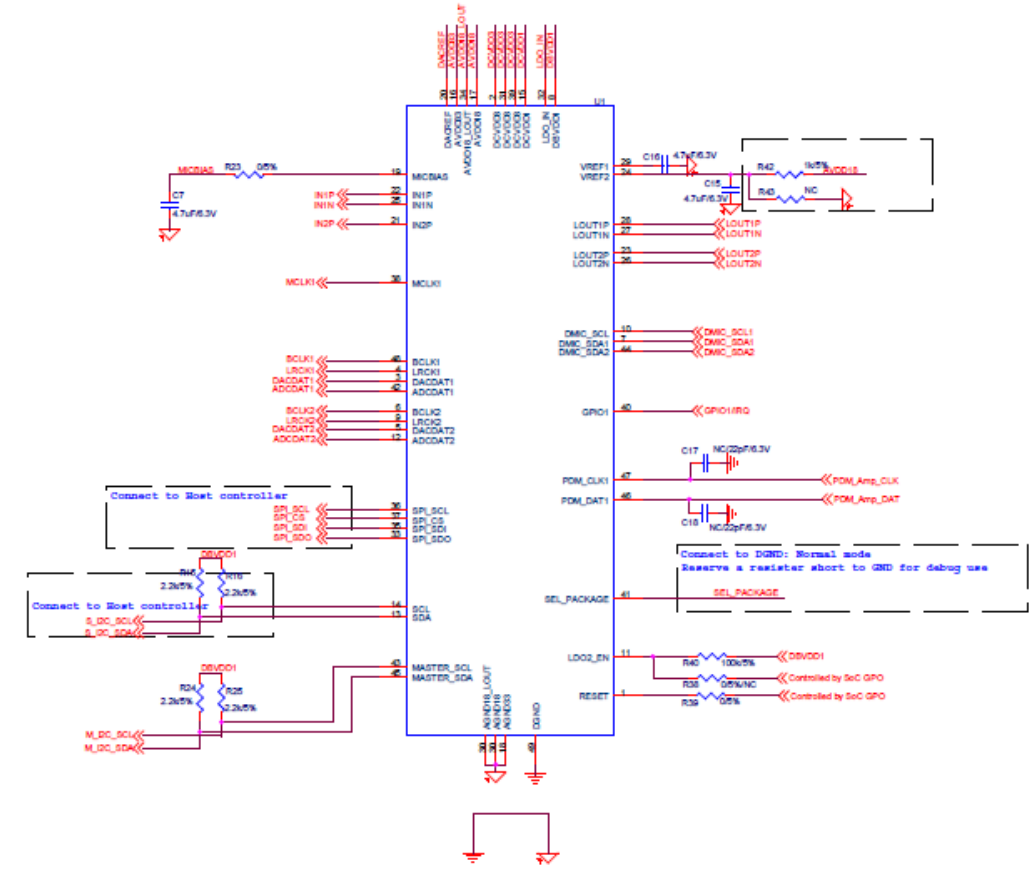


Figure 34. SPI Interface Timing

Table 275. SPI Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
SPI_CS falling edge to SPI_SCL rising edge	T_{CSS}	7			ns
SPI_SCL falling edge to SPI_CS rising edge	T_{CSE}	4			ns
SPI_SCL pulse period time	T_{CLKOUT}	33			ns
SPI_SCL pulse high width	T_{CLK_H}	13			ns
SPI_SCL pulse low width	T_{CLK_L}	13			ns
SPI_SDI setup time	T_{DAS}	7			ns
SPI_SDI hold time	T_{DAH}	4			ns
SPI_SDO output time	T_{SDO}			7	ns

12. Application Circuits



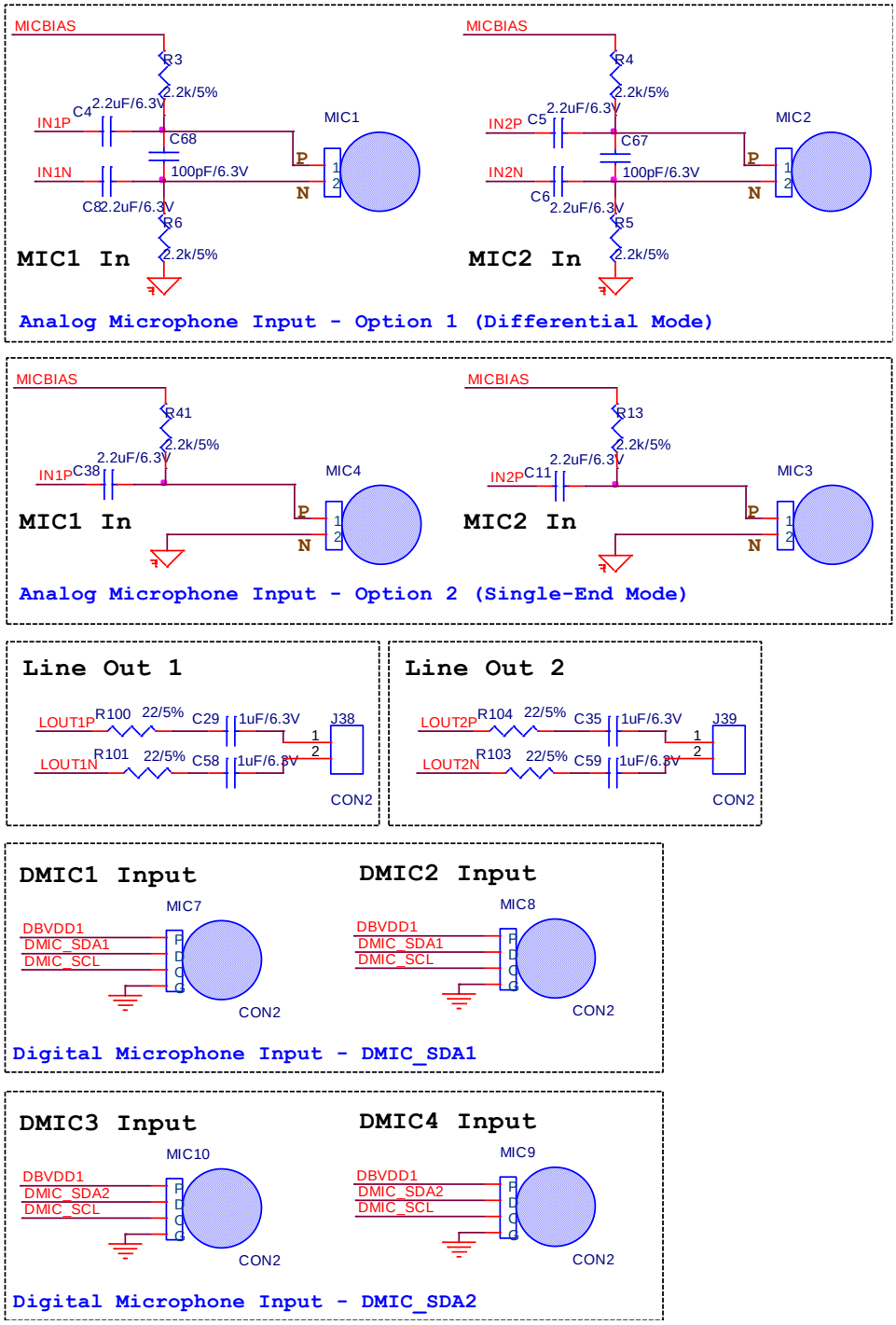
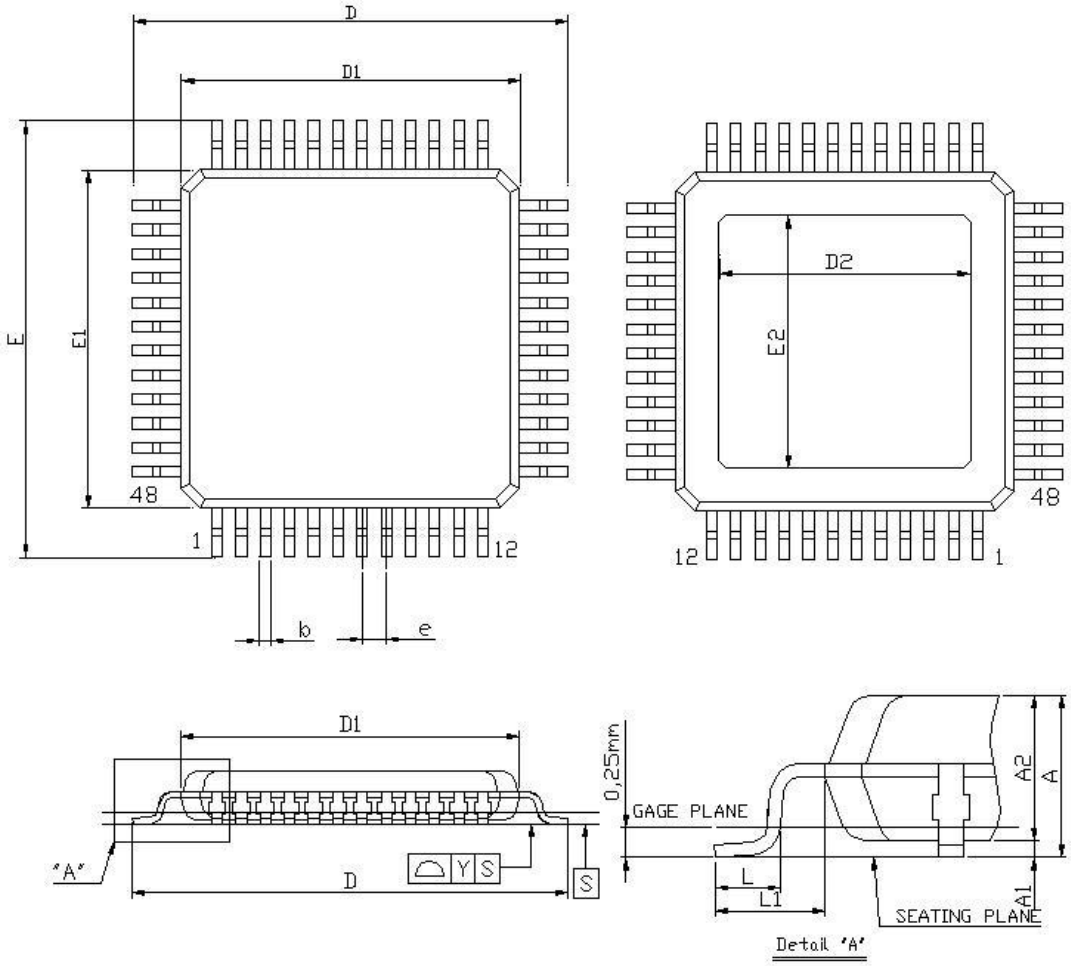


Figure 35. Application Circuit

13. Package Information

Low Profile Plastic Quad Flat Package 48 Leads 7x7mm^2 Outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
D/E		9.00BSC			0.354BSC	
D_1/E_1		7.00BSC			0.276BSC	
D_2/E_2	4.75	5.00	5.25	0.187	0.197	0.207
e		0.50BSC			0.020BSC	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00 REF			0.039 REF	

Notes‥

1. CONTROLLING DIMENSION‥ MILLIMETER(mm).
2. REFERENCE DOCUMENTL‥ JEDEC MS-26.

Figure 36. Package Dimension

14. Ordering Information

Table 276. Ordering Information

Part Number	Package	Status
CM7104	48-Pin LQFP, 7mm x 7mm (Tray)	Mass Production

C-MEDIA ELECTRONICS INC.

6F., 100, Sec. 4, Civil Boulevard, Taipei, Taiwan 106 R.O.C.
TEL‥ +886-2-8773-1100
FAX‥ +886-2-8773-2211
E-MAIL‥ sales@cmedia.com.tw