CM7120

Hi-Fi Audio Digital Signal Processor SOC with Low-Power Audio Codec

Rev. 1.10
Updated: 2021/11/23

Release notes

Revision	Date	Description
0.90	2017/09/08	Initial release
0.91	2017/11/15	Add Multi Function Pin Description
0.92	2018/09/28	Modify Codec Performance
0.93	2019/12/11	Add Register table and Electrical characteristics
1.00	2020/02/26	Formal Release
1.10	2021/11/23	Typo correction Add signal timing of Slave SPI I/F

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1. General Description

The CM7120 is a highly-integrated Audio DSP and CODEC Hub system. It combines advanced big and little DSP architecture with a high-performance and flexible CODEC hub, making it ideal for a wide range of mobile systems, such as Smartphone, Tablet, and Headset devices.

The CM7120 integrates two DSP cores with extensive memory resources. Given the advanced big and little DSP architecture, Tensilica HiFi-3 DSP core can support complicated signal processing applications with 300MIPS speed. Tensilica HiFi Mini DSP core can support light and ultra-low power applications, such as voice trigger and voice command. Given that Tensilica HiFi-3 and Mini DSP cores are widely used by many third-party software developers, it makes CM7120 create an extensive wide software reference design ecosystem, including multi-microphone advanced voice processing (NS, AEC,…etc.), voice trigger, command and high-quality, well-known branding audio post-processing.
The CM7120 integrates various method of the DSP code loading from SPI, I2S, UART and JTAG interface and supports auto code loading from external flash memory. Its fully-flexible digital mixing and routing with asynchronous sample rate converter (ASRC) supports the DSP core for wide use case flexibility.

Five digital audio interfaces are provided, supporting I^2S/PCM/TDM audio formats. Four differential analog microphone inputs and up to eight digital microphone inputs can accept audio signals from multiple microphone or line input sources.

The CM7120 features a low power cap-free Class-G headphone amplifier. It consumes low power during playback with 114dB SNR performance, providing mobile system longer battery life under Hi-Fi listening experience.

Mono Receiver amplifier provides 100mW/16Ω or 32Ω with 3.3V supply or 3.6V~5V to 3.3V embedded LDO power source and high SNR, THD+N and good PSRR on GSM 217Hz.

The CM7120 also combines a variety of low-power fixed-function signal processing components. The advanced multiband DRC (Dynamic Range Control) enables further digital audio processing capabilities on playback or record paths. Advanced DRC function comprises multi-section and multi-band parts, ensuring signal level maintenance, maximizes loudness, and prevents audio clipping and speaker damage. The 22-band parametric EQ consists of 11-band EQ for each L/R playback path. Each bands of EQ can be programmed independently to compensate frequency response of L/R speakers, and to meet various user preferences. An independent 12-band parametric Equalizer consists of 6-band EQ for each L/R channel on the record path, for compensating the frequency response of microphone/line inputs.

The CM7120 individual blocks are all design for power efficient target, helping devices to achieve long time playback, record, voice talk…etc. cases. The CM7120 is supplied by a small WLCSP package, ideal for mobile system design.

2. Feature

2.1. DSP and Digital Features:

- **Tensilica Hi-Fi 3 and Hi-Fi Mini DSP Cores**
  - Hi-Fi 3, 300MIPS
    128KByte IRAM
    128KByte DRAM
  - Hi-Fi Mini, 50MIPS
    40KByte IRAM
    80KByte DRAM
  - 192KByte SRAM for Hi-Fi 3 and Hi-Fi Mini DSPs sharing
  - Watch dog function
  - Support DSP wake-up by I^2C/SPI command
  - Firmware code loading by SPI I/F with CRC function
- **Auto Load DSP Code from External Flash Memory through SPI**
- **Five 8~32bits / 8kHz ~ 192kHz I^2S/PCM/TDM Interfaces**
  - Two I^2S/PCM/TDM interface with ASRC function
  - Three I^2S/PCM interface with ASRC function
- **UART Interface**
  - Support I/Os: RTS# / CTS# / Tx / Rx 4 Pins
  - Baud Rate up to 5Mbps
- **S/PDIF-In support up to 24bit Format and 192KHz Rate**
- **I^2C Control Interface**
  - 1 Slave Mode I^2C Control Interface (Up to 2MHz Clock Rate)
  - 3 Master Mode I^2C Control Interfaces (Up to 2MHz Clock Rate)
- **SPI Control Interface**
  - 1 Slave Mode SPI Control Interface for DSP firmware code loading (Up to 30MHz Clock Rate)
  - 2 Master Mode SPI Control Interfaces (Up to 2MHz Clock Rate)
- **Two Independent PDM Interfaces**
  - For External PDM Amp
  - 4 Channels Playback simultaneously
- **Support 4 stereo digital microphone interfaces for 8-CH recording**
  - Independent digital microphone clock output (DMIC1/2/3/4_CLK)
  - Dynamic DMIC clock on/off function for saving power at VAD mode
- **Support SPI Flash Controller (Up to 30MHz clock rate)**
  - Support 24-bits or 32-bits address length
- **Configurable Multi-band Parametric Equalizer (EQ)**
  - 11+11 bands for DAC L/R path (2*LPF + 3*HPF + 5*BPF + 1*Biquad)
  - 6+6 bands for ADC L/R path (1*LPF + 1*HPF + 4*BPF)
  - Mono DAC/ADC EQ mode for power saving
- **DRC**
  - Three-bands DRC with crossover filter for playback path
  - Dedicated DRC for DAC playback path
  - Dedicated DRC for ADC record path
  - Complement with Front-end Analog PGA for record path
- **VAD (Voice Active Detection) with internal 32K memory**
  - Flexible buffer read point control for reduce key phrase detection latency
  - Human Pitch Detection to avoid false alarm
- **Sidetone Generator**
- **Signal Generator for Vibrator**
- **Power Key Press Detection for avoiding pop noise when system hang up**

2.2. Analog Features:

- **Stereo Headphone Output without DC Blocking Capacitors**
  - SNR=114dBA (RL=32 Ohm, HPO=25mW, 20 ~ 20kHz)
  - DNR = 108dBA (Input=-60dBFS, RL=32 Ohm, HPO=25mW, 20 ~ 20kHz)
  - THD+N = -93dB (RL=32 Ohm, HPO=20mW, 20 ~ 20kHz)
  - FSOV=1Vrms (RL=32 Ohm, 20 ~ 20kHz)
  - Crosstalk < -100dB (32Ohm, 1kHz)
  - PSRR > 80dB (Vripple=100mVrms, 20~5kHz)

  Impedance sensing for headphone output
  - Independent detection for L-CH and R-CH of headphone device
  - Support 10 steps impedance sensing (0 ~ 8ohm / 9~23ohm / 24~41ohm / 42~75ohm / 76~150ohm / 151~450ohm / 451~1000ohm / 1000 ~ 5kohm / 5kohm ~ 50kohm / >50kohm (Floating State))
  - Auto mapping the adaptable gain for HP FSOV by impedance sensing results

  Headphone de-pop function
  - Offset level <= 100uV
- **Stereo Single-End or Differential Line Output Port**
  - SNR = 114dBA (RL=32 Ohm, 20 ~ 20kHz)
  - DNR = 101dBA (Input=-60dBFS, RL=32 Ohm, 20 ~ 20kHz)
  - THD+N = -97dB (RL=32 Ohm, 20 ~ 20kHz)
  - FSOV >= 1Vrms
  - Crosstalk < -80dB (Loading>=600 Ohm, 20 ~ 20kHz)
- **Mono Differential Receiver Amp Output**
  - Noise level < 8uV (16Ohm, 20 ~ 20kHz)
  - 50mW (VDD=3.3V, THD+N < 0.01%, 16Ohm, Differential)
  - 5mW (VDD=3.3V, THD+N < 0.01%, 16Ohm, Differential)
  - 100mW (VDD=3.3V, THD+N < 0.03%, 16Ohm, Differential)
  - 104mW (VDD=3.3V, THD+N < 5%, 32Ohm, Differential)
  - 115mW (VDD=3.3V, THD+N < 10%, 16Ohm, Differential)
  - PSRR >= 80dB (Vripple = 100mVrms, 20 ~ 5KHz)

  Mono Receiver Amp de-pop function
  - Offset level <= 100uV
- **4 Analog Input Ports Support 4 CH Analog MIC Recording**
  - Differential/Single-End analog microphone inputs with boost pre-amplifiers and low noise microphone bias
  - SNR=100dBA (single-ended/differential mode, 0dB gain, Vref=FSIV, 20 ~ 20kHz)
  - THD+N=-94dB (single-ended/differential mode, 0dB gain, Vref=FSIV, 20 ~ 20kHz)
  - THD+N=-80dB (single-ended/differential mode, 20dB gain, Vref=FSIV, 20 ~ 20kHz)
  - THD+N=-75dB (single-ended/differential mode, 40dB gain, Vref=FSIV, 20 ~ 20kHz)
  - Boost gain range: -12dB ~ +39.75dB with 0.75dB/step
- **Headphone or Handset Detection Function**
  - One pin to support microphone detection
- **MICBIAS**
  - MICBAS1 for Headset MIC, Adjustable Output Voltage (2.3V/2.5V/2.7V)
  - MICBAS2 and MICBIAS3 for AMEMS MIC, Adjustable Output Voltage (1.8V/1.9V/2.0V/2.7V)
  - High PSRR and Low Noise
- **Three inside PLLs with Wide Range Clock Input (For Tensilica DSP and Codec)**
- **Multi-Buttons Detection**

  4 Buttons Detection
  - Button1 Resistance Range support 0~70 Ohm (The value is parallel with R_{MIC})
  - Button2 Resistance Range support 110~180 Ohm (The value is parallel with R_{MIC})
  - Button3 Resistance Range support 210~290 Ohm (The value is parallel with R_{MIC})
  - Button4 Resistance Range support 360~680 Ohm (The value is parallel with R_{MIC})

  3 Buttons Detection
  - Up Button Resistance Range support 150~280 Ohm (The value is parallel with R_{MIC})

- Center button Resistance Range support 0~50 Ohm (The value is parallel with R_{MIC})
- Down Button Resistance Range support 550~650 Ohm (The value is parallel with R_{MIC})

3. System Applications

- Smartphone
- Tablet
- Wired/Wireless Gaming Headset Devices
- Karaoke application

4. Function Block and Mixer Path

4.1. Function Block

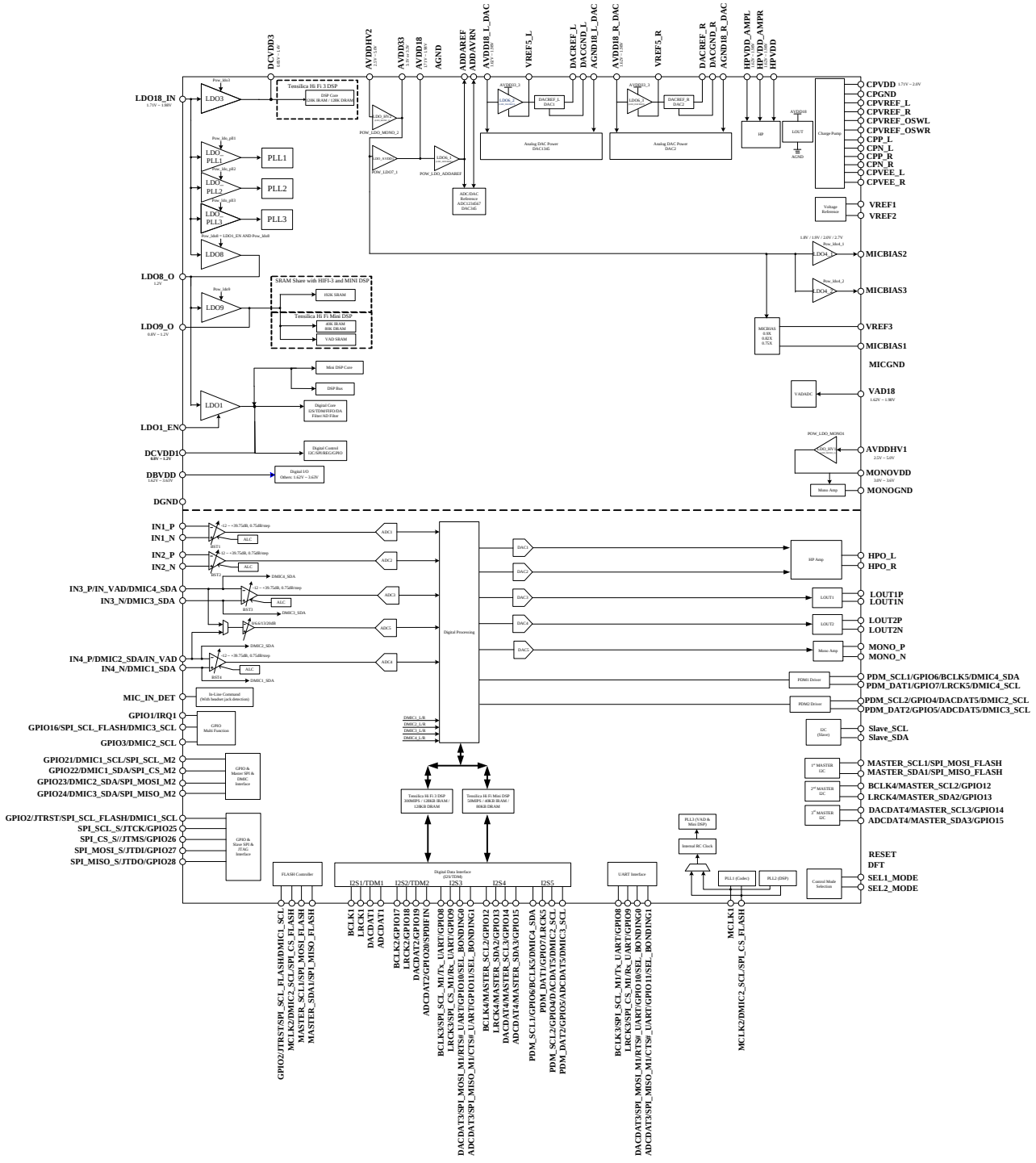


Figure 1. Function Block

4.2. Audio Mixer Path

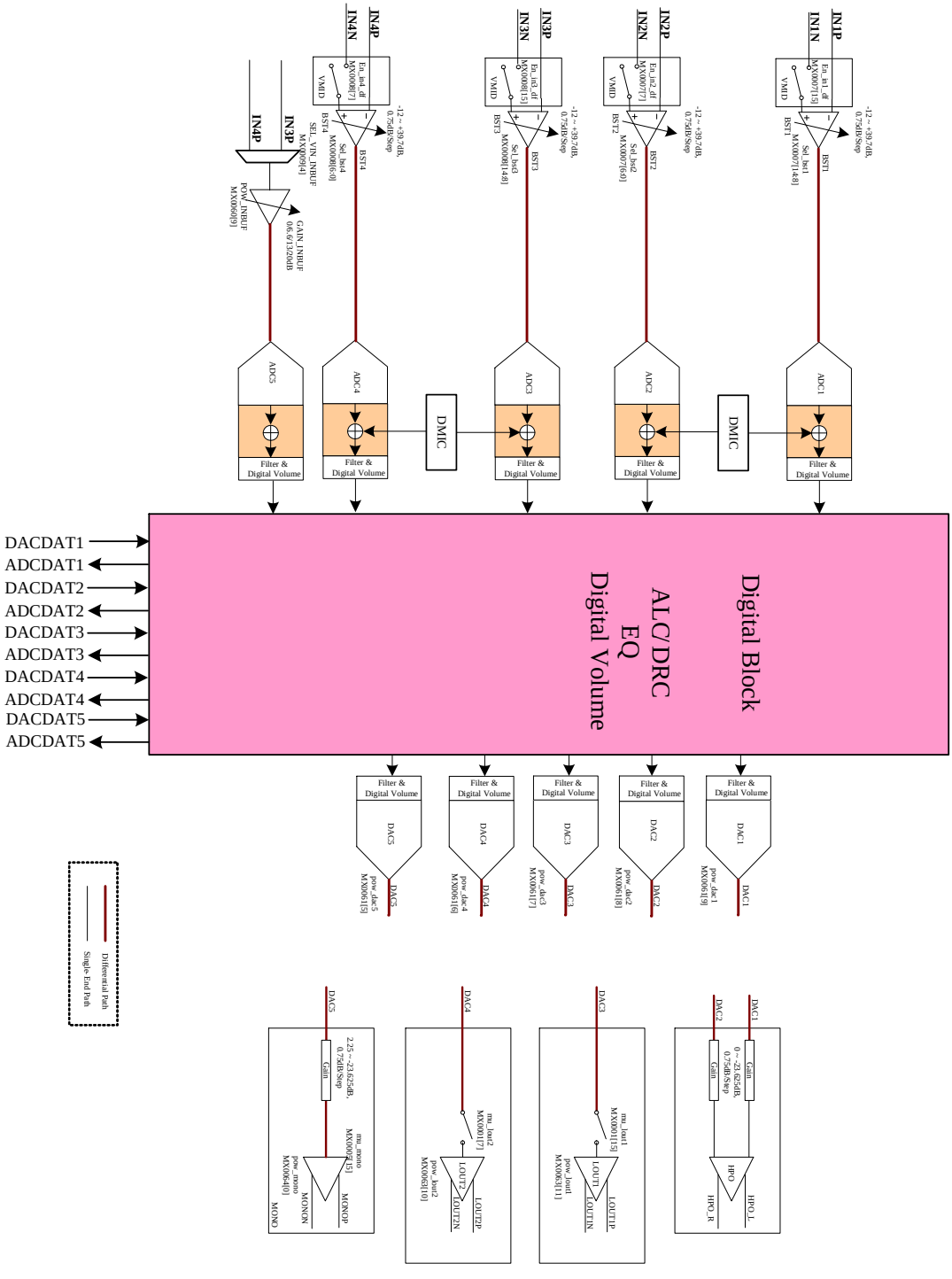


Figure 2. Analog Mixer Path

4.3. Digital Mixer Path

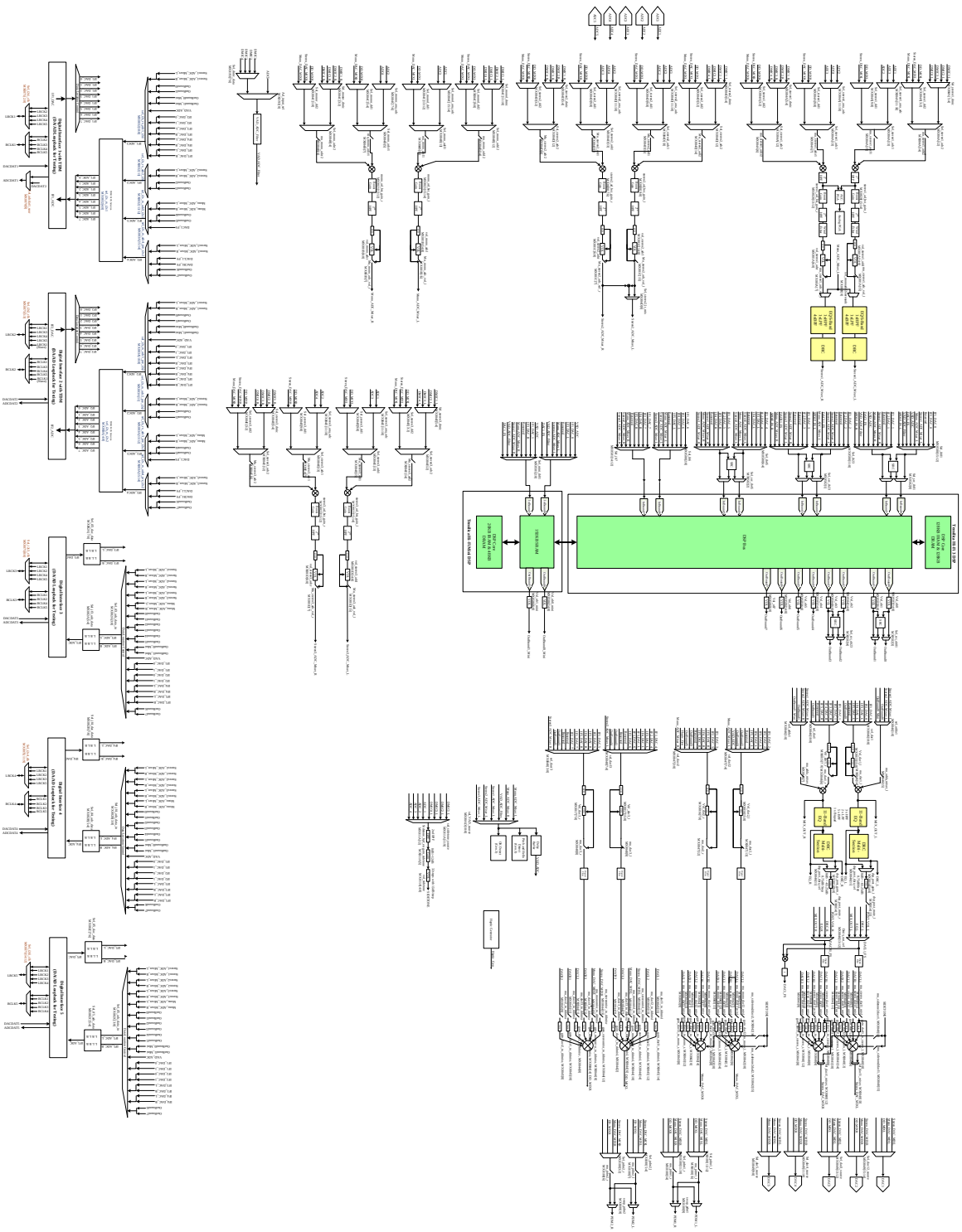
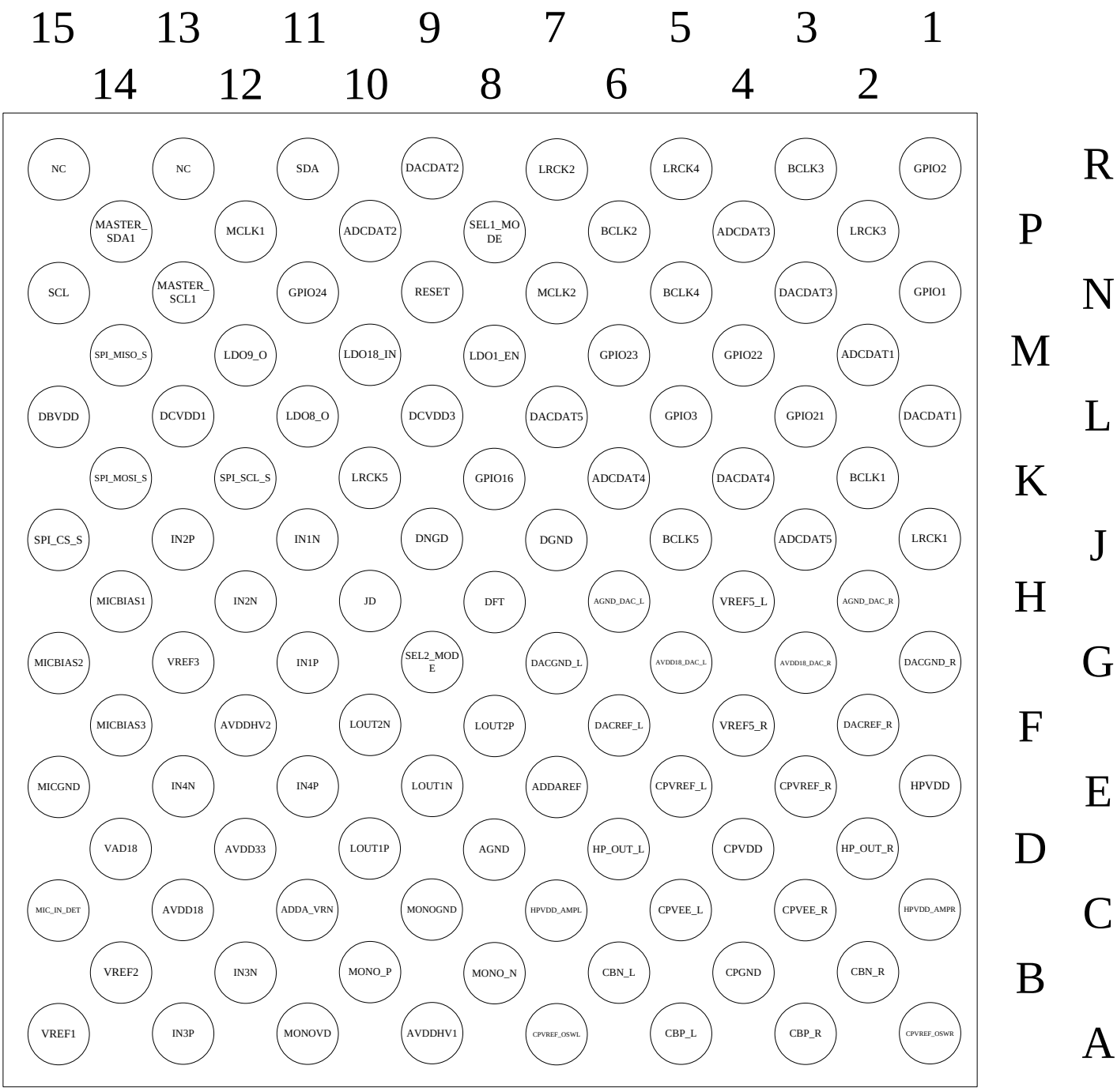


Figure 3. Digital Mixer Path

5. Pin Assignments



CM7120 WLCSP 113 Ball (Bottom View)

Figure 4. Pin Assignments

6. Pin Descriptions

6.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
LRCK1	I/O	J1	1st I2S interface synchronous signal	Master: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Slave: Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD) Default Status: Input Type (Floating) Initial State Control by MX0640[15] (Pull-Up) and MX0640[14] (Pull-Down)
BCLK1	I/O	K2	1st I2S interface serial bit clock	Master: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Slave: Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD) Default Status: Input Type (Floating) Initial State Control by MX0640[15] (Pull-Up) and MX0640[14] (Pull-Down)
ADCDAT1	O	M2	1st I2S interface serial data output	V_{OL}=0.1*DBVDD, V_{OH}=0.9*DBVDD Default Status: Output Type (Low)
DACDAT1	I	L1	1st I2S interface serial data input	Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD) Default Status: Input Type (Floating) Initial State Control by MX0640[15] (Pull-Up) and MX0640[14] (Pull-Down)
GPIO1/IRQ	I/O	N1	Multi-function pin (Table 12): GPIO function Interrupt output	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0640[4] (Pull-Up) and MX0640[3] (Pull-Down)
GPIO2/JTRST/SPI_SCL_FLASH/DMIC1_SCL	I/O	R1	Multi-function pin (Table 13): GPIO function JTAG test logic reset SPI serial clock for flash boot memory 1st DMIC Clock	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0640[2] (Pull-Up) and MX0640[1] (Pull-Down)
GPIO3/DMIC2_SCL	I/O	L5	Multi-function pin (Table 14): GPIO function 2nd DMIC Clock	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0641[15] (Pull-Up) and MX0641[14] (Pull-Down)
GPIO4/PDM_SCL2/DACDAT5/DMIC2_SCL	I/O	L7	Multi-function pin (Table 15): GPIO function 2nd DMIC Clock 2nd PDM serial clock 5th I2S interface serial data input	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0641[13] (Pull-Up) and MX0641[12] (Pull-Down)

Name	Type	Pin	Description	Characteristic Definition
GPIO5/PDM_DAT2/ADCDAT5/DMIC3_SCL	I/O	J3	Multi-function pin (Table 16): GPIO function 3rd DMIC Clock 2nd PDM serial data 5th I2S interface serial data output	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0641[11] (Pull-Up) and MX0641[10] (Pull-Down)
GPIO6/PDM_SCL1/BCLK5/DMIC4_SDA	I/O	J5	Multi-function pin (Table 17): GPIO function 4th DMIC data 1st PDM serial clock 5th I2S interface serial bit clock	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0641[10] (Pull-Up) and MX0641[9] (Pull-Down)
GPIO7/PDM_DAT1/LRCK5/DMIC4_SCL	I/O	K10	Multi-function pin (Table 18): GPIO function 4th DMIC clock 1st PDM serial data 5th I2S interface serial synchronous signal	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0641[7] (Pull-Up) and MX0641[6] (Pull-Down)
GPIO8/BCLK3/SPI_SCL_M/UART_TX	I/O	R3	Multi-function pin (Table 19): GPIO function 3rd I2S interface serial bit clock Master SPI serial clock UART serial data transmit	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0641[5] (Pull-Up) and MX0641[4] (Pull-Down)
GPIO9/LRCK3/SPI_CS_M1/UART_RX	I/O	P2	Multi-function pin (Table 20): GPIO function 3rd I2S interface synchronous signal Master SPI chip select UART serial data receive	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0641[3] (Pull-Up) and MX0641[2] (Pull-Down)
GPIO10/DACDAT3/SPI_MOSI_M1/UART_#RTS/SEL_BONDING0	I/O	N3	Multi-function pin(Table 21): GPIO function 3rd I2S interface serial data input 1st Master SPI MOSI UART request to send handshaking signal Hardware ID select pin	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0641[1] (Pull-Up) and MX0641[0] (Pull-Down)
GPIO11/ADCDAT3/SPI_MISO_M1/UART_#CTS/SEL_BONDING1	I/O	P4	Multi-function pin (Table 22): GPIO function 3rd I2S interface serial data output 1st Master SPI MISO UART clear to send handshaking signal Hardware ID select pin	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0642[15] (Pull-Up) and MX0642[14] (Pull-Down)

Name	Type	Pin	Description	Characteristic Definition
GPIO12/BCLK4/ MASTER_SCL2	I/O	N5	Multi-function pin (Table 23): GPIO function 4th I2S interface serial bit clock 2nd Master I2C serial clock	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0642[13] (Pull-Up) and MX0642[12] (Pull-Down)
GPIO13/LRCK4/ MASTER_SDA2	I/O	R5	Multi-function pin (Table 24): GPIO function 4th I2S interface synchronous signal 2nd Master I2C serial data	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0642[11] (Pull-Up) and MX0642[10] (Pull-Down)
GPIO14/DACDAT 4/MASTER_SCL3	I/O	K4	Multi-function pin (Table 25): GPIO function 4th I2S interface serial data input 3rd Master I2C serial clock	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0642[9] (Pull-Up) and MX0642[8] (Pull-Down)
GPIO15/ADCDAT 4/MASTER_SDA3	I/O	K6	Multi-function pin (Table 26): GPIO function 4th I2S interface serial data output 3rd Master I2C serial data	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0642[7] (Pull-Up) and MX0642[6] (Pull-Down)
GPIO16/SPI_SCL _FLASH/DMIC3_ SCL/PRESS_DET	I/O	K8	Multi-function pin (Table 27): GPIO function SPI serial clock for flash boot memory 3rd DMIC serial clock	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Output Type (Low)
GPIO17/BCLK2	I/O	P6	Multi-function pin (Table 28): GPIO function 2nd I2S interface bit clock	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0642[3] (Pull-Up) and MX0642[2] (Pull-Down)
GPIO18/LRCK2	I/O	R7	Multi-function pin (Table 29): GPIO function 2nd I2S interface synchronous signal	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0642[1] (Pull-Up) and MX0642[0] (Pull-Down)
GPIO19/DACDAT 2	I/O	R9	Multi-function pin (Table 30): GPIO function 2nd I2S interface serial data input	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0643[15] (Pull-Up) and MX0643[14] (Pull-Down)

Name	Type	Pin	Description	Characteristic Definition
GPIO20/ADCDAT2/SPDIFIN	I/O	P10	Multi-function pin (Table 31): GPIO function 2nd I2S interface serial data output SPDIF Input data	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0643[13] (Pull-Up) and MX0643[12] (Pull-Down)
GPIO21/DMIC1_SCL/SPI_SCL_M2	I/O	L3	Multi-function pin (Table 32): GPIO function 1st DMIC serial clock 2nd Master SPI serial clock	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0643[11] (Pull-Up) and MX0643[10] (Pull-Down)
GPIO22/DMIC1_SDA/SPI_CS_M2	I/O	M4	Multi-function pin (Table 33): GPIO function 1st DMIC serial data 2nd Master SPI chip select	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0643[9] (Pull-Up) and MX0643[8] (Pull-Down)
GPIO23/DMIC2_SDA/SPI_MOSI_M2	I/O	M6	Multi-function pin (Table 34): GPIO function 2nd DMIC serial data 2nd Master SPI MOSI	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0643[7] (Pull-Up) and MX0643[6] (Pull-Down)
GPIO24/DMIC3_SDA/SPI_MISO_M2	I/O	N11	Multi-function pin (Table 35): GPIO function 3rd DMIC serial data 2nd Master SPI MISO	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0643[5] (Pull-Up) and MX0643[4] (Pull-Down)
GPIO25/SPI_SCL_S/JTCK	I/O	K12	Multi-function pin (Table 36): GPIO function Slave SPI serial clock JTAG test clock	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0643[3] (Pull-Up) and MX0643[2] (Pull-Down)
GPIO26/SPI_CS_S/JTMS	I/O	J15	Multi-function pin (Table 37): GPIO function Slave SPI chip select JTAG test mode select	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0644[15] (Pull-Up) and MX0644[14] (Pull-Down)
GPIO27/SPI_MOSI_S/JTDI	I/O	K14	Multi-function pin (Table 38): GPIO function Slave SPI MOSI JTAG test data input	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD Default Status: Input Type (Floating) Initial State Control by MX0644[13] (Pull-Up) and MX0644[12] (Pull-Down)

<table>
<tr><th>Name</th><th>Type</th><th>Pin</th><th>Description</th><th>Characteristic Definition</th></tr>
<tr><td>GPIO28/SPI_MISO_S/JTDO</td><td>I/O</td><td>M14</td><td>Multi-function pin (Table 39):
GPIO function
Slave SPI MISO
JTAG test data output</td><td>Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD
Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD
Default Status: Output Type (Low)</td></tr>
<tr><td>SCL</td><td>I</td><td>N15</td><td>Slave I^2C interface serial clock</td><td>Open Drain</td></tr>
<tr><td>SDA</td><td>I/O</td><td>R11</td><td>Slave I^2C interface serial data</td><td>Open Drain</td></tr>
<tr><td>MASTER_SCL1/SPI_MOSI_FLASH</td><td>O</td><td>N13</td><td>Multi-function pin (Table 41):
1st Master I^2C interface serial clock
SPI MOSI for flash boot memory</td><td>Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD
Default Status: Output Type (Low)</td></tr>
<tr><td>MASTER_SDA1/SPI_MISO_FLASH</td><td>I/O</td><td>P14</td><td>Multi-function pin (Table 42):
1st Master I^2C interface serial data
SPI MISO for flash boot memory</td><td>Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD
Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD
Default Status: Input Type (Floating)
Initial State Control by MX0640[9] (Pull-Up) and MX0640[8] (Pull-Down)</td></tr>
<tr><td>MCLK1</td><td>O</td><td>P12</td><td>1st Master clock input</td><td>Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD
Default Status: Input Type (Floating)
Initial State Control by MX0640[13] (Pull-Up) and MX0640[12] (Pull-Down)</td></tr>
<tr><td>MCLK2/DMIC2_SCL/SPI_CS_FLASH</td><td>I/O</td><td>N7</td><td>Multi-function pin (Table 40):
2nd Mater clock input
2nd DMIC serial clock
SPI chip select for flash boot memory</td><td>Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD
Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD
Default Status: Output Type (Low)</td></tr>
<tr><td>SEL1_MODE</td><td>I</td><td>P8</td><td rowspan="2">Control Interface Selection
<table><tr><th>SEL2_MODE</th><th>SEL1_MODE</th><th></th></tr><tr><td>Low</td><td>Low</td><td>I2C</td></tr><tr><td>Low</td><td>High</td><td>Auto Boot</td></tr><tr><td>High</td><td>Low</td><td>SPI</td></tr><tr><td>High</td><td>High</td><td>NA</td></tr></table></td><td rowspan="2">Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD
Default Status: Input Type (Floating)</td></tr>
<tr><td>SEL2_MODE</td><td>I</td><td>G9</td></tr>
<tr><td>LDO1_EN</td><td>I</td><td>M8</td><td>LDO1 Enable Control
0’b: Disable
1’b: Enable</td><td>Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD
Default Status: Input Type (Floating)</td></tr>
<tr><td>RESET</td><td>I</td><td>N9</td><td>HW Reset Control
0’b: Reset
1’b: Normal Work</td><td>Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD
Default Status: Input Type (Floating)</td></tr>
<tr><td>DFT</td><td>I</td><td>H8</td><td>Digital Scan-Chain test
0’b: Disable
1’b: Entry Digital Test Mode</td><td>Input: Schmitt trigger, V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD
Default Status: Input Type (Floating)</td></tr>
<tr><td colspan="4">-</td><td>Total: 45 Pins</td></tr>
</table>

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
HP_OUT_L	O	D6	Headphone Output L Channel	Analog Output
HP_OUT_R	O	D2	Headphone Output R Channel	Analog Output
LOUT1P	O	D10	1st Line Output Differential Positive Output	Analog Output
LOUT1N	O	E9	1st Line Output Differential Negative Output	Analog Output
LOUT2P	O	F8	2nd Line Output Differential Positive Output	Analog Output
LOUT2N	O	F10	2nd Line Output Differential Negative Output	Analog Output
MONOP	O	B10	MONO Output Differential Positive Output	Analog Output
MONON	O	B8	MONO Output Differential Negative Output	Analog Output
IN1P	I	G11	1st Microphone Differential Positive Input	Analog Input
IN1N	I	J11	1st Microphone Differential Negative Input	Analog Input
IN2P	I	J13	1st Microphone Differential Positive Input	Analog Input
IN2N	I	H12	1st Microphone Differential Negative Input	Analog Input
IN3P	I	A13	1st Microphone Differential Positive Input	Analog Input
IN3N	I	B12	1st Microphone Differential Negative Input	Analog Input
IN4P	I	E11	1st Microphone Differential Positive Input	Analog Input
IN4N	I	E13	1st Microphone Differential Negative Input	Analog Input
MIC_IN_DET	I	C15	Microphone and Push Button Detect Pin	Analog Input
JD	I	H10	Jack Detection Input	Analog Input
-				Total: 17 Pins

6.3. Filter/Reference/Not Connected Pins

Table 3. Filter/Reference/Not Connected Pins

Name	Type	Pin	Description	Characteristic Definition
ADDAREF	R	E7	ADC, DAC3~5 Reference Voltage	4.7uF Capacitor to Analog Ground
DACREF_L	R	F6	DAC1 Reference Voltage	4.7uF Capacitor to Analog Ground
DACREF_R	R	F2	DAC2 Reference Voltage	4.7uF Capacitor to Analog Ground
VREF5_L	R	H4	LDO_DACREF1 Reference Voltage	2.2uF Capacitor to Analog Ground
VREF5_R	R	F4	LDO_DACREF2 Reference Voltage	2.2uF Capacitor to Analog Ground
CBP_L	-	A5	Charge Pump Bucket Capacitor	4.7uF Capacitor to CBN_L
CBN_L	-	B6	Charge Pump Bucket Capacitor	4.7uF Capacitor to CBP_L
CBP_R	-	A3	Charge Pump Bucket Capacitor	4.7uF Capacitor to CBN_R
CBN_R	-	B2	Charge Pump Bucket Capacitor	4.7uF Capacitor to CBP_R
VREF1	R	A15	Analog I/O Reference	4.7uF Capacitor to Analog Ground
VREF2	R	B14	Analog I/O Reference	4.7uF Capacitor to Analog Ground
VREF3	R	G13	MICBIAS Reference Voltage	4.7uF Capacitor to Analog Ground
MICBIAS1	O	H14	MICBIAS Voltage Output	Programmable Analog DC Output with 4mA Driving Capability
MICBIAS2	O	G15	MICBIAS Voltage Output	Programmable Analog DC Output with 4mA Driving Capability
MICBIAS3	O	F14	MICBIAS Voltage Output	Programmable Analog DC Output with 4mA Driving Capability
-				Total: 15 Pins

6.4. Power & Ground Pins

Table 4. Power & Ground Pins Table

Name	Type	Pin	Description	Characteristic Definition
HPVDD_AMPL	P	C7	HP Amp L Channel Power	1.71V ~ 1.98V
HPVDD_AMPR	P	C1	HP Amp R Channel Power	1.71V ~ 1.98V
HPVDD	P	E1	HP Amp Power	1.71V ~ 1.98V
DACGND_L	G	G7	DAC1 Reference Circuit Ground	
DACGND_R	G	G1	DAC2 Reference Circuit Ground	
CPVEE_L	P	C5	Charge Pump L Channel Negative Voltage Output	4.7uF capacitor to analog ground
CPVEE_R	P	C3	Charge Pump R Channel Negative Voltage Output	4.7uF capacitor to analog ground
CPVREF_L	G	E5	HP Amp L Channel Reference Ground	
CPVREF_R	G	E3	HP Amp R Channel Reference Ground	
AVDD18_DAC_L	P	G5	DAC1345 Power	1.71V ~ 1.98V
AVDD18_DAC_R	P	G3	DAC2 Power	1.71V ~ 1.98V
CPVDD	P	D4	Charge Pump Power	1.71V ~ 1.98V
AVDDHV1	P	A9	Internal LDO for MONO Amp Power If AVDDHV1<3.3V, MONOVDD=AVDDHV1 If AVDDHV1>3.3V, MONOVDD=3.3V	2.5V~5V
MONOVDD	P	A11	MONO Amp Power	3.0V~3.6V
ADDA_VRN	G	C11	ADC and DAC3~5 Reference Ground	
AVDD33	P	D12	MICBIAS Power Inter LDO for AVDD18_1 Power	3.0V~3.6V
AVDDHV2	P	F12	Internal LDO for AVDD33 Power	2.5V~5V
AVDD18	P	C13	Analog Power	1.71V ~ 1.98V
VAD18	P	D14	VAD Related Circuits Power	1.71V ~ 1.98V
LDO18_IN	P	M10	Analog and LDO Power	1.71V ~ 1.98V
DBVDD	P	L15	Digital I/O Power	1.71V~3.6V
DCVDD1	P	L13	Codec Core, HIFI-Mini DSP Core Power Supplied by LDO1 or external power source	
DCVDD3	P	L9	HIFI-3 DSP Core Power Supplied by LDO3 or external power source	

LDO9_O	P	M12	Digital Power for SRAM and HIFI-Mini I/DRAM Supplied by LDO9 or External power source	
LDO8_O	P	L11	Digital power for LDO1 and LDO9 Supplied by LDO8 or external power source	
CPVREF_OSWL	G	A7	HP_L Internal Pull Low Switch Ground	
CPVREF_OSWR	G	A1	HP_R Internal Pull Low Switch Ground	
AGND_DAC_L	G	H6	DAC1 Ground	
AGND_DAC_R	G	H2	DAC2 Ground	
MONOGND	G	C9	MONO Amp Ground	
MICGND	G	E15	MICBIAS Ground	
DGND	G	J7	Digital Ground	
DGND	G	J9	Digital Ground	
CPGND	G	B4	Charge Pump Ground	
AGND	G	D8	Analog Ground	
-				Total: 35 Pins

7. Power

There are different power types in CM7120. DBVDD is for digital I/O power, DCVDD1 is for digital core power, DCVDD3 is for DSP power, LDO9_O is for SRAM power, AVDD18 is for analog power, AVDD18_DAC_L/R is for DAC power, CPVDD/HPVDD/HPVDD_AMPL/HPVDD_AMPR is for HP and AVDD33 is for MICBIAS power.

Table 5. Power Supply for Best Performance

Power	**DBVDD**	**LDO18_IN**	**DCVDD1**	**DCVDD3**	**LDO8_O**	**LDO9_O**	**AVDD18**	**MONOVDD**
Setting	1.8V	1.8V	0.9*	1.2*	1.2*	0.9*	1.8V	3.3
Power	**AVDD18_DAC_L**	**AVDD18_DAC_R**	**CPVDD**	**HPVDD**	**HPVDD_AMPL**	**HPVDD_AMPR**	**AVDD_HV1**	**AVDD_HV2**
Setting	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	5V	5V

*DCVDD1, DCVDD3, LDO8_O and LDO9_O is generated by internal LDO, the voltage can be adjusted by loading of DSP.

To prevent all power down leakage, we suggest supply power for each power pin of CM7120 or remove power for all power pin of CM7120.
Case1:

Table 6. Power Supply Condition for Power Down Leakage on Case1

Power	**DBVDD**	**LDO18_IN**	**DCVDD1**	**DCVDD3**	**LDO8_O**	**LDO9_O**	**AVDD18**	**MONOVDD**
Setting	1.8V	1.8V	Off	Off	Off	Off	1.8V	3.3
Power	**AVDD18_DAC_L**	**AVDD18_DAC_R**	**CPVDD**	**HPVDD**	**HPVDD_AMPL**	**HPVDD_AMPR**	**AVDD_HV1**	**AVDD_HV2**
Setting	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	5V	5V

Case2:

Table 7. Power Supply Condition for Power Down Leakage on Case2

Power	**DBVDD**	**LDO18_IN**	**DCVDD1**	**DCVDD3**	**LDO8_O**	**LDO9_O**	**AVDD18**	**MONOVDD**
Setting	Off	Off	Off	Off	Off	Off	Off	Off
Power	**AVDD18_DAC_L**	**AVDD18_DAC_R**	**CPVDD**	**HPVDD**	**HPVDD_AMPL**	**HPVDD_AMPR**	**AVDD_HV1**	**AVDD_HV2**
Setting	Off	Off	Off	Off	Off	Off	Off	Off

7.1. Power Supply On/Off Sequence

To prevent shortly leakage and make sure function work normally, following power on and off sequence are recommended.

Case 1: Normal Load Code by SPI Interface

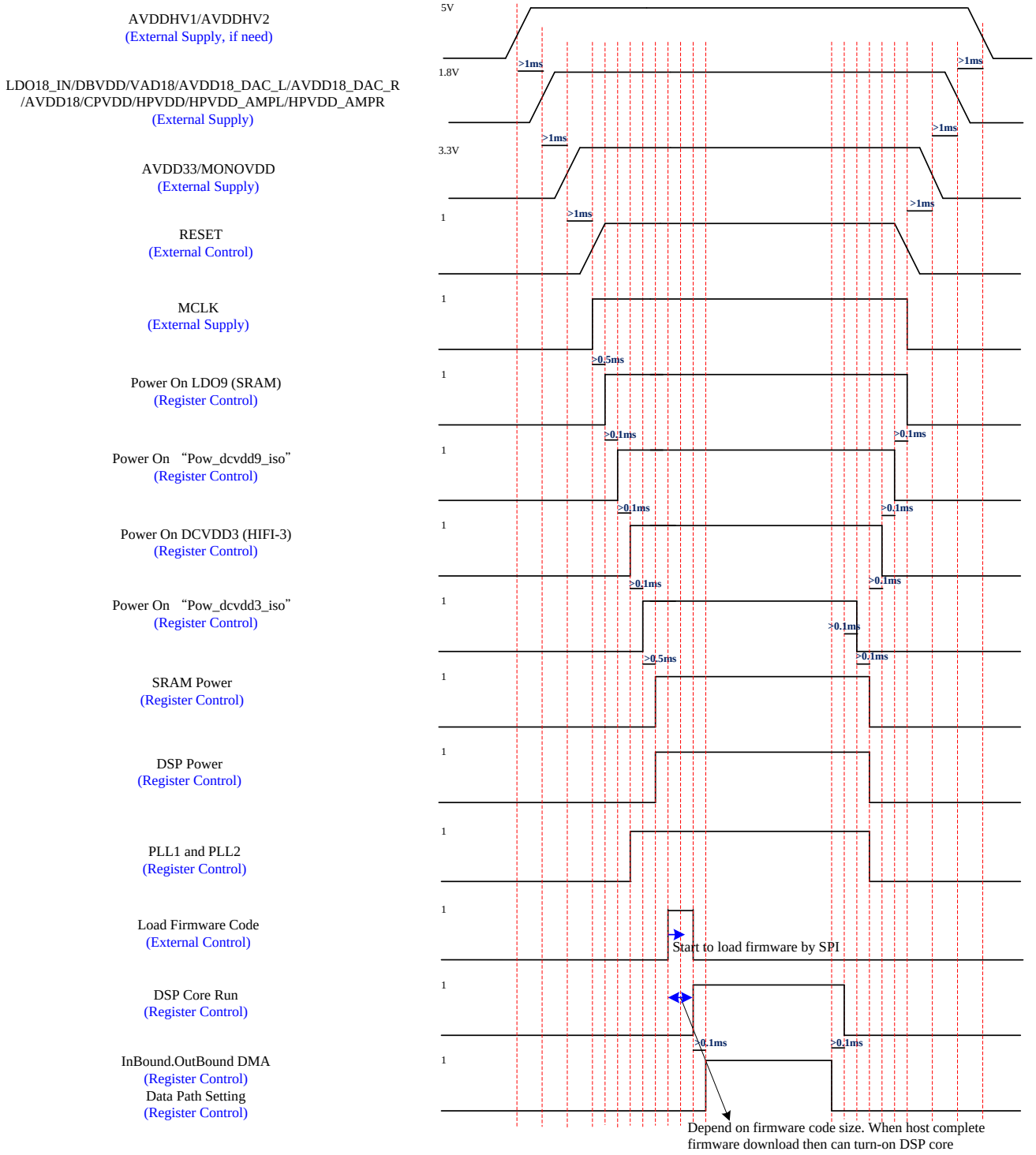


Figure 5. Power On/Off Timing when Normal Load Code by SPI Interface

Case 2: Normal Load Code by SPI Flash

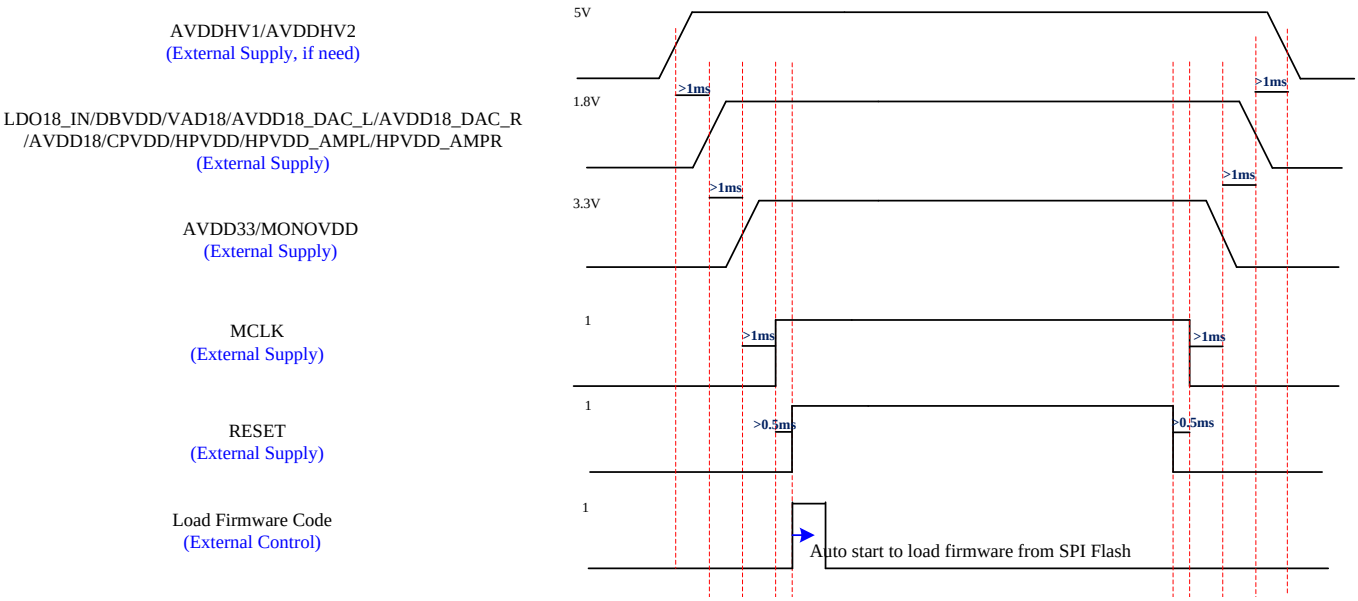


Figure 6. Power On/Off Timing when Normal Load Code by SPI Flash

8. Function Description

8.1. System Connection

8.1.1. Using Battery to Supply

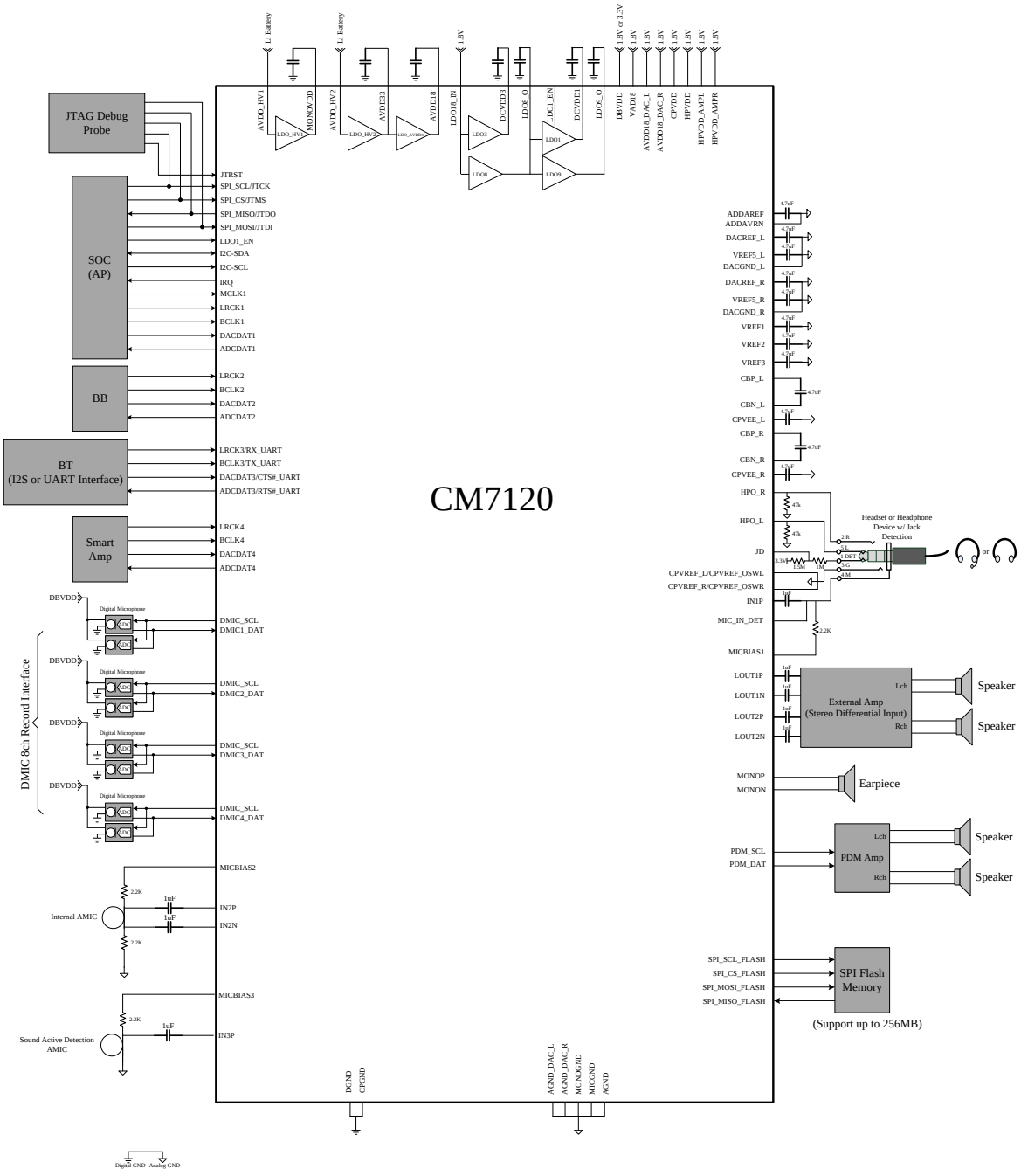


Figure 7. System Connection Using Battery to Supply

8.1.2. Using PMIC to Supply

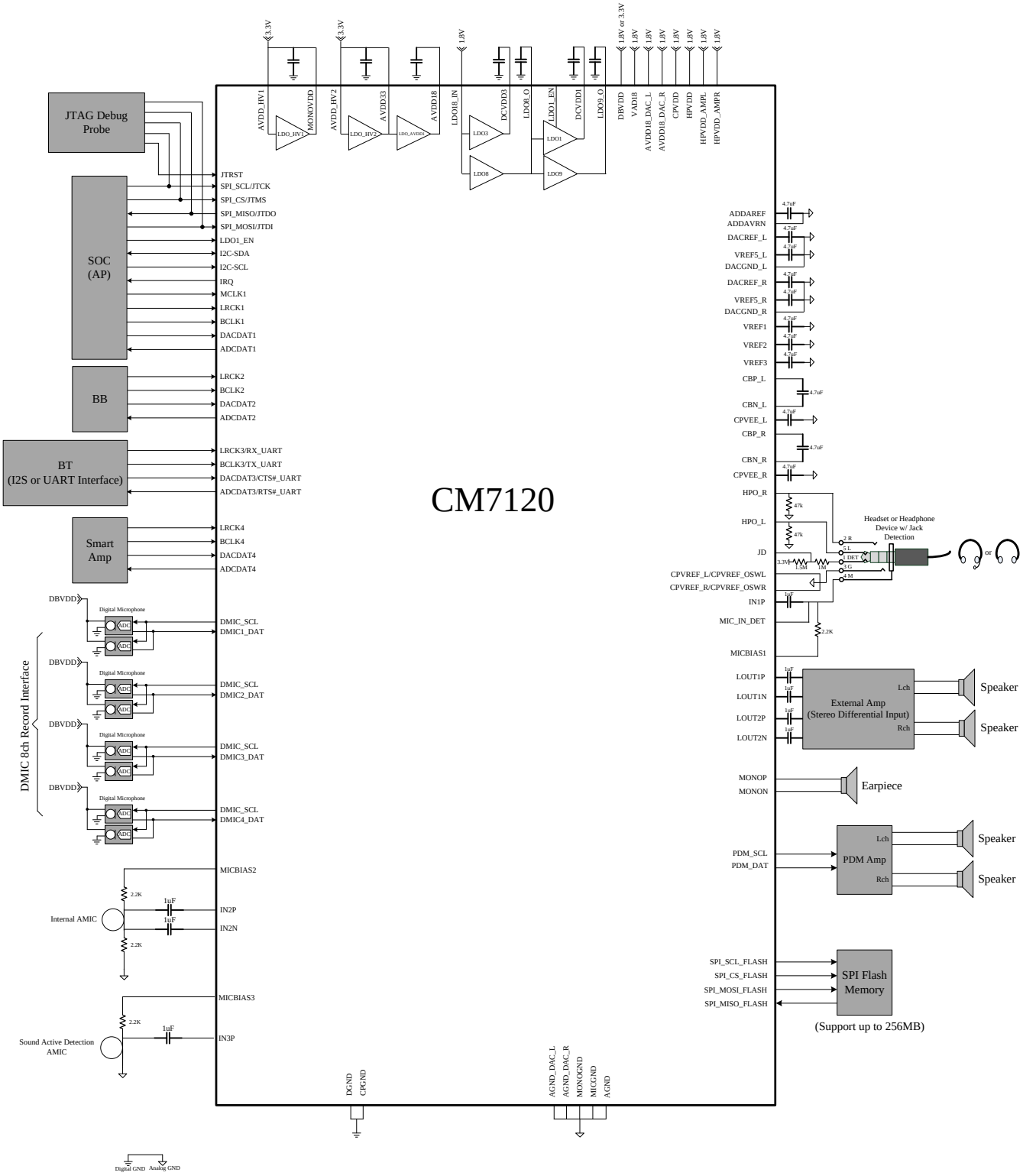


Figure 8. System Connection Using PMIC to Supply

8.2. Reset

There are 2 types of reset operation: power on reset (POR) and register reset.

Table 8. Reset Operation

Reset Type	Trigger Condition	CODEC Response
POR	Monitor digital power supply voltage reach V_{POR}	Reset all hardware logic and all registers to default values.
Register Reset	Write MX-0000h to 0x10ECh	Reset all registers to default values except some specify control registers and logic.

8.2.1. Power On Reset

When powered on, DCVDD passes through the V_{POR} band of the CM7120 (V_{POR_ON} ~V_{POR_OFF}). A power on reset (POR) will generate an internal reset signal (POR reset 'LOW') to reset the whole chip.

Table 9. Power-On Reset Voltage

Symbol	Min	Typical	Max	Unit
V_{POR_ON}	-	0.65	-	V
V_{POR_OFF}	-	0.55	-	V

Note:

1.V_{POR_OFF} must be below V_{POR_ON}

2. $T^oC = 25^oC$

3. When DCVDD is supplied 1.2V

8.2.2. Software Reset

When MX-0000h is wrote to 0x10Ech, all registers become to default value.

8.3. Clock Tree

The clock setting of the CM7120 can be group by function. There are five sections clock tree and the details are shown in the Section 7.3.1 ~ 7.3.5

8.3.1. Codec System Clock Tree

The CM7120 source of the system clock can be selected from MCLK1, MCLK2 or PLL. The clk_sys1 to clk_sys8 can be select as clock source of the DAC/ADC filter.

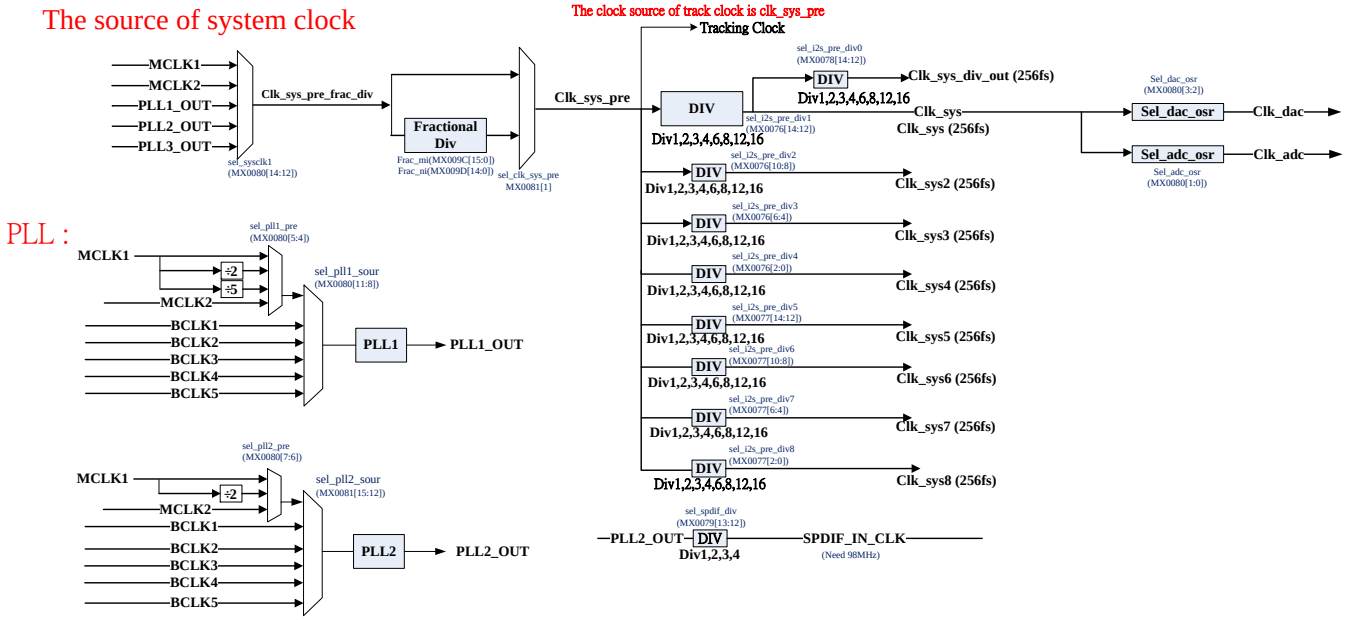


Figure 9. Codec System Clock Tree

8.3.2. ASRC Clock Tree

When enable ASRC (Asynchronous Sample Rate Converter) function, the clock sources from MCLK and BCLK1, BCLK2, BCLK3, BCLK4 and BCLK5 are allowed to be asynchronous. The Cmedia ASRC technology can ensure data accuracy and keep audio performance under clock source asynchronous. The ASRC clock source is also can be selected from each interface (I2S1, I2S2, I2S3, I2S4 or I2S5).

The ASRC Clock

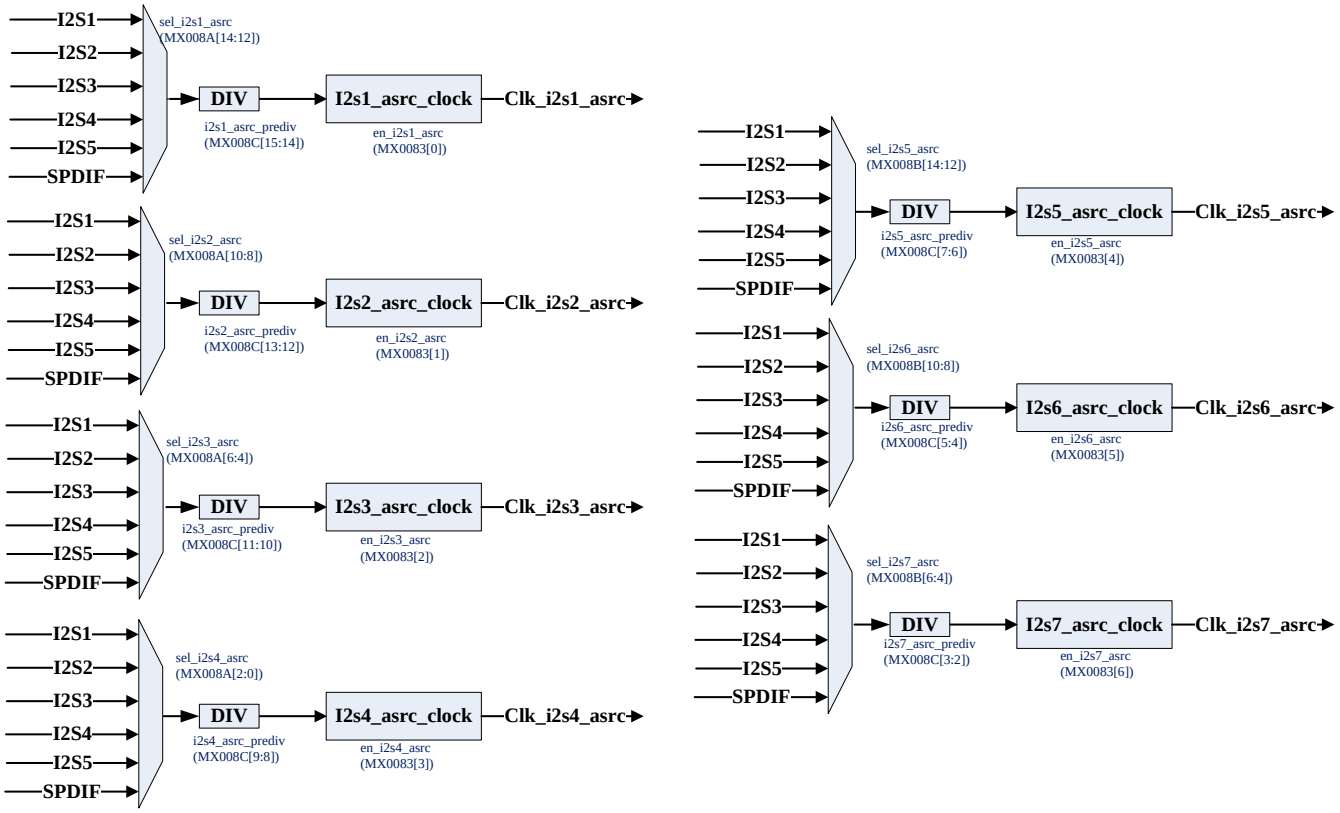


Figure 10. ASRC Tracking Clock Tree

8.3.3. Digital ADC/DAC Filter Clock Tree

The ADC/DAC digital filter clock is from Clock_system. For DAC/ADC stereo/mono digital filter can be selected from Clock_system ~ Clock_system8 or tracking clock clk_i2s1_asrc ~ clk_i2s7_asrc.

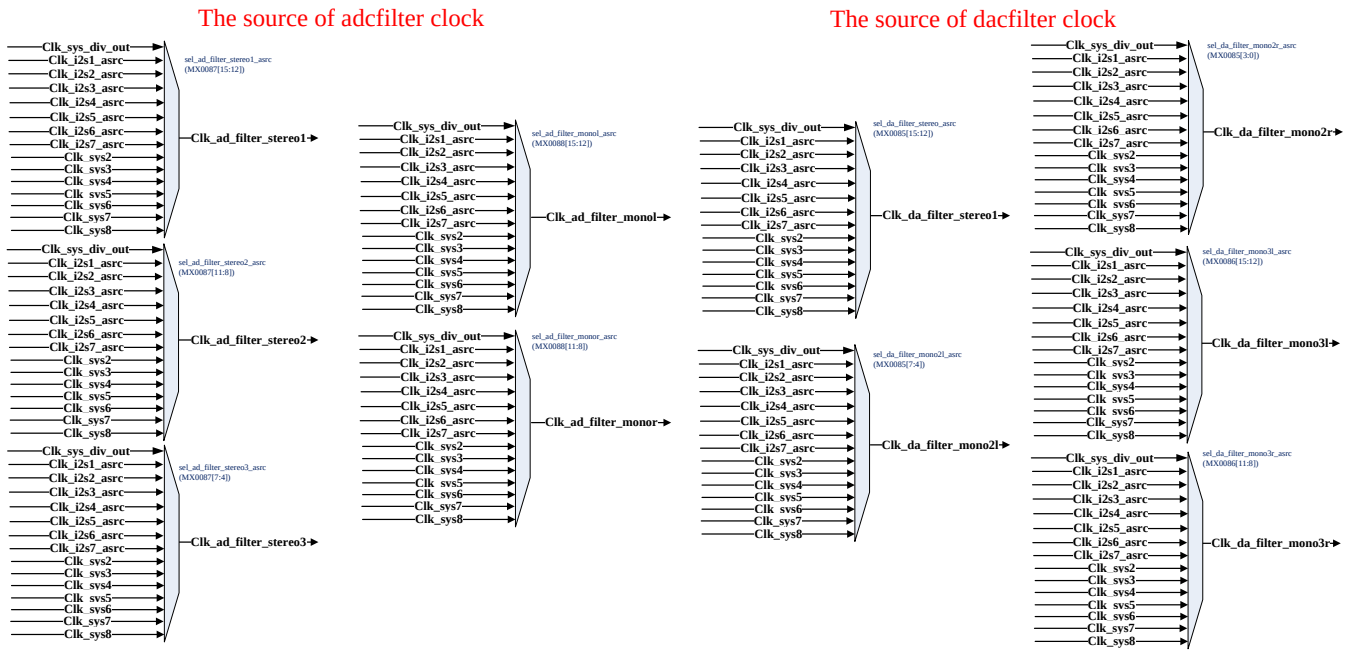


Figure 11. Digtal ADC/DAC Filter Clock Tree

8.3.4. I²S Interface Clock Tree when Master Mode

When I2S1 ~ I2S5 as the master mode interface, the each clock source can be selected from MCLK1, PLL1 or fractional divider.

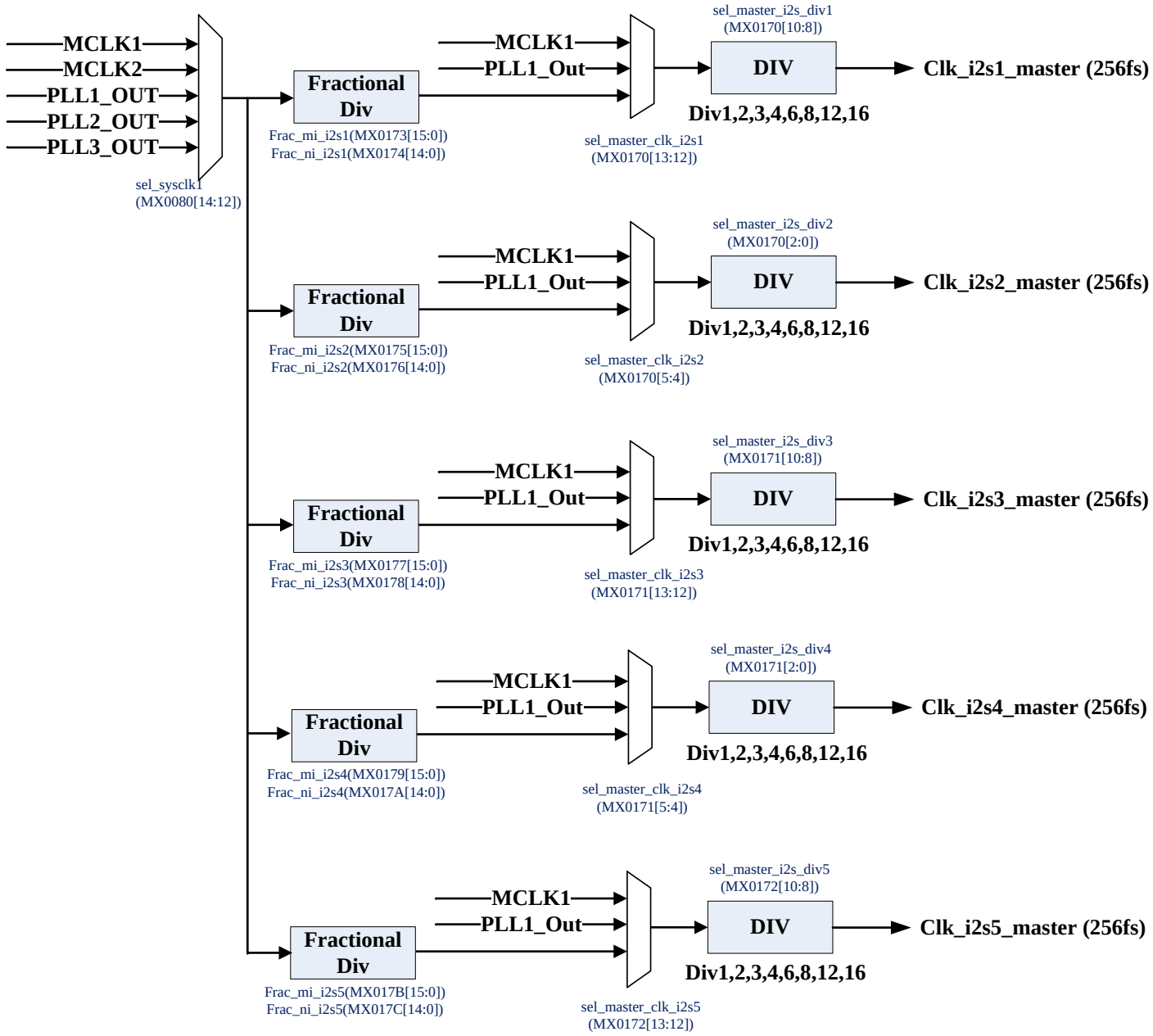
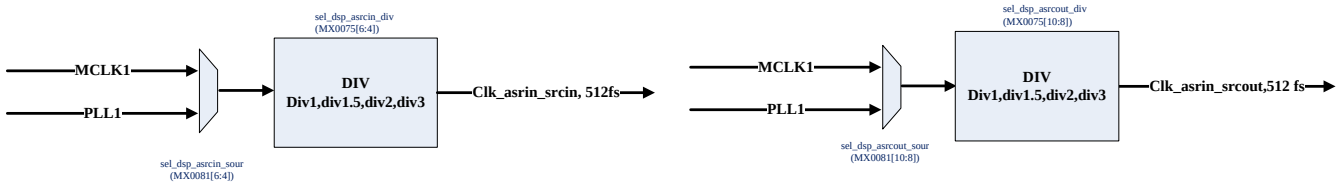


Figure 12. I²S Interface Clock Tree when Master Mode

8.3.5. SRC and Inbound/Outbound Clock Tree

The SRC (Sampling Rate Converter) locate in the front of the inbound and back of the outbound. The clock source of the SRC for the inbound and outbound can be selected to MCLK1 and PLL1.

The source of DSP SRC



Outbond Clock

Clk_dsp_out_fs_sec1 : for outbond0~outbond3

Clk_dsp_out_fs_sec2 : for outbond4-outbond5

Clk_dsp_mini_fs_out : for mini dsp output

In srcout path :

Clk_asrcin_srcout = 2*clk_dsp_out_fs_sec1

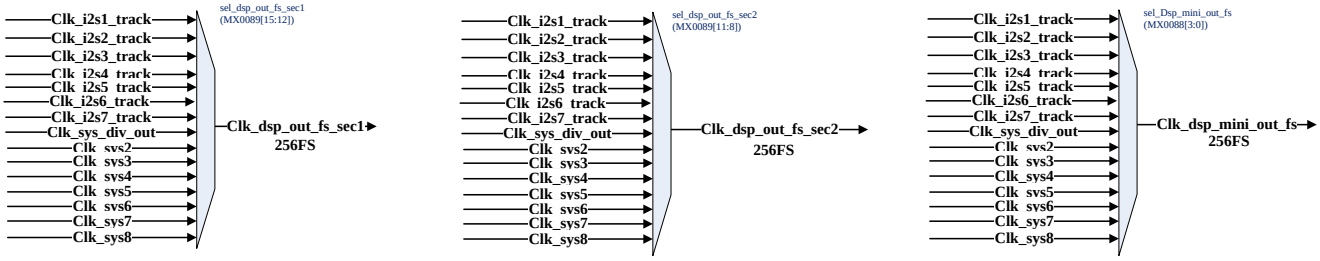


Figure 13. SRC and Inbound/Outbound Clock Tree

8.4. Control Interface Configuration

There are four methods to control CM7120 registers – I2C control interface, SPI control interface and DSP direct to control. In the pure Codec mode, the pin pad_mode_sel2 and pad_mode_sel1 are used to determine which control interface will can control the Codec register.
For DSP control interface, when power on DSP by MX-0065[3], the Codec register control will be controlled by DSP.

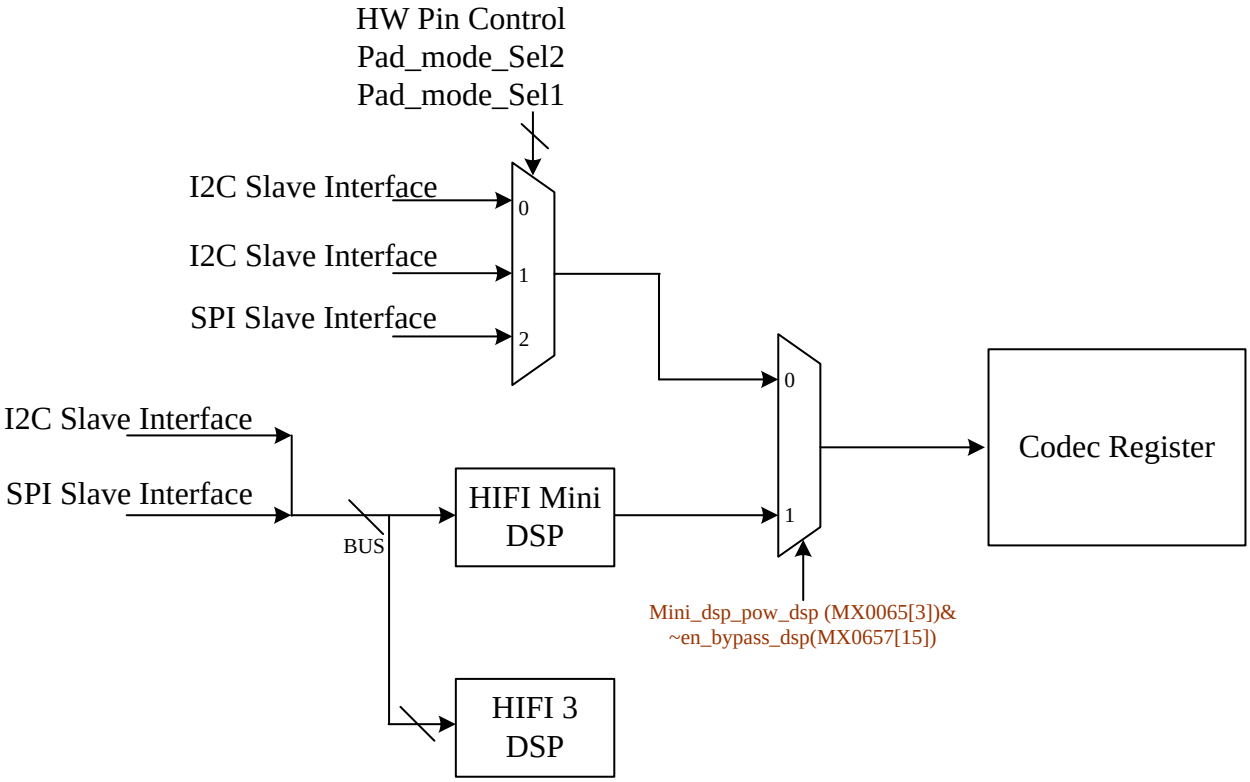


Figure 14. Control Interface Configuration

8.5. I²C Control Interface

I²C is a 2-wire (SCL/SDA) half-duplex serial communication interface, supporting only slave mode. SCL is used for clock and SDA is for data. SCL clock supports up to 400kHz rate and SDA data is a open drain structure. The input has built-in spike filter and can remove less than 50ns spike at SCL and SDA.

8.5.1. Device Address Setting

Device address is 0x2D'h for 7 bits format definition

Table 10. 7 Bits Device Address Setting include the R/W bit (0x2D'h)

(MSB)			BIT			(LSB)
0	1	0	1	1	0	1

Device address is 0x5A'h for 8 bits format definition

Table 11. 8 Bits Device Address Setting include the R/W bit (0x5A'h)

(MSB)			BIT				(LSB)
0	1	0	1	1	0	1	R/W

8.5.2. Complete Data Transfer

Data Transfer over I²C Control Interface

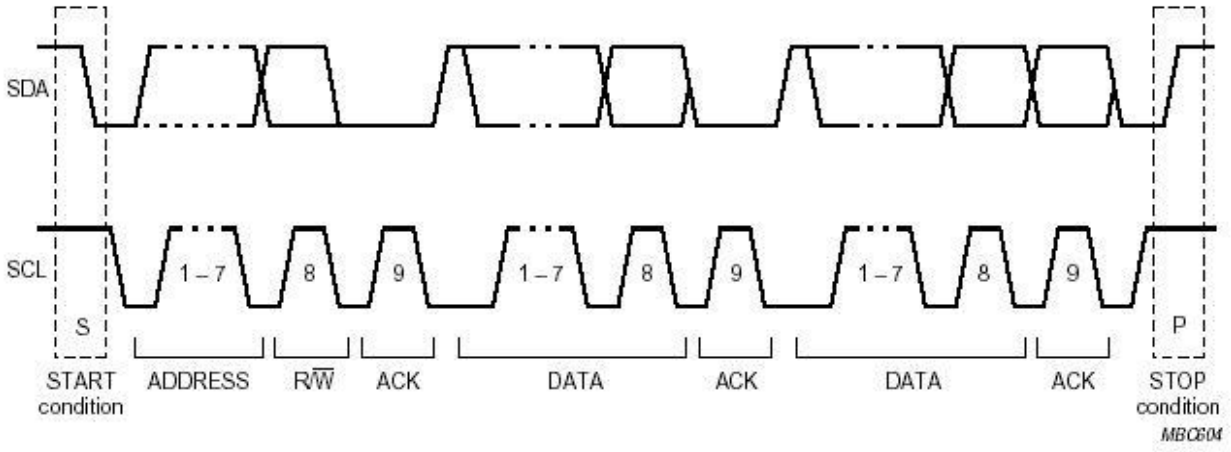
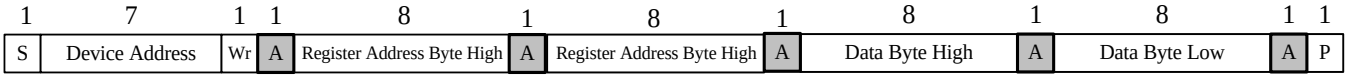
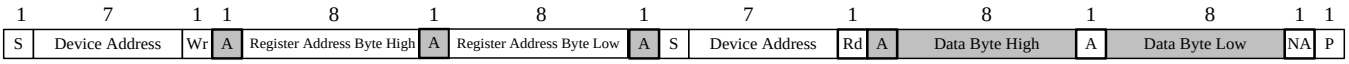


Figure 15. Data Transfer Over I2C Control Interface

16 bits Register Address Write WORD Protocol:



16 bits Register Address Read WORD Protocol:



S: Start Condition

Slave Address: 7-bit Device Address

Wr: 0 for Write Command

Rd: 1 for Read Command

Command Code: 8-bit Mixer Address

A: **0 FOR ACK, 1 FOR NACK**

Register Address Byte: 16-bit Mixer data

Data Byte: 16-bit Mixer data

☐:Master-to-Slave

☐:Slave-to-Master

8.5.3. Memory Map Conversion for I2C Control Interface

When in DSP mode (power-on DSP), read/write registers by I2C interface needs to use memory map method to convert. For global control registers locate at 0x1800_C000 ~ 0x1800_CFFF.

Register: 0x0000				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	**15:2**	**R**	**0'h**	Reserved
Op_code	**1:0**	**R/W**	**1'h**	Operation Mode Control 00'b: Reserved 01'b: 16-bit Write 10'b: 32-bit Read 11'b: 32-bit Write

Register: 0x0001				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
I2c_port_address	**15:0**	**R/W**	**0'h**	Memory Address[15:0]

Register: 0x0002				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
I2c_port_address	**15:0**	**R/W**	**0'h**	Memory Address[31:16]

Register: 0x0003				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
I2c_port_data	**15:0**	**R/W**	**0'h**	Memory Address Data[15:0]

Register: 0x0004				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
I2c_port_data	**15:0**	**R/W**	**0'h**	Memory Address Data[31:16]

8.6. I²S/PCM/TDM Digital Audio Data Interface

For digital audio data interface, CM7120 supports up to five I²S/PCM interface and two of five with TDM function. These I²S/PCM audio digital interfaces are used to send data to 5 DACs or receive data from 5 ADCs. These five I²S/PCM audio digital interfaces also can be configured to Master mode or Slave mode.

Master Mode

Under the master mode, BCLK and LRCK are configured as output port and output clock signal base on MCLK1, PLL1 or Fractional Divider output clock. That has two kinds of clock can be selected, one is 32FS and the other is 64FS. For data format, CM7120 supports normal I2S, Left Justified, PCM Mode A and PCM Mode B, total four types can be supported.

The master mode clock source is selected from each control register from MCLK1, PLL1 or Fractional Divider output. For each I2S BCLK/LRCK has independent divider control, the independent divider control provides flexible clock output for each I2S interface. The detail shows in Figure 12. I²S Interface Clock Tree when Master Mode.

Example for Master mode:
Example 1:

MCLK input clock frequency:
MCLK=12.288MHz (256 * 48kHz)

Target format:
Sample Rate: 48kHz
Channel Length: 32 Bits
I2S1 LRCK=48KHz
I2S1 BCLK=3.072MHz (64 * 48kHz)
Clk_i2s1_master=12.288MHz (256 * 48kHz)

Register settings:
Set MX-00FA[0] to "1" // For MCLK input clock getting control
Set MX-0061[15] to "1" // Enable I2S-1
Set MX-0070[15] to "0" // Enable Master mode
Set MX-0170[10:8] to "000" // Set the I2S1 Master Divider = Div1

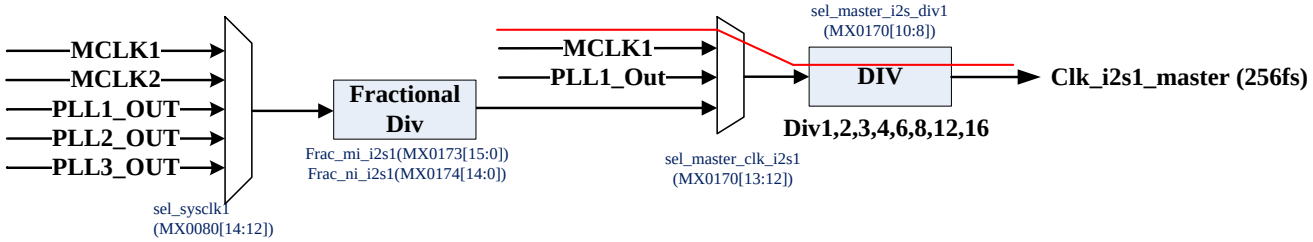


Figure 16. Example for the I2S1 Master Mode Clock Setting

Example 2:

MCLK input clock frequency:
MCLK=25MHz

Target format:
Sample Rate: 48kHz
Channel Length: 32 Bits
I2S3 LRCK=48KHz
I2S3 BCLK=3.072MHz (64 * 48kHz)
Clk_i2s3_master=12.288MHz (256 * 48kHz)

Register settings:
Set MX-00FA[0] to "1" // For MCLK input clock getting control
Set MX-0061[13] to "1" // Enable I2S-3
Set MX-00C0[7] to "1" // Set GPIO8 and GPIO9 as LRCK3 and BCLK3
Set MX-00C1[7:6] to "00" // Set GPIO8 and GPIO9 as LRCK3 and BCLK3
Set MX-0080[14:12] to '000' // Select the source of the system clock to MCLK1
Set MX-0072[15] to "0" // Enable I2S3 Master mode
Set MX-0076[7] to "1" // Set BCLK3 to 64FS
Set MX-0171[13:12] to "10" // Select the source of the clk_i2s3_master to fraction divider
Set MX-0171[10:8] to "000" // Set the I2S3 Master Divider = Div1
Set MX-0177[15:0] to "61A8" // Set the mi of the fractional divider (mi=25000)
Set MX-0178[14:0] to "3000" // Set the ni of the fractional divider (ni=12288)
Set MX-0178[15] to "1" // Update the mi and ni code

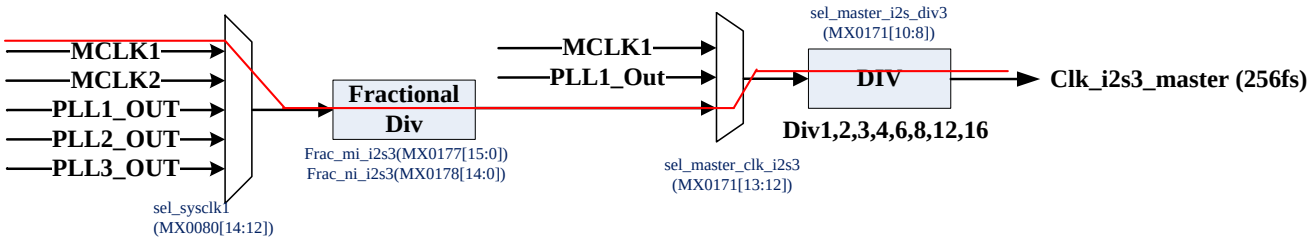


Figure 17. Example for the I2S3 Master Mode Clock Setting

Slave Mode
Under slave mode BCLK and LRCK are configured as input port and receive clock signal. In synchronous I2S mode, MCLK and BCLK/LRCK should be synchronous. That means MCLK is equal to 256FS or 512FS, BCLK is equal to 64FS or 32FS and the clock rising edge of MCLK is aligned with BCLK.

In asynchronous I2S mode, MCLK and BCLK/LRCK are asynchronous and no any relationship. At this condition, needs to turn on internal ASRC function of CM7120. As the Figure 18, in this connection, the MCLK is from external oscillator that clock is no relation (or asynchronous) with SOC and BT or 3G BaseBand. SOC (master mode) connects to I2S1 (slave mode) and BT (master mode) connects to I2S2 (slave mode). When turn on ASRC function, the SYSCLK is need to higher than 512FS clock rate. If the MCLK is lower than 512*FS, that can use internal PLL to generate higher than 512*FS clock.

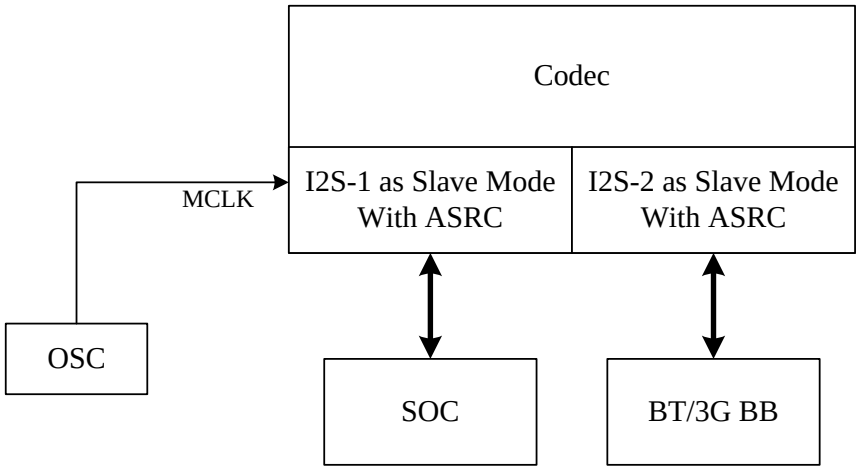


Figure 18. System Connection for ASRC Function

8.7. Audio Digital Data Interface

8.7.1. I²S/PCM Interface

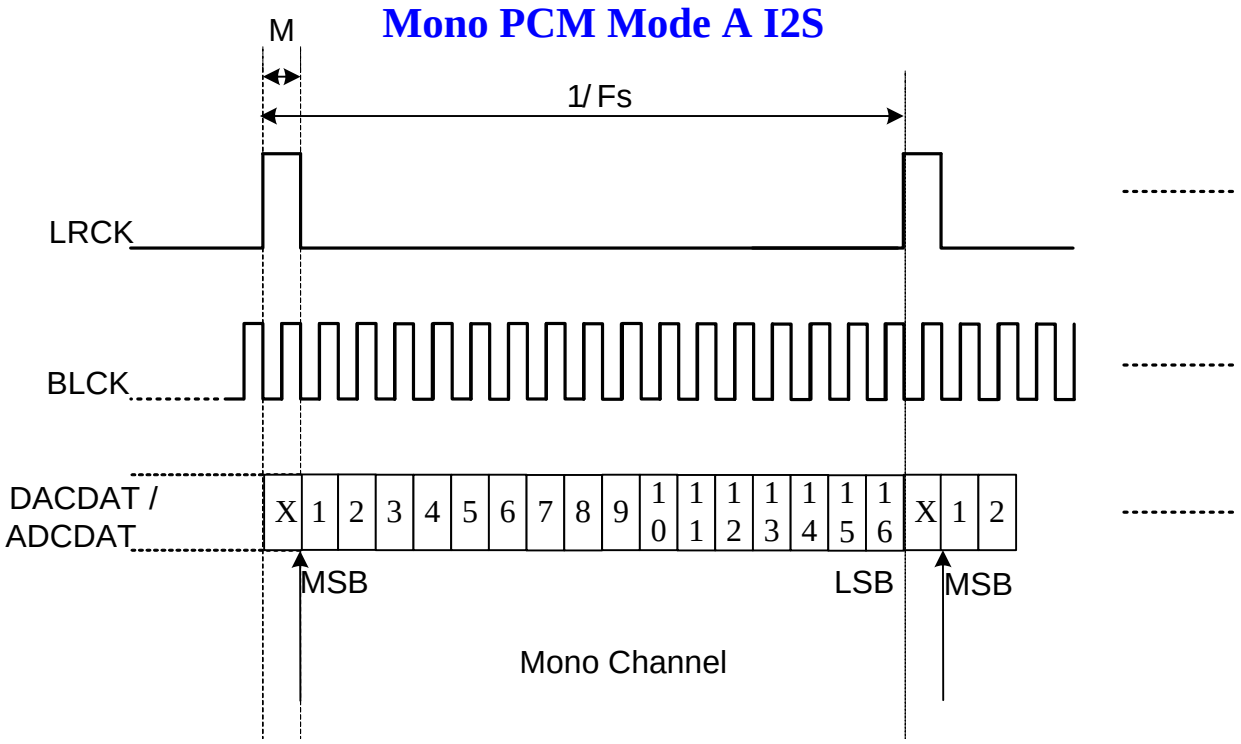
The chip has two independent I²S/PCM interfaces for Stereo Audio. The I²S/PCM interface can be configured as Master mode and Slave mode and different audio data formats are supported:

- PCM Mono Mode A and Mode B

⇨ BCLK is 16FS for PCM Mode B, 17FS for PCM Mode A

⇨ Data length is 16bit

- PCM/DSP mode **(Pulse Mode)**
- Left justified mode
- I^2S mode
- Compress



1. Support BCLK = (channel_length+1)*FS
channel_length: 16bit
2. BCLK Polarity: Falling latch or Rising latch
3. "M" only support: 1*BCLK

Figure 19. PCM/DSP Mono Data Mode A Format (bclk_polarity=0)

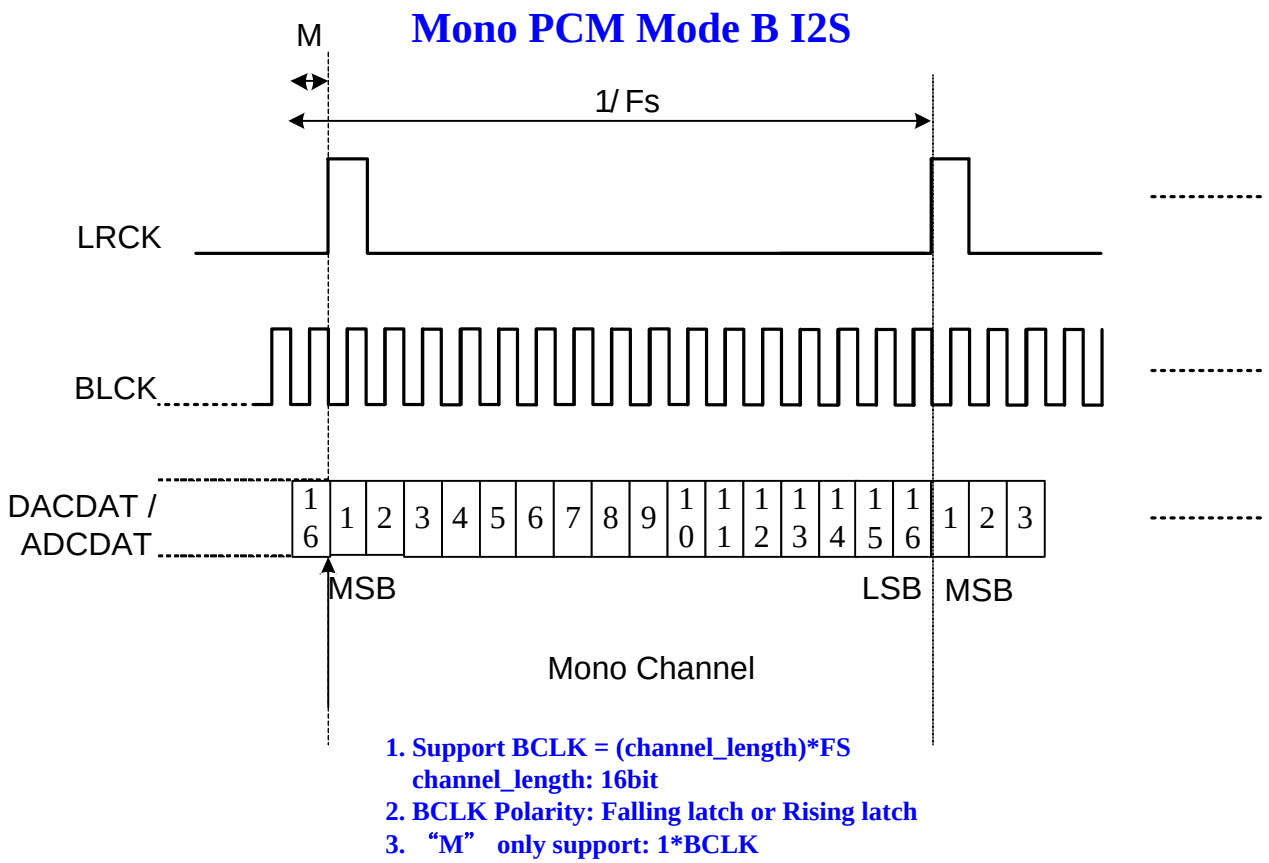


Figure 20. PCM/DSP Mono Data Mode B Format (bclk_polarity=0)

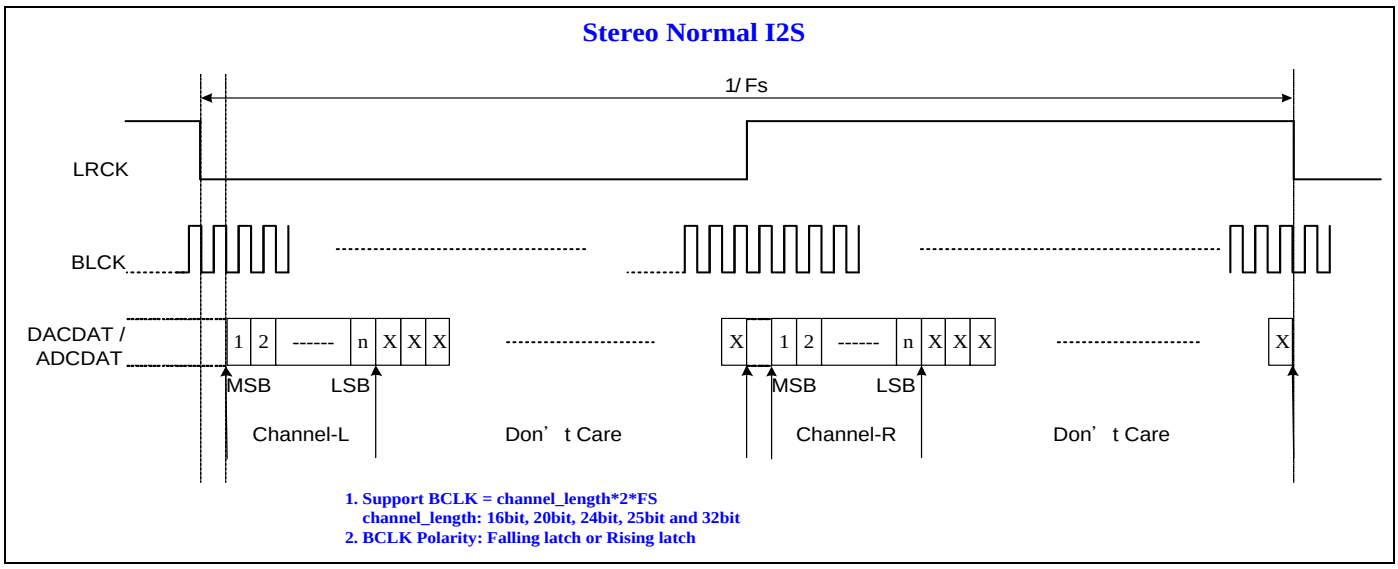


Figure 21. Stereo Normal I2S Data Format

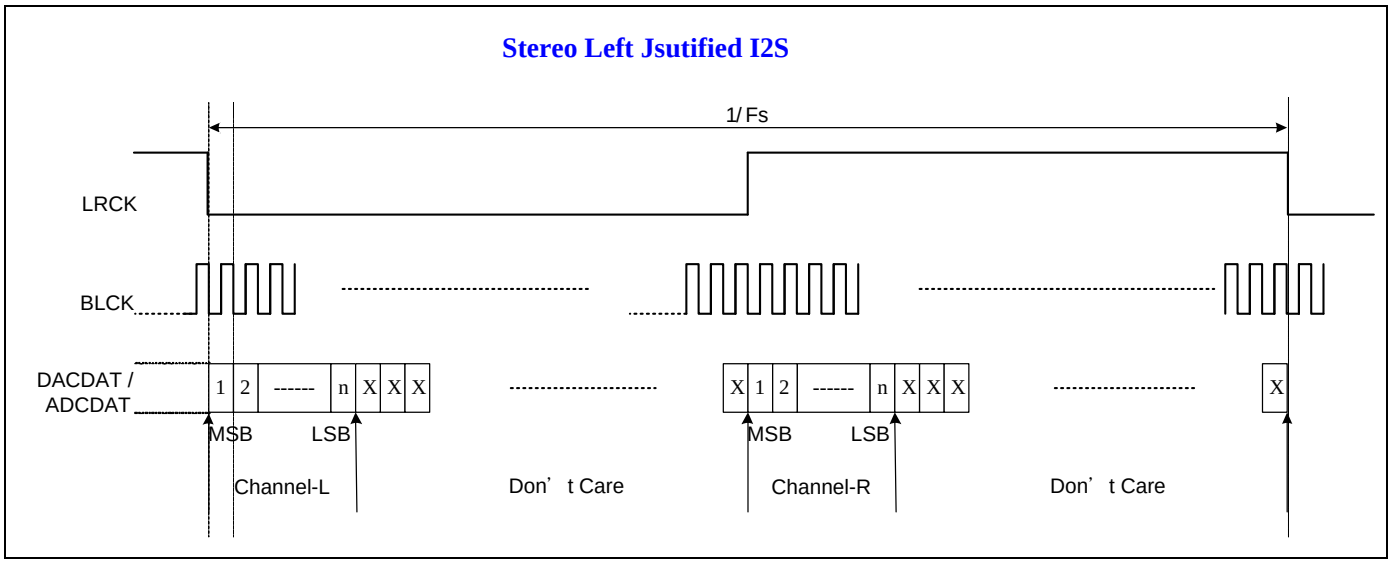


Figure 22. Stereo Left justified I2S Data Format

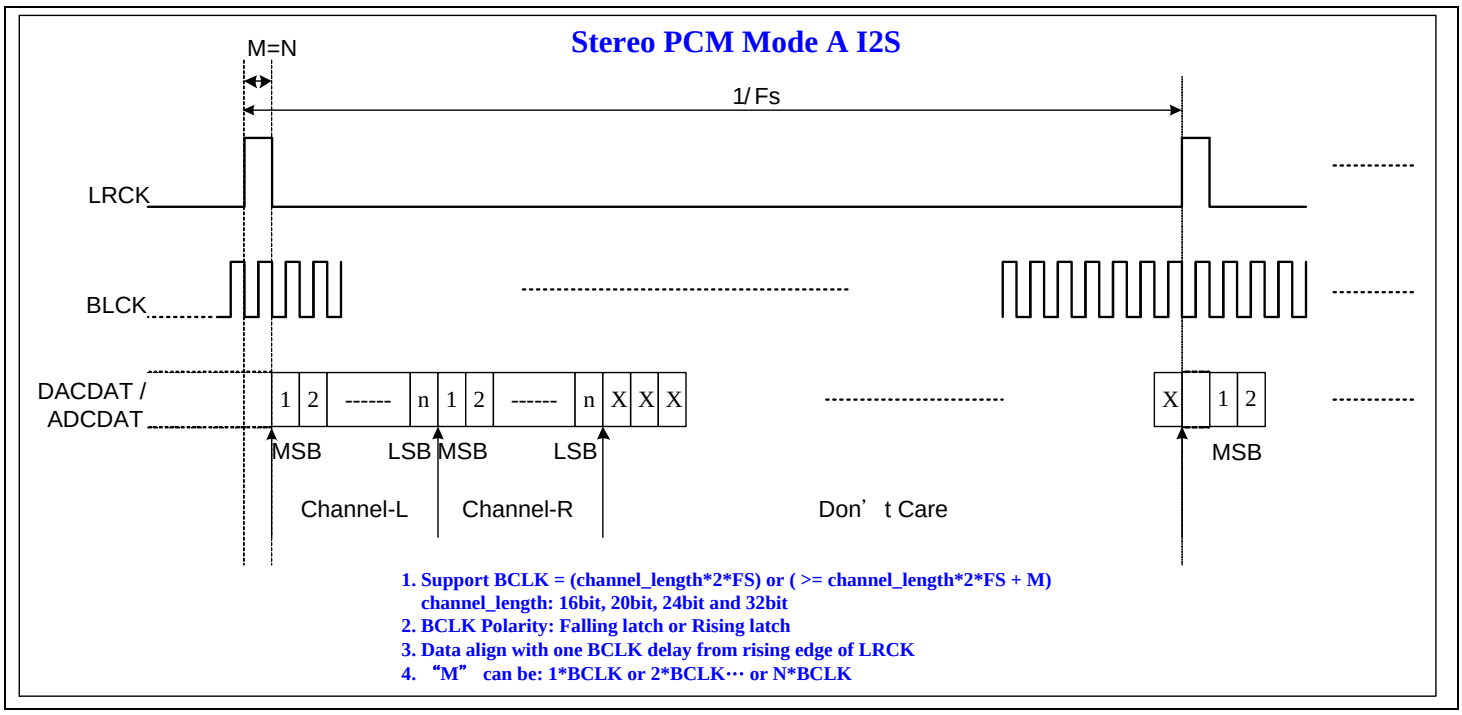


Figure 23. Stereo PCM Data Mode A Format

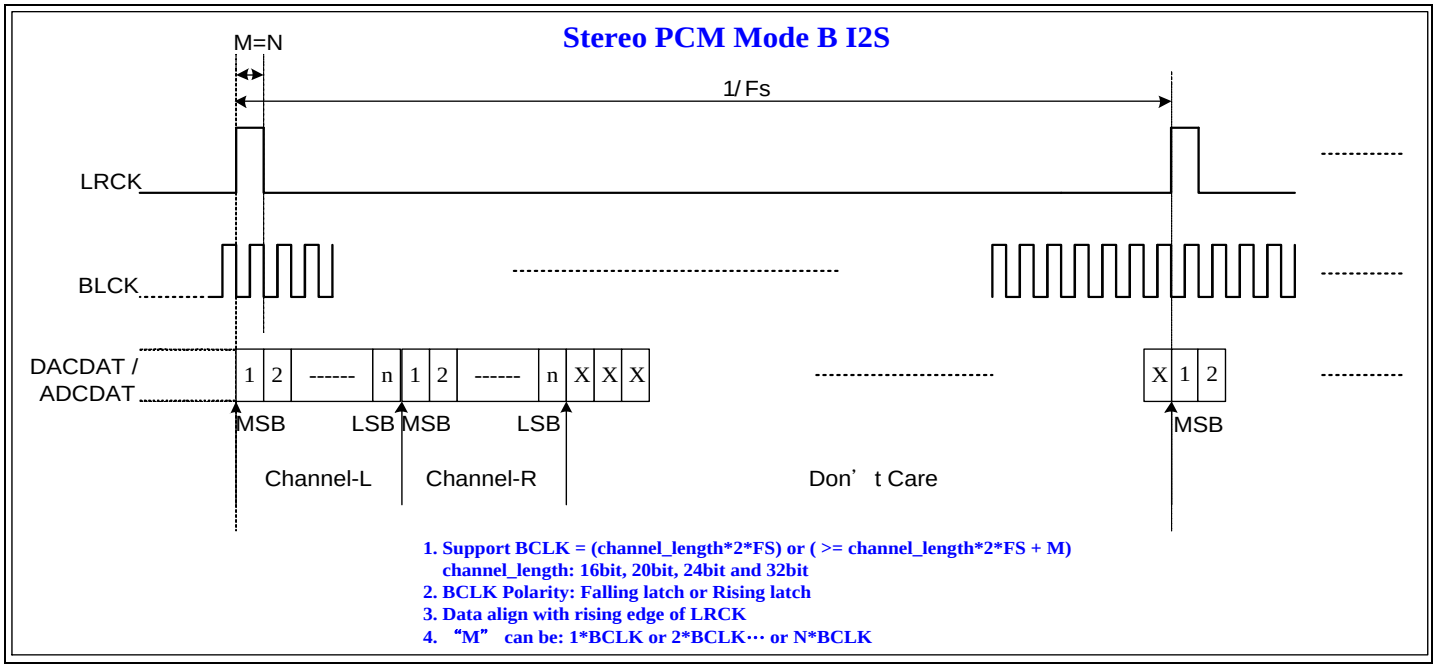


Figure 24. Stereo PCM Data Mode B Format

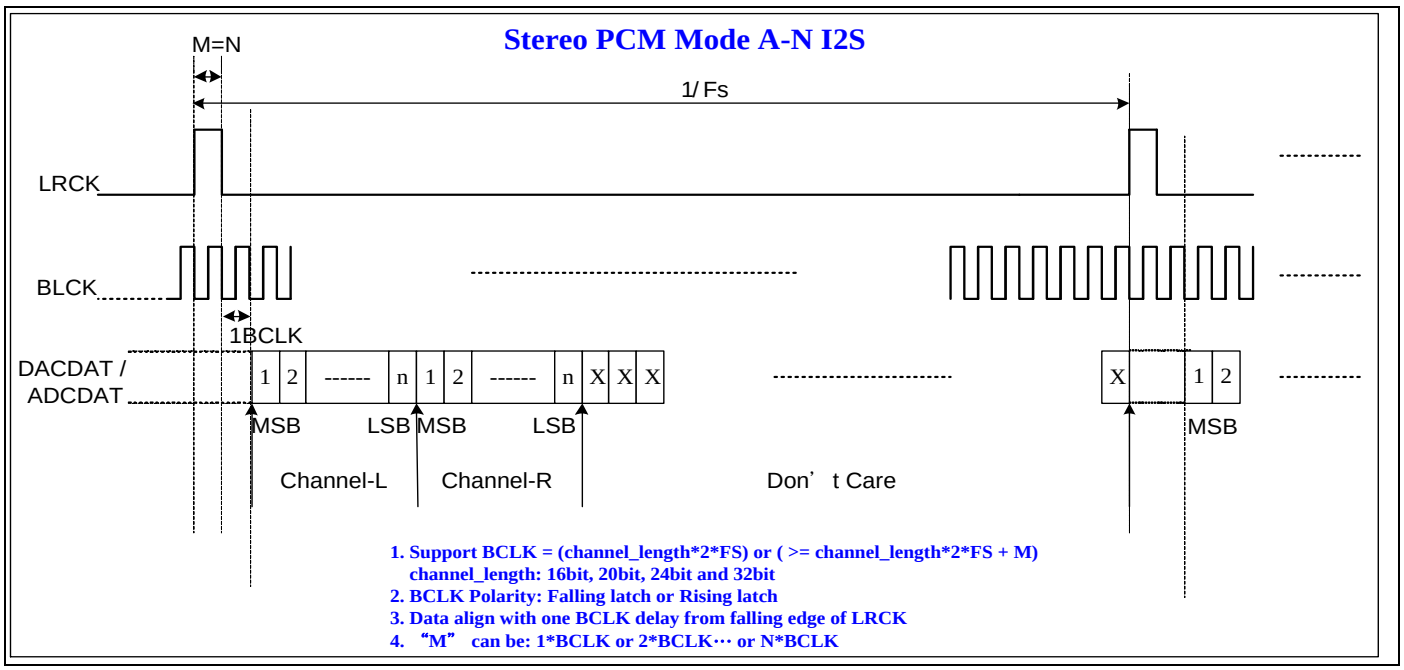


Figure 25. Stereo PCM Data Mode A-N Format

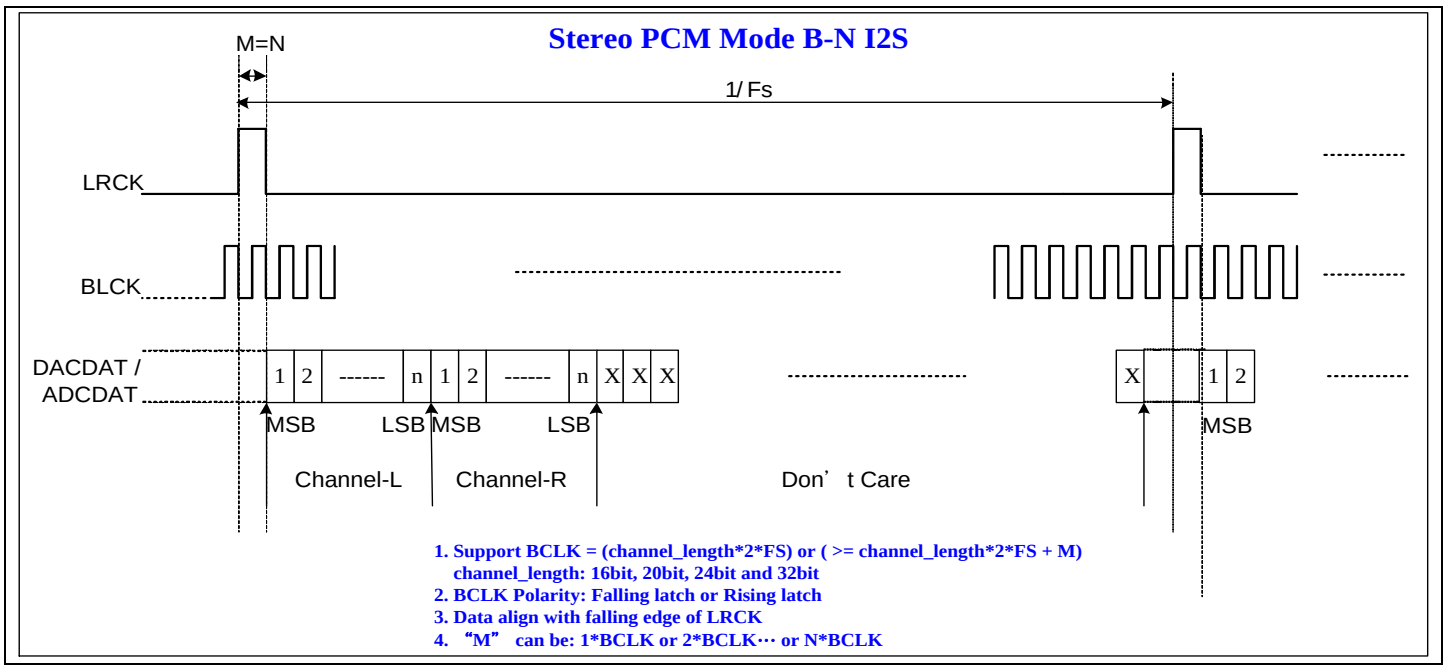


Figure 26. Stereo PCM Data Mode B-N Format

8.7.2. TDM Interface

There are four data format can be supported in TDM mode – I2S format, Left Justified format, PCM Mode A format, PCM Mode B format.

1. Up to 8 channels supporting (channel number is from 2 to 8)
2. Channel length: 16/20/24/32 bits
3. Word length: 16/20/24
4. Bit order: MSB only first
5. BCLK polarity – Normal or Inverter

I2S Data Format in TDM Mode:

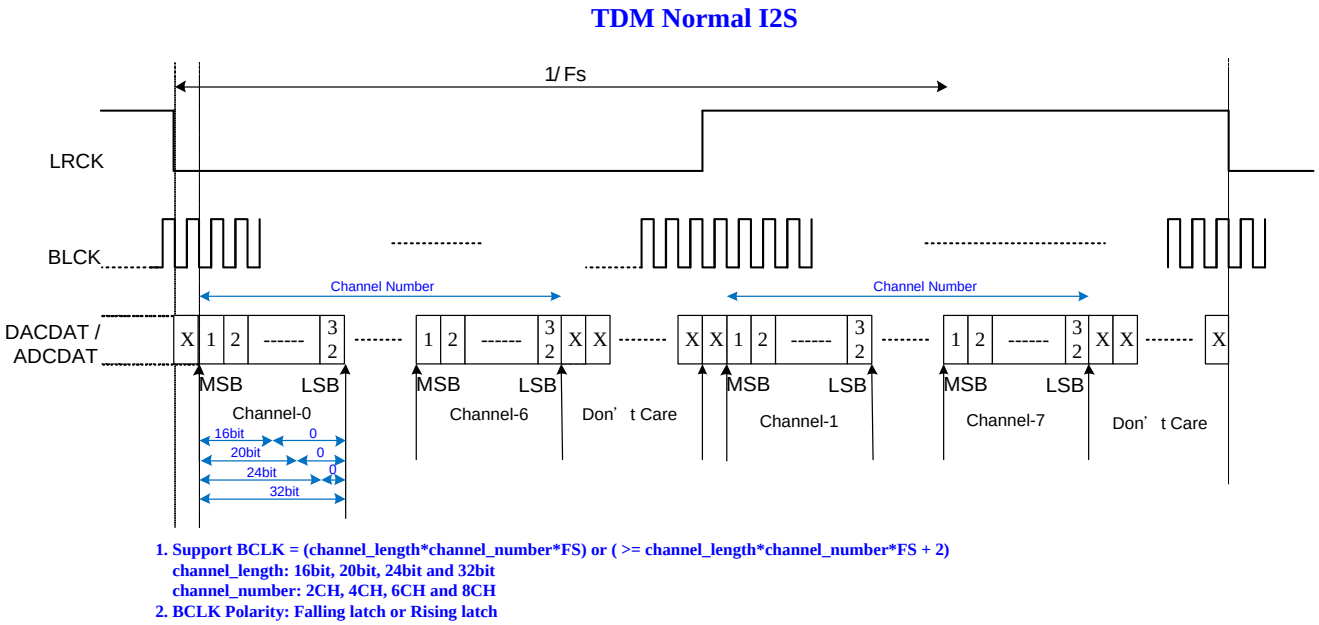


Figure 27. I2S Data Format in TDM MODE

Left Justified Data Format in TDM Mode:

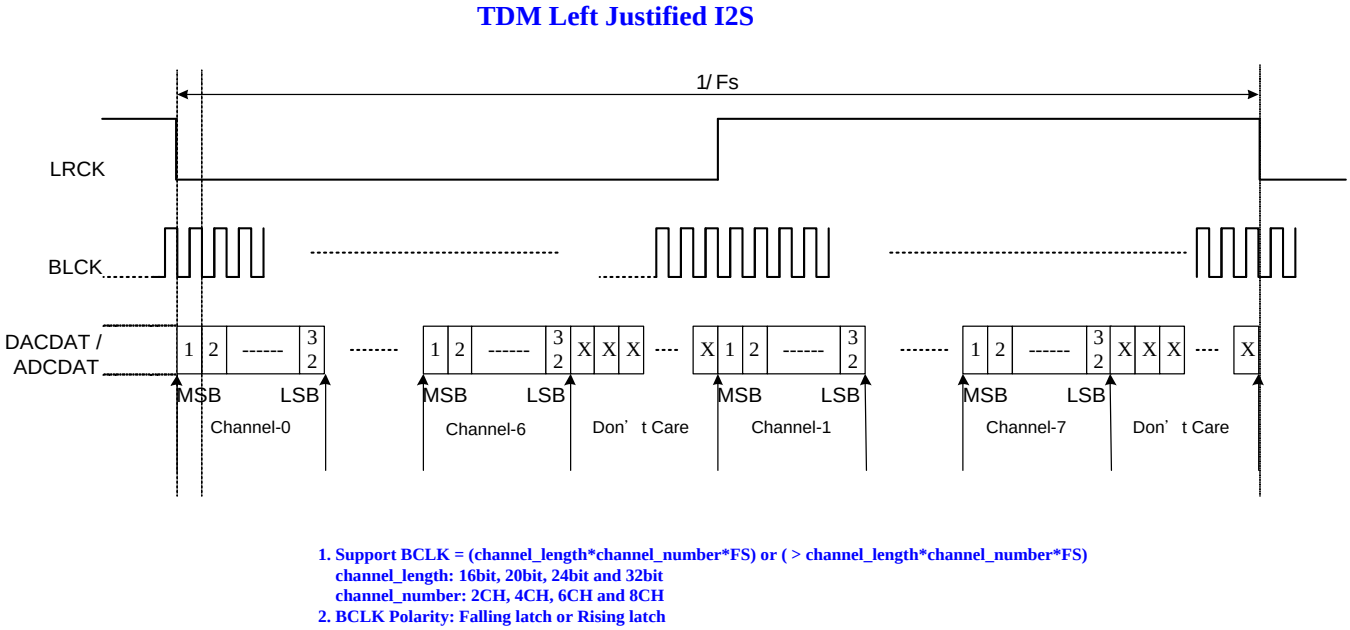


Figure 28. Left Justified Data Format in TDM Mode

PCM Mode A Data Format in TDM Mode:

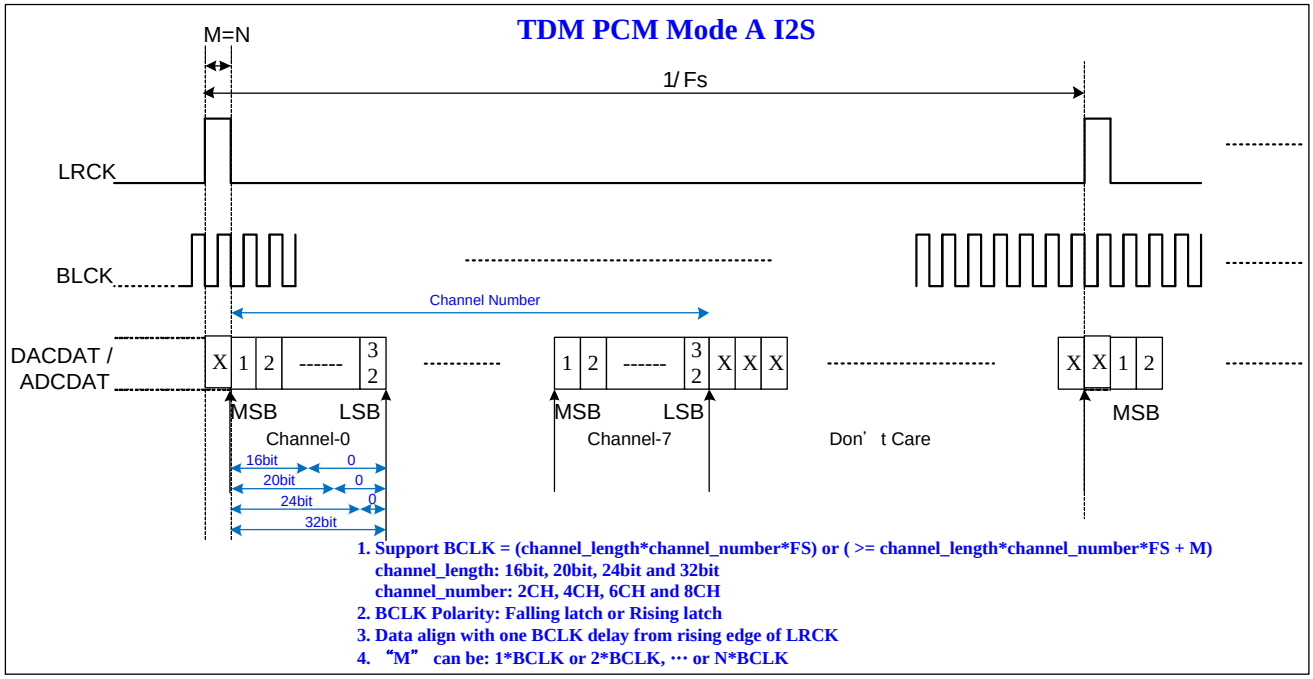


Figure 29. PCM Mode A Data Format in TDM Mode

PCM Mode B Data Format in TDM Mode:

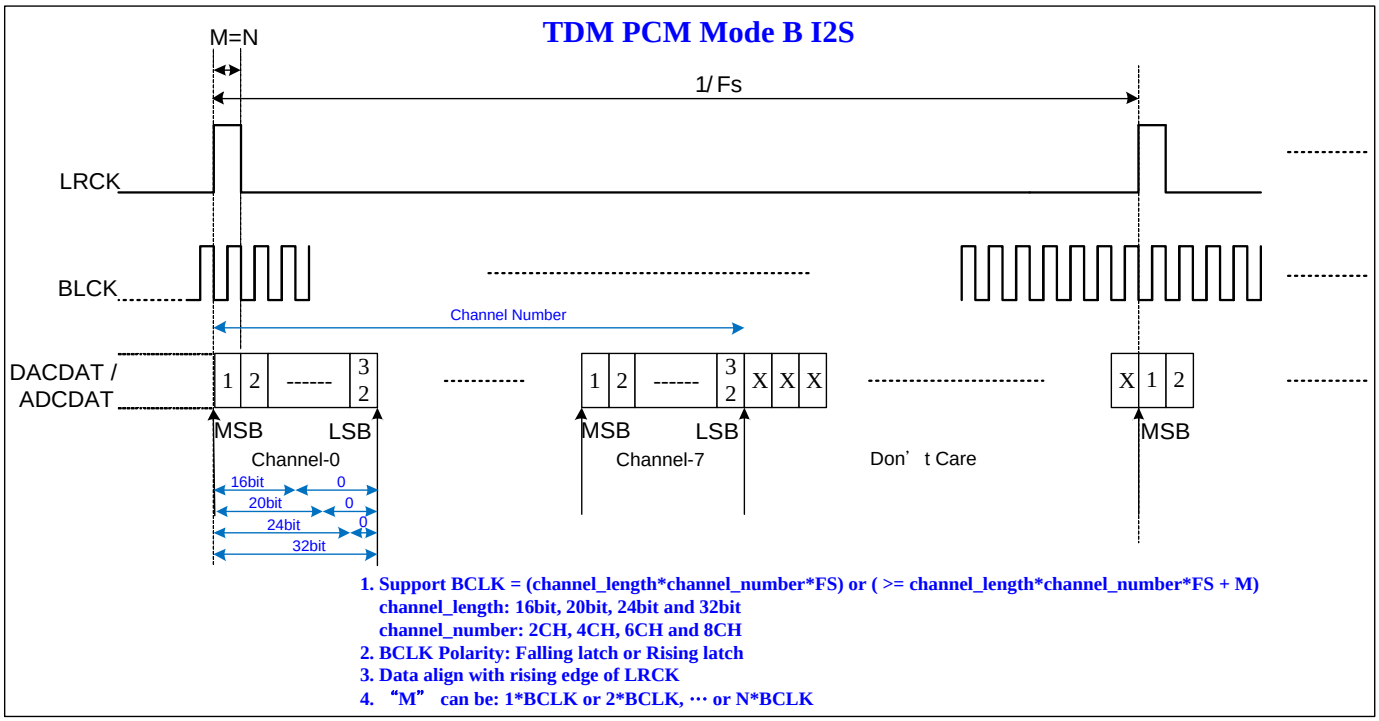


Figure 30. PCM Mode B Data Format in TDM Mode

PCM Mode A-N Data Format in TDM Mode:

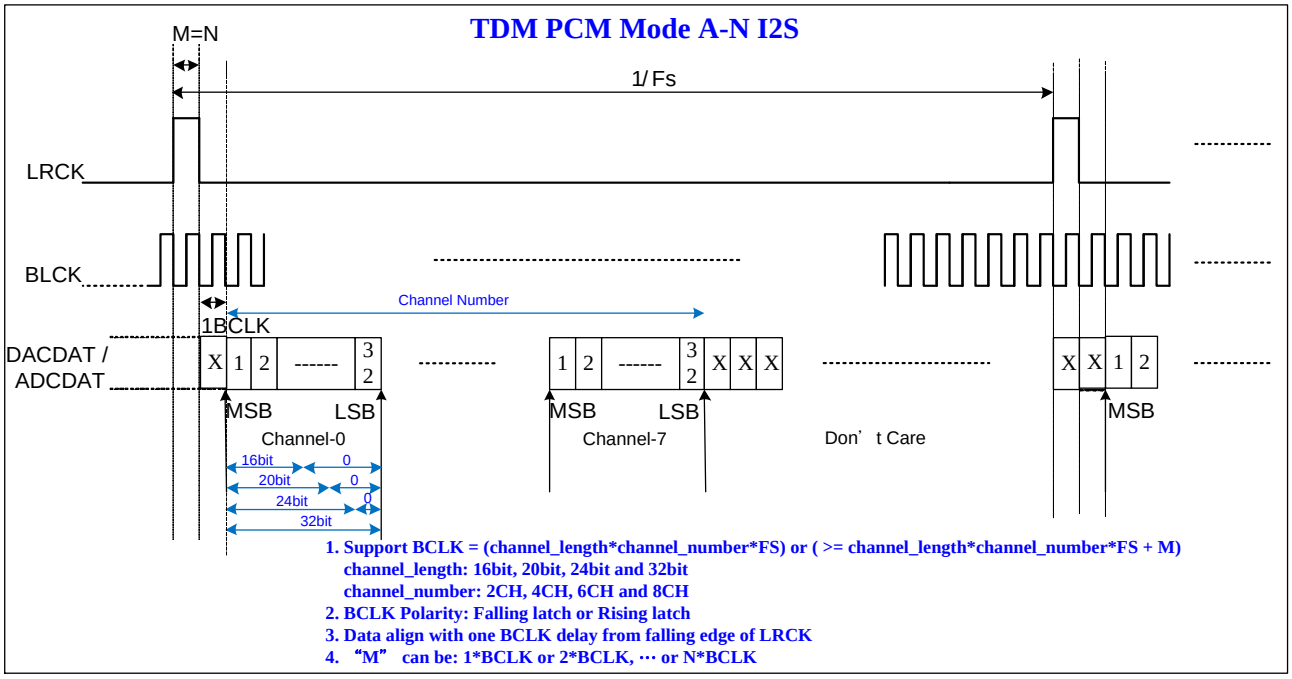


Figure 31. PCM Mode A-N Data Format in TDM Mode

PCM Mode B-N Data Format in TDM Mode:

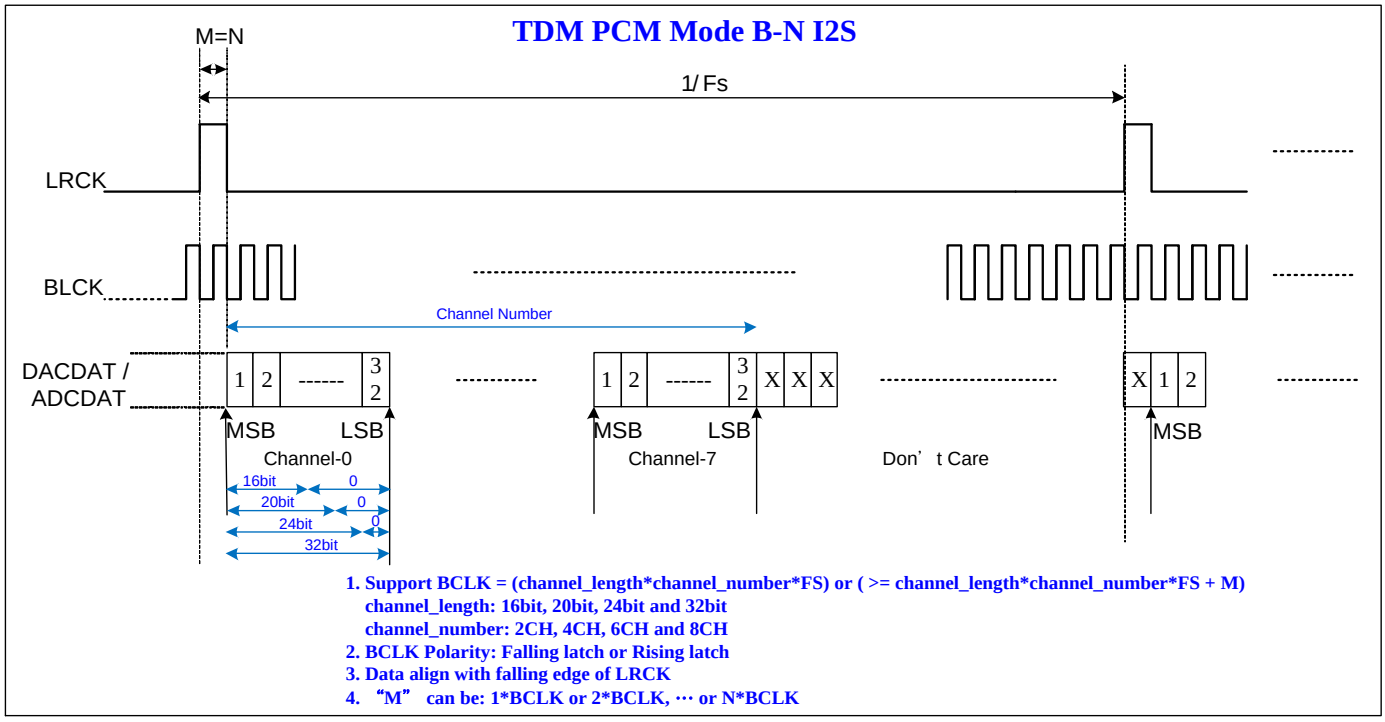


Figure 32. PCM Mode B-N Data Format in TDM Mode

8.8. Audio Data Path

The CM7120 provides 5-channel analog DACs for playback and 5-channel analog ADCs for recording.

8.8.1. 8-Channels DMIC Recording Function

CM7120 can support up to 8 channels recording by using 4 digital microphone interfaces. The 8 channels data sent back to host by TDM interface. CM7120 also builds in two analog ADCs for external analog microphone or other analog audio signal. Only I2S1/I2S2 digital interface support TDM mode and I2S3/I2S4/I2S5 digital interface support normal I2S mode (2 channel mode). The below figure shows the 8 channels recording on TDM interface.

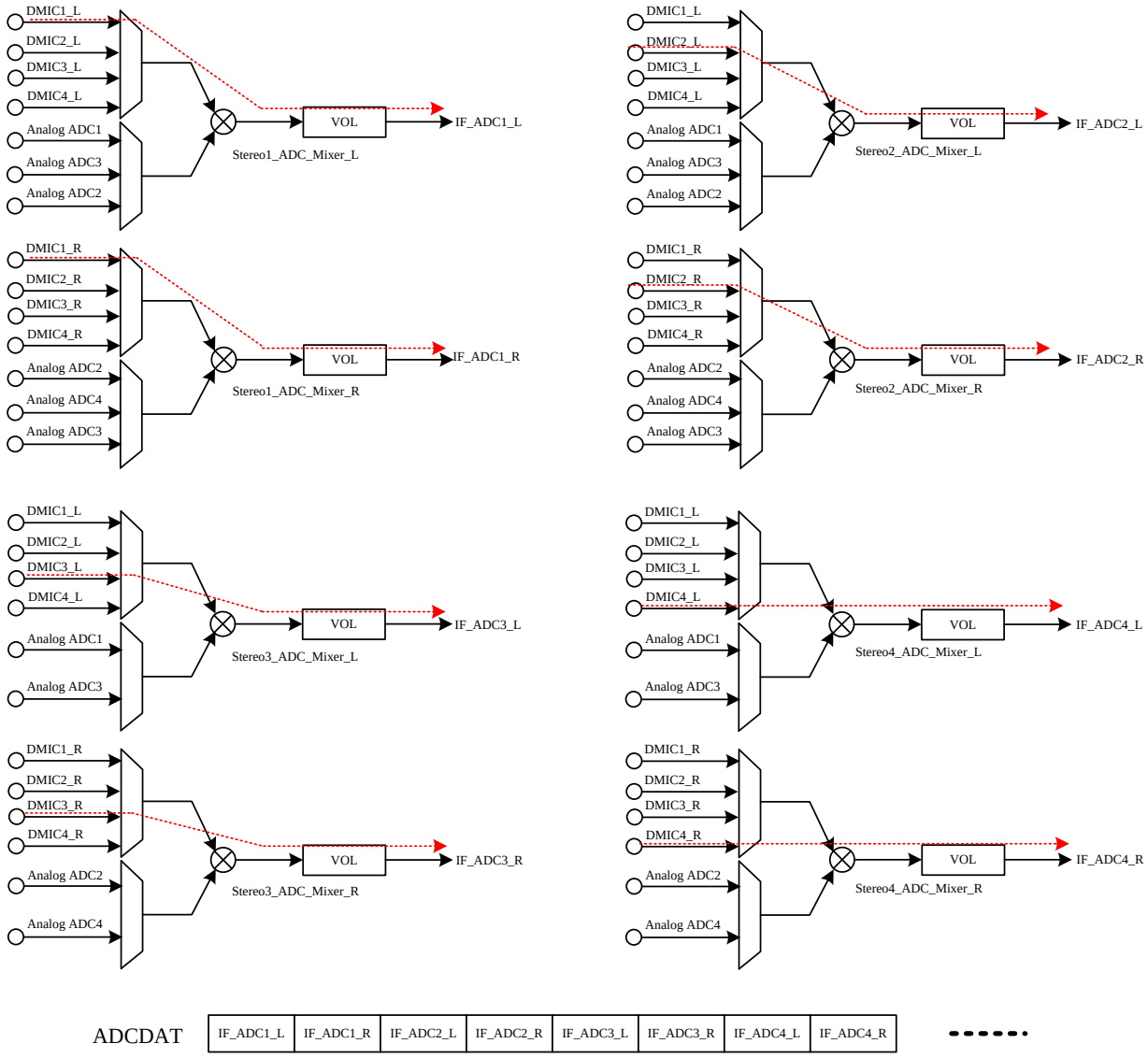


Figure 33. 8-Channels DMIC Recording Path

8.8.2. 4-Channels AMIC Recording Function

CM7120 also builds in four analog ADCs for external analog microphone or other analog audio signal. The below figure shows the 4 channels AMIC recording on TDM interface.

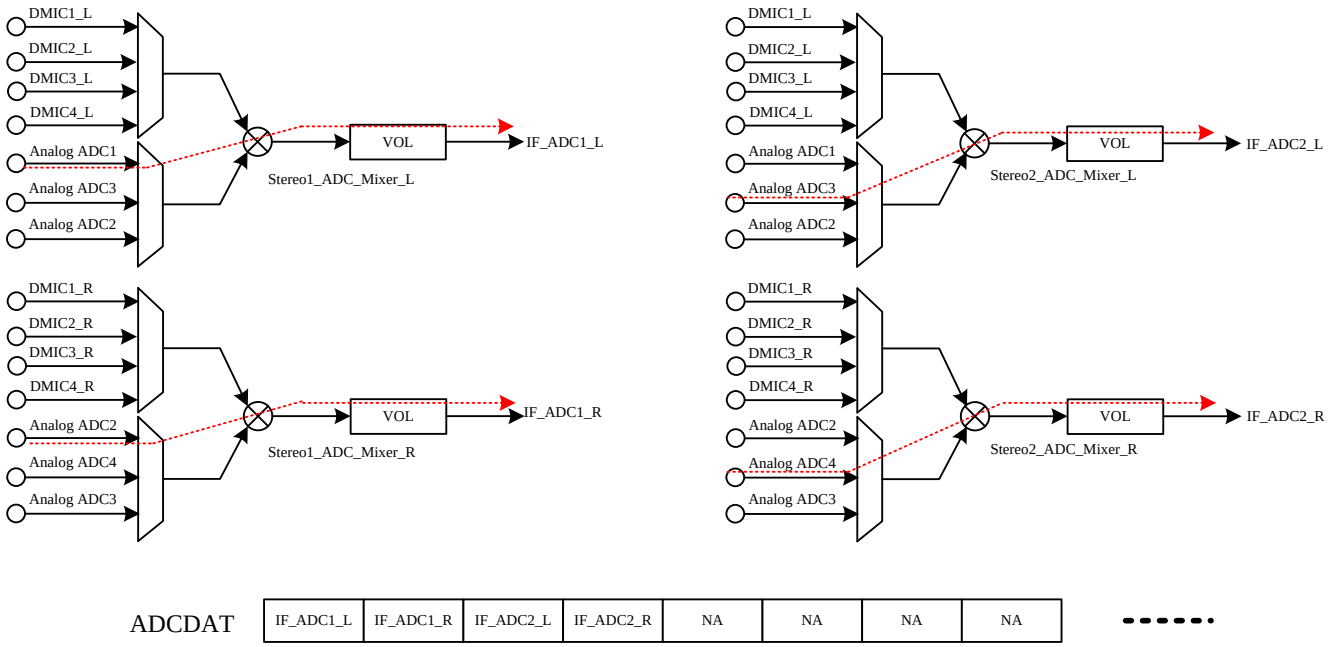


Figure 34. 4-Channels AMIC Recording Path

8.8.3. Multi-Channels Playback Function

CM7120 supports up to 4 channels playback function by two PDM digital interfaces with external PDM amplifiers. Each PDM interface can support 2 channels data. The 4 channels data only supported on I2S1 and I2S2 by use TDM mode. I2S3, I2S4 and I2S5 don't support TDM mode. CM7120 also builds in five analog DACs for HP, MONO and LOUT amplifier. The analog DAC data can be selected from I2S1, I2S2, I2S3, I2S4 or I2S5.

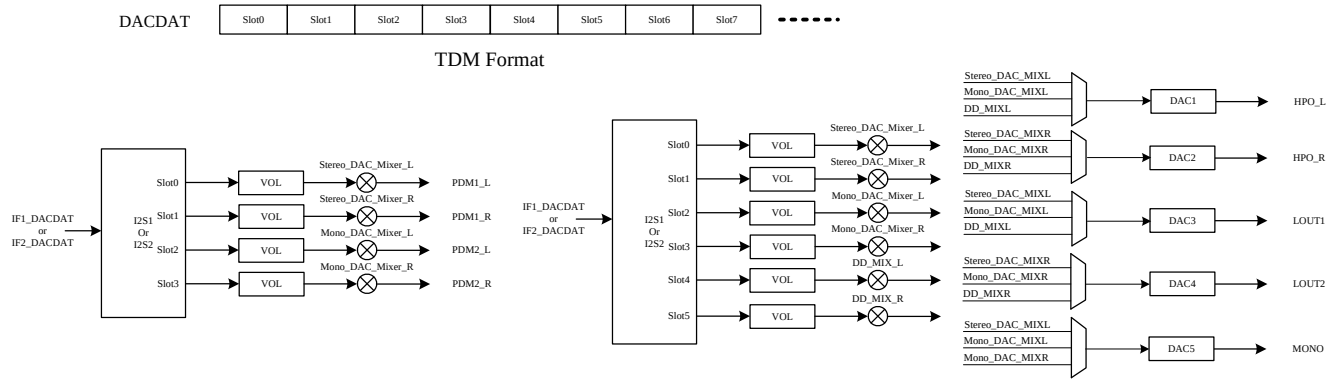


Figure 35. Multi-Channel Playback Path

8.8.4. Digital Loopback Function

Same Sampling Rate:

CM7120 supports digital loopback function. The digital loopback function includes I2S_DACDAT to I2S_ADCDAT. Where, the DACDATn and ADCDATn is DACDAT1 ~ DACDAT5 and ADCDAT1 ~ ADCDAT5, respectively.
In the below Figure 36, the red dashed line shows the data loopback from I2S DACDAT3 to I2S ADCDAT1. The green dashed line shows the data loopback from I2S DADAT4 to I2S DACDAT5. The data is loopback between the each interface. The LRCK and BCLK should be synchronized.

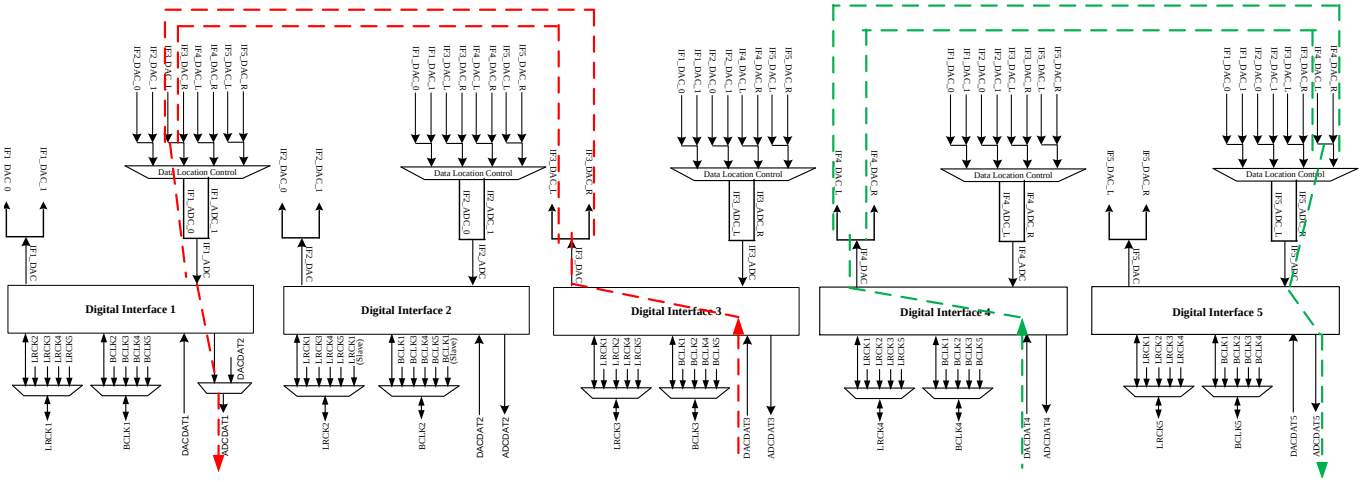


Figure 36. Digital Loopback Function from I2S DACDATn to I2S ADCDATn

On the I2S ADCDAT1 pin, it supports bypass data from I2S DACDAT2 to I2S ADCDAT1. The system connection is shown in the red dashed line of the Figure 37. In this case, the I2S1 should be slave mode and the I2S2 should be as master mode. The LRCK and BCLK of the I2S1 and I2S2 should be synchronized.

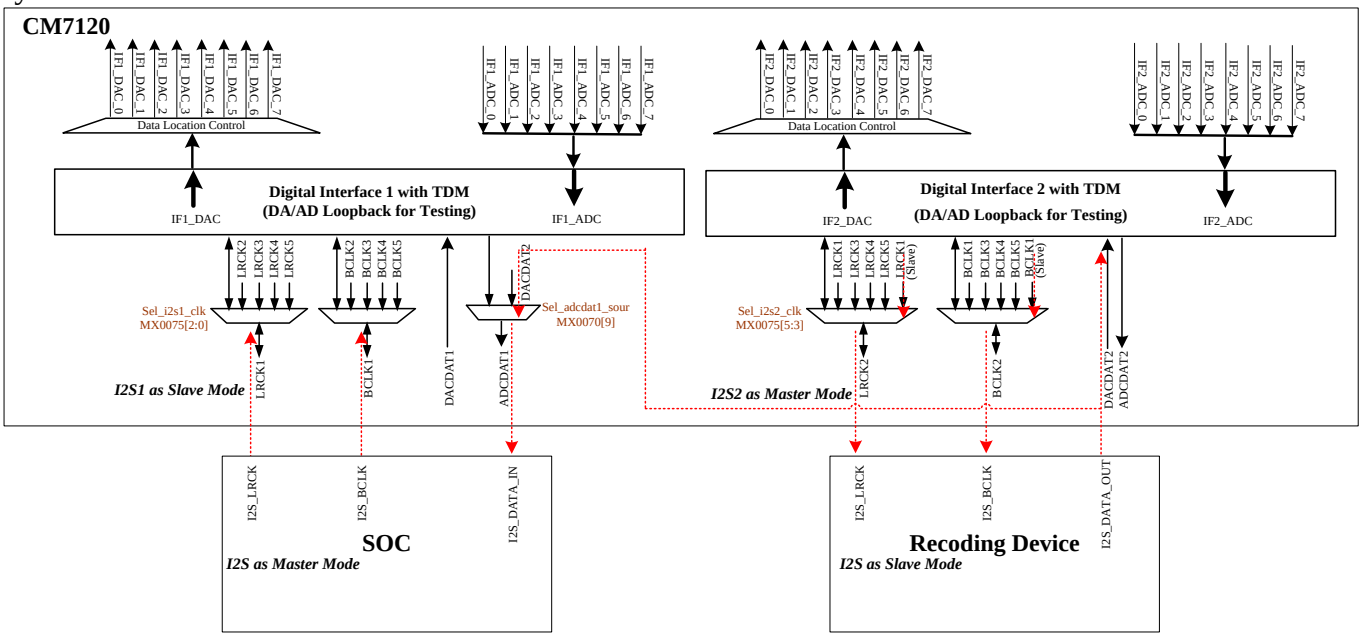


Figure 37. Data Bypass from I2S DACDAT2 to I2S ADCDAT1

Difference Sampling Rate:

The digital loopback function also supports SRC (Sample Rate Converter) function. For example, 48kHz sample rate data on I2S1_DACDAT can converter to 8kHz or 16kHz sample rate data on I2S2_ADCDAT by codec digital loopback function.

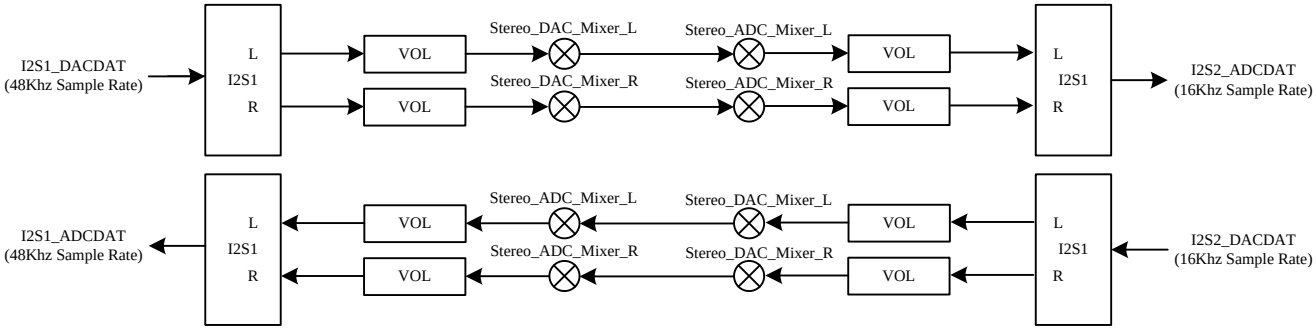


Figure 38. Digital Loopback Function (Difference Sampling Rate)

8.8.5. Mixers

The CM7120 has digital mixers build-in.

- **Digital mixer**

  There are many digital mixers in CM7120. Eight digital mixers are assigned for ADC recording. These ten mixers can mix analog line input, analog microphone input, digital microphone input and digital loopback data then output to I2S interface to other device. Another eight digital mixers are assigned for DAC playback. These mixers can mix digital data from I2S interface, DSP processed data and ADC data from external analog signal. The mixed data is output to analog DAC and output port to drive external device.

8.9. Analog Audio Input Port

The CM7120 has two types of analog input port: microphone input and line input.

IN1P / IN1N

This port is a microphone type input port. This input port supports single-ended or differential mode. The microphone input port features built-in microphone boost gain. Low noise microphone bias is also built-in. It provides analog microphone driving voltage. Multi-step microphone boost gain is set by gain_bst1 (MX-0007[14:8]) and is easy to use for analog microphone compensation. Pow_bst1(MX-0064[15]) can be used to power down the MIC1 boost.

IN2P / IN2N

This port is a microphone type input port. This input port supports single-ended or differential mode. The microphone input port features built-in microphone boost gain. Low noise microphone bias is also built-in. It provides analog microphone driving voltage. Multi-step microphone boost gain is set by gain_bst2 (MX-0007[6:0]) and is easy to use for analog microphone compensation. Pow_bst2(MX-0064[14]) can be used to power down the MIC2 boost.

IN3P(IN_VAD) / IN3N

This port is a microphone type input port. This input port supports single-ended or differential mode. The microphone input port features built-in microphone boost gain. Low noise microphone bias is also built-in. It provides analog microphone driving voltage. Multi-step microphone boost gain is set by gain_bst3 (MX-0008[14:8]) and is easy to use for analog microphone compensation. Pow_bst3(MX-0064[13]) can be used to power down the MIC3 boost. The port of the IN3P also can as input of the power saving ADC for sound active detection.

IN4P(IN_VAD) / IN4N

This port is a microphone type input port. This input port supports single-ended or differential mode. The microphone input port features built-in microphone boost gain. Low noise microphone bias is also built-in. It provides analog microphone driving voltage. Multi-step microphone boost gain is set by gain_bst4 (MX-0008[6:0]) and is easy to use for analog microphone compensation. Pow_bst4(MX-0064[12]) can be used to power down the MIC4 boost. The port of the IN4P also can as input of the power saving ADC for sound active detection.

8.10. Analog Audio Output Port

The CM7120 has 3 types of analog output ports – Headphone Output L/R, Line Output 1/2 and Mono Receiver Output:

- **HP_OUT_L/R**

  The output type is headphone output. The output is single ended output. The input is only from DAC1 and DAC2 output.

- **LINE_OUT_1/2**

  The output type is line type output. The output can configure as single ended output or differential output. The input is only from DAC3 and DAC4 output.

- **MONO_P/N**

  The output type is differential output. The input is only from DAC5 output.

8.11. Multi-Function Pins

There are eight multi-function pins in CM7120. For different functions of each pin are controlled by register. You need to set the right register settings for each multi-function pins by your application.

GPIO1/IRQ – Pin N1

The function configuration of the GPIO1 is shown as the below Table 12.

Table 12. GPIO1 Multi-Function Configuration

Function	MX00C0[15]	Note
GPIO1 (Default)	0'b	GPIO Function
IRQ	1'b	Interrupt Status

GPIO2/JTRST/DMIC1_SCL/SPI_SCL_FLASH – Pin R1

The function configuration of the GPIO2 is shown as the below Table 13.

Table 13. GPIO2 Multi-Function Configuration

Function	MX00C0[13]	MX00C1[15:14]	Note
GPIO2	0'b	X	GPIO Function
JTRST	1'b	00'b	JTAG Function
DMIC1_SCL	1'b	01'b	DMIC Clock
SPI_SCL_FLASH (Default)	1'b	10'b	SPI Flash Serial Clock

GPIO3/DMIC2_SCL – Pin L5

The function configuration of the GPIO3 is shown as the below Table 14.

Table 14. GPIO3 Multi-Function Configuration

Function	MX00C0[15]	Note
GPIO3 (Default)	0'b	GPIO Function
DMIC2_SCL	1'b	DMIC Clock

GPIO4/DMIC2_SCL/DACDAT5/PDM_SCL2/IRQ2 – Pin L7

The function configuration of the GPIO4 is shown as the below Table 15.

Table 15. GPIO4 Multi-Function Configuration

Function	MX00C0[11]	MX00C0[6:5]	Note
GPIO4 (Default)	0'b	X	GPIO Function
DMIC2_SCL	1'b	00'b	DMIC Clock
DACDAT5	1'b	01'b	I^2S Data Input
PDM_SCL2	1'b	10'b	2^{nd} PDM Serial Clock
IRQ2	1'b	11'b	Interrupt Status

GPIO5/DMIC3_SCL/ADCDAT5/PDM_SDA2/IRQ2 – Pin J3

The function configuration of the GPIO5 is shown as the below Table 16.

Table 16. GPIO5 Multi-Function Configuration

Function	MX00C0[10]	MX00C1[13:12]	Note
GPIO5 (Default)	0'b	X	GPIO Function
DMIC3_SCL	1'b	00'b	3rd DMIC Clock
ADCDAT5	1'b	01'b	I2S Data Output
PDM_SDA2	1'b	10'b	2nd PDM Serial Data
IRQ2	1'b	11'b	Interrupt Status

GPIO6/PDM1_SCL/BCLK5/DMIC4_SDA – Pin J5

The function configuration of the GPIO6 is shown as the below Table 17.

Table 17. GPIO6 Multi-Function Configuration

Function	MX00C1[1:0]	MX00C1[11]	Note
GPIO6 (Default)	00'b	X	GPIO Function
PDM1_SCL	01'b	0'b	1st PDM Serial Clock
BCLK5	01'b	1'b	I2S Bit Clock
DMIC4_SDA	10'b	X	4th DMIC Data

GPIO7/PDM1_DAT/LRCK5/DMIC4_SCL – Pin K10

The function configuration of the GPIO7 is shown as the below Table 18.

Table 18. GPIO7 Multi-Function Configuration

Function	MX00C0[9:8]	MX00C1[11]	Note
GPIO7 (Default)	00'b	X	GPIO Function
PDM1_DAT	01'b	0'b	1st PDM Serial Data
LRCK5	01'b	1'b	I2S Serial Synchronous Clock
DMIC4_SCL	10'b	X	4th DMIC Clock

GPIO8/BCLK3/SPI_SCL_M1/UART_TX – Pin R3

The function configuration of the GPIO8 is shown as the below Table 19.

Table 19. GPIO8 Multi-Function Configuration

Function	MX00C0[7]	MX00C1[7:6]	Note
GPIO8 (Default)	0'b	X	GPIO Function
BCLK3	1'b	00'b	I2S Bit Clock

SPI_SCL_M1	1'b	01'b	1st Master SPI Serial Clock
UART_TX	1'b	10'b	UART Serial Data Transmit

GPIO9/LRCK3/SPI_CS_M1/UART_RX – Pin P2

The function configuration of the GPIO9 is shown as the below Table 20.

Table 20. GPIO9 Multi-Function Configuration

Function	MX00C0[7]	MX00C1[7:6]	Note
GPIO9 (Default)	0'b	X	GPIO Function
LRCK3	1'b	00'b	I2S Serial Synchronous Clock
SPI_CS_M1	1'b	01'b	1st Master SPI Chip Select
UART_RX	1'b	10'b	UART Serial Data Receive

GPIO10/DACDAT3/SPI_MOSI_M1/UART_#RTS/SEL_BONDING0 – Pin N3

The function configuration of the GPIO10 is shown as the below Table 21.

Table 21. GPIO10 Multi-Function Configuration

Function	MX00C0[7]	MX00C1[7:6]	Note
GPIO10 (Default)	0'b	X	GPIO Function
DACDAT3	1'b	00'b	I2S Data Input
SPI_MOSI_M1	1'b	01'b	1st Master SPI MOSI
UART_#RTS	1'b	10'b	UART Request to Send
SEL_BONDIGN0	1'b	11'b	HW ID Select Pin

GPIO11/ADCDAT3/SPI_MISO_M1/UART_#CTS/SEL_BONDING1 – Pin P4

The function configuration of the GPIO11 is shown as the below Table 21.

Table 22. GPIO11 Multi-Function Configuration

Function	MX00C0[7]	MX00C1[7:6]	Note
GPIO11 (Default)	0'b	X	GPIO Function

ADCDAT3	1'b	00'b	I²S Data Output
SPI_MISO_M1	1'b	01'b	1st Master SPI MISO
UART_#CTS	1'b	10'b	UART Clear to Send
SEL_BONDIGN1	1'b	11'b	HW ID Select Pin

GPIO12/BCLK4/MASTER_SCL2 – Pin N5

The function configuration of the GPIO12 is shown as the below Table 23.

Table 23. GPIO12 Multi-Function Configuration

Function	MX00C0[4]	MX00C1[5]	Note
GPIO12 (Default)	0'b	X	GPIO Function
BCLK4	1'b	0'b	I²S Bit Clock
MASTER_SCL2	1'b	1'b	2nd Master I²C Serial Clock

GPIO13/LRCK4/MASTER_SDA2 – Pin R5

The function configuration of the GPIO13 is shown as the below Table 24.

Table 24. GPIO13 Multi-Function Configuration

Function	MX00C0[4]	MX00C1[5]	Note
GPIO13(Default)	0'b	X	GPIO Function
LRCK4	1'b	0'b	I²S Serial Synchronous Clock
MASTER_SDA2	1'b	1'b	2nd Master I²C Serial Data

GPIO14/DACDAT4/MASTER_SCL3 – Pin K4

The function configuration of the GPIO14 is shown as the below Table 25.

Table 25. GPIO14 Multi-Function Configuration

Function	MX00C0[14]	MX00C1[4]	Note
GPIO14(Default)	0'b	X	GPIO Function
DACDAT4	1'b	0'b	I²S Data Input
MASTER_SCL3	1'b	1'b	3rd Master I²C Serial Clock

GPIO15/ADCDAT4/MASTER_SDA3 – Pin K6

The function configuration of the GPIO15 is shown as the below Table 26.

Table 26. GPIO15 Multi-Function Configuration

Function	MX00C0[14]	MX00C1[4]	Note
GPIO15(Default)	0'b	X	GPIO Function
ADCDAT4	1'b	0'b	I^2S Data Output
MASTER_SDA3	1'b	1'b	3rd Master I^2C Serial Data

GPIO16/SPI_SCL_FLASH/DMIC3_SCL/PRESS_DET – Pin K8

The function configuration of the GPIO16 is shown as the below Table 27.

Table 27. GPIO16 Multi-Function Configuration

Function	MX00C0[3:2]	MX00CF[15]	Note
GPIO16	0'b	00'b	GPIO Function
DMIC3_SCL	0'b	01'b	DMIC Clock
SPI_SCL_FLASH (Default)	0'b	10'b	SPI Flash Serial Clock
PRESS_DET	1'b	X	Power Key Press Detection

GPIO17/BCLK2 – Pin P6

The function configuration of the GPIO17 is shown as the below Table 28.

Table 28. GPIO17 Multi-Function Configuration

Function	MX00C0[0]	Note
GPIO17(Default)	0'b	GPIO Function
BCLK2	1'b	I^2S Bit Clock

GPIO18/LRCK2 – Pin R7

The function configuration of the GPIO18 is shown as the below Table 29.

Table 29. GPIO18 Multi-Function Configuration

Function	MX00C0[0]	Note
GPIO18(Default)	0'b	GPIO Function
LRCK2	1'b	I^2S Serial Synchronous Clock

GPIO19/DACDAT2 – Pin R9

The function configuration of the GPIO19 is shown as the below Table 30.

Table 30. GPIO19 Multi-Function Configuration

Function	MX00C0[0]	Note
GPIO19(Default)	0'b	GPIO Function
DACDAT2	1'b	I^2S Data Input

GPIO20/ADCDAT2/SPDIFIN – Pin P10

The function configuration of the GPIO20 is shown as the below Table 31.

Table 31. GPIO20 Multi-Function Configuration

Function	MX00C0[0]	MX00C0[1]	Note
GPIO20(Default)	0'b	0'b	GPIO Function
ADCDAT2	1'b	X	I^2S Data Output
SPDIFIN	0'b	1'b	SPDIF Data Input

GPIO21/DMIC1_SCL/SPI_SCL_M2 – Pin L3

The function configuration of the GPIO21 is shown as the below Table 32.

Table 32. GPIO21 Multi-Function Configuration

Function	MX00C2[15:14]	Note
GPIO21(Default)	00'b	GPIO Function
DMIC1_SCL	01'b	DMIC Clock
SPI_SCL_M2	10'b	2nd Master SPI Serial Clock

GPIO22/DMIC1_SDA/SPI_CS_M2 – Pin M4

The function configuration of the GPIO22 is shown as the below Table 33.

Table 33. GPIO22 Multi-Function Configuration

Function	MX00C2[13:12]	Note
GPIO22(Default)	00'b	GPIO Function
DMIC1_SDA	01'b	DMIC Data
SPI_CS_M2	10'b	2nd Master SPI Chip Select

GPIO23/DMIC2_SDA/SPIO_MOSI_M2 – Pin M6

The function configuration of the GPIO23 is shown as the below Table 34.

Table 34. GPIO23 Multi-Function Configuration

Function	MX00C2[11:10]	Note
GPIO23(Default)	00'b	GPIO Function
DMIC2_SDA	01'b	DMIC Data
SPI_MOSI_M2	10'b	2nd Master SPI MOSI

GPIO24/DMIC3_SDA/SPIO_MISO_M2 – Pin N11

The function configuration of the GPIO24 is shown as the below Table 35.

Table 35. GPIO24 Multi-Function Configuration

Function	MX00C2[9:8]	Note
GPIO24(Default)	00'b	GPIO Function
DMIC3_SDA	01'b	DMIC Data
SPI_MISO_M2	10'b	2nd Master SPI MISO

GPIO25/SPI_SCL_S/JTCK – Pin K12
The function configuration of the GPIO25 is shown as the below Table 36.

Table 36. GPIO25 Multi-Function Configuration

Function	MX00C1[3:2]	Note
SPI_SCL_S (Default)	00’b	Slave SPI Serial Clock
JTCK	01’b	JTAG Function
GPIO25	10’b	GPIO Function

GPIO26/SPI_CS_S/JTMS – Pin J15
The function configuration of the GPIO26 is shown as the below Table 37.

Table 37. GPIO26 Multi-Function Configuration

Function	MX00C1[3:2]	Note
SPI_CS_S (Default)	00’b	Slave SPI Chip Select
JTMS	01’b	JTAG Function
GPIO26	10’b	GPIO Function

GPIO27/SPI_MOSI_S/JTDI – Pin K14
The function configuration of the GPIO27 is shown as the below Table 38.

Table 38. GPIO27 Multi-Function Configuration

Function	MX00C1[3:2]	Note
SPI_MOSI_S (Default)	00’b	Slave SPI MOSI
JTDI	01’b	JTAG Function
GPIO27	10’b	GPIO Function

GPIO28/SPI_MISO_S/JTDO – Pin M14
The function configuration of the GPIO28 is shown as the below Table 39.

Table 39. GPIO28 Multi-Function Configuration

Function	MX00C1[3:2]	Note
SPI_MISO_S (Default)	00’b	Slave SPI MISO
JTDO	01’b	JTAG Function
GPIO28	10’b	GPIO Function

MCLK2/DMIC2_SCL/SPI_CS_FLASH– Pin N7
The function configuration of the MCLK2 is shown as the below Table 40.

Table 40. MCLK2 Multi-Function Configuration

Function	MX00C1[3:2]	Note
MCLK2	00’b	2nd Master Clock
DMIC2_SCL	01’b	DMIC Clock
SPI_CS_FLASH (Default)	10’b	SPI Flash Chip

		Select

MASTER_SCL1/SPI_MOSI_FLASH– Pin N13

The function configuration of the MASTER_SCL1 is shown as the below Table 41.

Table 41. MASTER_SCL1 Multi-Function Configuration

Function	MX00C1[10]	Note
MASTER_SCL1	0'b	1st Master I2C Serial Clock
SPI_MOSI_FLASH (Default)	1'b	SPI Flash MOSI

MASTER_SDA1/SPI_MOSI_FLASH– Pin P14

The function configuration of the MASTER_SDA1 is shown as the below Table 42.

Table 42. MASTER_SDA1 Multi-Function Configuration

Function	MX00C1[10]	Note
MASTER_SDA1	0'b	1st Master I2C Serial Data
SPI_MISO_FLASH (Default)	1'b	SPI Flash MISO

8.12. DRC and AGC Function

The CM7120 supports three-band DRC on the paly back path and single band DRC on the record path. The three-band DRC uses crossover filter to separate low frequency band, middle frequency band and high frequency band. The low frequency band signal will pass Bass Band DRC block, the middle band signal will pass Middle Band DRC block and the high frequency bad signal will pass High Band DRC block. The three bands signal sum with the digital mixer and pass the Post DRC block. The corner frequency of crossover filter can be adjusted by register settings. The details structure of the Three-Band DRC is shown in blow Figure 39

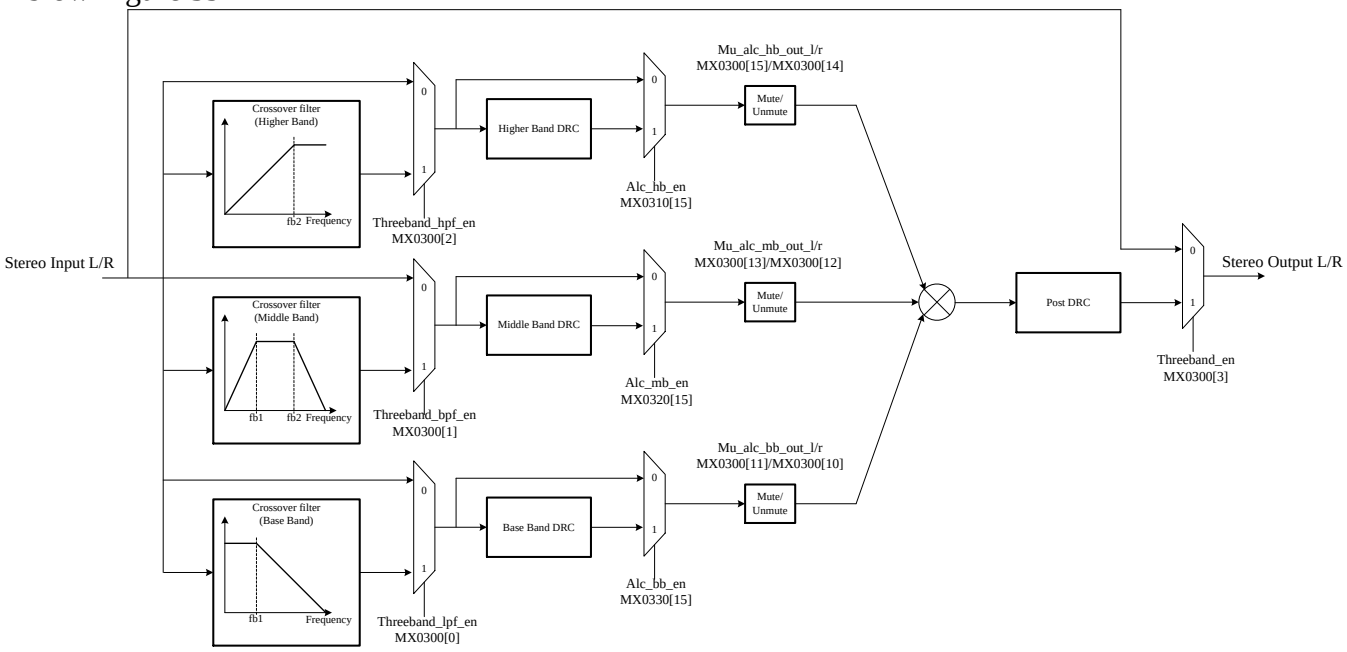


Figure 39. Three-Band DRC Structure

8.13. Equalizer Block

The CM7120 supports independent EQ function for DAC playback and ADC record.

For DAC playback path, the equalizer block cascades 22 bands (Figure 40) of equalizer to each channel to tailor the frequency characteristics of embedded speaker system according to user preferences and to emulate environment sound. The 22 bands equalizer includes three high pass filters, five band pass filters, two low pass filter and one biquad filter on the Lch an Rch. One high pass filter cascaded in the front end is used to drop low frequency tone, The tone has a large amplitude and may damage a mini speaker. The high pass filter can be used to adjust Treble strength with gain control. One low pass filter with gain control can adjust the Bass strength. Three bands of band pass filters are used to emulate environment sounds, e.g., 'Pub', 'Live', 'Rock',… etc.. The gain, center frequency and bandwidth of each filter are all programmable. One biquad filter can switch to high-pass, low-pass or band-pass filter by register settings.

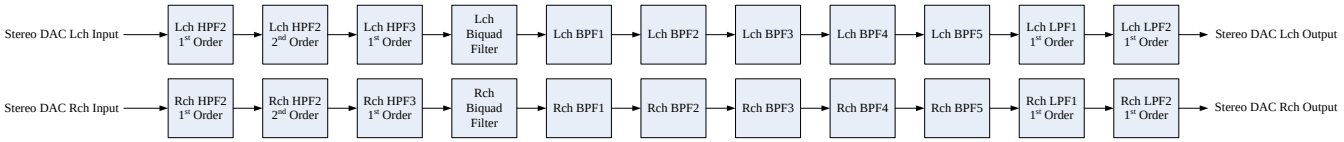


Figure 40. EQ Structure on the Playback Path

For ADC record path, the equalizer block cascades 12 bands (Figure 41) of equalizer to left and 62ight channel. The equalizers can used to do microphone device frequency compensation. The 12 bands equalizer include one low-pass-filter, four band-pass-filter and one high-pass-filter. The gain, center frequency and bandwidth of filter are also all programmable.

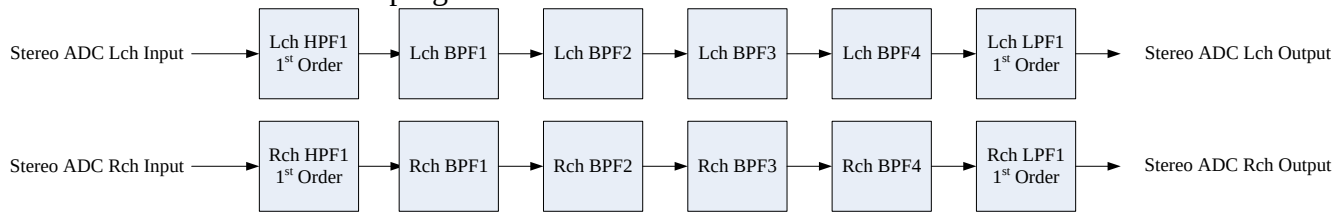


Figure 41. EQ Structure on the Record Path

8.14. Wind Noise Reduction Filter

The wind filter is implemented by a high pass filter equalizer. The wind filter is mainly for ADC recording used. The cut-off frequency of wind filter is programmable and is varied according to different sample rate. The filter is used to remove DC offset at normal condition, and to remove wind noise at application mode. There are four wind filters for four ADC filters:
Stereo1 ADC Wind Filter => MX-00D0 & MX-00D1
Mono ADC Wind Filter => MX-00D2 & MX-00D3
Stereo2 ADC Wind Filter => MX-00D4 & MX-00D5
Stereo3 ADC Wind Filter => MX-00D6 & MX-00D7

Wind filter setting procedure (For example: Stereo1 ADC Filter):

Step1: Disable wind filter – MX-00D0[15]

Step2: Select filter coarse coefficient – MX-00D0[14:12] and MX-00D0[10:8]

Step3: Select filter fine coefficient – MX-00D1[13:8] and MX-00D1[5:0]

Step4: Enable wind filter – MX-00D0[15]

The following table (Table 43~Table 47.) is shown the Fc with sample rate selection.
For the formula of Fc calculation is also shown as:

$Fc = (Fs * \tan^{-1}(a/(2-a))) / \pi$

Where:
When MX-00D0[14:12] and MX-00D0[10:8]=000'b , $a = 2^{-6} + n * 2^{-6}$ (n is MX-00D1[13:8] & MX-00D1[5:0])
When MX-00D0[14:12] and MX-00D0[10:8]=001'b , $a = 2^{-7} + n * 2^{-7}$ (n is MX-00D1[13:8] & MX-00D1[5:0])
When MX-00D0[14:12] and MX-00D0[10:8]=010'b , $a = 2^{-8} + n * 2^{-8}$ (n is MX-00D1[13:8] & MX-00D1[5:0])
When MX-00D0[14:12] and MX-00D0[10:8]=011'b , $a = 2^{-9} + n * 2^{-9}$ (n is MX-00D1[13:8] & MX-00D1[5:0])
When MX-00D0[14:12] and MX-00D0[10:8]=100'b , $a = 2^{-10} + n * 2^{-10}$ (n is MX-00D1[13:8] & MX-00D1[5:0])

Table 43. Stereo ADC 1 Filter Wind Filter Fc Selection when MX00D0[14:12] and MX00D0[10:8]=000'b

MX00D1[13:8] MX00D1[5:0]		L & R Channel Sampling Rate Setting (Hz)				
		8000	16000	32000	44100	48000
n(HEX)	n(DEC)	Fc (Hz)				
000000	0	20.05062	40.10124	80.20248	110.529	120.3037
000001	1	40.41694	80.83389	161.6678	222.7984	242.5017
000010	2	61.10382	122.2076	244.4153	336.8348	366.6229
000011	3	82.11608	164.2322	328.4643	452.6649	492.6965
000100	4	103.4585	206.9171	413.8341	570.3152	620.7512
000101	5	125.136	250.2719	500.5438	689.812	750.8157
000110	6	147.1531	294.3062	588.6123	811.1814	882.9185

000111	**7**	169.5146	339.0292	678.0583	934.4491	1017.087
001000	**8**	192.2251	384.4501	768.9003	1059.641	1153.35
001001	**9**	215.2891	430.5782	861.1563	1186.781	1291.735
001010	**10**	238.7111	477.4222	954.8443	1315.895	1432.266
001011	**11**	262.4954	524.9908	1049.982	1447.006	1574.972
001100	**12**	286.6462	573.2925	1146.585	1580.137	1719.877
001101	**13**	311.1677	622.3354	1244.671	1715.312	1867.006
001110	**14**	336.0638	672.1275	1344.255	1852.552	2016.383
001111	**15**	361.3382	722.6764	1445.353	1991.877	2168.029
010000	**16**	386.9946	773.9891	1547.978	2133.308	2321.967
010001	**17**	413.0363	826.0726	1652.145	2276.863	2478.218
010010	**18**	439.4665	878.9331	1757.866	2422.559	2636.799
010011	**19**	466.2883	932.5765	1865.153	2570.414	2797.73
010100	**20**	493.5041	987.0083	1974.017	2720.441	2961.025
010101	**21**	521.1165	1042.233	2084.466	2872.655	3126.699
010110	**22**	549.1276	1098.255	2196.51	3027.066	3294.765
010111	**23**	577.539	1155.078	2310.156	3183.684	3465.234
011000	**24**	606.3523	1212.705	2425.409	3342.517	3638.114
011001	**25**	635.5684	1271.137	2542.274	3503.571	3813.411
011010	**26**	665.1881	1330.376	2660.752	3666.849	3991.129
011011	**27**	695.2115	1390.423	2780.846	3832.354	4171.269
011100	**28**	725.6385	1451.277	2902.554	4000.082	4353.831
011101	**29**	756.4684	1512.937	3025.874	4170.032	4538.811
011110	**30**	787.7001	1575.4	3150.8	4342.197	4726.2
011111	**31**	819.3318	1638.664	3277.327	4516.566	4915.991
100000	**32**	851.3613	1702.723	3405.445	4693.129	5108.168
100001	**33**	883.7859	1767.572	3535.143	4871.87	5302.715
100010	**34**	916.6022	1833.204	3666.409	5052.769	5499.613
100011	**35**	949.8062	1899.612	3799.225	5235.807	5698.837
100100	**36**	983.3935	1966.787	3933.574	5420.957	5900.361
100101	**37**	1017.359	2034.717	4069.435	5608.19	6104.152
100110	**38**	1051.696	2103.392	4206.784	5797.474	6310.176
100111	**39**	1086.399	2172.798	4345.596	5988.774	6518.393
101000	**40**	1121.46	2242.92	4485.84	6182.049	6728.761
101001	**41**	1156.872	2313.743	4627.487	6377.255	6941.23
101010	**42**	1192.625	2385.25	4770.501	6574.346	7155.751

101011	**43**	1228.711	2457.422	4914.844	6773.27	7372.266
101100	**44**	1265.119	2530.239	5060.478	6973.971	7590.716
101101	**45**	1301.839	2603.679	5207.358	7176.39	7811.037
101110	**46**	1338.86	2677.719	5355.439	7380.464	8033.158
101111	**47**	1376.168	2752.336	5504.672	7586.127	8257.009
110000	**48**	1413.752	2827.504	5655.007	7793.307	8482.511
110001	**49**	1451.597	2903.195	5806.389	8001.93	8709.584
110010	**50**	1489.691	2979.381	5958.762	8211.919	8938.143
110011	**51**	1528.017	3056.033	6112.066	8423.192	9168.1
110100	**52**	1566.56	3133.12	6266.241	8635.663	9399.361
110101	**53**	1605.305	3210.611	6421.222	8849.246	9631.832
110110	**54**	1644.236	3288.471	6576.943	9063.849	9865.414
110111	**55**	1683.334	3366.668	6733.336	9279.379	10100
111000	**56**	1722.583	3445.166	6890.332	9495.739	10335.5
111001	**57**	1761.965	3523.93	7047.859	9712.831	10571.79
111010	**58**	1801.461	3602.922	7205.844	9930.554	10808.77
111011	**59**	1841.053	3682.107	7364.213	10148.81	11046.32
111100	**60**	1880.723	3761.445	7522.891	10367.48	11284.34
111101	**61**	1920.45	3840.9	7681.8	10586.48	11522.7
111110	**62**	1960.216	3920.432	7840.865	10805.69	11761.3
111111	**63**	2000.002	4000.003	8000.007	11025.01	12000.01

Table 44. Stereo ADC 1 Filter Wind Filter Fc Selection when MX00D0[14:12] and MX00D0[10:8]=001'b

MX00D1[13:8] MX00D1[5:0]		**L & R Channel Sampling Rate Setting (Hz)**				
		8000	**16000**	**32000**	**44100**	**48000**
n(HEX)	**n(DEC)**	**Fc (Hz)**				
000000	**0**	9.98615	19.9723	39.9446	55.04865	59.9169
000001	**1**	20.05062	40.10124	80.20248	110.529	120.3037
000010	**2**	30.19401	60.38803	120.7761	166.4445	181.1641
000011	**3**	40.41694	80.83389	161.6678	222.7984	242.5017
000100	**4**	50.72001	101.44	202.88	279.5941	304.3201
000101	**5**	61.10382	122.2076	244.4153	336.8348	366.6229
000110	**6**	71.56898	143.138	286.2759	394.524	429.4139
000111	**7**	82.11608	164.2322	328.4643	452.6649	492.6965
001000	**8**	92.74574	185.4915	370.9829	511.2609	556.4744
001001	**9**	103.4585	206.9171	413.8341	570.3152	620.7512
001010	**10**	114.2551	228.5102	457.0203	629.8311	685.5305

001011	**11**	125.136	250.2719	500.5438	689.812	750.8157
001100	**12**	136.1018	272.2035	544.4071	750.261	816.6106
001101	**13**	147.1531	294.3062	588.6123	811.1814	882.9185
001110	**14**	158.2905	316.581	633.162	872.5763	949.743
001111	**15**	169.5146	339.0292	678.0583	934.4491	1017.087
010000	**16**	180.8259	361.6518	723.3037	996.8029	1084.955
010001	**17**	192.2251	384.4501	768.9003	1059.641	1153.35
010010	**18**	203.7126	407.4252	814.8504	1122.966	1222.276
010011	**19**	215.2891	430.5782	861.1563	1186.781	1291.735
010100	**20**	226.9551	453.9101	907.8202	1251.09	1361.73
010101	**21**	238.7111	477.4222	954.8443	1315.895	1432.266
010110	**22**	250.5577	501.1153	1002.231	1381.199	1503.346
010111	**23**	262.4954	524.9908	1049.982	1447.006	1574.972
011000	**24**	274.5247	549.0495	1098.099	1513.318	1647.148
011001	**25**	286.6462	573.2925	1146.585	1580.137	1719.877
011010	**26**	298.8604	597.7208	1195.442	1647.468	1793.162
011011	**27**	311.1677	622.3354	1244.671	1715.312	1867.006
011100	**28**	323.5687	647.1374	1294.275	1783.672	1941.412
011101	**29**	336.0638	672.1275	1344.255	1852.552	2016.383
011110	**30**	348.6535	697.3069	1394.614	1921.952	2091.921
011111	**31**	361.3382	722.6764	1445.353	1991.877	2168.029
100000	**32**	374.1184	748.2368	1496.474	2062.328	2244.71
100001	**33**	386.9946	773.9891	1547.978	2133.308	2321.967
100010	**34**	399.9671	799.9341	1599.868	2204.818	2399.802
100011	**35**	413.0363	826.0726	1652.145	2276.863	2478.218
100100	**36**	426.2027	852.4053	1704.811	2349.442	2557.216
100101	**37**	439.4665	878.9331	1757.866	2422.559	2636.799
100110	**38**	452.8283	905.6566	1811.313	2496.216	2716.97
100111	**39**	466.2883	932.5765	1865.153	2570.414	2797.73
101000	**40**	479.8468	959.6935	1919.387	2645.155	2879.081
101001	**41**	493.5041	987.0083	1974.017	2720.441	2961.025
101010	**42**	507.2606	1014.521	2029.042	2796.274	3043.564
101011	**43**	521.1165	1042.233	2084.466	2872.655	3126.699
101100	**44**	535.0721	1070.144	2140.288	2949.585	3210.433
101101	**45**	549.1276	1098.255	2196.51	3027.066	3294.765
101110	**46**	563.2831	1126.566	2253.133	3105.098	3379.699

101111	**47**	577.539	1155.078	2310.156	3183.684	3465.234
110000	**48**	591.8953	1183.791	2367.581	3262.823	3551.372
110001	**49**	606.3523	1212.705	2425.409	3342.517	3638.114
110010	**50**	620.9099	1241.82	2483.64	3422.766	3725.46
110011	**51**	635.5684	1271.137	2542.274	3503.571	3813.411
110100	**52**	650.3278	1300.656	2601.311	3584.932	3901.967
110101	**53**	665.1881	1330.376	2660.752	3666.849	3991.129
110110	**54**	680.1494	1360.299	2720.597	3749.323	4080.896
110111	**55**	695.2115	1390.423	2780.846	3832.354	4171.269
111000	**56**	710.3746	1420.749	2841.499	3915.94	4262.248
111001	**57**	725.6385	1451.277	2902.554	4000.082	4353.831
111010	**58**	741.0032	1482.006	2964.013	4084.78	4446.019
111011	**59**	756.4684	1512.937	3025.874	4170.032	4538.811
111100	**60**	772.0341	1544.068	3088.137	4255.838	4632.205
111101	**61**	787.7001	1575.4	3150.8	4342.197	4726.2
111110	**62**	803.466	1606.932	3213.864	4429.106	4820.796
111111	**63**	819.3318	1638.664	3277.327	4516.566	4915.991

Table 45. Stereo ADC 1 Filter Wind Filter Fc Selection when MX00D0[14:12] and MX00D0[10:8]=010'b

MX00D1[13:8] MX00D1[5:0]		**L & R Channel Sampling Rate Setting (Hz)**				
		8000	**16000**	**32000**	**44100**	**48000**
n(HEX)	**n(DEC)**	**Fc (Hz)**				
000000	**0**	4.983323	9.966646	19.93329	27.47057	29.89994
000001	**1**	9.98615	19.9723	39.9446	55.04865	59.9169
000010	**2**	15.00856	30.01711	60.03423	82.73467	90.05134
000011	**3**	20.05062	40.10124	80.20248	110.529	120.3037
000100	**4**	25.11241	50.22483	100.4497	138.4322	150.6745
000101	**5**	30.19401	60.38803	120.7761	166.4445	181.1641
000110	**6**	35.2955	70.591	141.182	194.5664	211.773
000111	**7**	40.41694	80.83389	161.6678	222.7984	242.5017
001000	**8**	45.55842	91.11684	182.2337	251.1408	273.3505
001001	**9**	50.72001	101.44	202.88	279.5941	304.3201
001010	**10**	55.90178	111.8036	223.6071	308.1586	335.4107
001011	**11**	61.10382	122.2076	244.4153	336.8348	366.6229
001100	**12**	66.32619	132.6524	265.3048	365.6231	397.9572
001101	**13**	71.56898	143.138	286.2759	394.524	429.4139
001110	**14**	76.83225	153.6645	307.329	423.5378	460.9935

001111	**15**	82.11608	164.2322	328.4643	452.6649	492.6965
010000	**16**	87.42055	174.8411	349.6822	481.9058	524.5233
010001	**17**	92.74574	185.4915	370.9829	511.2609	556.4744
010010	**18**	98.0917	196.1834	392.3668	540.7305	588.5502
010011	**19**	103.4585	206.9171	413.8341	570.3152	620.7512
010100	**20**	108.8463	217.6926	435.3852	600.0152	653.0778
010101	**21**	114.2551	228.5102	457.0203	629.8311	685.5305
010110	**22**	119.6849	239.3699	478.7398	659.7632	718.1096
010111	**23**	125.136	250.2719	500.5438	689.812	750.8157
011000	**24**	130.6082	261.2164	522.4328	719.9777	783.6492
011001	**25**	136.1018	272.2035	544.4071	750.261	816.6106
011010	**26**	141.6167	283.2334	566.4668	780.662	849.7002
011011	**27**	147.1531	294.3062	588.6123	811.1814	882.9185
011100	**28**	152.711	305.422	610.844	841.8193	916.2659
011101	**29**	158.2905	316.581	633.162	872.5763	949.743
011110	**30**	163.8917	327.7833	655.5667	903.4528	983.35
011111	**31**	169.5146	339.0292	678.0583	934.4491	1017.087
100000	**32**	175.1593	350.3186	700.6372	965.5657	1050.956
100001	**33**	180.8259	361.6518	723.3037	996.8029	1084.955
100010	**34**	186.5145	373.029	746.0579	1028.161	1119.087
100011	**35**	192.2251	384.4501	768.9003	1059.641	1153.35
100100	**36**	197.9578	395.9155	791.831	1091.242	1187.747
100101	**37**	203.7126	407.4252	814.8504	1122.966	1222.276
100110	**38**	209.4897	418.9794	837.9588	1154.812	1256.938
100111	**39**	215.2891	430.5782	861.1563	1186.781	1291.735
101000	**40**	221.1109	442.2217	884.4434	1218.874	1326.665
101001	**41**	226.9551	453.9101	907.8202	1251.09	1361.73
101010	**42**	232.8218	465.6436	931.2871	1283.43	1396.931
101011	**43**	238.7111	477.4222	954.8443	1315.895	1432.266
101100	**44**	244.623	489.246	978.4921	1348.484	1467.738
101101	**45**	250.5577	501.1153	1002.231	1381.199	1503.346
101110	**46**	256.5151	513.0302	1026.06	1414.04	1539.091
101111	**47**	262.4954	524.9908	1049.982	1447.006	1574.972
110000	**48**	268.4986	536.9971	1073.994	1480.098	1610.991
110001	**49**	274.5247	549.0495	1098.099	1513.318	1647.148
110010	**50**	280.5739	561.1479	1122.296	1546.664	1683.444

110011	**51**	286.6462	573.2925	1146.585	1580.137	1719.877
110100	**52**	292.7417	585.4834	1170.967	1613.739	1756.45
110101	**53**	298.8604	597.7208	1195.442	1647.468	1793.162
110110	**54**	305.0024	610.0047	1220.009	1681.326	1830.014
110111	**55**	311.1677	622.3354	1244.671	1715.312	1867.006
111000	**56**	317.3565	634.7129	1269.426	1749.427	1904.139
111001	**57**	323.5687	647.1374	1294.275	1783.672	1941.412
111010	**58**	329.8044	659.6089	1319.218	1818.047	1978.827
111011	**59**	336.0638	672.1275	1344.255	1852.552	2016.383
111100	**60**	342.3468	684.6935	1369.387	1887.187	2054.081
111101	**61**	348.6535	697.3069	1394.614	1921.952	2091.921
111110	**62**	354.9839	709.9678	1419.936	1956.849	2129.903
111111	**63**	361.3382	722.6764	1445.353	1991.877	2168.029

Table 46. Stereo ADC 1 Filter Wind Filter Fc Selection when MX00D0[14:12] and MX00D0[10:8]=011'b

MX00D1[13:8] MX00D1[5:0]		**L & R Channel Sampling Rate Setting (Hz)**				
		8000	**16000**	**32000**	**44100**	**48000**
n(HEX)	**n(DEC)**	**Fc (Hz)**				
000000	**0**	2.489228	4.978456	9.956913	13.72187	14.93537
000001	**1**	4.983323	9.966646	19.93329	27.47057	29.89994
000010	**2**	7.482294	14.96459	29.92917	41.24614	44.89376
000011	**3**	9.98615	19.9723	39.9446	55.04865	59.9169
000100	**4**	12.4949	24.9898	49.9796	68.87814	74.96941
000101	**5**	15.00856	30.01711	60.03423	82.73467	90.05134
000110	**6**	17.52713	35.05425	70.1085	96.61828	105.1628
000111	**7**	20.05062	40.10124	80.20248	110.529	120.3037
001000	**8**	22.57904	45.15809	90.31618	124.467	135.4743
001001	**9**	25.11241	50.22483	100.4497	138.4322	150.6745
001010	**10**	27.65073	55.30147	110.6029	152.4247	165.9044
001011	**11**	30.19401	60.38803	120.7761	166.4445	181.1641
001100	**12**	32.74227	65.48453	130.9691	180.4917	196.4536
001101	**13**	35.2955	70.591	141.182	194.5664	211.773
001110	**14**	37.85372	75.70744	151.4149	208.6686	227.1223
001111	**15**	40.41694	80.83389	161.6678	222.7984	242.5017
010000	**16**	42.98517	85.97035	171.9407	236.9558	257.911
010001	**17**	45.55842	91.11684	182.2337	251.1408	273.3505
010010	**18**	48.1367	96.27339	192.5468	265.3535	288.8202

010011	**19**	50.72001	101.44	202.88	279.5941	304.3201
010100	**20**	53.30837	106.6167	213.2335	293.8624	319.8502
010101	**21**	55.90178	111.8036	223.6071	308.1586	335.4107
010110	**22**	58.50026	117.0005	234.0011	322.4827	351.0016
010111	**23**	61.10382	122.2076	244.4153	336.8348	366.6229
011000	**24**	63.71246	127.4249	254.8498	351.2149	382.2748
011001	**25**	66.32619	132.6524	265.3048	365.6231	397.9572
011010	**26**	68.94503	137.8901	275.7801	380.0595	413.6702
011011	**27**	71.56898	143.138	286.2759	394.524	429.4139
011100	**28**	74.19805	148.3961	296.7922	409.0167	445.1883
011101	**29**	76.83225	153.6645	307.329	423.5378	460.9935
011110	**30**	79.47159	158.9432	317.8864	438.0871	476.8295
011111	**31**	82.11608	164.2322	328.4643	452.6649	492.6965
100000	**32**	84.76573	169.5315	339.0629	467.2711	508.5944
100001	**33**	87.42055	174.8411	349.6822	481.9058	524.5233
100010	**34**	90.08055	180.1611	360.3222	496.569	540.4833
100011	**35**	92.74574	185.4915	370.9829	511.2609	556.4744
100100	**36**	95.41612	190.8322	381.6645	525.9813	572.4967
100101	**37**	98.0917	196.1834	392.3668	540.7305	588.5502
100110	**38**	100.7725	201.545	403.09	555.5085	604.635
100111	**39**	103.4585	206.9171	413.8341	570.3152	620.7512
101000	**40**	106.1498	212.2996	424.5992	585.1508	636.8988
101001	**41**	108.8463	217.6926	435.3852	600.0152	653.0778
101010	**42**	111.5481	223.0961	446.1922	614.9087	669.2884
101011	**43**	114.2551	228.5102	457.0203	629.8311	685.5305
101100	**44**	116.9674	233.9347	467.8695	644.7826	701.8042
101101	**45**	119.6849	239.3699	478.7398	659.7632	718.1096
101110	**46**	122.4078	244.8156	489.6312	674.773	734.4468
101111	**47**	125.136	250.2719	500.5438	689.812	750.8157
110000	**48**	127.8694	255.7388	511.4777	704.8802	767.2165
110001	**49**	130.6082	261.2164	522.4328	719.9777	783.6492
110010	**50**	133.3523	266.7046	533.4093	735.1047	800.1139
110011	**51**	136.1018	272.2035	544.4071	750.261	816.6106
110100	**52**	138.8566	277.7131	555.4262	765.4467	833.1393
110101	**53**	141.6167	283.2334	566.4668	780.662	849.7002
110110	**54**	144.3822	288.7644	577.5288	795.9069	866.2932

110111	**55**	147.1531	294.3062	588.6123	811.1814	882.9185
111000	**56**	149.9293	299.8587	599.7174	826.4855	899.576
111001	**57**	152.711	305.422	610.844	841.8193	916.2659
111010	**58**	155.498	310.9961	621.9921	857.1829	932.9882
111011	**59**	158.2905	316.581	633.162	872.5763	949.743
111100	**60**	161.0884	322.1767	644.3535	887.9996	966.5302
111101	**61**	163.8917	327.7833	655.5667	903.4528	983.35
111110	**62**	166.7004	333.4008	666.8016	918.936	1000.202
111111	**63**	169.5146	339.0292	678.0583	934.4491	1017.087

Table 47. Stereo ADC 1 Filter Wind Filter Fc Selection when MX00D0[14:12] and MX00D0[10:8]=100'b

MX00D1[13:8] MX00D1[5:0]		**L & R Channel Sampling Rate Setting (Hz)**				
		8000	**16000**	**32000**	**44100**	**48000**
n(HEX)	**n(DEC)**	**Fc (Hz)**				
000000	**0**	1.244006	2.488013	4.976025	6.857585	7.464038
000001	**1**	2.489228	4.978456	9.956913	13.72187	14.93537
000010	**2**	3.735667	7.471333	14.94267	20.59286	22.414
000011	**3**	4.983323	9.966646	19.93329	27.47057	29.89994
000100	**4**	6.232198	12.4644	24.92879	34.35499	37.39319
000101	**5**	7.482294	14.96459	29.92917	41.24614	44.89376
000110	**6**	8.73361	17.46722	34.93444	48.14403	52.40166
000111	**7**	9.98615	19.9723	39.9446	55.04865	59.9169
001000	**8**	11.23991	22.47983	44.95965	61.96002	67.43948
001001	**9**	12.4949	24.9898	49.9796	68.87814	74.96941
001010	**10**	13.75112	27.50223	55.00446	75.80302	82.50669
001011	**11**	15.00856	30.01711	60.03423	82.73467	90.05134
001100	**12**	16.26723	32.53445	65.06891	89.67309	97.60336
001101	**13**	17.52713	35.05425	70.1085	96.61828	105.1628
001110	**14**	18.78826	37.57651	75.15303	103.5703	112.7295
001111	**15**	20.05062	40.10124	80.20248	110.529	120.3037
010000	**16**	21.31421	42.62843	85.25686	117.4946	127.8853
010001	**17**	22.57904	45.15809	90.31618	124.467	135.4743
010010	**18**	23.84511	47.69022	95.38044	131.4462	143.0707
010011	**19**	25.11241	50.22483	100.4497	138.4322	150.6745
010100	**20**	26.38095	52.76191	105.5238	145.425	158.2857
010101	**21**	27.65073	55.30147	110.6029	152.4247	165.9044
010110	**22**	28.92175	57.84351	115.687	159.4312	173.5305

010111	**23**	30.19401	60.38803	120.7761	166.4445	181.1641
011000	**24**	31.46752	62.93504	125.8701	173.4647	188.8051
011001	**25**	32.74227	65.48453	130.9691	180.4917	196.4536
011010	**26**	34.01826	68.03652	136.073	187.5257	204.1096
011011	**27**	35.2955	70.591	141.182	194.5664	211.773
011100	**28**	36.57399	73.14797	146.2959	201.6141	219.4439
011101	**29**	37.85372	75.70744	151.4149	208.6686	227.1223
011110	**30**	39.13471	78.26941	156.5388	215.7301	234.8082
011111	**31**	40.41694	80.83389	161.6678	222.7984	242.5017
100000	**32**	41.70043	83.40086	166.8017	229.8736	250.2026
100001	**33**	42.98517	85.97035	171.9407	236.9558	257.911
100010	**34**	44.27117	88.54234	177.0847	244.0448	265.627
100011	**35**	45.55842	91.11684	182.2337	251.1408	273.3505
100100	**36**	46.84693	93.69386	187.3877	258.2437	281.0816
100101	**37**	48.1367	96.27339	192.5468	265.3535	288.8202
100110	**38**	49.42772	98.85545	197.7109	272.4703	296.5663
100111	**39**	50.72001	101.44	202.88	279.5941	304.3201
101000	**40**	52.01356	104.0271	208.0542	286.7247	312.0813
101001	**41**	53.30837	106.6167	213.2335	293.8624	319.8502
101010	**42**	54.60444	109.2089	218.4178	301.007	327.6267
101011	**43**	55.90178	111.8036	223.6071	308.1586	335.4107
101100	**44**	57.20039	114.4008	228.8016	315.3172	343.2023
101101	**45**	58.50026	117.0005	234.0011	322.4827	351.0016
101110	**46**	59.80141	119.6028	239.2056	329.6553	358.8084
101111	**47**	61.10382	122.2076	244.4153	336.8348	366.6229
110000	**48**	62.4075	124.815	249.63	344.0214	374.445
110001	**49**	63.71246	127.4249	254.8498	351.2149	382.2748
110010	**50**	65.01869	130.0374	260.0748	358.4155	390.1121
110011	**51**	66.32619	132.6524	265.3048	365.6231	397.9572
110100	**52**	67.63497	135.2699	270.5399	372.8378	405.8098
110101	**53**	68.94503	137.8901	275.7801	380.0595	413.6702
110110	**54**	70.25636	140.5127	281.0254	387.2882	421.5382
110111	**55**	71.56898	143.138	286.2759	394.524	429.4139
111000	**56**	72.88287	145.7657	291.5315	401.7668	437.2972
111001	**57**	74.19805	148.3961	296.7922	409.0167	445.1883
111010	**58**	75.5145	151.029	302.058	416.2737	453.087

111011	**59**	76.83225	153.6645	307.329	423.5378	460.9935
111100	**60**	78.15128	156.3026	312.6051	430.8089	468.9077
111101	**61**	79.47159	158.9432	317.8864	438.0871	476.8295
111110	**62**	80.79319	161.5864	323.1728	445.3725	484.7591
111111	**63**	82.11608	164.2322	328.4643	452.6649	492.6965

8.15. SPI Slave Mode Control Interface

The SPI slave interface was support in CM7120. The transmit rate is up to 28Mhz.

SPI Write Command:

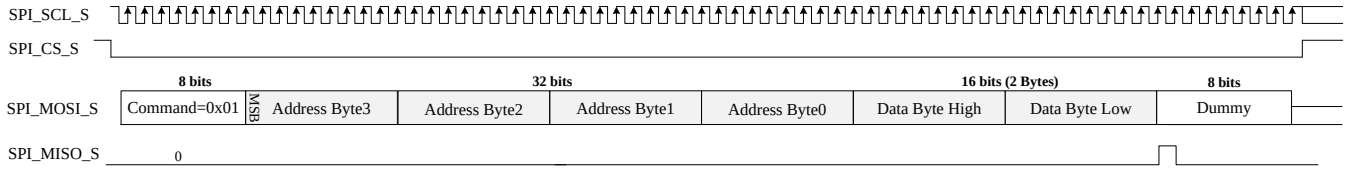
CMD Phase	Address Phase	Data Phase	Dummy Phase

Table 48. SPI Slave Write Command Format

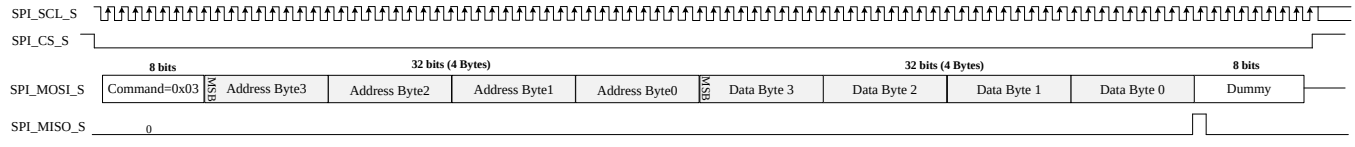
	CMD Phase	Address Phase	Data Phase	Dummy Phase	ACK
Single 32 Bits Address/16 Bits Data Write	0x01	32 bits	16 bits	8bits	1bit
Single 32 Bits Address/32 Bits Data Write	0x03	32 bits	32 bits	8bits	1bit
Burst Write	0x05	32 bits	64*N bits	8bits	1bit per 64bits
Single 16 Bits Address/16 Bits Data Write	0x09	16 bits	16 bits	8bits	1 bit

CMD PHASE: 8 bits command code
Address Phase: System bus memory space address
Data Phase: Write data
Dummy Phase: System bus write data
ACK Phase: Response ACK to SPI_MISO_S pin

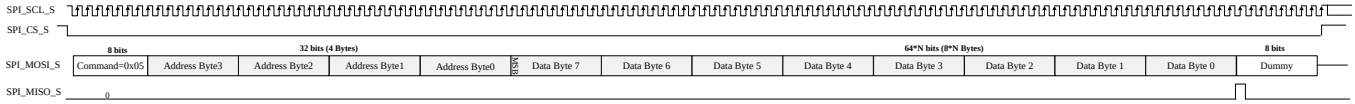
Single 32 Bits Address/16 Bits Data Write Mode:



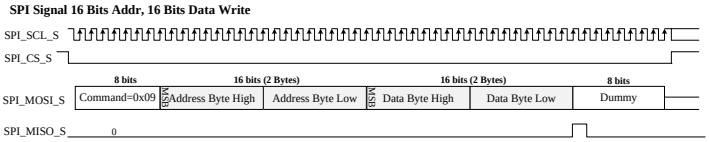
Single 32 Bits Address/32 Bits Data Write Mode:



Burst Write:



Single 16 Bits Address/16 Bits Data Write Mode:



SPI Read Command:

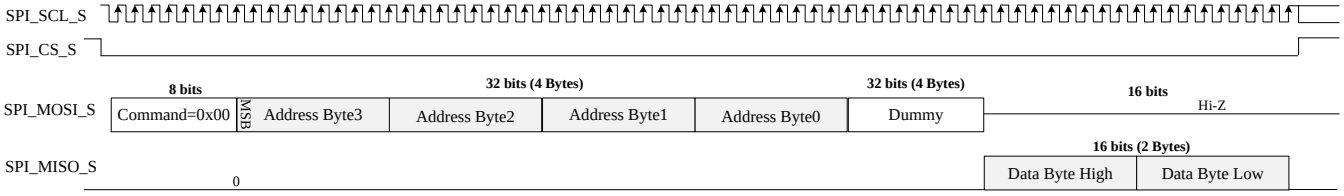
CMD Phase	Address Phase	Dummy Phase	Data Phase

Table 49. SPI Slave Read Command Format

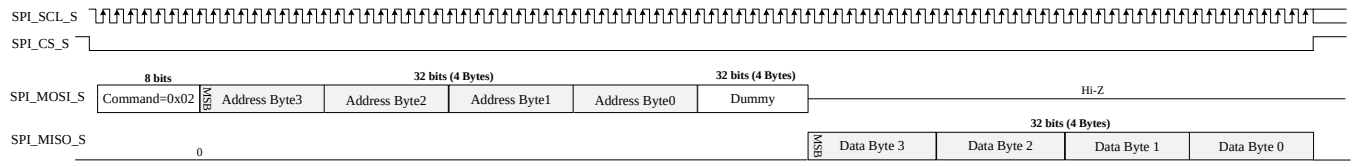
	CMD Phase	Address Phase	Data Phase	Dummy Phase	ACK
Single 32 Bits Address/16 Bits Data Read	0x00	32 bits	32 bits	16 bits	0 bit
Single 32 Bits Address/32 Bits Data Read	0x02	32 bits	32 bits	32 bits	0 bit
Burst Read	0x04	32 bits	32 bits	64*N bits	0 bit
Single 16 Bits Address/16 Bits Data Read	0x08	16 bits	32 bits	16 bits	0 bit

CMD PHASE: 8 bits command code
Address Phase: System bus memory space address
Dummy Phase: System bus prepare data
Data Phase: Read data

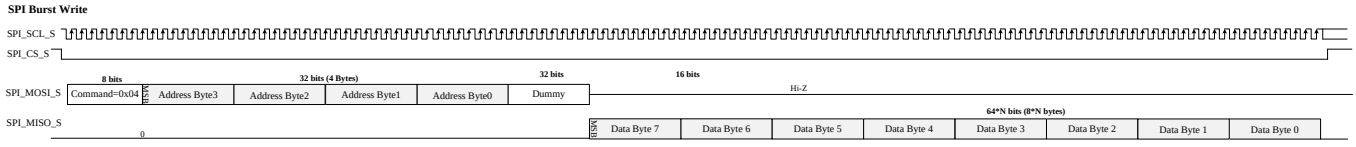
Single 32 Bits Address/16 Bits Data Read Mode:



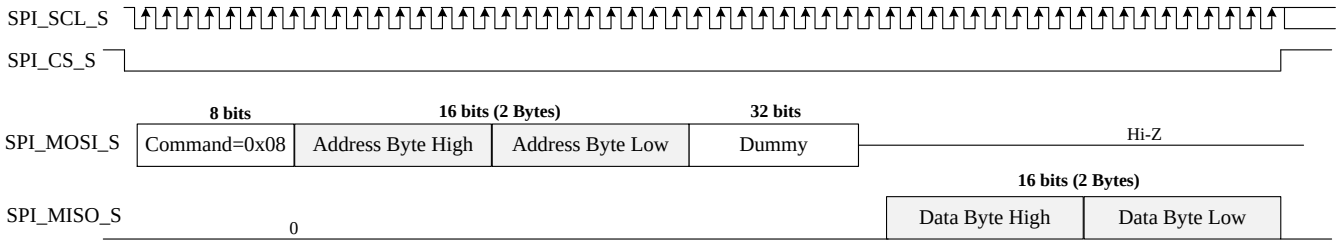
Single 32 Bits Address/32 Bits Data Read Mode:



Burst Read Mode:



Single 16 Bits Address/16 Bits Data Read Mode:



8.16. I²C Master Mode Control Interface

CM7120 can support three independent I²C master serial communication interface. MASTER_SCL1/2/3 are used for clock and MASTER_SDA1/2/3 are used for data. SCL clock supports up to 6.25MHz and can be selected to 1.5MHz, 400kHz or 100kHz. The register of the configuration is shown as below Table 50.

Table 50. Master I²C Clock Rate Selection

0x1800_9100 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Sel_i2cm_clk	1:0	+ 0x34	R/W	0'h	I2C master clock rate selection 00'b: 6.25MHz 01'b: 1.5MHz 10'b: 400kHz 11'b: 100kHz

7 Bits Device ID

There are 7 bits device ID can be set. 0x000 0000'b ~ 0x111 1111'b. The Table 52 ~ Table 54 show the configuration for the device ID of the each master I2C interface.

Table 51. 7-Bits Device ID

(MSB)			BIT				(LSB)
x	x	x	x	X	x	X	R/W

Table 52. 1st Master I²C Device ID Configuration

0x1800_9700 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Sel_i2c1_device_id	14:8	+ 0x0C	R/W	0'h	1st Master I²C Device ID

Table 53. 2nd Master I²C Device ID Configuration

0x1800_9C00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Sel_i2c2_device_id	14:8	+ 0x0C	R/W	0'h	2nd Master I²C Device ID

Table 54. 3rd Master I²C Device ID Configuration

0x1800_9D00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Sel_i2c3_device_id	14:8	+ 0x0C	R/W	0'h	3rd Master I2C Device ID

Register Address Length

There are up to 5 Bytes register address can be set. The below Table 55~Table 57 show the configuration for the address length.

Table 55. 1st Master I2C Address Length Configuration

0x1800_9700 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Sel_i2c1_addr_len	2:0	+ 0x0C	R/W	0'h	1st Master I2C Address Length 000'b: 1 Byte 001'b: 2 Bytes 010'b: 3 Bytes 011'b: 4 Bytes 100'b: 5 Bytes Other: Reserved

Table 56. 2nd Master I2C Address Length Configuration

0x1800_9C00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Sel_i2c2_addr_len	2:0	+ 0x0C	R/W	0'h	2nd Master I2C Address Length 000'b: 1 Byte 001'b: 2 Bytes 010'b: 3 Bytes 011'b: 4 Bytes 100'b: 5 Bytes Other: Reserved

Table 57. 3rd Master I2C Address Length Configuration

0x1800_9D00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Sel_i2c3_addr_len	2:0	+ 0x0C	R/W	0'h	3rd Master I2C Address Length 000'b: 1 Byte 001'b: 2 Bytes 010'b: 3 Bytes 011'b: 4 Bytes 100'b: 5 Bytes Other: Reserved

Register Address

The below Table 58~Table 60 show the configuration for the register address.
For example,
If the register address 0x01(1 Bytes) of the target will be read/wrote by CM7120 2nd Master I2C interface, the 0x18009C00 should be set to 0x00000001

If the register address 0x1234(2 Bytes) of the target will be read/wrote by CM7120 2nd Master I2C interface, the 0x18009C00 should be set to 0x00003412

Table 58. 1st Master I2C Register Address Configuration

0x1800_9700 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
i2c1_addr_byte5	7:0	+ 0x04	R/W	0'h	1st Master I2C Register Address
i2c1_addr_byte4	31:24	+ 0x00	R/W	0'h	
i2c1_addr_byte3	23:16	+ 0x00	R/W	0'h	
i2c1_addr_byte2	15:8	+ 0x00	R/W	0'h	
i2c1_addr_byte1	7:0	+ 0x00	R/W	0'h	

Table 59. 2nd Master I2C Register Address Configuration

0x1800_9C00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
i2c2_addr_byte5	7:0	+ 0x04	R/W	0'h	2nd Master I2C Register Address
i2c2_addr_byte4	31:24	+ 0x00	R/W	0'h	
i2c2_addr_byte3	23:16	+ 0x00	R/W	0'h	
i2c2_addr_byte2	15:8	+ 0x00	R/W	0'h	
i2c2_addr_byte1	7:0	+ 0x00	R/W	0'h	

Table 60. 3rd Master I2C Register Address Configuration

0x1800_9D00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
i2c3_addr_byte5	7:0	+ 0x04	R/W	0'h	3rd Master I2C Register Address
i2c3_addr_byte4	31:24	+ 0x00	R/W	0'h	
i2c3_addr_byte3	23:16	+ 0x00	R/W	0'h	
i2c3_addr_byte2	15:8	+ 0x00	R/W	0'h	
i2c3_addr_byte1	7:0	+ 0x00	R/W	0'h	

Register Data Length

There are up to 4 Bytes register data can be set. The below Table 61~Table 63 show the configuration for the data length.

Table 61. 1st Master I2C Data Length Configuration

0x1800_9700 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Sel_i2c1_data_len	6:4	+ 0x0C	R/W	0'h	1st Master I2C Data Length 000'b: 0 Byte 001'b: 1 Byte 010'b: 2 Bytes 011'b: 3 Bytes 100'b: 4 Bytes Other: Reserved

Table 62. 2nd Master I2C Data Length Configuration

0x1800_9C00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Sel_i2c2_data_len	6:4	+ 0x0C	R/W	0'h	2nd Master I2C Data Length 000'b: 0 Byte 001'b: 1 Byte 010'b: 2 Bytes 011'b: 3 Bytes 100'b: 4 Bytes Other: Reserved

Table 63. 3rd Master I2C Data Length Configuration

0x1800_9D00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Sel_i2c3_data_len	6:4	+ 0x0C	R/W	0'h	3rd Master I2C Data Length 000'b: 0 Byte 001'b: 1 Byte 010'b: 2 Bytes 011'b: 3 Bytes 100'b: 4 Bytes Other: Reserved

Write Register Data

The below Table 64~Table 66 show the configuration for the write register data.
For example,
If the register data 0x01(1 Bytes) of the target will be wrote by CM7120 2nd Master I2C interface, the 0x18009C08 should be set to 0x00000001
If the register data 0x1234(2 Bytes) of the target will be wrote by CM7120 2nd Master I2C interface, the 0x18009C08 should be set to 0x00003412

Table 64. 1st Master I2C Write Register Data Configuration

0x1800_9700 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
i2c1_wdata_byte4	31:24	+ 0x08	R/W	0'h	1st Master I2C Write Register Data
i2c1_wdata_byte3	23:16	+ 0x08	R/W	0'h	
i2c1_wdata_byte2	15:8	+ 0x08	R/W	0'h	
i2c1_wdata_byte1	7:0	+ 0x08	R/W	0'h	

Table 65. 2nd Master I2C Write Register Data Configuration

0x1800_9C00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
i2c2_wdata_byte4	31:24	+ 0x08	R/W	0'h	2nd Master I2C Write Register Data
i2c2_wdata_byte3	23:16	+ 0x08	R/W	0'h	
i2c2_wdata_byte2	15:8	+ 0x08	R/W	0'h	
i2c2_wdata_byte1	7:0	+ 0x08	R/W	0'h	

Table 66. 3rd Master I2C Write Register Data Configuration

0x1800_9D00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
i2c3_wdata_byte4	31:24	+ 0x08	R/W	0'h	3rd Master I2C Write Register Data
i2c3_wdata_byte3	23:16	+ 0x08	R/W	0'h	
i2c3_wdata_byte2	15:8	+ 0x08	R/W	0'h	
i2c3_wdata_byte1	7:0	+ 0x08	R/W	0'h	

Read Register Data

The below Table 67~Table 69 show the read register data for device.

Table 67. 1st Master I2C Read Register Data Configuration

0x1800_9700 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
i2c1_rdata_ 2	31:16	+ 0x18	R	0'h	1st Master I2C Read Register Data
i2c1_rdata_1	15:0	+ 0x18	R	0'h	

Table 68. 2nd Master I2C Read Register Data Configuration

0x1800_9C00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
i2c2_rdata_2	31:16	+ 0x18	R	0'h	2nd Master I2C Read Register Data
i2c2_rdata_1	15:0	+ 0x18	R	0'h	

Table 69. 3rd Master I2C Read Register Data Configuration

0x1800_9D00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
i2c3_rdata_2	31:16	+ 0x18	R	0'h	3rd Master I2C Read Register Data
i2c3_rdata_1	15:0	+ 0x18	R	0'h	

Read/Write Command

The setting of the read or write command on the Master I2C interface of CM7120 can be set by the below control bits.

Table 70. 1st Master I2C Read/Write Command Configuration

0x1800_9700 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
i2c1_r_w_cmd	1	+ 0x10	R/W	0'h	1st Master I2C Read/Write Command 0'b: Write Command 1'b: Read Command
i2c1_cmd_start	0	+ 0x10	R	0'h	1st Master I2C Command Start Write "1'b" to Start

Table 71. 2nd Master I2C Read/Write Command Configuration

0x1800_9C00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
i2c2_r_w_cmd	1	+ 0x10	R/W	0'h	2nd Master I2C Read/Write Command 0'b: Write Command 1'b: Read Command
i2c2_cmd_start	0	+ 0x10	R	0'h	2nd Master I2C Command Start Write "1'b" to Start

Table 72. 3rd Master I2C Read/Write Command Configuration

0x1800_9D00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
i2c3_r_w_cmd	1	+ 0x10	R/W	0'h	3rd Master I2C Read/Write Command 0'b: Write Command 1'b: Read Command
i2c3_cmd_start	0	+ 0x10	R	0'h	3rd Master I2C Command Start Write "1'b" to Start

8.17. SPI Master Mode Control Interface

CM7120 can support two independent SPI master serial communication interface. The SPI_SCL_M1/2 are used to generate SPI serial clock. The SPI_CS_M1/2 are used to as SPI chip selected. The SPI_MISO_M1/M2 are used to as SPI master input slave output. The SPI_MOSI_M1/M2 are used to as SPI master output slave input. The frequency of the SPI serial clock (spic_clk) can be selected by below clock tree (Figure 42).

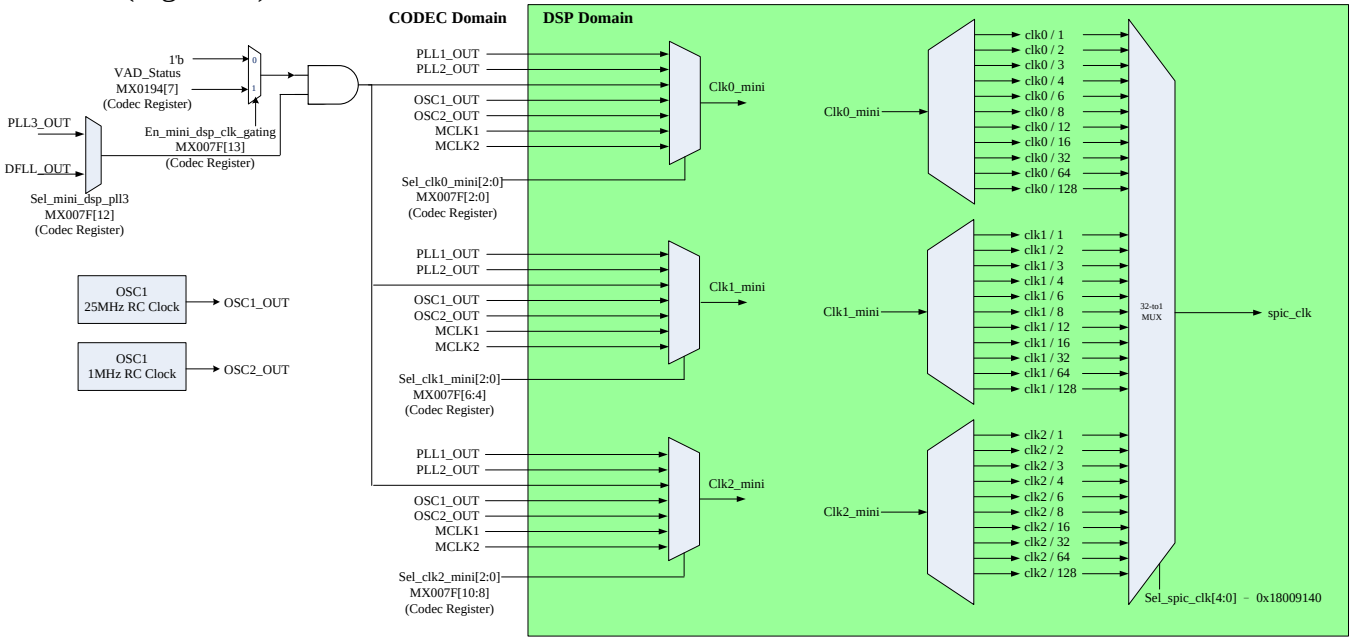


Figure 42. SPI Serial Clock Configuration

Auto/User Mode:

The below control register are used to select the Master SPI is auto or user mode. If you want to control the payload of the Tx (SPI_MOSI). The mode should be set to user mode

Table 73. 1st Master SPI Mode Configuration

0x1800_9A00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Spi_m1_mode_sel	3	+ 0x0C	R/W	0'h	1st Master SPI Mode Selection 0'b: Auto Mode 1'b: User Mode

Table 74. 2nd Master SPI Mode Configuration

0x1800_9B00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Spi_m2_mode_sel	3	+ 0x0C	R/W	0'h	2nd Master SPI Mode Selection 0'b: Auto Mode 1'b: User Mode

SPI_MOSI and SPI MISO Payload and Length:

The Master SPI Interface of CM7120 supports transmit 1~13 Bytes payload and receive 1~8 Bytes payload. The contents and length of the SPI_MOSI and SPI_MISO payload can be set by below register.

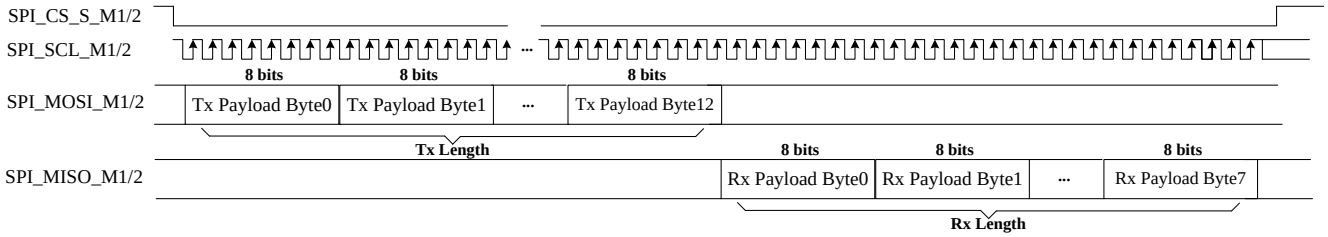


Figure 43. Master SPI Tx and Rx Payload Location

Table 75. 1st Master SPI Tx Length Configuration

0x1800_9A00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Spi_m1_tx_length	3:0	+ 0x20	R/W	0'h	1st Master SPI Tx Length Selection 0'h: 0 Byte 1'h: 1 Byte 2'h: 2 Bytes 3'h: 3 Bytes 4'h: 4 Bytes 5'h: 5 Bytes 6'h: 6 Bytes 7'h: 7 Bytes 8'h: 8 Bytes 9'h: 9 Bytes A'h: 10 Bytes B'h: 11 Bytes C'h: 12 Bytes

					D'h: 13 Bytes Others: Reserved

Table 76. 1st Master SPI Tx Payload Configuration

0x1800_9A00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Spi_m1_tx_payload12	7:0	+ 0x1C	R/W	0'h	1st Master SPI Tx Payload Byte 12
Spi_m1_tx_payload11	31:24	+ 0x18	R/W	0'h	1st Master SPI Tx Payload Byte 11
Spi_m1_tx_payload10	23:16	+ 0x18	R/W	0'h	1st Master SPI Tx Payload Byte 10
Spi_m1_tx_payload9	15:8	+ 0x18	R/W	0'h	1st Master SPI Tx Payload Byte 9
Spi_m1_tx_payload8	7:0	+ 0x18	R/W	0'h	1st Master SPI Tx Payload Byte 8
Spi_m1_tx_payload7	31:24	+ 0x14	R/W	0'h	1st Master SPI Tx Payload Byte 7
Spi_m1_tx_payload6	23:16	+ 0x14	R/W	0'h	1st Master SPI Tx Payload Byte 6
Spi_m1_tx_payload5	15:8	+ 0x14	R/W	0'h	1st Master SPI Tx Payload Byte 5
Spi_m1_tx_payload4	7:0	+ 0x14	R/W	0'h	1st Master SPI Tx Payload Byte 4
Spi_m1_tx_payload3	31:24	+ 0x10	R/W	0'h	1st Master SPI Tx Payload Byte 3
Spi_m1_tx_payload2	23:16	+ 0x10	R/W	0'h	1st Master SPI Tx Payload Byte 2
Spi_m1_tx_payload1	15:8	+ 0x10	R/W	0'h	1st Master SPI Tx Payload Byte 1
Spi_m1_tx_payload0	7:0	+ 0x10	R/W	0'h	1st Master SPI Tx Payload Byte 0

Table 77. 2nd Master SPI Tx Length Configuration

0x1800_9B00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Spi_m2_tx_length	3:0	+ 0x20	R/W	0'h	2nd Master SPI Tx Length Selection 0'h: 0 Byte 1'h: 1 Byte 2'h: 2 Bytes 3'h: 3 Bytes 4'h: 4 Bytes 5'h: 5 Bytes 6'h: 6 Bytes 7'h: 7 Bytes 8'h: 8 Bytes 9'h: 9 Bytes A'h: 10 Bytes B'h: 11 Bytes C'h: 12 Bytes D'h: 13 Bytes Others: Reserved

Table 78. 2nd Master SPI Tx Payload Configuration

0x1800_9B00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Spi_m2_tx_payload12	7:0	+ 0x1C	R/W	0'h	2nd Master SPI Tx Payload Byte 12
Spi_m2_tx_payload11	31:24	+ 0x18	R/W	0'h	2nd Master SPI Tx Payload Byte 11
Spi_m2_tx_payload10	23:16	+ 0x18	R/W	0'h	2nd Master SPI Tx Payload Byte 10
Spi_m2_tx_payload9	15:8	+ 0x18	R/W	0'h	2nd Master SPI Tx Payload Byte 9
Spi_m2_tx_payload8	7:0	+ 0x18	R/W	0'h	2nd Master SPI Tx Payload Byte 8

Spi_m2_tx_payload7	31:24	+ 0x14	R/W	0'h	2nd Master SPI Tx Payload Byte 7
Spi_m2_tx_payload6	23:16	+ 0x14	R/W	0'h	2nd Master SPI Tx Payload Byte 6
Spi_m2_tx_payload5	15:8	+ 0x14	R/W	0'h	2nd Master SPI Tx Payload Byte 5
Spi_m2_tx_payload4	7:0	+ 0x14	R/W	0'h	2nd Master SPI Tx Payload Byte 4
Spi_m2_tx_payload3	31:24	+ 0x10	R/W	0'h	2nd Master SPI Tx Payload Byte 3
Spi_m2_tx_payload2	23:16	+ 0x10	R/W	0'h	2nd Master SPI Tx Payload Byte 2
Spi_m2_tx_payload1	15:8	+ 0x10	R/W	0'h	2nd Master SPI Tx Payload Byte 1
Spi_m2_tx_payload0	7:0	+ 0x10	R/W	0'h	2nd Master SPI Tx Payload Byte 0

Table 79. 1st Master SPI Rx Length Configuration

0x1800_9A00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Spi_m1_rx_length	7:4	+ 0x20	R/W	0'h	1st Master SPI Rx Length Selection 0'h: 0 Byte 1'h: 1 Byte 2'h: 2 Bytes 3'h: 3 Bytes 4'h: 4 Bytes 5'h: 5 Bytes 6'h: 6 Bytes 7'h: 7 Bytes 8'h: 8 Bytes Others: Reserved

Table 80. 1st Master SPI Rx Payload Data

0x1800_9A00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Spi_m1_rx_payload7	31:24	+ 0x2C	R	0'h	1st Master SPI Rx Payload Byte 7
Spi_m1_rx_payload6	23:16	+ 0x2C	R	0'h	1st Master SPI Rx Payload Byte 6
Spi_m1_rx_payload5	15:8	+ 0x2C	R	0'h	1st Master SPI Rx Payload Byte 5
Spi_m1_rx_payload4	7:0	+ 0x2C	R	0'h	1st Master SPI Rx Payload Byte 4
Spi_m1_rx_payload3	31:24	+ 0x28	R	0'h	1st Master SPI Rx Payload Byte 3
Spi_m1_rx_payload2	23:16	+ 0x28	R	0'h	1st Master SPI Rx Payload Byte 2
Spi_m1_rx_payload1	15:8	+ 0x28	R	0'h	1st Master SPI Rx Payload Byte 1
Spi_m1_rx_payload0	7:0	+ 0x28	R	0'h	1st Master SPI Rx Payload Byte 0

Table 81. 2nd Master SPI Rx Length Configuration

0x1800_9B00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Spi_m2_rx_length	7:4	+ 0x20	R/W	0'h	2nd Master SPI Rx Length Selection 0'h: 0 Byte 1'h: 1 Byte 2'h: 2 Bytes 3'h: 3 Bytes 4'h: 4 Bytes 5'h: 5 Bytes 6'h: 6 Bytes 7'h: 7 Bytes 8'h: 8 Bytes Others: Reserved

Table 82. 2nd Master SPI Tx Length Configuration

0x1800_9B00 + Offset Address

Port Name	Bits	Offset Addr	Read/Write	Reset State	Description
Spi_m2_rx_payload7	31:24	+ 0x2C	R	0'h	2nd Master SPI Rx Payload Byte 7
Spi_m2_rx_payload6	23:16	+ 0x2C	R	0'h	2nd Master SPI Rx Payload Byte 6
Spi_m2_rx_payload5	15:8	+ 0x2C	R	0'h	2nd Master SPI Rx Payload Byte 5
Spi_m2_rx_payload4	7:0	+ 0x2C	R	0'h	2nd Master SPI Rx Payload Byte 4

Spi_m2_rx_payload3	31:24	+ 0x28	R	0'h	2nd Master SPI Rx Payload Byte 3
Spi_m2_rx_payload2	23:16	+ 0x28	R	0'h	2nd Master SPI Rx Payload Byte 2
Spi_m2_rx_payload1	15:8	+ 0x28	R	0'h	2nd Master SPI Rx Payload Byte 1
Spi_m2_rx_payload0	7:0	+ 0x28	R	0'h	2nd Master SPI Rx Payload Byte 0

8.18. GPIO, Interrupt and Jack Detection

The CM7120 supports 28 GPIOs – GPIO1~28. For GPIO function, the GPIO can be configured to input or output. For input type, the internal circuit can read pin status and report to register table. For output type, the internal circuit can drive this pin to high or low to control external device. In GPIO function, the pin polarity can be controlled by register at output type.

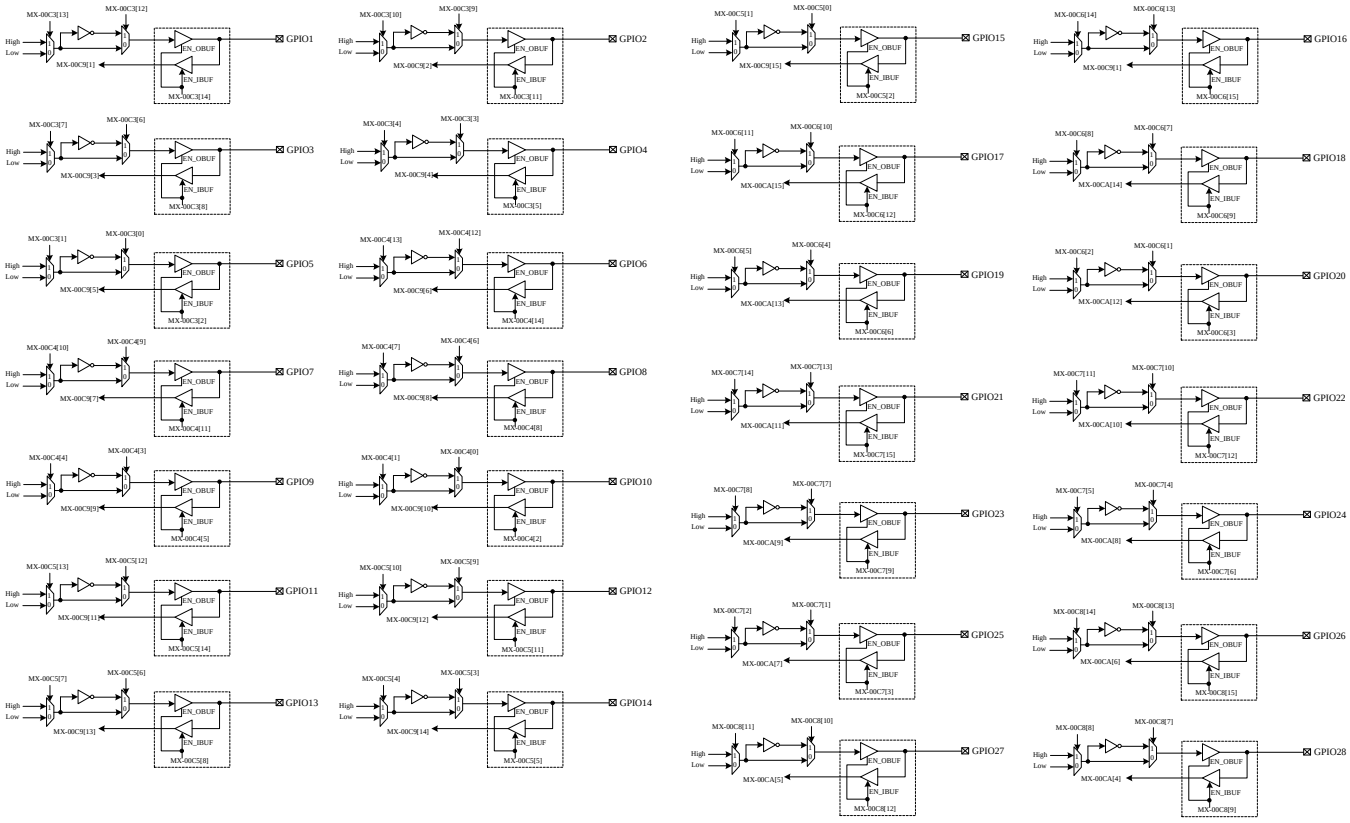


Figure 44. GPIO1~GPIO28 Function Block

For the jack detection function, All of the digital GPIO and analog JD port can be configured as jack detection pins. There are six JD status can be used. The block diagram is shown as below.

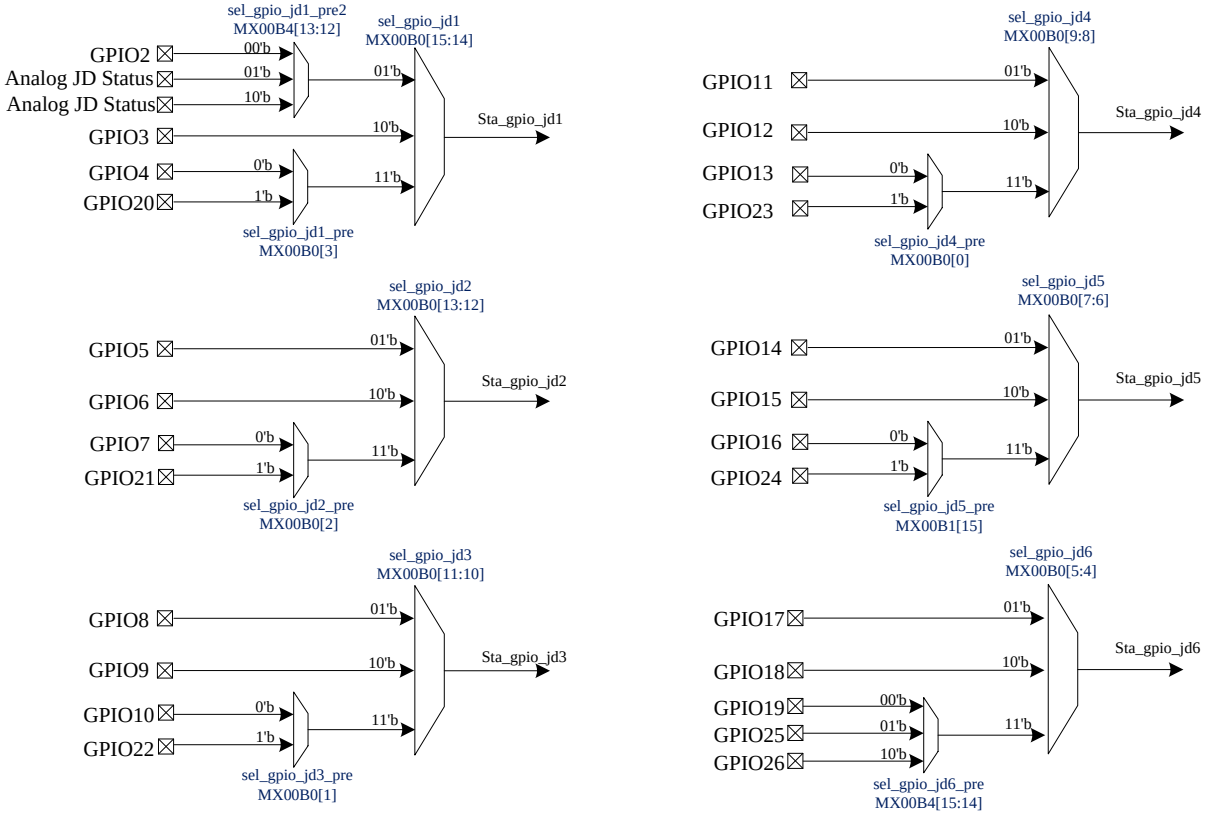


Figure 45. Jack Detection Input Source Selection

For IRQ function, there are many status can be changed polarity and output to the IRQ and IRQ2. The detail logic block is shown in the Figure 46 and Figure 47.

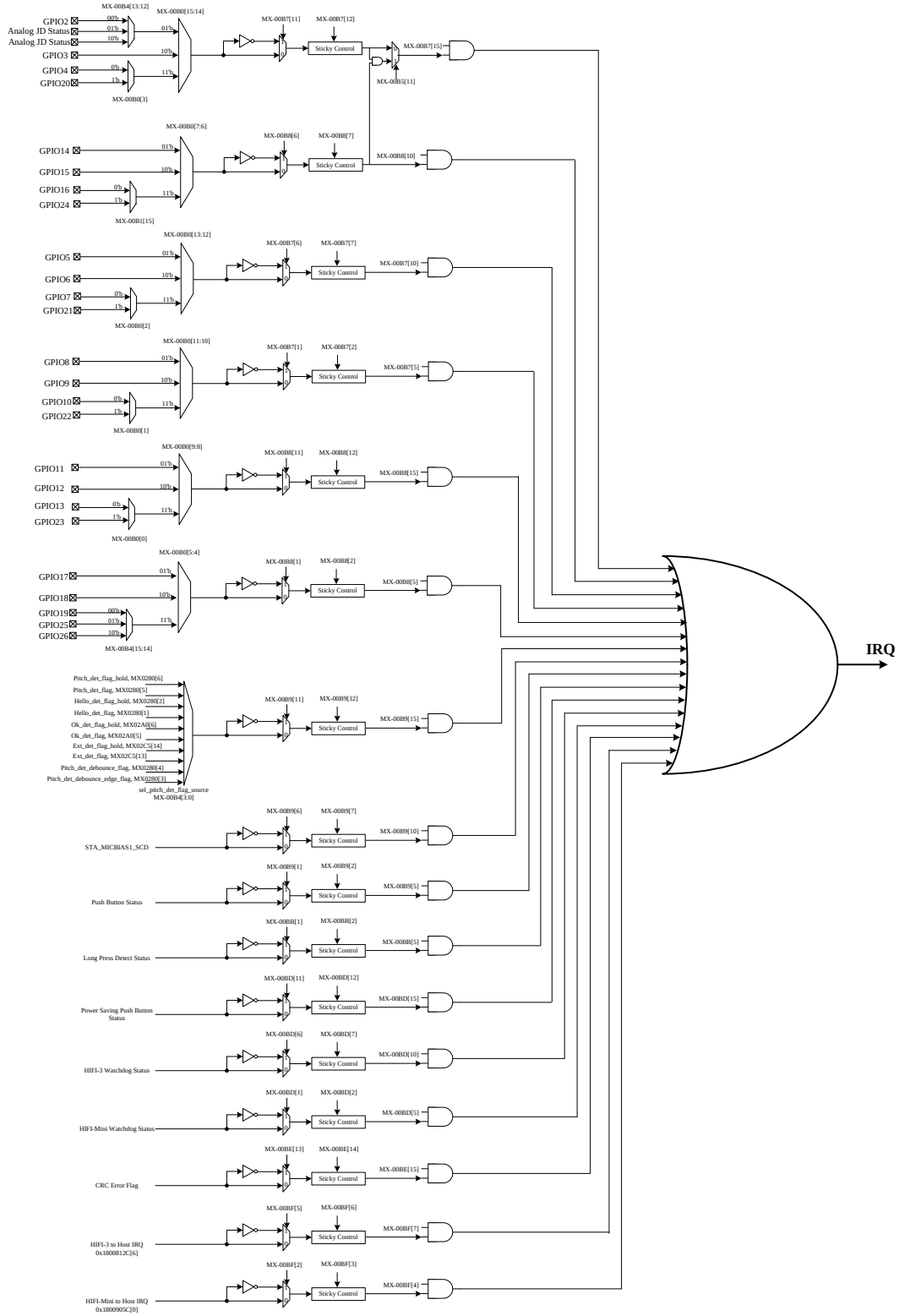


Figure 46. IRQ Function Block

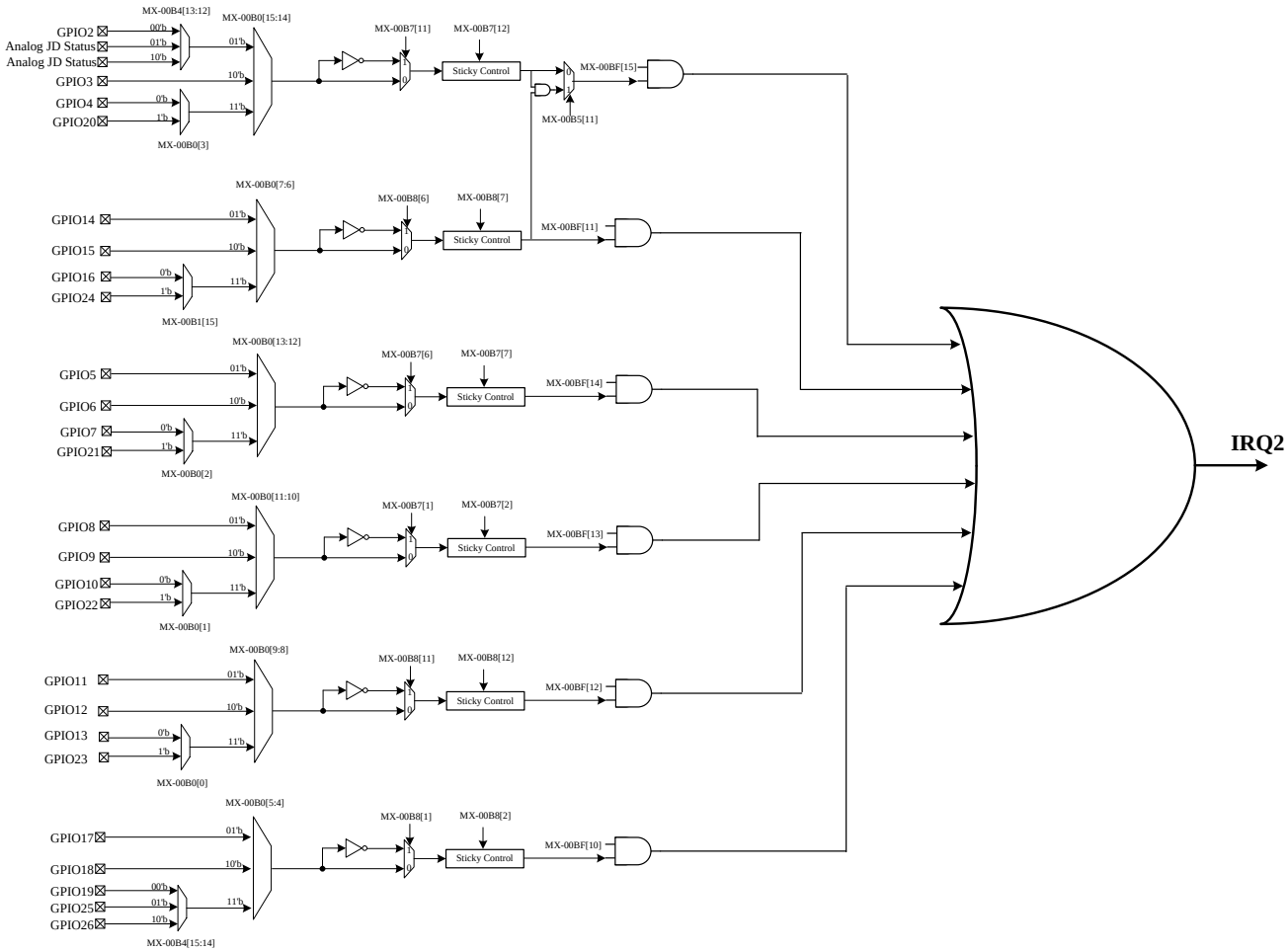


Figure 47. IRQ2 Function Block

These internal statuses will also as an interrupt of the HIFI-3 and HIFI-Mini DSP. The detail logic block is shown in the Figure 46 and Figure 47.

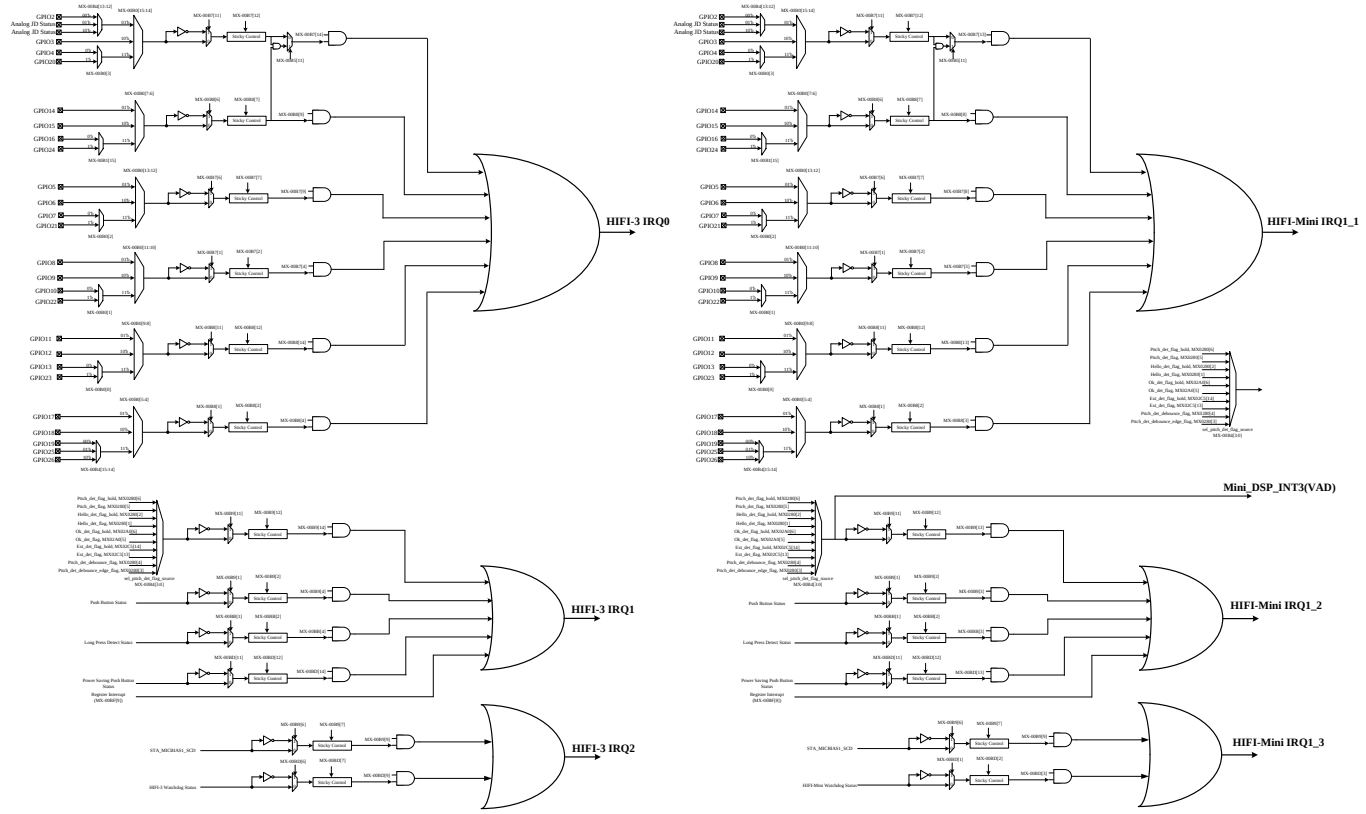
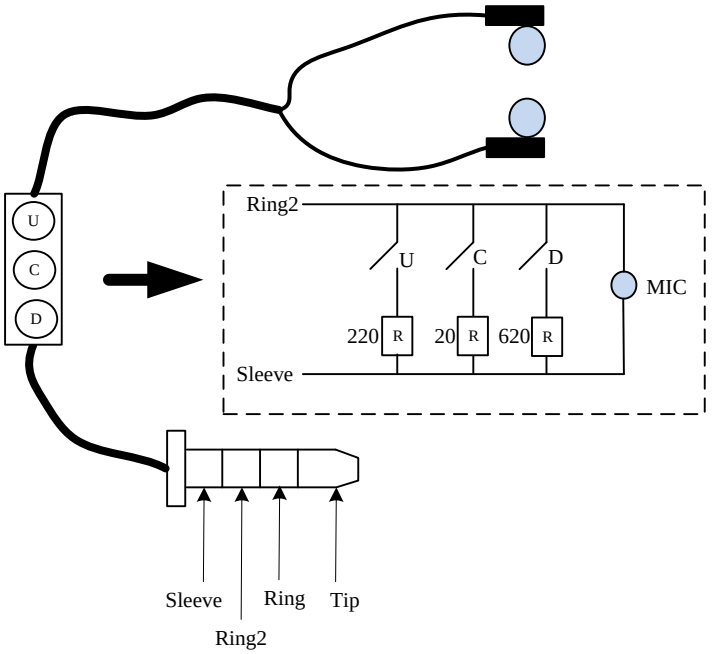


Figure 48. DSP IRQ Function Block

8.19. Push Button Detection

8.19.1.3 Push Button Detection

The CM7120 has built-in push button detection circuit inside. It can supports up to three push buttons. Each button has three status can be shown on register (MX-00DBh) – one click, double click and hold. The push button event will also cause an interrupt to IRQ output to notice external host.



Push Button Resistance	Resistance Range	Recommend Value
Up button, R2	150 ~ 280 Ohm	220 Ohm
Center button, R1	0 ~ 50 Ohm	20 Ohm
Down button, R3	550 ~ 650 Ohm	620 Ohm

Push Button Detection Status:

Button #	Button Behavior	Register Status
Up button	One click	MX-00DBh[15]
	Double click	MX-00DBh[14]
	Hold	MX-00DBh[13]
Center button	One click	MX-00DBh[12]
	Double click	MX-00DBh[11]
	Hold	MX-00DBh[10]
Down button	One click	MX-00DBh[9]
	Double click	MX-00DBh[8]
	Hold	MX-00DBh[7]

Push Button Detection Flow Chart:

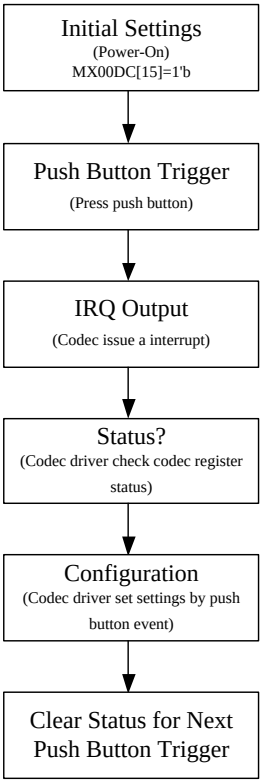
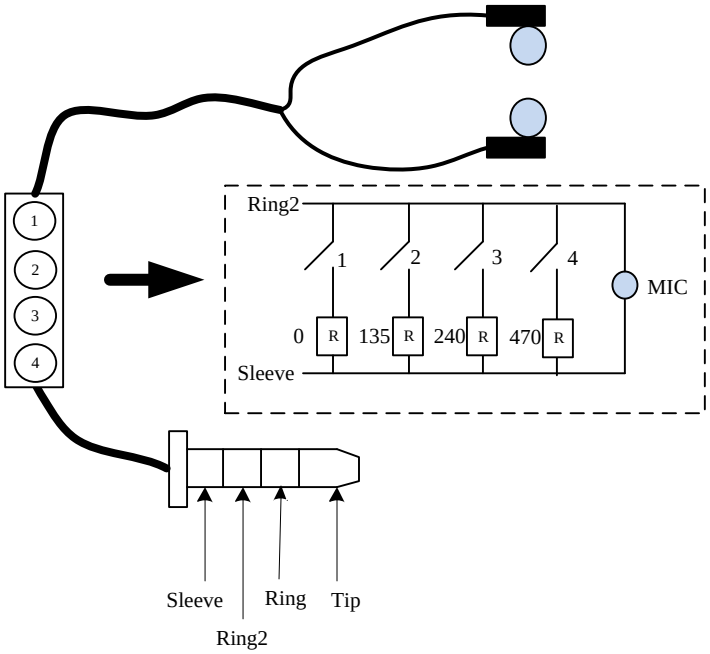


Figure 49. 3 Push Button Detection Flow

8.19.2.4 Push Button Detection

The CM7120 has also built-in 4 push button detection circuit inside. It can supports up to four push buttons. Each button has three status can be shown on register (MX-00DFh) – one click, double click and hold. The push button event will also cause an interrupt to IRQ output to notice external host.



Push Button Resistance	Resistance Range	Recommend Value
Button1, R1	0~70 Ohm	0 Ohm
Button2, R2	110~180 Ohm	135 Ohm
Button3, R3	210~290 Ohm	240 Ohm
Button4, R4	360~680 Ohm	470 Ohm

Push Button Detection Status:

Button #	Button Behavior	Register Status
Button 1	One click	MX-00DFh[15]
	Double click	MX-00DFh[14]
	Hold	MX-00DFh[13]
Button 2	One click	MX-00DFh[12]
	Double click	MX-00DFh[11]
	Hold	MX-00DFh[10]
Button 3	One click	MX-00DFh[9]
	Double click	MX-00DFh[8]
	Hold	MX-00DFh[7]
Button 4	One click	MX-00DFh[6]
	Double click	MX-00DFh[5]
	Hold	MX-00DFh[4]

Push Button Detection Flow Chart:

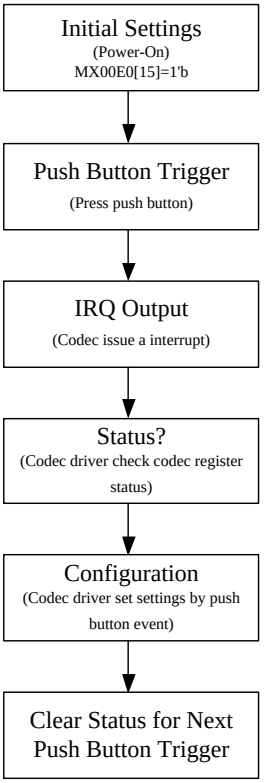


Figure 50. 4 Push Button Detection Flow

8.20. HP Impedance Sensing

There is HP impedance sensing function in the CM7120. The left and right channel of the headphone can be detected independently. The detected impedance range is 0~8 Ohm, 9~23 Ohm, 24~41 Ohm, 42~75 Ohm, 76~150 Ohm, 151~450 Ohm, 451~1000 Ohm, 1001~5000 Ohm, 5001~50000 Ohm and >50000 Ohm. When the HP impedance is detected done, the CM7120 will auto adjust the HP parameter and FSOV to optimize performance for each range impedance.
The detection flow is shown below:

Case A: Auto Adjust the HP parameter when impedance sensing done

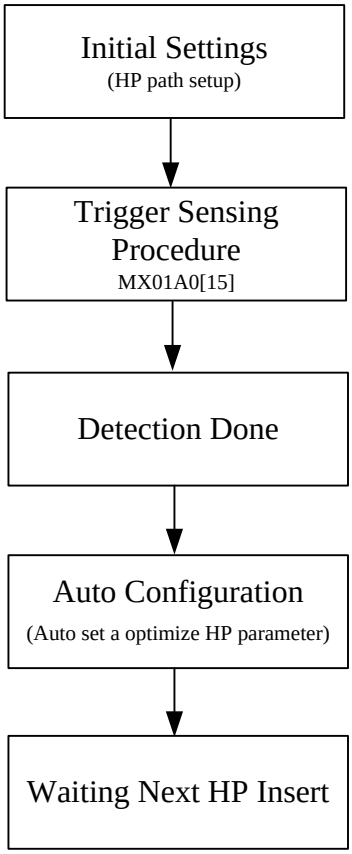


Figure 51. HP impedance detection flow (Auto adjust HP parameter)

Case B: Driver Adjust the HP parameter when impedance done

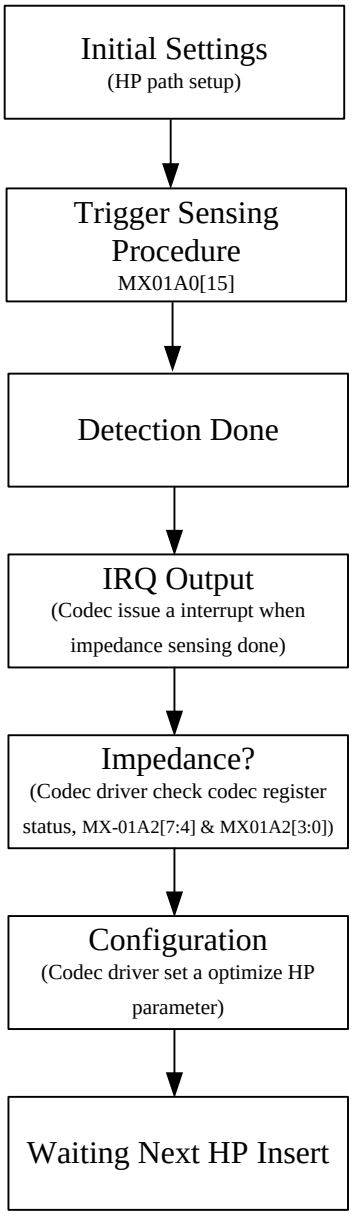


Figure 52. HP impedance detection flow (Driver manual adjust HP parameter)

9. Register List

9.1. Register Map

Table 83. Register Map

Type	Name	Description	Register Address	DSP Address	Reset State
Reset	S/W Reset	S/W Reset & Device ID & Status	MX-0000h	0x1800_C000	0x0000'h
Analog Output	LOUT1/LOUT2	LOUT Amp Control 1	MX-0001h	0x1800_C002	0x8080'h
		LOUT Amp Control 2	MX-0710h	0x1800_CE20	0x0055'h
	HPOUT	Headphone Amp Control 1	MX-0003h	0x1800_C002	0x0000'h
		Headphone Amp Control 2	MX-0120h	0x1800_C240	0x1D22'h
		Headphone Amp Control 3	MX-0121h	0x1800_C242	0x0003'h
		Headphone Amp Control 4	MX-0122h	0x1800_C244	0x0003'h
		Headphone Amp Control 5	MX-019Bh	0x1800_C336	0x0000'h
		Headphone Amp Control 6	MX-0671h	0x1800_CCE2	0x30C2'h
		Headphone Amp Control 7	MX-0674h	0x1800_CCE8	0x1100'h
	MONOOUT	MONO Amp Control 1	MX-0005h	0x1800_C00A	0x0000'h
		MONO Amp Control 2	MX-012Bh	0x1800_C256	0x0000'h
Analog Input	BST1/BST2	IN1 and IN2 Control	MX-0007h	0x1800_C00E	0x0000'h
	BST3/BST4	IN3 and IN4 Control	MX-0008h	0x1800_C010	0x0000'h
	Voice Active Detection	VAD Input Control	MX-0009h	0x1800_C010	0x0005'h
MICBIAS	MICBIAS1	Micbais1 Control	MX-0010h	0x1800_C020	0x0091'h
DAC Digital Volume	DAC1 Volume	DAC1 Post Digital Volume	MX-0014h	0x1800_C028	0x5757'h
	DAC1 Volume	DAC1 Digital Volume	MX-0015h	0x1800_C02A	0xAFAF'h
	DAC2 Volume	DAC2 Digital Volume	MX-0016h	0x1800_C02C	0xAFAF'h
	DAC3 Volume	DAC3 Digital Volume	MX-0017h	0x1800_C02E	0xAFAF'h
ADC Digital Mute/Unmute and Volume	Stereo1 ADC	Stereo1 ADC Digital Mute/Unmute and Volume	MX-001Ah	0x1800_C034	0x2F2F'h
	Mono ADC	Mono ADC Digital Mute/Unmute and Volume	MX-001Bh	0x1800_C036	0x2F2F'h
	Stereo2 ADC	Stereo2 ADC Digital Mute/Unmute and Volume	MX-001Ch	0x1800_C038	0x2F2F'h
	Stereo3 ADC	Stereo3 ADC Digital Mute/Unmute and Volume	MX-001Dh	0x1800_C03A	0x2F2F'h
ADC Digital Boost	Stereo1/2 ADC	Stereo1/2 ADC Boost Gain	MX-0020h	0x1800_C040	0x0000'h
	Mono ADC	Mono ADC Boost Gain	MX-0021h	0x1800_C042	0x0000'h
	Stereo3 ADC	Stereo3 ADC Boost Gain	MX-0022h	0x1800_C044	0x0000'h
SPDIF	SPDIF In	SPDIF In Contrl	MX-0028h	0x1800_C050	0x6000'h
Interface Data Control	IF3 Data	IF3 Data Control	MX-002Ah	0x1800_C054	0x0000'h
	IF4 Data	IF4 Data Control	MX-002Bh	0x1800_C056	0x0000'h
	IF5 Data	IF5 Data Control	MX-002Ch	0x1800_C058	0x0000'h
TDM Interface Control	TDM1	TDM1 Control 1	MX-0030h	0x1800_C060	0x00F0'h
		TDM1 Control 2	MX-0031h	0x1800_C062	0x0000'h
		TDM1 Control 3	MX-0032h	0x1800_C064	0x0000'h

Type	Name	Description	Register Address	DSP Address	Reset State
		TDM1 Control 4	MX-0033h	0x1800_C066	0x0000'h
		TDM1 Control 5	MX-0034h	0x1800_C068	0x0123'h
		TDM1 Control 6	MX-0035h	0x1800_C06A	0x4567'h
		TDM1 Control 7	MX-0036h	0x1800_C06C	0x8003'h
	TDM2	TDM2 Control 1	MX-0038h	0x1800_C070	0x00F0'h
		TDM2 Control 2	MX-0039h	0x1800_C072	0x0000'h
		TDM2 Control 3	MX-003Ah	0x1800_C074	0x0000'h
		TDM2 Control 4	MX-003Bh	0x1800_C076	0x0000'h
		TDM2 Control 5	MX-003Ch	0x1800_C078	0x0123'h
		TDM2 Control 6	MX-003Dh	0x1800_C07A	0x4567'h
		TDM2 Control 7	MX-003Eh	0x1800_C07C	0x8003'h
Digital DAC Mixer	Stereo1 DAC Mixer	Stereo1 DAC Mixer Control 1	MX-0040h	0x1800_C080	0xCAAA'h
		Stereo1 DAC Mixer Control 2	MX-0041h	0x1800_C082	0xAA00'h
	Mono DAC Mixer	Mono DAC Mixer Control 1	MX-0042h	0x1800_C084	0xCAAA'h
		Mono DAC Mixer Control 2	MX-0043h	0x1800_C086	0xAA00'h
	DD DAC Mixer	DD DAC Mixer Control 1	MX-0044h	0x1800_C088	0xAAAA'h
		DD DAC Mixer Control 2	MX-0045h	0x1800_C08A	0xAA00'h
Digital DAC Source	DAC1 Source	Digital DAC1 Source Control	MX-0046h	0x1800_C08C	0xB080'h
	DAC2 Source	Digital DAC2 Source Control	MX-0047h	0x1800_C08E	0x0000'h
	DAC3 Source	Digital DAC3 Source Control	MX-0048h	0x1800_C090	0x0000'h
Analog DAC Source	DAC1~5 Source	Analog DAC Source Control	MX-0049h	0x1800_C092	0x0000'h
Digital ADC Mixer	Stereo1 ADC Mixer	Stereo1 ADC Mixer Control	MX-004Ah	0x1800_C094	0xC0C0'h
	Mono ADC Mixer	Mono ADC Mixer Control 1	MX-004Bh	0x1800_C096	0xC0C0'h
		Mono ADC Mixer Control 2	MX-004Ch	0x1800_C098	0x0000'h
	Stereo2 ADC Mixer	Stereo2 ADC Mixer Control	MX-004Dh	0x1800_C09A	0xC0C0'h
	Stereo3 ADC Mixer	Stereo3 ADC Mixer Control	MX-004Eh	0x1800_C09C	0xC0C0'h
Digital Microphone	DMIC1~DMIC4	Digital Microphone Control 1	MX-0050h	0x1800_C0A0	0x0550'h
		Digital Microphone Control 2	MX-0052h	0x1800_C0A2	0x0055'h
Power	Power	Power Management 1	MX-0060h	0x1800_C0C0	0x0000'h
		Power Management 2	MX-0061h	0x1800_C0C2	0x0000'h
		Power Management 3	MX-0062h	0x1800_C0C4	0x0000'h
		Power Management 4	MX-0063h	0x1800_C0C6	0x0040'h
		Power Management 5	MX-0064h	0x1800_C0C8	0x0000'h
		Power Management 6	MX-0065h	0x1800_C0CA	0x0181'h
		Power Management 7	MX-0066h	0x1800_C0CC	0x0000'h
		Power Management 8	MX-0067h	0x1800_C0CE	0x0002'h
		Power Management 9	MX-0068h	0x1800_C0D0	0x3703'h
		Power Management 10	MX-0069h	0x1800_C0D2	0x0100'h
		Power Management 11	MX-006Ah	0x1800_C0D4	0x0000'h
I2S Interface	I2S1	I2S1 Audio Serial Data Port Control	MX-0070h	0x1800_C0E0	0x8000'h

Type	Name	Description	Register Address	DSP Address	Reset State
Control	I2S2	I2S2 Audio Serial Data Port Control	MX-0071h	0x1800_C0E2	0x8000'h
	I2S3	I2S3 Audio Serial Data Port Control	MX-0072h	0x1800_C0E4	0x8000'h
	I2S4	I2S4 Audio Serial Data Port Control	MX-0073h	0x1800_C0E6	0x8000'h
	I2S5	I2S5 Audio Serial Data Port Control	MX-0074h	0x1800_C0E8	0x8000'h
	LRCK/BCLK Selection	I2S LRCK/BCLK Source Selection	MX-0075h	0x1800_C0EA	0x0000'h
Global Clock	Clock Tree 1	Clock Tree Control 1	MX-0076h	0x1800_C0EC	0x7777'h
	Clock Tree 2	Clock Tree Control 2	MX-0077h	0x1800_C0EE	0x7777'h
	Clock Tree 3	Clock Tree Control 3	MX-0078h	0x1800_C0F0	0x7000'h
	Clock Tree 4	Clock Tree Control 4	MX-0079h	0x1800_C0F2	0x3000'h
	PLL1	PLL1 Control 1	MX-007Ah	0x1800_C0F4	0x0000'h
		PLL1 Control 2	MX-007Bh	0x1800_C0F6	0x0000'h
	PLL2	PLL2 Control 1	MX-007Ch	0x1800_C0F8	0x0000'h
		PLL2 Control 2	MX-007Dh	0x1800_C0FA	0x0000'h
	HIFI-3 DSP	DSP Clock Source Selection 1	MX-007Eh	0x1800_C0FC	0x0111'h
	HIFI-Mini DSP	DSP Clock Source Selection 2	MX-007Fh	0x1800_C0FE	0x0333'h
	Global Clock	Global Clock Control 1	MX-0080h	0x1800_C100	0x0000'h
		Global Clock Control 2	MX-0081h	0x1800_C102	0x0000'h
	ASRC	ASRC Control 1	MX-0083h	0x1800_C106	0x0000'h
		ASRC Control 2	MX-0084h	0x1800_C108	0x0000'h
		ASRC Control 3	MX-0085h	0x1800_C10A	0x0000'h
		ASRC Control 4	MX-0086h	0x1800_C10C	0x0000'h
		ASRC Control 5	MX-0087h	0x1800_C10E	0x0000'h
		ASRC Control 6	MX-0088h	0x1800_C110	0x0000'h
		ASRC Control 7	MX-0089h	0x1800_C112	0x0000'h
		ASRC Control 8	MX-008Ah	0x1800_C114	0x0000'h
		ASRC Control 9	MX-008Bh	0x1800_C116	0x0000'h
		ASRC Control 10	MX-008Ch	0x1800_C118	0x0000'h
	Fractional Divider	Fractional Divider for System Clock Control 1	MX-009Ch	0x1800_C138	0x0002'h
		Fractional Divider for System Clock Control 2	MX-009Dh	0x1800_C13A	0x0001'h
Jack Detection	Jack Detection	Jack and Microphone Detection Control 1	MX-00A0h	0x1800_C140	0x7080'h
		Jack and Microphone Detection Control 2	MX-00A1h	0x1800_C142	0x4A00'h
		Jack and Microphone Detection Control 3	MX-00A3h	0x1800_C146	0xA000'h
		Jack Detection Control 1	MX-00B0h	0x1800_C160	0x0000'h
		Jack Detection Control 2	MX-00B1h	0x1800_C162	0x0000'h
		Jack Detection Control 3	MX-00B4h	0x1800_C168	0x0000'h
Internal Status		Internal Status 1	MX-00B5h	0x1800_C16A	0x0000'h
		Internal Status 2	MX-00B6h	0x1800_C16C	0x0000'h
IRQ		IRQ Control 1	MX-00B7h	0x1800_C16E	0x0000'h
		IRQ Control 2	MX-00B8h	0x1800_C170	0x0000'h
		IRQ Control 3	MX-00B9h	0x1800_C172	0x0000'h
		IRQ Control 4	MX-00BBh	0x1800_C176	0x0000'h

Type	Name	Description	Register Address	DSP Address	Reset State
		IRQ Control 5	MX-00BDh	0x1800_C17A	0x0000'h
		IRQ Control 6	MX-00Beh	0x1800_C17C	0x0000'h
		IRQ Control 7	MX-00BFh	0x1800_C17E	0x0000'h
Multi-Function		Multi-Function Pin Control 1	MX-00C0h	0x1800_C180	0x2008'h
		Multi-Function Pin Control 2	MX-00C1h	0x1800_C182	0x8600'h
		Multi-Function Pin Control 3	MX-00C2h	0x1800_C184	0x0000'h
GPIO		GPIO Control 1	MX-00C3h	0x1800_C186	0x0000'h
		GPIO Control 2	MX-00C4h	0x1800_C188	0x0000'h
		GPIO Control 3	MX-00C5h	0x1800_C18A	0x0000'h
		GPIO Control 4	MX-00C6h	0x1800_C18C	0x0000'h
		GPIO Control 5	MX-00C7h	0x1800_C18E	0x0000'h
		GPIO Control 6	MX-00C8h	0x1800_C190	0x0000'h
		GPIO Status 1	MX-00C9h	0x1800_C192	0x0000'h
		GPIO Status 2	MX-00Cah	0x1800_C194	0x0000'h
Long Press Detection		Long Press Detection Control	MX-00CFh	0x1800_C19E	0x0300'h
Wind Filter		Stereo1 ADC Wind Filter Control 1	MX-00D0h	0x1800_C1A0	0xB320'h
		Stereo1 ADC Wind Filter Control 2	MX-00D1h	0x1800_C1A2	0x0000'h
		MONO ADC Wind Filter Control 1	MX-00D2h	0x1800_C1A4	0xB320'h
		MONO ADC Wind Filter Control 2	MX-00D3h	0x1800_C1A6	0x0000'h
		Stereo2 ADC Wind Filter Control 1	MX-00D4h	0x1800_C1A8	0xB320'h
		Stereo2 ADC Wind Filter Control 2	MX-00D5h	0x1800_C1AA	0x0000'h
		Stereo3 ADC Wind Filter Control 1	MX-00D6h	0x1800_C1AC	0xB320'h
		Stereo3 ADC Wind Filter Control 2	MX-00D7h	0x1800_C1AE	0x0000'h
Push Button Detection		3 Push Buttons Detect Control 1	MX-00DBh	0x1800_C1B6	0x0008'h
		3 Push Buttons Detect Control 2	MX-00DCh	0x1800_C1B8	0x00C0'h
		Push Buttons Detect Control	MX-00DDh	0x1800_C1BA	0x6724'h
		3 Push Buttons Detect Control 3	MX-00Deh	0x1800_C1BC	0x3131'h
		4 Push Buttons Detect Control 1	MX-00DFh	0x1800_C1BE	0x0008'h
		4 Push Buttons Detect Control 2	MX-00E0h	0x1800_C1C0	0x4000'h
		4 Push Buttons Detect Control 3	MX-00E1h	0x1800_C1C2	0x3131'h
		Power Saving Push Button Detect Control	MX-00E4h	0x1800_C1C8	0x402C'h
Clock Gating		System Clock Enable Control	MX-00Fah	0x1800_C1F4	0x0000'h
Vender ID		Vender ID	MX-00Feh	0x1800_C1FC	0x10EC'h
PDM		PDM Output Control	MX-0100h	0x1800_C200	0xC0C0'h
Sidetone		Sidetone Control	MX-011Ah	0x1800_C234	0x000B'h
Clock Detection		System Clock Detection	MX-011Dh	0x1800_C23A	0x0000'h
Noise Gate Function		Stereo1 DAC Path Noise Gate Control	MX-0150h	0x1800_C2A0	0x4131'h
		MONO2 DAC Lch Path Noise Gate Control	MX-0151h	0x1800_C2A2	0x4131'h
		MONO2 DAC Rch Path Noise Gate Control	MX-0152h	0x1800_C2A4	0x4131'h

Type	Name	Description	Register Address	DSP Address	Reset State
		MONO3 DAC Lch Path Noise Gate Control	MX-0153h	0x1800_C2A6	0x4131'h
		MONO3 DAC Rch Path Noise Gate Control	MX-0154h	0x1800_C2A8	0x4131'h
		Noise Gate for Output Port	MX-0155h	0x1800_C2AA	0x0000'h
ADC EQ		ADC EQ Control 1	MX-0160h	0x1800_C2C0	0x6000'h
		ADC EQ Control 2	MX-0161h	0x1800_C2C2	0x0000'h
DAC EQ		DAC EQ Control 1	MX-0164h	0x1800_C2C8	0xC000'h
		DAC EQ Control 2	MX-0166h	0x1800_C2CC	0x0000'h
		DAC EQ Control 3	MX-0167h	0x1800_C2CE	0x0000'h
I2S Master Clock	I2S1 and I2S2	I2S Master Mode Clock Control 1	MX-0170h	0x1800_C2E0	0x0000'h
	I2S3 and I2S4	I2S Master Mode Clock Control 2	MX-0171h	0x1800_C2E2	0x0000'h
	I2S5	I2S Master Mode Clock Control 3	MX-0172h	0x1800_C2E4	0x0000'h
	Fractional Divider	I2S Master Mode Clock Control 4	MX-0173h	0x1800_C2E6	0x0002'h
	Fractional Divider	I2S Master Mode Clock Control 5	MX-0174h	0x1800_C2E8	0x0001'h
	Fractional Divider	I2S Master Mode Clock Control 6	MX-0175h	0x1800_C2EA	0x0002'h
	Fractional Divider	I2S Master Mode Clock Control 7	MX-0176h	0x1800_C2EC	0x0001'h
	Fractional Divider	I2S Master Mode Clock Control 8	MX-0177h	0x1800_C2EE	0x0002'h
	Fractional Divider	I2S Master Mode Clock Control 9	MX-0178h	0x1800_C2F0	0x0001'h
	Fractional Divider	I2S Master Mode Clock Control 10	MX-0179h	0x1800_C2F2	0x0002'h
	Fractional Divider	I2S Master Mode Clock Control 11	MX-017Ah	0x1800_C2F4	0x0001'h
	Fractional Divider	I2S Master Mode Clock Control 12	MX-017Bh	0x1800_C2F6	0x0002'h
	Fractional Divider	I2S Master Mode Clock Control 13	MX-017Ch	0x1800_C2F8	0x0001'h
VAD ADC Filter	VAD ADC Filter	VAD ADC Filter Control 1	MX-0192h	0x1800_C324	0x882F'h
		VAD ADC Filter Control 2	MX-0193h	0x1800_C326	0x0000'h
HP Impedance Sensing		Headphone Impedance Sensing Control 1	MX-01A0h	0x1800_C340	0x433D'h
		Headphone Impedance Sensing Control 2	MX-01A2h	0x1800_C344	0x0000'h
		Headphone Impedance Sensing Control 3	MX-01B3h	0x1800_C366	0x40AF'h
IRQ De-bounce Clock		IRQ De-bounce Clock Control	MX-01F0h	0x1800_C3E0	0x0000'h
Pitch Detection	Pitch and Hello Detection	Pitch Detection Control 1	MX-0280h	0x1800_C500	0x7681'h
	Ok Detection	Pitch Detection Control 2	MX-02A0h	0x1800_C540	0x4089'h
DAC ALC/DRC		Multi-Band DRC Control 1	MX-0300h	0x1800_C600	0x3C10'h
		Multi-Band DRC Control 2	MX-0310h	0x1800_C620	0x5254'h
		Multi-Band DRC Control 3	MX-0311h	0x1800_C622	0x0300'h
		Multi-Band DRC Control 4	MX-0312h	0x1800_C624	0x5F5F'h
		Multi-Band DRC Control 4	MX-0313h	0x1800_C626	0x133E'h
		Multi-Band DRC Control 5	MX-0315h	0x1800_C62A	0x040C'h
		Multi-Band DRC Control 6	MX-0320h	0x1800_C640	0x5254'h
		Multi-Band DRC Control 7	MX-0321h	0x1800_C642	0x0300'h
		Multi-Band DRC Control 8	MX-0322h	0x1800_C644	0x5F5F'h
		Multi-Band DRC Control 9	MX-0323h	0x1800_C646	0x133E'h
		Multi-Band DRC Control 10	MX-0325h	0x1800_C64A	0x040C'h

Type	Name	Description	Register Address	DSP Address	Reset State
		Multi-Band DRC Control 11	MX-0330h	0x1800_C660	0x5254'h
		Multi-Band DRC Control 12	MX-0331h	0x1800_C662	0x0300'h
		Multi-Band DRC Control 13	MX-0332h	0x1800_C664	0x5F5F'h
		Multi-Band DRC Control 14	MX-0333h	0x1800_C666	0x133E'h
		Multi-Band DRC Control 15	MX-0335h	0x1800_C66A	0x040C'h
		Multi-Band DRC Control 16	MX-0340h	0x1800_C680	0x4951'h
		Multi-Band DRC Control 17	MX-0341h	0x1800_C682	0x1860'h
		Multi-Band DRC Control 18	MX-0342h	0x1800_C684	0x5F5F'h
		Multi-Band DRC Control 19	MX-0344h	0x1800_C688	0x0450'h
		Multi-Band DRC Control 20	MX-0345h	0x1800_C68A	0x00FF'h
		Multi-Band DRC Control 21	MX-0346h	0x1800_C68C	0x040C'h
		Multi-Band DRC Control 22	MX-0348h	0x1800_C690	0x0000'h
ADC ALC/DRC		ADC ALC/DRC Control 1	MX-0350h	0x1800_C6A0	0x4905'h
		ADC ALC/DRC Control 2	MX-0352h	0x1800_C6A2	0x0100'h
		ADC ALC/DRC Control 3	MX-0353h	0x1800_C6A6	0x5F5F'h
		ADC ALC/DRC Control 4	MX-0354h	0x1800_C6A6	0x5F5F'h
		ADC ALC/DRC Control 5	MX-0355h	0x1800_C6AA	0x0022'h
		ADC ALC/DRC Control 6	MX-0356h	0x1800_C6AC	0x45FF'h
		ADC ALC/DRC Control 7	MX-0357h	0x1800_C6AE	0x040C'h
		ADC ALC/DRC Control 8	MX-0359h	0x1800_C6B2	0x0000'h
		ADC ALC/DRC Control 9	MX-035Ah	0x1800_C6B4	0x0000'h
DSP Inbound/Outbound Control	Inbound/Outbound	DSP Inbound/Outbound Control 1	MX-0500h	0x1800_CA00	0x0000'h
	Inbound/Outbound	DSP Inbound/Outbound Control 2	MX-0501h	0x1800_CA02	0x0000'h
	Inbound/Outbound	DSP Inbound/Outbound Control 3	MX-0502h	0x1800_CA04	0x0000'h
	Inbound/Outbound	DSP Inbound/Outbound Control 4	MX-0503h	0x1800_CA06	0x2F2F'h
	Inbound/Outbound	DSP Inbound/Outbound Control 5	MX-0504h	0x1800_CA08	0x2F2F'h
	Inbound/Outbound	DSP Inbound/Outbound Control 6	MX-0505h	0x1800_CA0A	0x2F2F'h
	Inbound/Outbound	DSP Inbound/Outbound Control 7	MX-0506h	0x1800_CA0C	0x2F2F'h
	Inbound/Outbound	DSP Inbound/Outbound Control 8	MX-0507h	0x1800_CA0E	0x2F2F'h
HIFI-MINI	HIFI-MINI	HIFI-Mini DSP Control and Status	MX-0520h	0x1800_CA40	0x0041'h
ADC Clock	ADC1/ADC2	Analog ADC Clock Control 1	MX-0610h	0x1800_CC20	0xA490'h
	ADC3/ADC4	Analog ADC Clock Control 2	MX-0611h	0x1800_CC22	0xA490'h
	ADC5	Analog ADC Clock Control 3	MX-0612h	0x1800_CC24	0x0210'h
DSP Bus Bypass	DSP Bus Bypass	DSP Bus Bypass Control	MX-0657h	0x1800_CCAE	0x0000'h
DAC Clock	DAC1	Analog DAC Clock Control 1	MX-0660h	0x1800_CCC0	0x0010'h
	DAC2	Analog DAC Clock Control 2	MX-0661h	0x1800_CCC2	0x0010'h
	DAC3	Analog DAC Clock Control 3	MX-0662h	0x1800_CCC4	0x0010'h
	DAC4	Analog DAC Clock Control 4	MX-0663h	0x1800_CCC6	0x0010'h
	DAC5	Analog DAC Clock Control 5	MX-0664h	0x1800_CCC8	0x0010'h

9.2. MX-0000h: S/W Reset & Device ID

Default: 0000'h

Table 84. MX-0000h: S/W Reset & Status

DSP Address: 0x1800_C000 **I2C Address: 0x0000**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:3	R	0'h	Reserved
Pad_sel2_mode	2	R	0'h	Control Mode Selection 00'b: I2C 01'b: Flash Boot Mode 10'b: SPI 11'b: Reserved
Pad_sel1_mode	1	R	0'h	
Reserved	0	R	0'h	Reserved

Note: Writing **"0x10ECh"** into this register will reset all registers to their default value. The written data is ignored.

9.3. MX-0001h: LOUT Amp Control 1

Default: 8080'h

Table 85. MX-0001h: LOUT Amp Control

DSP Address: 0x1800_CE20 **I2C Address: 0x0710**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_lout1	15	R/W	1'h	LOUT1 (Lch) mute control 0'b: Unmute 1'b: Mute
en_amp_lout1	14	R/W	0'h	Enhance LOUT1 driving ability 0'b: Disable 1'b: Enable
en_dfo1	13	R/W	0'h	Enable differential mode of LOUT1 (Lch) 0'b: Disable 1'b: Enable
en_dac3_lout1	12	R/W	0'h	Enable DAC3 to LOUT1 Output 0'b: Disable 1'b: Enable
reserved	11:8	R	0'h	Reserved
mu_lout2	7	R/W	1'h	LOUT2 (Rch) mute control 0'b: Unmute 1'b: Mute
en_amp_lout2	6	R/W	0'h	Enhance LOUT2 driving ability 0'b: Disable 1'b: Enable
en_dfo2	5	R/W	0'h	Enable differential mode of LOUT2 (Rch) 0'b: Disable 1'b: Enable

DSP Address: 0x1800_CE20 I2C Address: 0x0710				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_dac4_lout2	4	R/W	0'h	Enable DAC4 to LOUT2 Output 0'b: Disable 1'b: Enable
reserved	3:0	R	0'h	Reserved

9.4. MX-0710h: LOUT Amp Control 2

Default: 0055'h

Table 86. MX-0710h: LOUT Amp Control 2

DSP Address: 0x1800_CE20 I2C Address: 0x0710				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:10	R	0'h	Reserved
Sel_lout_sig_sour	9	R/W	0'h	Select the LOUT Related Signal Source 0'b: Register Control 1'b: Auto Mode or Noise Gate Mode
Reserved	8:0	R	0'h	Reserved

9.5. MX-0003h: HP Amp Control 1

Default: 0000'h

Table 87. MX-0003h: HP Amp Control 1

DSP Address: 0x1800_C006 I2C Address: 0x0003				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_dac1_hpol	15	R/W	0'h	Enable DAC1 to HPO_L Output(Auto Mode) 0'b: Disable output 1'b: Enable output
Reserved	14:8	R	0'h	Reserved
en_dac2_hpor	7	R/W	0'h	Enable DAC2 to HPO_R Output(Auto Mode) 0'b: Disable output 1'b: Enable output
Reserved	6:0	R	0'h	Reserved

9.6. MX-0120h: HP Amp Control 2

Default: 1D22'h

Table 88. MX-0120h: HP Amp Control 2

DSP Address: 0x1800_C240 **I2C Address: 0x0120**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
En_hp_noise_gate 1	15	R/W	0'h	HP Noise Gate Mode 1 Control 0'b: Disable 1'b: Enable
Reserved	14:0	R	0'h	Reserved

9.7. MX-0121h: HP Amp Control 3

Default: 0003'h

Table 89. MX-0121h: HP Amp Control 3

DSP Address: 0x1800_C242 **I2C Address: 0x0121**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:6	R	0'h	Reserved
Hp_gain_l	5:0	R/W	3'h	Headphone-amp-l gain 6'h00: 2.25dB 6'h01: 1.5dB 6'h02: 0.75dB 6'h03: 0dB …… 6'h21: -22.50dB 6'h22: -23.25dB

9.8. MX-0122h: HP Amp Control 4

Default: 0003'h

Table 90. MX-0122h: HP Amp Control 4

DSP Address: 0x1800_C244 **I2C Address: 0x0122**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:6	R	0'h	Reserved
Hp_gain_r	5:0	R/W	3'h	Headphone-amp-r gain 6'h00: 2.25dB 6'h01: 1.5dB 6'h02: 0.75dB 6'h03: 0dB …… 6'h21: -22.50dB 6'h22: -23.25dB

9.9. MX-019Bh: HP Amp Control 5

Default: 0000'h

Table 91. MX-019Bh: HP Amp Control 5

DSP Address: 0x1800_C336 I2C Address: 0x019B				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
Sel_hp_sig_sour4	12	R/W	0'h	Select the HP signal source 4 0'b: HP Noise Gate Mode 1'b: HP Impedance Sensing Mode
Reserved	11:10	R	0'h	Reserved
Sel_hp_sig_sour3	9:8	R/W	0'h	Select the HP signal source 3 00'b: Register Mode 01'b: Register Mode 10'b: Register Mode 11'b: Register Mode
Reserved	7:6	R	0'h	Reserved
Sel_hp_sig_sour2	5:4	R/W	0'h	Select the HP signal source 2 00'b: Register Mode 01'b: HP Impedance Sensing Mode 10'b: Register Mode 11'b: Register Mode
Reserved	3:2	R	0'h	Reserved
Sel_hp_sig_sour1	1:0	R/W	0'h	Select the HP signal source 1 00'b: Register Mode 01'b: HP Impedance Sensing Mode 10'b: Register Mode 11'b: Auto or HP Noise Gate Mode

9.10. MX-0671h: HP Amp Control 6

Default: 30C2'h

Table 92. MX-0671h: HP Amp Control 6

DSP Address: 0x1800_CCE2 **I2C Address: 0x0671**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
En_out_r_hp	15	R/W	0'h	Enable HPR output buffer 0'b: Disable 1'b: Enable
En_out_l_hp	14	R/W	0'h	Enable HPL output buffer 0'b: Disable 1'b: Enable
En_osw_r_hp	13	R/W	1'h	Enable HPOR to GND Res short 0'b: Disable 1'b: Enable
En_osw_l_hp	12	R/W	1'h	Enable HPOL to GND Res short 0'b: Disable 1'b: Enable
Reserved	11:0	R	C2'h	Reserved

9.11. MX-0674h: HP Amp Control 7

Default: 1100'h

Table 93. MX-0674h: HP Amp Control 7

DSP Address: 0x1800_CCE8 **I2C Address: 0x0674**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:8	R	11'h	Reserved
Pow_reg_r_hp	7	R/W	0'h	HPR VEE regulator power control 0'b: Disable 1'b: Enable
Pow_reg_l_hp	6	R/W	0'h	HPL VEE regulator power control 0'b: Disable 1'b: Enable
Pow_pump_r_hp	5	R/W	0'h	HPR Pump power control 0'b: Disable 1'b: Enable
Pow_pump_l_hp	4	R/W	0'h	HPL Pump power control 0'b: Disable 1'b: Enable
Pow_capless_r	3	R/W	0'h	HPR power control 0'b: Disable 1'b: Enable
Pow_capless_l	2	R/W	0'h	HPL power control 0'b: Disable 1'b: Enable
Reserved	1:0	R	0'h	Reserved

9.12. MX-0005h: MONO Amp Control 1

Default: 0000'h

Table 94. MX-0005h: MONO Amp Control

DSP Address: 0x1800_C00A **I2C Address: 0x0005**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15	R	0'h	Reserved
en_dac5_mono	14	R/W	0'h	Enable DAC5 to MONO Output (Auto Mode) 0'b: Disable output 1'b: Enable output
Reserved	13	R	0'h	Reserved
Sel_mono_sig_sour	12	R/W	0'h	Select the MONO Related Signal Source 0'b: Register Control 1'b: Auto Mode or MONO Noise Gate Mode
Reserved	11:0	R	0'h	Reserved

9.13. MX-012Bh: MONO Amp Control 2

Default: 0000'h

Table 95. MX-012Bh: MONO Amp Control 2

DSP Address: 0x1800_C256 **I2C Address: 0x012B**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:6	R	0'h	Reserved
Mono_gain	5:0	R/W	0'h	Mono-amp gain (0.75dB/step) 6'h00: 2.25dB 6'h01: 1.5dB 6'h02: 0.75dB 6'h03: 0dB …… 6'h21: -22.50dB 6'h22: -23.25dB

9.14. MX-0007h: IN1 and IN2 Control

Default: 0000'h

Table 96. MX-0007h: IN1 and IN2 Control

DSP Address: 0x1800_C00E **I2C Address: 0x0007**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_df_bst1	15	R/W	0'h	IN1 Differential input 0'b: Disable 1'b: Enable
Gain_bst1	14:8	R/W	0'h	MIC BST1 +0.75/Step Gain Control 0000000:-12dB 0000001:-11.25dB .... 0010000:0dB .... 0101000:+18dB ..... 1000101:+39.75dB
en_df_bst2	7	R/W	0'h	IN2 Differential input 0'b: Disable 1'b: Enable
Gain_bst2	6:0	R/W	0'h	MIC BST2 +0.75/Step Gain Control 0000000:-12dB 0000001:-11.25dB .... 0010000:0dB .... 0101000:+18dB ..... 1000101:+39.75dB

9.15. MX-0008h: IN3 and IN4 Control

Default: 0000'h

Table 97. MX-0008h: IN3 and IN4 Control

DSP Address: 0x1800_C010 **I2C Address: 0x0008**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
En_df_bst3	15	R/W	0'h	IN3 Differential input 0'b: Disable 1'b: Enable
Gain_bst3	14:8	R/W	0'h	MIC BST3 +0.75/Step Gain Control 0000000:-12dB 0000001:-11.25dB .... 0010000:0dB .... 0101000:+18dB ..... 1000101:+39.75dB
En_df_bst4	7	R/W	0'h	IN4 Differential input 0'b: Disable 1'b: Enable
Gain_bst4	6:0	R/W	0'h	MIC BST4 +0.75/Step Gain Control 0000000:-12dB 0000001:-11.25dB .... 0010000:0dB .... 0101000:+18dB ..... 1000101:+39.75dB

9.16. MX-0009h: VAD Input Control

Default: 0005'h

Table 98. MX-0009h: VAD Input Control

DSP Address: 0x1800_C012 **I2C Address: 0x0009**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:5	R	0'h	Reserved
Sel_vin_inbuf	4	R/W	0'h	Select input signal of VAD ADC 0'b: IN3P 1'b: IN4P
Gain_inbuf	3:0	R/W	5'h	Gain control of VAD ADC 0000'b: -1.5dB 0001'b: 0dB 0010'b: 1.5dB 0011'b: 3dB 0100'b: 4.5dB 0101'b: 6dB 0110'b: 7.5dB 0111'b: 9dB 1000'b: 13dB 1001'b: 15dB 1010'b: 16dB 1011'b: 17dB 1100'b: 18dB 1101'b: 19dB 1110'b: 20dB 1111'b: 21dB

9.17. MX-0010h: Micbias1 Control

Default: 0091'h

Table 99. MX-0010h: Micbas1 Control

DSP Address: 0x1800_C020 **I2C Address: 0x0010**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Dvo_micbias1	15:14	R/W	0'h	MICBIAS1 Output Voltage 00'b: 3.10V 01'b: 3.05V 10'b: 3.00V 11'b: 2.95V
Reserved	13:0	R	91'h	Reserved

9.18. MX-0014h: DAC1 Post Digital Volume

Default: 5757'h

Table 100. MX-0014h: DAC1 Post Digital Volume

DSP Address: 0x1800_C028 **I2C Address: 0x0014**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Dsp_post_mute_l	15	R/W	0'h	Stereo DAC_L Post Volume Mute Control 0'b: Un-mute 1'b: Mute
Dsp_post_gain_l	14:8	R/W	57'h	DAC1 left channel post digital volume in 0.75 dB step❶
Dsp_post_mute_r	7	R/W	0'h	Stereo DAC_R Post Volume Mute Control 0'b: Un-mute 1'b: Mute
Dsp_post_gain_r	6:0	R/W	57'h	DAC1 right channel post digital volume in 0.75 dB step❶

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-65.25	23	17	-48	46	2E	-30.75	69	45	-13.5
1	1	-64.5	24	18	-47.25	47	2F	-30	70	46	-12.75
2	2	-63.75	25	19	-46.5	48	30	-29.25	71	47	-12
3	3	-63	26	1A	-45.75	49	31	-28.5	72	48	-11.25
4	4	-62.25	27	1B	-45	50	32	-27.75	73	49	-10.5
5	5	-61.5	28	1C	-44.25	51	33	-27	74	4A	-9.75
6	6	-60.75	29	1D	-43.5	52	34	-26.25	75	4B	-9
7	7	-60	30	1E	-42.75	53	35	-25.5	76	4C	-8.25
8	8	-59.25	31	1F	-42	54	36	-24.75	77	4D	-7.5
9	9	-58.5	32	20	-41.25	55	37	-24	78	4E	-6.75
10	A	-57.75	33	21	-40.5	56	38	-23.25	79	4F	-6
11	B	-57	34	22	-39.75	57	39	-22.5	80	50	-5.25
12	C	-56.25	35	23	-39	58	3A	-21.75	81	51	-4.5
13	D	-55.5	36	24	-38.25	59	3B	-21	82	52	-3.75
14	E	-54.75	37	25	-37.5	60	3C	-20.25	83	53	-3
15	F	-54	38	26	-36.75	61	3D	-19.5	84	54	-2.25
16	10	-53.25	39	27	-36	62	3E	-18.75	85	55	-1.5
17	11	-52.5	40	28	-35.25	63	3F	-18	86	56	-0.75
18	12	-51.75	41	29	-34.5	64	40	-17.25	87	57	0
19	13	-51	42	2A	-33.75	65	41	-16.5			
20	14	-50.25	43	2B	-33	66	42	-15.75			
21	15	-49.5	44	2C	-32.25	67	43	-15			

22	16	-48.75	45	2D	-31.5	68	44	-14.25			

9.19. MX-0015h: DAC1 Digital Volume

Default: AFAF'h

Table 101. MX-0015h: DAC1 Digital Volume

DSP Address: 0x1800_C02A **I2C Address: 0x0015**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
vol_dac1_l	15:8	R/W	AF'h	DAC1 left channel digital volume in 0.375 dB step❶
vol_dac1_r	7:0	R/W	AF'h	DAC1 right channel digital volume in 0.375 dB step❶

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-65.625	36	24	-52.125	72	48	-38.625	108	6C	-25.125	144	90	-11.625
1	1	-65.25	37	25	-51.75	73	49	-38.25	109	6D	-24.75	145	91	-11.25
2	2	-64.875	38	26	-51.375	74	4A	-37.875	110	6E	-24.375	146	92	-10.875
3	3	-64.5	39	27	-51	75	4B	-37.5	111	6F	-24	147	93	-10.5
4	4	-64.125	40	28	-50.625	76	4C	-37.125	112	70	-23.625	148	94	-10.125
5	5	-63.75	41	29	-50.25	77	4D	-36.75	113	71	-23.25	149	95	-9.75
6	6	-63.375	42	2A	-49.875	78	4E	-36.375	114	72	-22.875	150	96	-9.375
7	7	-63	43	2B	-49.5	79	4F	-36	115	73	-22.5	151	97	-9
8	8	-62.625	44	2C	-49.125	80	50	-35.625	116	74	-22.125	152	98	-8.625
9	9	-62.25	45	2D	-48.75	81	51	-35.25	117	75	-21.75	153	99	-8.25
10	A	-61.875	46	2E	-48.375	82	52	-34.875	118	76	-21.375	154	9A	-7.875
11	B	-61.5	47	2F	-48	83	53	-34.5	119	77	-21	155	9B	-7.5
12	C	-61.125	48	30	-47.625	84	54	-34.125	120	78	-20.625	156	9C	-7.125
13	D	-60.75	49	31	-47.25	85	55	-33.75	121	79	-20.25	157	9D	-6.75
14	E	-60.375	50	32	-46.875	86	56	-33.375	122	7A	-19.875	158	9E	-6.375
15	F	-60	51	33	-46.5	87	57	-33	123	7B	-19.5	159	9F	-6
16	10	-59.625	52	34	-46.125	88	58	-32.625	124	7C	-19.125	160	A0	-5.625
17	11	-59.25	53	35	-45.75	89	59	-32.25	125	7D	-18.75	161	A1	-5.25
18	12	-58.875	54	36	-45.375	90	5A	-31.875	126	7E	-18.375	162	A2	-4.875
19	13	-58.5	55	37	-45	91	5B	-31.5	127	7F	-18	163	A3	-4.5
20	14	-58.125	56	38	-44.625	92	5C	-31.125	128	80	-17.625	164	A4	-4.125
21	15	-57.75	57	39	-44.25	93	5D	-30.75	129	81	-17.25	165	A5	-3.75
22	16	-57.375	58	3A	-43.875	94	5E	-30.375	130	82	-16.875	166	A6	-3.375
23	17	-57	59	3B	-43.5	95	5F	-30	131	83	-16.5	167	A7	-3
24	18	-56.625	60	3C	-43.125	96	60	-29.625	132	84	-16.125	168	A8	-2.625

25	19	-56.25	61	3D	-42.75	97	61	-29.25	133	85	-15.75	169	A9	-2.25
26	1A	-55.875	62	3E	-42.375	98	62	-28.875	134	86	-15.375	170	AA	-1.875
27	1B	-55.5	63	3F	-42	99	63	-28.5	135	87	-15	171	AB	-1.5
28	1C	-55.125	64	40	-41.625	100	64	-28.125	136	88	-14.625	172	AC	-1.125
29	1D	-54.75	65	41	-41.25	101	65	-27.75	137	89	-14.25	173	AD	-0.75
30	1E	-54.375	66	42	-40.875	102	66	-27.375	138	8A	-13.875	174	AE	-0.375
31	1F	-54	67	43	-40.5	103	67	-27	139	8B	-13.5	175	AF	0
32	20	-53.625	68	44	-40.125	104	68	-26.625	140	8C	-13.125			
33	21	-53.25	69	45	-39.75	105	69	-26.25	141	8D	-12.75			
34	22	-52.875	70	46	-39.375	106	6A	-25.875	142	8E	-12.375			
35	23	-52.5	71	47	-39	107	6B	-25.5	143	8F	-12			

9.20. MX-0016h: DAC2 Digital Volume

Default: AFAF'h

Table 102. MX-0016h: DAC2 Digital Volume

DSP Address: 0x1800_C02C **I2C Address: 0x0016**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
vol_dac2_l	15:8	R/W	AF'h	DAC2 left channel digital volume in 0.375 dB step❶
vol_dac2_r	7:0	R/W	AF'h	DAC2 right channel digital volume in 0.375 dB step❶

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-65.625	36	24	-52.125	72	48	-38.625	108	6C	-25.125	144	90	-11.625
1	1	-65.25	37	25	-51.75	73	49	-38.25	109	6D	-24.75	145	91	-11.25
2	2	-64.875	38	26	-51.375	74	4A	-37.875	110	6E	-24.375	146	92	-10.875
3	3	-64.5	39	27	-51	75	4B	-37.5	111	6F	-24	147	93	-10.5
4	4	-64.125	40	28	-50.625	76	4C	-37.125	112	70	-23.625	148	94	-10.125
5	5	-63.75	41	29	-50.25	77	4D	-36.75	113	71	-23.25	149	95	-9.75
6	6	-63.375	42	2A	-49.875	78	4E	-36.375	114	72	-22.875	150	96	-9.375
7	7	-63	43	2B	-49.5	79	4F	-36	115	73	-22.5	151	97	-9
8	8	-62.625	44	2C	-49.125	80	50	-35.625	116	74	-22.125	152	98	-8.625
9	9	-62.25	45	2D	-48.75	81	51	-35.25	117	75	-21.75	153	99	-8.25
10	A	-61.875	46	2E	-48.375	82	52	-34.875	118	76	-21.375	154	9A	-7.875
11	B	-61.5	47	2F	-48	83	53	-34.5	119	77	-21	155	9B	-7.5
12	C	-61.125	48	30	-47.625	84	54	-34.125	120	78	-20.625	156	9C	-7.125
13	D	-60.75	49	31	-47.25	85	55	-33.75	121	79	-20.25	157	9D	-6.75
14	E	-60.375	50	32	-46.875	86	56	-33.375	122	7A	-19.875	158	9E	-6.375

15	F	-60	51	33	-46.5	87	57	-33	123	7B	-19.5	159	9F	-6
16	10	-59.625	52	34	-46.125	88	58	-32.625	124	7C	-19.125	160	A0	-5.625
17	11	-59.25	53	35	-45.75	89	59	-32.25	125	7D	-18.75	161	A1	-5.25
18	12	-58.875	54	36	-45.375	90	5A	-31.875	126	7E	-18.375	162	A2	-4.875
19	13	-58.5	55	37	-45	91	5B	-31.5	127	7F	-18	163	A3	-4.5
20	14	-58.125	56	38	-44.625	92	5C	-31.125	128	80	-17.625	164	A4	-4.125
21	15	-57.75	57	39	-44.25	93	5D	-30.75	129	81	-17.25	165	A5	-3.75
22	16	-57.375	58	3A	-43.875	94	5E	-30.375	130	82	-16.875	166	A6	-3.375
23	17	-57	59	3B	-43.5	95	5F	-30	131	83	-16.5	167	A7	-3
24	18	-56.625	60	3C	-43.125	96	60	-29.625	132	84	-16.125	168	A8	-2.625
25	19	-56.25	61	3D	-42.75	97	61	-29.25	133	85	-15.75	169	A9	-2.25
26	1A	-55.875	62	3E	-42.375	98	62	-28.875	134	86	-15.375	170	AA	-1.875
27	1B	-55.5	63	3F	-42	99	63	-28.5	135	87	-15	171	AB	-1.5
28	1C	-55.125	64	40	-41.625	100	64	-28.125	136	88	-14.625	172	AC	-1.125
29	1D	-54.75	65	41	-41.25	101	65	-27.75	137	89	-14.25	173	AD	-0.75
30	1E	-54.375	66	42	-40.875	102	66	-27.375	138	8A	-13.875	174	AE	-0.375
31	1F	-54	67	43	-40.5	103	67	-27	139	8B	-13.5	175	AF	0
32	20	-53.625	68	44	-40.125	104	68	-26.625	140	8C	-13.125			
33	21	-53.25	69	45	-39.75	105	69	-26.25	141	8D	-12.75			
34	22	-52.875	70	46	-39.375	106	6A	-25.875	142	8E	-12.375			
35	23	-52.5	71	47	-39	107	6B	-25.5	143	8F	-12			

9.21. MX-0017h: DAC3 Digital Volume

Default: AFAF'h

Table 103. MX-0017h: DAC3 Digital Volume

DSP Address: 0x1800_C02E I2C Address: 0x0017				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
vol_dac3_l	15:8	R/W	AF'h	DAC3 left channel digital volume in 0.375 dB step❶
vol_dac3_r	7:0	R/W	AF'h	DAC3 right channel digital volume in 0.375 dB step❶

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-65.625	36	24	-52.125	72	48	-38.625	108	6C	-25.125	144	90	-11.625
1	1	-65.25	37	25	-51.75	73	49	-38.25	109	6D	-24.75	145	91	-11.25
2	2	-64.875	38	26	-51.375	74	4A	-37.875	110	6E	-24.375	146	92	-10.875
3	3	-64.5	39	27	-51	75	4B	-37.5	111	6F	-24	147	93	-10.5
4	4	-64.125	40	28	-50.625	76	4C	-37.125	112	70	-23.625	148	94	-10.125
5	5	-63.75	41	29	-50.25	77	4D	-36.75	113	71	-23.25	149	95	-9.75
6	6	-63.375	42	2A	-49.875	78	4E	-36.375	114	72	-22.875	150	96	-9.375
7	7	-63	43	2B	-49.5	79	4F	-36	115	73	-22.5	151	97	-9
8	8	-62.625	44	2C	-49.125	80	50	-35.625	116	74	-22.125	152	98	-8.625
9	9	-62.25	45	2D	-48.75	81	51	-35.25	117	75	-21.75	153	99	-8.25
10	A	-61.875	46	2E	-48.375	82	52	-34.875	118	76	-21.375	154	9A	-7.875
11	B	-61.5	47	2F	-48	83	53	-34.5	119	77	-21	155	9B	-7.5
12	C	-61.125	48	30	-47.625	84	54	-34.125	120	78	-20.625	156	9C	-7.125
13	D	-60.75	49	31	-47.25	85	55	-33.75	121	79	-20.25	157	9D	-6.75
14	E	-60.375	50	32	-46.875	86	56	-33.375	122	7A	-19.875	158	9E	-6.375
15	F	-60	51	33	-46.5	87	57	-33	123	7B	-19.5	159	9F	-6
16	10	-59.625	52	34	-46.125	88	58	-32.625	124	7C	-19.125	160	A0	-5.625
17	11	-59.25	53	35	-45.75	89	59	-32.25	125	7D	-18.75	161	A1	-5.25
18	12	-58.875	54	36	-45.375	90	5A	-31.875	126	7E	-18.375	162	A2	-4.875
19	13	-58.5	55	37	-45	91	5B	-31.5	127	7F	-18	163	A3	-4.5
20	14	-58.125	56	38	-44.625	92	5C	-31.125	128	80	-17.625	164	A4	-4.125
21	15	-57.75	57	39	-44.25	93	5D	-30.75	129	81	-17.25	165	A5	-3.75
22	16	-57.375	58	3A	-43.875	94	5E	-30.375	130	82	-16.875	166	A6	-3.375
23	17	-57	59	3B	-43.5	95	5F	-30	131	83	-16.5	167	A7	-3
24	18	-56.625	60	3C	-43.125	96	60	-29.625	132	84	-16.125	168	A8	-2.625
25	19	-56.25	61	3D	-42.75	97	61	-29.25	133	85	-15.75	169	A9	-2.25

26	1A	-55.875	62	3E	-42.375	98	62	-28.875	134	86	-15.375	170	AA	-1.875
27	1B	-55.5	63	3F	-42	99	63	-28.5	135	87	-15	171	AB	-1.5
28	1C	-55.125	64	40	-41.625	100	64	-28.125	136	88	-14.625	172	AC	-1.125
29	1D	-54.75	65	41	-41.25	101	65	-27.75	137	89	-14.25	173	AD	-0.75
30	1E	-54.375	66	42	-40.875	102	66	-27.375	138	8A	-13.875	174	AE	-0.375
31	1F	-54	67	43	-40.5	103	67	-27	139	8B	-13.5	175	AF	0
32	20	-53.625	68	44	-40.125	104	68	-26.625	140	8C	-13.125			
33	21	-53.25	69	45	-39.75	105	69	-26.25	141	8D	-12.75			
34	22	-52.875	70	46	-39.375	106	6A	-25.875	142	8E	-12.375			
35	23	-52.5	71	47	-39	107	6B	-25.5	143	8F	-12			

9.22. MX-001Ah: Stereo1 ADC Digital Mute/Unmute and Volume

Default: 2F2F'h

Table 104. MX-001Ah: Stereo1 ADC Digital Mute/Unmute and Volume

DSP Address: 0x1800_C034 **I2C Address: 0x001A**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_stereo1_adc_vol_l	15	R/W	0'h	Digital Mute From Stereo1 ADC Left Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_stereo1_adcl	14:8	R/W	2F'h	Stereo1 ADC left channel digital volume in 0.375 dB step❶
mu_stereo1_adc_vol_r	7	R/W	0'h	Digital Mute From Stereo1 ADC Right Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_stereo1_adcr	6:0	R/W	2F'h	Stereo1 ADC right channel digital volume in 0.375 dB step❶

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-17.625	26	1A	-7.875	52	34	1.875	78	4E	11.625	104	68	21.375
1	1	-17.25	27	1B	-7.5	53	35	2.25	79	4F	12	105	69	21.75
2	2	-16.875	28	1C	-7.125	54	36	2.625	80	50	12.375	106	6A	22.125
3	3	-16.5	29	1D	-6.75	55	37	3	81	51	12.75	107	6B	22.5
4	4	-16.125	30	1E	-6.375	56	38	3.375	82	52	13.125	108	6C	22.875
5	5	-15.75	31	1F	-6	57	39	3.75	83	53	13.5	109	6D	23.25
6	6	-15.375	32	20	-5.625	58	3A	4.125	84	54	13.875	110	6E	23.625
7	7	-15	33	21	-5.25	59	3B	4.5	85	55	14.25	111	6F	24
8	8	-14.625	34	22	-4.875	60	3C	4.875	86	56	14.625	112	70	24.375
9	9	-14.25	35	23	-4.5	61	3D	5.25	87	57	15	113	71	24.75
10	A	-13.875	36	24	-4.125	62	3E	5.625	88	58	15.375	114	72	25.125
11	B	-13.5	37	25	-3.75	63	3F	6	89	59	15.75	115	73	25.5
12	C	-13.125	38	26	-3.375	64	40	6.375	90	5A	16.125	116	74	25.875
13	D	-12.75	39	27	-3	65	41	6.75	91	5B	16.5	117	75	26.25

14	E	-12.375	40	28	-2.625	66	42	7.125	92	5C	16.875	118	76	26.625
15	F	-12	41	29	-2.25	67	43	7.5	93	5D	17.25	119	77	27
16	10	-11.625	42	2A	-1.875	68	44	7.875	94	5E	17.625	120	78	27.375
17	11	-11.25	43	2B	-1.5	69	45	8.25	95	5F	18	121	79	27.75
18	12	-10.875	44	2C	-1.125	70	46	8.625	96	60	18.375	122	7A	28.125
19	13	-10.5	45	2D	-0.75	71	47	9	97	61	18.75	123	7B	28.5
20	14	-10.125	46	2E	-0.375	72	48	9.375	98	62	19.125	124	7C	28.875
21	15	-9.75	47	2F	0	73	49	9.75	99	63	19.5	125	7D	29.25
22	16	-9.375	48	30	0.375	74	4A	10.125	100	64	19.875	126	7E	29.625
23	17	-9	49	31	0.75	75	4B	10.5	101	65	20.25	127	7F	30
24	18	-8.625	50	32	1.125	76	4C	10.875	102	66	20.625			
25	19	-8.25	51	33	1.5	77	4D	11.25	103	67	21			

9.23. MX-001Bh: Mono ADC Digital Mute/Unmute and Volume

Default: 2F2F'h

Table 105. MX-001Bh: Mono ADC Digital Mute/Unmute and Volume

DSP Address: 0x1800_C036 **I2C Address: 0x001B**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_mono_adc_vol_l	15	R/W	0'h	Digital Mute From Mono ADC Left Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_mono_adcl	14:8	R/W	2F'h	Mono ADC left channel digital volume in 0.375 dB step❶
mu_mono_adc_vol_r	7	R/W	0'h	Digital Mute From Mono ADC Right Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_mono_adcr	6:0	R/W	2F'h	Mono ADC right channel digital volume in 0.375 dB step❶

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-17.625	26	1A	-7.875	52	34	1.875	78	4E	11.625	104	68	21.375
1	1	-17.25	27	1B	-7.5	53	35	2.25	79	4F	12	105	69	21.75
2	2	-16.875	28	1C	-7.125	54	36	2.625	80	50	12.375	106	6A	22.125
3	3	-16.5	29	1D	-6.75	55	37	3	81	51	12.75	107	6B	22.5
4	4	-16.125	30	1E	-6.375	56	38	3.375	82	52	13.125	108	6C	22.875
5	5	-15.75	31	1F	-6	57	39	3.75	83	53	13.5	109	6D	23.25
6	6	-15.375	32	20	-5.625	58	3A	4.125	84	54	13.875	110	6E	23.625
7	7	-15	33	21	-5.25	59	3B	4.5	85	55	14.25	111	6F	24
8	8	-14.625	34	22	-4.875	60	3C	4.875	86	56	14.625	112	70	24.375
9	9	-14.25	35	23	-4.5	61	3D	5.25	87	57	15	113	71	24.75
10	A	-13.875	36	24	-4.125	62	3E	5.625	88	58	15.375	114	72	25.125
11	B	-13.5	37	25	-3.75	63	3F	6	89	59	15.75	115	73	25.5
12	C	-13.125	38	26	-3.375	64	40	6.375	90	5A	16.125	116	74	25.875
13	D	-12.75	39	27	-3	65	41	6.75	91	5B	16.5	117	75	26.25
14	E	-12.375	40	28	-2.625	66	42	7.125	92	5C	16.875	118	76	26.625
15	F	-12	41	29	-2.25	67	43	7.5	93	5D	17.25	119	77	27
16	10	-11.625	42	2A	-1.875	68	44	7.875	94	5E	17.625	120	78	27.375

17	11	-11.25	43	2B	-1.5	69	45	8.25	95	5F	18	121	79	27.75
18	12	-10.875	44	2C	-1.125	70	46	8.625	96	60	18.375	122	7A	28.125
19	13	-10.5	45	2D	-0.75	71	47	9	97	61	18.75	123	7B	28.5
20	14	-10.125	46	2E	-0.375	72	48	9.375	98	62	19.125	124	7C	28.875
21	15	-9.75	47	2F	0	73	49	9.75	99	63	19.5	125	7D	29.25
22	16	-9.375	48	30	0.375	74	4A	10.125	100	64	19.875	126	7E	29.625
23	17	-9	49	31	0.75	75	4B	10.5	101	65	20.25	127	7F	30
24	18	-8.625	50	32	1.125	76	4C	10.875	102	66	20.625			
25	19	-8.25	51	33	1.5	77	4D	11.25	103	67	21			

9.24. MX-001Ch: Stereo2 ADC Digital Mute/Unmute and Volume

Default: 2F2F'h

Table 106. MX-001Ch: Stereo2 ADC Digital Mute/Unmute and Volume

DSP Address: 0x1800_C038 **I2C Address: 0x001C**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_stereo2_adc_vol_l	15	R/W	0'h	Digital Mute From Stereo2 ADC Left Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_stereo2_adcl	14:8	R/W	2F'h	Stereo2 ADC left channel digital volume in 0.375 dB step❶
mu_stereo2_adc_vol_r	7	R/W	0'h	Digital Mute From Stereo2 ADC Right Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_stereo2_adcr	6:0	R/W	2F'h	Stereo2 ADC right channel digital volume in 0.375 dB step❶

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-17.625	26	1A	-7.875	52	34	1.875	78	4E	11.625	104	68	21.375
1	1	-17.25	27	1B	-7.5	53	35	2.25	79	4F	12	105	69	21.75
2	2	-16.875	28	1C	-7.125	54	36	2.625	80	50	12.375	106	6A	22.125
3	3	-16.5	29	1D	-6.75	55	37	3	81	51	12.75	107	6B	22.5
4	4	-16.125	30	1E	-6.375	56	38	3.375	82	52	13.125	108	6C	22.875
5	5	-15.75	31	1F	-6	57	39	3.75	83	53	13.5	109	6D	23.25
6	6	-15.375	32	20	-5.625	58	3A	4.125	84	54	13.875	110	6E	23.625
7	7	-15	33	21	-5.25	59	3B	4.5	85	55	14.25	111	6F	24
8	8	-14.625	34	22	-4.875	60	3C	4.875	86	56	14.625	112	70	24.375
9	9	-14.25	35	23	-4.5	61	3D	5.25	87	57	15	113	71	24.75
10	A	-13.875	36	24	-4.125	62	3E	5.625	88	58	15.375	114	72	25.125
11	B	-13.5	37	25	-3.75	63	3F	6	89	59	15.75	115	73	25.5
12	C	-13.125	38	26	-3.375	64	40	6.375	90	5A	16.125	116	74	25.875
13	D	-12.75	39	27	-3	65	41	6.75	91	5B	16.5	117	75	26.25
14	E	-12.375	40	28	-2.625	66	42	7.125	92	5C	16.875	118	76	26.625
15	F	-12	41	29	-2.25	67	43	7.5	93	5D	17.25	119	77	27
16	10	-11.625	42	2A	-1.875	68	44	7.875	94	5E	17.625	120	78	27.375
17	11	-11.25	43	2B	-1.5	69	45	8.25	95	5F	18	121	79	27.75
18	12	-10.875	44	2C	-1.125	70	46	8.625	96	60	18.375	122	7A	28.125

19	13	-10.5	45	2D	-0.75	71	47	9	97	61	18.75	123	7B	28.5
20	14	-10.125	46	2E	-0.375	72	48	9.375	98	62	19.125	124	7C	28.875
21	15	-9.75	47	2F	0	73	49	9.75	99	63	19.5	125	7D	29.25
22	16	-9.375	48	30	0.375	74	4A	10.125	100	64	19.875	126	7E	29.625
23	17	-9	49	31	0.75	75	4B	10.5	101	65	20.25	127	7F	30
24	18	-8.625	50	32	1.125	76	4C	10.875	102	66	20.625			
25	19	-8.25	51	33	1.5	77	4D	11.25	103	67	21			

9.25. MX-001Dh: Stereo3 ADC Digital Mute/Unmute and Volume

Default: 2F2F'h

Table 107. MX-001Dh: Stereo3 ADC Digital Mute/Unmute and Volume

DSP Address: 0x1800_C03A **I2C Address: 0x001D**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_stereo3_adc_vol_l	15	R/W	0'h	Digital Mute From Stereo3 ADC Left Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_stereo3_adcl	14:8	R/W	2F'h	Stereo3 ADC left channel digital volume in 0.375 dB step❶
mu_stereo3_adc_vol_r	7	R/W	0'h	Digital Mute From Stereo3 ADC Right Channel Digital Mixer 0'b : Un-Mute 1'b : Mute (-∞ dB)
Vol_stereo3_adcr	6:0	R/W	2F'h	Stereo3 ADC right channel digital volume in 0.375 dB step❶

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-17.625	26	1A	-7.875	52	34	1.875	78	4E	11.625	104	68	21.375
1	1	-17.25	27	1B	-7.5	53	35	2.25	79	4F	12	105	69	21.75
2	2	-16.875	28	1C	-7.125	54	36	2.625	80	50	12.375	106	6A	22.125
3	3	-16.5	29	1D	-6.75	55	37	3	81	51	12.75	107	6B	22.5
4	4	-16.125	30	1E	-6.375	56	38	3.375	82	52	13.125	108	6C	22.875
5	5	-15.75	31	1F	-6	57	39	3.75	83	53	13.5	109	6D	23.25
6	6	-15.375	32	20	-5.625	58	3A	4.125	84	54	13.875	110	6E	23.625
7	7	-15	33	21	-5.25	59	3B	4.5	85	55	14.25	111	6F	24
8	8	-14.625	34	22	-4.875	60	3C	4.875	86	56	14.625	112	70	24.375
9	9	-14.25	35	23	-4.5	61	3D	5.25	87	57	15	113	71	24.75
10	A	-13.875	36	24	-4.125	62	3E	5.625	88	58	15.375	114	72	25.125
11	B	-13.5	37	25	-3.75	63	3F	6	89	59	15.75	115	73	25.5
12	C	-13.125	38	26	-3.375	64	40	6.375	90	5A	16.125	116	74	25.875
13	D	-12.75	39	27	-3	65	41	6.75	91	5B	16.5	117	75	26.25
14	E	-12.375	40	28	-2.625	66	42	7.125	92	5C	16.875	118	76	26.625
15	F	-12	41	29	-2.25	67	43	7.5	93	5D	17.25	119	77	27
16	10	-11.625	42	2A	-1.875	68	44	7.875	94	5E	17.625	120	78	27.375
17	11	-11.25	43	2B	-1.5	69	45	8.25	95	5F	18	121	79	27.75
18	12	-10.875	44	2C	-1.125	70	46	8.625	96	60	18.375	122	7A	28.125
19	13	-10.5	45	2D	-0.75	71	47	9	97	61	18.75	123	7B	28.5
20	14	-10.125	46	2E	-0.375	72	48	9.375	98	62	19.125	124	7C	28.875

21	15	-9.75	47	2F	0	73	49	9.75	99	63	19.5	125	7D	29.25
22	16	-9.375	48	30	0.375	74	4A	10.125	100	64	19.875	126	7E	29.625
23	17	-9	49	31	0.75	75	4B	10.5	101	65	20.25	127	7F	30
24	18	-8.625	50	32	1.125	76	4C	10.875	102	66	20.625			
25	19	-8.25	51	33	1.5	77	4D	11.25	103	67	21			

9.26. MX-0020h: Stereo1/2 ADC Boost Gain

Default: 0000'h

Table 108. MX-0020h: Stereo1/2 ADC Boost Gain

DSP Address: 0x1800_C040 **I2C Address: 0x0020**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Stereo1_ad_bst_gain_l	15:14	R/W	0'h	Stereo1 ADC left channel digital boost gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Stereo1_ad_bst_gain_r	13:12	R/W	0'h	Stereo 1ADC Right channel digital boost gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Stereo1_ad_comp_gain	11:10	R/W	0'h	Stereo1 ADC compensate gain 00'b : 0dB 01'b: 1dB 10'b : 2dB 11'b: 3dB
Stereo2_ad_bst_gain_l	9:8	R/W	0'h	Stereo2 ADC left channel digital boost gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Stereo2_ad_bst_gain_r	7:6	R/W	0'h	Stereo 2ADC Right channel digital boost gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Stereo2_ad_comp_gain	5:4	R/W	0'h	Stereo2 ADC compensate gain 00'b : 0dB 01'b: 1dB 10'b : 2dB 11'b: 3dB
reserved	3:1	R	0'h	Reserved
Sel_monoadcl2stereoadc	0	R/W	0'h	Mono_ADC_L to Stereo_ADC_L/R Control 0'b: From Stereo_ADC 1'b: From Mono_ADC_L

9.27. MX-0021h: Mono ADC Boost Gain

Default: 0000'h

Table 109. MX-0021h: Mono ADC Boost Gain

DSP Address: 0x1800_C042 **I2C Address: 0x0021**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Mono_ad_bst_gain_l	15:14	R/W	0'h	Mono ADC left channel digital boost gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Mono_ad_bst_gain_r	13:12	R/W	0'h	Mono 1ADC Right channel digital boost gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Mono_ad_comp_gain	11:10	R/W	0'h	Mono ADC compensate gain 00'b : 0dB 01'b: 1dB 10'b : 2dB 11'b: 3dB
reserved	9:0	R	0'h	Reserved

9.28. MX-0022h: Stereo3 ADC Boost Gain

Default: 0000'h

Table 110. MX-0022h: Stereo3 ADC Boost Gain

DSP Address: 0x1800_C044 I2C Address: 0x0022				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Stereo3_ad_bst_gain_l	15:14	R/W	0'h	Stereo3 ADC left channel digital boost gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Stereo3_ad_bst_gain_r	13:12	R/W	0'h	Stereo3 1ADC Right channel digital boost gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b: 36dB
Stereo3_ad_comp_gain	11:10	R/W	0'h	Stereo3 ADC compensate gain 00'b : 0dB 01'b: 1dB 10'b : 2dB 11'b: 3dB
reserved	9:0	R	0'h	Reserved

9.29. MX-0028h: SPDIF In Control

Default: 6000'h

Table 111. MX-0028h: SPDIF In Control

DSP Address: 0x1800_C050 I2C Address: 0x0028				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Spdif_in_en	15	R/W	0'h	Enable SPDIF In 0'b: Disable 1'b: Enable
Reserved	14:3	R	C00'h	Reserved
Spdif_in_hwrate	2:0	R	0'h	Real Sampling rate of S/PDIF-IN 000'b: 32kHz 001'b: 48kHz 010'b: 96kHz 011'b: 192kHz 101'b: 44.1kHz 110'b: 88.2kHz Others: Unknown

9.30. MX-002Ah: IF3 Data Control

Default: 0000'h

Table 112. MX-002Ah: IF3 Data Control

DSP Address: 0x1800_C054 **I2C Address: 0x002A**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:8	R	0'h	Reserved
sel_if3_dac_data	7:6	R/W	0'h	Select Interface3 DAC Data Swap 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
sel_if3_adc_data	5:4	R/W	0'h	Select Interface3 ADC Data Swap 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
Sel_if3_adc_data_in	3:0	R/W	0'h	Select Interface3 ADC Data Input 0000'b: Stereo1_ADC_Mixer_L/R 0001'b: Stereo2_ADC_Mixer_L/R 0010'b: Stereo3_ADC_Mixer_L/R 0011'b: Mono_ADC_Mixer_L/R 0100'b: OutBound0/1 0101'b: OutBound2/3 0110'b: OutBound4/5 0111'b: OutBound0/1_Mini 1000'b: VAD_ADC 1001'b: IF1_DAC_0/1 1010'b: IF2_DAC_0/1 1011'b: IF4_DAC_L/R 1100'b: IF5_DAC_L/R 1101'b: OutBound6/7 Others: Reserved

9.31. MX-002Bh: IF4 Data Control

Default: 0000'h

Table 113. MX-002Bh: IF4 Data Control

DSP Address: 0x1800_C056 **I2C Address: 0x002B**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:8	R	0'h	Reserved
sel_if4_dac_data	7:6	R/W	0'h	Select Interface4 DAC Data Swap 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
sel_if4_adc_data	5:4	R/W	0'h	Select Interface4 ADC Data Swap 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
Sel_if4_adc_data_in	3:0	R/W	0'h	Select Interface4 ADC Data Input 0000'b: Stereo1_ADC_Mixer_L/R 0001'b: Stereo2_ADC_Mixer_L/R 0010'b: Stereo3_ADC_Mixer_L/R 0011'b: Mono_ADC_Mixer_L/R 0100'b: OutBound0/1 0101'b: OutBound2/3 0110'b: OutBound4/5 0111'b: OutBound0/1_Mini 1000'b: VAD_ADC 1001'b: IF1_DAC_0/1 1010'b: IF2_DAC_0/1 1011'b: IF3_DAC_L/R 1100'b: IF5_DAC_L/R 1101'b: OutBound6/7 Others: Reserved

9.32. MX-002Ch: IF5 Data Control

Default: 0000’h

Table 114. MX-002Ch: IF5 Data Control

DSP Address: 0x1800_C058 **I2C Address: 0x002C**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:8	R	0’h	Reserved
sel_if5_dac_data	7:6	R/W	0’h	Select Interface5 DAC Data Swap 00’b: L/R 01’b: R/L 10’b: L/L 11’b: R/R
sel_if5_adc_data	5:4	R/W	0’h	Select Interface5 ADC Data Swap 00’b: L/R 01’b: R/L 10’b: L/L 11’b: R/R
Sel_if5_adc_data_in	3:0	R/W	0’h	Select Interface5 ADC Data Input 0000’b: Stereo1_ADC_Mixer_L/R 0001’b: Stereo2_ADC_Mixer_L/R 0010’b: Stereo3_ADC_Mixer_L/R 0011’b: Mono_ADC_Mixer_L/R 0100’b: OutBound0/1 0101’b: OutBound2/3 0110’b: OutBound4/5 0111’b: OutBound0/1_Mini 1000’b: VAD_ADC 1001’b: IF1_DAC_0/1 1010’b: IF2_DAC_0/1 1011’b: IF3_DAC_L/R 1100’b: IF4_DAC_L/R 1101’b: OutBound6/7 Others: Reserved

9.33. MX-0030h: TDM1 Control 1

Default: 00F0'h

Table 115. MX-0030h: TDM1 Control 1

DSP Address: 0x1800_C060 **I2C Address: 0x0030**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Tdm1_mode_sel	15	R/W	0'h	I2S1 / TDM1 Mode Control 0'b: Normal I2S Mode 1'b: TDM Mode
Reserved	14:12	R	0'h	Reserved
Tdm1_in_slot_sel	11:10	R/W	0'h	TDM1 Input Channel Number Select 00'b: 2ch 01'b: 4ch 10'b: 6ch 11'b: 8ch
Tdm1_out_slot_sel	9:8	R/W	0'h	TDM1 Output Channel Number Select 00'b: 2ch 01'b: 4ch 10'b: 6ch 11'b: 8ch
Tdm1_in_channel_length	7:6	R/W	3'h	TDM1 Input Channel Length 00'b: 16bit (For Slave Mode) 01'b: 20bit (For Slave Mode) 10'b: 24bit (For Slave Mode) 11'b: 32bit (For Slave Mode)
Tdm1_out_channel_length	5:4	R/W	3'h	TDM1 Output Channel Length 00'b: 16bit (For Slave Mode) 01'b: 20bit (For Slave Mode) 10'b: 24bit (For Slave Mode) 11'b: 32bit (For Slave Mode)
Reserved	3:0	R	0'h	Reserved

9.34. MX-0031h: TDM1 Control 2

Default: 0000'h

Table 116. MX-0031h: TDM1 Control 2

DSP Address: 0x1800_C062 I2C Address: 0x0031				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s1_rx_ch2	15:14	R/W	0'h	Data Swap for Slot0/1 in ADCDAT1 2'b00: L/R 2'b01: R/L 2'b10: L/L 2'b11: R/R
sel_i2s1_rx_ch4	13:12	R/W	0'h	Data Swap for Slot2/3 in ADCDAT1 2'b00: L/R 2'b01: R/L 2'b10: L/L 2'b11: R/R
sel_i2s1_rx_ch6	11:10	R/W	0'h	Data Swap for Slot4/5 in ADCDAT1 2'b00: L/R 2'b01: R/L 2'b10: L/L 2'b11: R/R
sel_i2s1_rx_ch8	9:8	R/W	0'h	Data Swap for Slot6/7 in ADCDAT1 2'b00: L/R 2'b01: R/L 2'b10: L/L 2'b11: R/R
Reserved	7:0	R	0'h	Reserved

9.35. MX-0032h: TDM1 Control 3

Default: 0000'h

Table 117. MX-0032h: TDM1 Control 3

DSP Address: 0x1800_C064 I2C Address: 0x0032				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_i2s_rx_adc4_pre_i2s1	15:14	R/W	0'h	TDM1 IF1_ADC4 Data Selection 00'b: Stereo3_ADC_Mixer_L/R 01'b: DACL1_FS/DACR1_FS 10'b: OutBound6/7 11'b: Reserved
Sel_i2s_rx_adc3_pre_i2s1	13:12	R/W	0'h	TDM1 IF1_ADC3 Data Selection 00'b: Mono_ADC_Mixer_L/R 01'b: OutBound4/5 10'b: DAC1_FS 11'b: VAD_ADC_Filter
Sel_i2s_rx_adc2_pre_i2s1	11	R/W	0'h	TDM1 IF1_ADC2 Data Selection 0'b: Stereo2_ADC_Mixer_L/R 1'b: OutBound2/3
Sel_i2s_rx_adc1_pre_i2s1	10:8	R/W	0'h	TDM1 IF1_ADC1 Data Selection 000'b: Stereo1_ADC_Mixer_L/R 001'b: OutBound0/1 010'b: OutBound0/1_Mini 011'b: VAD_ADC 100'b: IF2_DAC_0/1 101'b: IF3_DAC_L/R 110'b: IF4_DAC_L/R 111'b: IF5_DAC_L/R
Reserved	7:5	R	0'h	Reserved

Sel_i2s_rx_i2s1	4:0	R/W	0'h	TDM1 ADC Data Control 00'h: 1/2/3/4 01'h: 1/2/4/3 02'h: 1/3/2/4 03'h: 1/3/4/2 04'h: 1/4/3/2 05'h: 1/4/2/3 06'h: 2/1/3/4 07'h: 2/1/4/3 08'h: 2/3/1/4 09'h: 2/3/4/1 0A'h: 2/4/3/1 0B'h: 2/4/1/3 0C'h: 3/1/2/4 0D'h: 3/1/4/2 0E'h: 3/2/1/4 0F'h: 3/2/4/1 10'h: 3/4/2/1 11'h: 3/4/1/2 12'h: 4/1/2/3 13'h: 4/1/3/2 14'h: 4/2/1/3 15'h: 4/2/3/1 16'h: 4/3/2/1 17'h: 4/3/1/2 Others: Reserved

9.36. MX-0033h: TDM1 Control 4

Default: 0000'h

Table 118. MX-0033h: TDM1 Control 4

DSP Address: 0x1800_C066 **I2C Address: 0x0033**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s1_lrck_polarity	15	R/W	0'h	LRCK1 Polarity Inverter 0'b: Don't invert 1'b: Invert
Reserved	14:13	R	0'h	Reserved
if_self_lpbk_en	12	R/W	0'h	Interface Loopback test 0'b: loopback disable 1'b: loopback enable
Reserved	11:8	R	0'h	Reserved
mute_tdm2_outl_i2s1	7	R/W	0'h	adc1 left data mute/unmute ctrl 0'b : Un-Mute 1'b : Mute
mute_tdm2_outr_i2s1	6	R/W	0'h	adc1 right data mute/unmute ctrl 0'b : Un-Mute 1'b : Mute
mute_tdm4_outl_i2s1	5	R/W	0'h	adc2 left data mute/unmute ctrl 0'b : Un-Mute 1'b : Mute
mute_tdm4_outr_i2s1	4	R/W	0'h	adc2 right data mute/unmute ctrl 0'b : Un-Mute 1'b : Mute
mute_tdm6_outl_i2s1	3	R/W	0'h	adc3 left data mute/unmute ctrl 0'b : Un-Mute 1'b : Mute
mute_tdm6_outr_i2s1	2	R/W	0'h	adc3 right data mute/unmute ctrl 0'b : Un-Mute 1'b : Mute
mute_tdm8_outl_i2s1	1	R/W	0'h	adc4 left data mute/unmute ctrl 0'b : Un-Mute 1'b : Mute
mute_tdm8_outr_i2s1	0	R/W	0'h	adc4 right data mute/unmute ctrl 0'b : Un-Mute 1'b : Mute

9.37. MX-0034h: TDM1 Control 5

Default: 0123'h

Table 119. MX-0034h: TDM1 Control 5

DSP Address: 0x1800_C068 **I2C Address: 0x0034**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
sel_i2s1_tx_l_ch2	14:12	R/W	0'h	IF1_DAC_0 Data Selection 3'b000: Slot0 3'b001: Slot1 3'b010: Slot2 3'b011: Slot3 3'b100: Slot4 3'b101: Slot5 3'b110: Slot6 3'b111: Slot7
Reserved	11	R	0'h	Reserved
sel_i2s1_tx_r_ch2	10:8	R/W	1'h	IF1_DAC_1 Data Selection 3'b000: Slot0 3'b001: Slot1 3'b010: Slot2 3'b011: Slot3 3'b100: Slot4 3'b101: Slot5 3'b110: Slot6 3'b111: Slot7
Reserved	7	R	0'h	Reserved
sel_i2s1_tx_l_ch4	6:4	R/W	2'h	IF1_DAC_2 Data Selection 3'b000: Slot0 3'b001: Slot1 3'b010: Slot2 3'b011: Slot3 3'b100: Slot4 3'b101: Slot5 3'b110: Slot6 3'b111: Slot7
Reserved	3	R	0'h	Reserved
sel_i2s1_tx_r_ch4	2:0	R/W	3'h	IF1_DAC_3 Data Selection 3'b000: Slot0 3'b001: Slot1 3'b010: Slot2 3'b011: Slot3 3'b100: Slot4 3'b101: Slot5 3'b110: Slot6 3'b111: Slot7

9.38. MX-0035h: TDM1 Control 6

Default: 4567'h

Table 120. MX-0035h: TDM1 Control 6

DSP Address: 0x1800_C06A **I2C Address: 0x0035**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
sel_i2s1_tx_l_ch6	14:12	R/W	4'h	IF1_DAC_4 Data Selection 3'b000: Slot0 3'b001: Slot1 3'b010: Slot2 3'b011: Slot3 3'b100: Slot4 3'b101: Slot5 3'b110: Slot6 3'b111: Slot7
Reserved	11	R	0'h	Reserved
sel_i2s1_tx_r_ch6	10:8	R/W	5'h	IF1_DAC_5 Data Selection 3'b000: Slot0 3'b001: Slot1 3'b010: Slot2 3'b011: Slot3 3'b100: Slot4 3'b101: Slot5 3'b110: Slot6 3'b111: Slot7
Reserved	7	R	0'h	Reserved
sel_i2s1_tx_l_ch8	6:4	R/W	6'h	IF1_DAC_6 Data Selection 3'b000: Slot0 3'b001: Slot1 3'b010: Slot2 3'b011: Slot3 3'b100: Slot4 3'b101: Slot5 3'b110: Slot6 3'b111: Slot7
Reserved	3	R	0'h	Reserved
sel_i2s1_tx_r_ch8	2:0	R/W	7'h	IF1_DAC_7 Data Selection 3'b000: Slot0 3'b001: Slot1 3'b010: Slot2 3'b011: Slot3 3'b100: Slot4 3'b101: Slot5 3'b110: Slot6 3'b111: Slot7

9.39. MX-0036h: TDM1 Control 7

Default: 8003'h

Table 121. MX-0036h: TDM1 Control 7

DSP Address: 0x1800_C06C **I2C Address: 0x0036**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:7	R	100'h	Reserved
Tdm1_mode_sel_mst	6	R/W	0'h	TDM1 I2S / TDM Mode Control for Master mode 0'b: Normal I2S Mode 1'b: TDM Mode
Tdm1_lrck_sel_mst	5:4	R/W	0'h	TDM1 LRCK Divider Control for Master mode 00'b: ÷ 256 01'b: ÷ 128 10'b: ÷ 64 11'b: ÷ 32
Tdm1_slot_sel_mst	3:2	R/W	0'h	TDM1 Channel Number Select for Master mode 00'b: 2ch 01'b: 4ch 10'b: Reserved 11'b: 8ch
Tdm1_channel_length_mst	1:0	R/W	3'h	TDM1 Channel Length for Master mode 00'b: 16bit 01'b: 20bit 10'b: 24bit 11'b: 32bit

9.40. MX-0038h: TDM2 Control 1

Default: 00F0'h

Table 122. MX-0038h: TDM2 Control 1

DSP Address: 0x1800_C070 **I2C Address: 0x0038**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Tdm2_mode_sel	15	R/W	0'h	I2S1 / TDM2 Mode Control 0'b: Normal I2S Mode 1'b: TDM Mode
Reserved	14:12	R	0'h	Reserved
Tdm2_in_slot_sel	11:10	R/W	0'h	TDM2 Input Channel Number Select 00'b: 2ch 01'b: 4ch 10'b: 6ch 11'b: 8ch
Tdm2_out_slot_sel	9:8	R/W	0'h	TDM2 Output Channel Number Select 00'b: 2ch 01'b: 4ch 10'b: 6ch 11'b: 8ch
Tdm2_in_channel_length	7:6	R/W	3'h	TDM2 Input Channel Length 00'b: 16bit (For Slave Mode) 01'b: 20bit (For Slave Mode) 10'b: 24bit (For Slave Mode) 11'b: 32bit (For Slave Mode)
Tdm2_out_channel_length	5:4	R/W	3'h	TDM2 Output Channel Length 00'b: 16bit (For Slave Mode) 01'b: 20bit (For Slave Mode) 10'b: 24bit (For Slave Mode) 11'b: 32bit (For Slave Mode)
Reserved	3:0	R	0'h	Reserved

9.41. MX-0039h: TDM2 Control 2

Default: 0000'h

Table 123. MX-0039h: TDM2 Control 2

DSP Address: 0x1800_C072 I2C Address: 0x0039				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s2_rx_ch2	15:14	R/W	0'h	Data Swap for Slot0/1 in ADCDAT2 2'b00: L/R 2'b01: R/L 2'b10: L/L 2'b11: R/R
sel_i2s2_rx_ch4	13:12	R/W	0'h	Data Swap for Slot2/3 in ADCDAT2 2'b00: L/R 2'b01: R/L 2'b10: L/L 2'b11: R/R
sel_i2s2_rx_ch6	11:10	R/W	0'h	Data Swap for Slot4/5 in ADCDAT2 2'b00: L/R 2'b01: R/L 2'b10: L/L 2'b11: R/R
sel_i2s2_rx_ch8	9:8	R/W	0'h	Data Swap for Slot6/7 in ADCDAT2 2'b00: L/R 2'b01: R/L 2'b10: L/L 2'b11: R/R
Reserved	7:0	R	0'h	Reserved

9.42. MX-003Ah: TDM2 Control 3

Default: 0000'h

Table 124. MX-003Ah: TDM2 Control 3

DSP Address: 0x1800_C074 I2C Address: 0x003A				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_i2s_rx_adc4_pre_i2s2	15:14	R/W	0'h	TDM2 IF2_ADC4 Data Selection 00'b: Stereo3_ADC_Mixer_L/R 01'b: DACL1_FS/DACR1_FS 10'b: OutBound6/7 11'b: Reserved
Sel_i2s_rx_adc3_pre_i2s2	13:12	R/W	0'h	TDM2 IF2_ADC3 Data Selection 00'b: Mono_ADC_Mixer_L/R 01'b: OutBound4/5 10'b: DAC1_FS 11'b: Reserved
Sel_i2s_rx_adc2_pre_i2s2	11	R/W	0'h	TDM2 IF2_ADC2 Data Selection 0'b: Stereo2_ADC_Mixer_L/R 1'b: OutBound2/3
Sel_i2s_rx_adc1_pre_i2s2	10:8	R/W	0'h	TDM2 IF2_ADC1 Data Selection 000'b: Stereo1_ADC_Mixer_L/R 001'b: OutBound0/1 010'b: OutBound0/1_Mini 011'b: VAD_ADC 100'b: IF1_DAC_0/1 101'b: IF3_DAC_L/R 110'b: IF4_DAC_L/R 111'b: IF5_DAC_L/R
Reserved	7:5	R	0'h	Reserved

Sel_i2s_rx_i2s2	4:0	R/W	0'h	TDM2 ADC Data Control 00'h: 1/2/3/4 01'h: 1/2/4/3 02'h: 1/3/2/4 03'h: 1/3/4/2 04'h: 1/4/3/2 05'h: 1/4/2/3 06'h: 2/1/3/4 07'h: 2/1/4/3 08'h: 2/3/1/4 09'h: 2/3/4/1 0A'h: 2/4/3/1 0B'h: 2/4/1/3 0C'h: 3/1/2/4 0D'h: 3/1/4/2 0E'h: 3/2/1/4 0F'h: 3/2/4/1 10'h: 3/4/2/1 11'h: 3/4/1/2 12'h: 4/1/2/3 13'h: 4/1/3/2 14'h: 4/2/1/3 15'h: 4/2/3/1 16'h: 4/3/2/1 17'h: 4/3/1/2 Others: Reserved

9.43. MX-003Bh: TDM2 Control 4

Default: 0000'h

Table 125. MX-003Bh: TDM2 Control 4

DSP Address: 0x1800_C076 **I2C Address: 0x003B**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s2_lrck_polarity	15	R/W	0'h	LRCK2 Polarity Inverter 0'b: Don't invert 1'b: Invert
Reserved	14:8	R	0'h	Reserved
mute_tdm2_outl_i2s2	7	R/W	0'h	adc1 left data mute/unmute ctrl 0'b : Un-Mute 1'b : Mute
mute_tdm2_outr_i2s2	6	R/W	0'h	adc1 right data mute/unmute ctrl 0'b : Un-Mute 1'b : Mute
mute_tdm4_outl_i2s2	5	R/W	0'h	adc2 left data mute/unmute ctrl 0'b : Un-Mute 1'b : Mute
mute_tdm4_outr_i2s2	4	R/W	0'h	adc2 right data mute/unmute ctrl 0'b : Un-Mute 1'b : Mute
mute_tdm6_outl_i2s2	3	R/W	0'h	adc3 left data mute/unmute ctrl 0'b : Un-Mute 1'b : Mute
mute_tdm6_outr_i2s2	2	R/W	0'h	adc3 right data mute/unmute ctrl 0'b : Un-Mute 1'b : Mute
mute_tdm8_outl_i2s2	1	R/W	0'h	adc4 left data mute/unmute ctrl 0'b : Un-Mute 1'b : Mute
mute_tdm8_outr_i2s2	0	R/W	0'h	adc4 right data mute/unmute ctrl 0'b : Un-Mute 1'b : Mute

9.44. MX-003Ch: TDM2 Control 5

Default: 0123'h

Table 126. MX-003Ch: TDM2 Control 5

DSP Address: 0x1800_C078 I2C Address: 0x003C				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
sel_i2s2_tx_l_ch2	14:12	R/W	0'h	IF2_DAC_0 Data Selection 3'b000: Slot0 3'b001: Slot1 3'b010: Slot2 3'b011: Slot3 3'b100: Slot4 3'b101: Slot5 3'b110: Slot6 3'b111: Slot7
Reserved	11	R	0'h	Reserved
sel_i2s2_tx_r_ch2	10:8	R/W	1'h	IF2_DAC_1 Data Selection 3'b000: Slot0 3'b001: Slot1 3'b010: Slot2 3'b011: Slot3 3'b100: Slot4 3'b101: Slot5 3'b110: Slot6 3'b111: Slot7
Reserved	7	R	0'h	Reserved
sel_i2s2_tx_l_ch4	6:4	R/W	2'h	IF2_DAC_2 Data Selection 3'b000: Slot0 3'b001: Slot1 3'b010: Slot2 3'b011: Slot3 3'b100: Slot4 3'b101: Slot5 3'b110: Slot6 3'b111: Slot7
Reserved	3	R	0'h	Reserved
sel_i2s2_tx_r_ch4	2:0	R/W	3'h	IF2_DAC_3 Data Selection 3'b000: Slot0 3'b001: Slot1 3'b010: Slot2 3'b011: Slot3 3'b100: Slot4 3'b101: Slot5 3'b110: Slot6 3'b111: Slot7

9.45. MX-003Dh: TDM2 Control 6

Default: 4567'h

Table 127. MX-003Dh: TDM2 Control 6

DSP Address: 0x1800_C07A I2C Address: 0x003D				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
sel_i2s2_tx_l_ch6	14:12	R/W	4'h	IF2_DAC_4 Data Selection 3'b000: Slot0 3'b001: Slot1 3'b010: Slot2 3'b011: Slot3 3'b100: Slot4 3'b101: Slot5 3'b110: Slot6 3'b111: Slot7
Reserved	11	R	0'h	Reserved
sel_i2s2_tx_r_ch6	10:8	R/W	5'h	IF2_DAC_5 Data Selection 3'b000: Slot0 3'b001: Slot1 3'b010: Slot2 3'b011: Slot3 3'b100: Slot4 3'b101: Slot5 3'b110: Slot6 3'b111: Slot7
Reserved	7	R	0'h	Reserved
sel_i2s2_tx_l_ch8	6:4	R/W	6'h	IF2_DAC_6 Data Selection 3'b000: Slot0 3'b001: Slot1 3'b010: Slot2 3'b011: Slot3 3'b100: Slot4 3'b101: Slot5 3'b110: Slot6 3'b111: Slot7
Reserved	3	R	0'h	Reserved
sel_i2s2_tx_r_ch8	2:0	R/W	7'h	IF2_DAC_7 Data Selection 3'b000: Slot0 3'b001: Slot1 3'b010: Slot2 3'b011: Slot3 3'b100: Slot4 3'b101: Slot5 3'b110: Slot6 3'b111: Slot7

9.46. MX-003Eh: TDM2 Control 7

Default: 8003'h

Table 128. MX-003Eh: TDM2 Control 7

DSP Address: 0x1800_C07C I2C Address: 0x003E				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:7	R	100'h	Reserved
Tdm2_mode_sel_mst	6	R/W	0'h	TDM2 I2S / TDM Mode Control for Master mode 0'b: Normal I2S Mode 1'b: TDM Mode
Tdm2_lrck_sel_mst	5:4	R/W	0'h	TDM2 LRCK Divider Control for Master mode 00'b: ÷ 256 01'b: ÷ 128 10'b: ÷ 64 11'b: ÷ 32
Tdm2_slot_sel_mst	3:2	R/W	0'h	TDM2 Channel Number Select for Master mode 00'b: 2ch 01'b: 4ch 10'b: Reserved 11'b: 8ch
Tdm2_channel_length_mst	1:0	R/W	3'h	TDM2 Channel Length for Master mode 00'b: 16bit 01'b: 20bit 10'b: 24bit 11'b: 32bit

9.47. MX-0040h: Stereo1 DAC Mixer Control 1

Default: CAAA'h

Table 129. MX-0040h: Stereo1 DAC Mixer Control 1

DSP Address: 0x1800_C080 **I2C Address: 0x0040**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Mu_sidetone2dacl1	15	R/W	1'h	Mute Side Tone to DAC1L 0'b: UnMute 1'b: Mute
Mu_sidetone2dacr1	14	R/W	1'h	Mute Side Tone to DAC1R 0'b: UnMute 1'b: Mute
Sel_dacl1_mixer	13	R/W	0'h	Stereo_DAC_MIXL Source Selection 0'b: From DACL1 1'b: From Mixer
Sel_dacr1_mixer	12	R/W	0'h	Stereo_DAC_MIXR Source Selection 0'b: From DACR1 1'b: From Mixer
mu_stereo_dacl1_mixl	11	R/W	1'h	Mute Stereo DACL1 to Stereo_DAC_MIXL 0'b:UnMute 1'b:Mute
gain_dacl1_to_stereo_l	10	R/W	0'h	Gain Control for DACL1 to Stereo_DAC_MIXL 0'b: 0dB 1'b: -6dB
mu_stereo_dacr1_mixr	9	R/W	1'h	Mute Stereo DACR1 to Stereo_DAC_MIXR 0'b:UnMute 1'b:Mute
gain_dacr1_to_stereo_r	8	R/W	0'h	Gain Control for DACR1 to Stereo_DAC_MIXR 0'b: 0dB 1'b: -6dB
mu_stereo_dacr1_mixl	7	R/W	1'h	Mute Stereo DACR1 to Stereo_DAC_MIXL 0'b:UnMute 1'b:Mute
gain_dacr1_to_stereo_l	6	R/W	0'h	Gain Control for DACR1 to Stereo_DAC_MIXL 0'b: 0dB 1'b: -6dB
mu_stereo_dacl1_mixr	5	R/W	1'h	Mute Stereo DACL1 to Stereo_DAC_MIXR 0'b:UnMute 1'b:Mute
gain_dacl1_to_stereo_r	4	R/W	0'h	Gain Control for DACL1 to Stereo_DAC_MIXR 0'b: 0dB 1'b: -6dB
mu_stereo_dacl2_mixl	3	R/W	1'h	Mute Stereo DACL2 to Stereo_DAC_MIXL 0'b:UnMute 1'b:Mute

DSP Address: 0x1800_C080 I2C Address: 0x0040				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
gain_dacl2_to_stereo_l	2	R/W	0'h	Gain Control for DACL2 to Stereo_DAC_MIXL 0'b: 0dB 1'b: -6dB
mu_stereo_dacr2_mixr	1	R/W	1'h	Mute Stereo DACR2 to Stereo_DAC_MIXR 0'b:UnMute 1'b:Mute

9.48. MX-0041h: Stereo1 DAC Mixer Control 2

Default: AA00'h

Table 130. MX-0041h: Stereo1 DAC Mixer Control 2

DSP Address: 0x1800_C082 I2C Address: 0x0041				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_stereo_dacr2_mixl	15	R/W	1'h	Mute Stereo DACR2 to Stereo_DAC_MIXL 0'b:UnMute 1'b:Mute
gain_dacr2_to_stereo_l	14	R/W	0'h	Gain Control for DACR2 to Stereo_DAC_MIXL 0'b: 0dB 1'b: -6dB
mu_stereo_dacl2_mixr	13	R/W	1'h	Mute Stereo DACL2 to Stereo_DAC_MIXR 0'b:UnMute 1'b:Mute
gain_dacl2_to_stereo_r	12	R/W	0'h	Gain Control for DACL2 to Stereo_DAC_MIXR 0'b: 0dB 1'b: -6dB
mu_stereo_dacl3_mixl	11	R/W	1'h	Mute Stereo DACL3 to Stereo_DAC_MIXL 0'b:UnMute 1'b:Mute
gain_dacl3_to_stereo_l	10	R/W	0'h	Gain Control for DACL3 to Stereo_DAC_MIXL 0'b: 0dB 1'b: -6dB
mu_stereo_dacr3_mixr	9	R/W	1'h	Mute Stereo DACR3 to Stereo_DAC_MIXR 0'b:UnMute 1'b:Mute
gain_dacr3_to_stereo_r	8	R/W	0'h	Gain Control for DACR3 to Stereo_DAC_MIXR 0'b: 0dB 1'b: -6dB
Reserved	7:0	R	0'h	Reserved

9.49. MX-0042h: Mono DAC Mixer Control 1

Default: CAAA'h

Table 131. MX-0042h: Mono DAC Mixer Control 1

DSP Address: 0x1800_C084 I2C Address: 0x0042				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Mu_sidetone2dacl2	15	R/W	1'h	Mute Side Tone to DAC2L 0'b: UnMute 1'b: Mute
Mu_sidetone2dacr2	14	R/W	1'h	Mute Side Tone to DAC2R 0'b: UnMute 1'b: Mute
Reserved	13:12	R	0'h	reserved
mu_mono_dacl2_mixl	11	R/W	1'h	Mute DACL2 to Mono_DAC_MIXL 0'b:UnMute 1'b:Mute
gain_dacl2_to_mono_l	10	R/W	0'h	Gain Control for DACL2 to Mono_DAC_MIXL 0'b: 0dB 1'b: -6dB
mu_mono_dacr2_mixr	9	R/W	1'h	Mute DACR2 to Mono_DAC_MIXR 0'b:UnMute 1'b:Mute
gain_dacr2_to_mono_r	8	R/W	0'h	Gain Control for DACR2 to Mono_DAC_MIXR 0'b: 0dB 1'b: -6dB
mu_mono_dacl1_mixl	7	R/W	1'h	Mute DACL1 to Mono_DAC_MIXL 0'b:UnMute 1'b:Mute
gain_dacl1_to_mono_l	6	R/W	0'h	Gain Control for DACL1 to Mono_DAC_MIXL 0'b: 0dB 1'b: -6dB
mu_mono_dacr1_mixr	5	R/W	1'h	Mute DACR1 to Mono_DAC_MIXR 0'b:UnMute 1'b:Mute
gain_dacr1_to_mono_r	4	R/W	0'h	Gain Control for DACR1 to Mono_DAC_MIXR 0'b: 0dB 1'b: -6dB
mu_mono_dacr2_mixl	3	R/W	1'h	Mute DACR2 to Mono_DAC_MIXL 0'b:UnMute 1'b:Mute
gain_dacr2_to_mono_l	2	R/W	0'h	Gain Control for DACR2 to Mono_DAC_MIXL 0'b: 0dB 1'b: -6dB
mu_mono_dacl2_mixr	1	R/W	1'h	Mute DACL2 to Mono_DAC_MIXR 0'b:UnMute 1'b:Mute
gain_dacl2_to_mono_r	0	R/W	0'h	Gain Control for DACL2 to Mono_DAC_MIXR 0'b: 0dB 1'b: -6dB

9.50. MX-0043h: Mono DAC Mixer Control 2

Default: AA00'h

Table 132. MX-0043h: Mono DAC Mixer Control 2

DSP Address: 0x1800_C086 **I2C Address: 0x0043**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_mono_dacl3_mixl	15	R/W	1'h	Mute DACL3 to Mono_DAC_MIXL 0'b:UnMute 1'b:Mute
gain_dacl3_to_mono_l	14	R/W	0'h	Gain Control for DACL3 to Mono_DAC_MIXL 0'b: 0dB 1'b: -6dB
mu_mono_dacr3_mixr	13	R/W	1'h	Mute DACR3 to Mono_DAC_MIXR 0'b:UnMute 1'b:Mute
gain_dacr3_to_mono_r	12	R/W	0'h	Gain Control for DACR3 to Mono_DAC_MIXR 0'b: 0dB 1'b: -6dB
mu_mono_dacr3_mixl	11	R/W	1'h	Mute DACR3 to Mono_DAC_MIXL 0'b:UnMute 1'b:Mute
gain_dacr3_to_mono_l	10	R/W	0'h	Gain Control for DACR3 to Mono_DAC_MIXL 0'b: 0dB 1'b: -6dB
mu_mono_dacl3_mixr	9	R/W	1'h	Mute DACL3 to Mono_DAC_MIXR 0'b:UnMute 1'b:Mute
gain_dacl3_to_mono_r	8	R/W	0'h	Gain Control for DACL3 to Mono_DAC_MIXR 0'b: 0dB 1'b: -6dB
reserved	7:0	R	0'h	Reserved

9.51. MX-0044h: DD DAC Mixer Control 1

Default: AAAA'h

Table 133. MX-0044h: DD DAC Mixer Control 1

DSP Address: 0x1800_C088 I2C Address: 0x0044				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_stereomixl_to_ddmixl	15	R/W	1'h	Mute Stereo_DAC_Mixer_L to DD_MIXL 0'b:UnMute 1'b:Mute
gain_stereomixl_to_ddmixl	14	R/W	0'h	Gain Control for Stereo_DAC_Mixer_L to DD_MIXL 0'b: 0dB 1'b: -6dB
mu_stereomixr_to_ddmixr	13	R/W	1'h	Mute Stereo_DAC_Mixer_R to DD_MIXR 0'b:UnMute 1'b:Mute
gain_stereomixr_to_ddmixr	12	R/W	0'h	Gain Control for Stereo_DAC_Mixer_R to DD_MIXR 0'b: 0dB 1'b: -6dB
mu_monomixl_to_ddmixl	11	R/W	1'h	Mute Mono_DAC_Mixer_L to DD_MIXL 0'b:UnMute 1'b:Mute
gain_monomixl_to_ddmixl	10	R/W	0'h	Gain Control for Mono_DAC_Mixer_L to DD_MIXL 0'b: 0dB 1'b: -6dB
mu_monomixr_to_ddmixr	9	R/W	1'h	Mute Mono_DAC_Mixer_R to DD_MIXR 0'b:UnMute 1'b:Mute
gain_monomixr_to_ddmixr	8	R/W	0'h	Gain Control for Mono_DAC_Mixer_R to DD_MIXR 0'b: 0dB 1'b: -6dB
mu_dacl3_to_ddmixl	7	R/W	1'h	Mute DACL3 to DD_MIXL 0'b:UnMute 1'b:Mute
gain_dacl3_to_ddmixl	6	R/W	0'h	Gain Control for DACL3 to DD_MIXL 0'b: 0dB 1'b: -6dB
mu_dacr3_to_ddmixr	5	R/W	1'h	Mute DACR3 to DD_MIXR 0'b:UnMute 1'b:Mute
gain_dacr3_to_ddmixr	4	R/W	0'h	Gain Control for DACR3 to DD_MIXR 0'b: 0dB 1'b: -6dB
mu_dacr3_to_ddmixl	3	R/W	1'h	Mute DACR3 to DD_MIXL 0'b:UnMute 1'b:Mute
gain_dacr3_to_ddmixl	2	R/W	0'h	Gain Control for DACR3 to DD_MIXL 0'b: 0dB 1'b: -6dB
mu_dacl3_to_ddmixr	1	R/W	1'h	Mute DACL3 to DD_MIXR 0'b:UnMute 1'b:Mute
gain_dacl3_to_ddmixr	0	R/W	0'h	Gain Control for DACL3 to DD_MIXR 0'b: 0dB 1'b: -6dB

9.52. MX-0045h: DD DAC Mixer Control 2

Default: AA00'h

Table 134. MX-0045h: DD DAC Mixer Control 2

DSP Address: 0x1800_C08A I2C Address: 0x0045				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_dacl1_to_ddmixl	15	R/W	1'h	Mute DACL1 to DD_MIXL 0'b:UnMute 1'b:Mute
gain_dacl1_to_ddmixl	14	R/W	0'h	Gain Control for DACL1 to DD_MIXL 0'b: 0dB 1'b: -6dB
mu_dacl2_to_ddmixl	13	R/W	1'h	Mute DACL2 to DD_MIXL 0'b:UnMute 1'b:Mute
gain_dacl2_to_ddmixl	12	R/W	0'h	Gain Control for DACL2 to DD_MIXL 0'b: 0dB 1'b: -6dB
mu_dacr1_to_ddmixr	11	R/W	1'h	Mute DACR1 to DD_MIXR 0'b:UnMute 1'b:Mute
gain_dacr1_to_ddmixr	10	R/W	0'h	Gain Control for DACR1 to DD_MIXR 0'b: 0dB 1'b: -6dB
mu_dacr2_to_ddmixr	9	R/W	1'h	Mute DACR2 to DD_MIXR 0'b:UnMute 1'b:Mute
gain_dacr2_to_ddmixr	8	R/W	0'h	Gain Control for DACR2 to DD_MIXR 0'b: 0dB 1'b: -6dB
reserved	7:0	R	0'h	Reserved

9.53. MX-0046h: Digital DAC1 Source Control

Default: B080'h

Table 135. MX-0046h: Digital DAC1 Source Control

DSP Address: 0x1800_C08C I2C Address: 0x0046				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_adda_mixer1_l	15	R/W	1'h	Mute ADC Filter to DAC1 Filter Left Channel 0'b:UnMute 1'b:Mute
mu_dac1_l	14	R	0'h	Mute IF1 DAC Left Channel 0'b:UnMute 1'b:Mute
dmix_out_sel	13:12	R/W	3'h	Stereo1 DAC Post MUX Selection 00'b: POST_VOL 01'b: EQ 10'b: DRC 11'b: MIX_OUT
dsp_post_data_sel	11	R/W	0'h	Stereo1 DAC Post Volume Source Selection 0'b: From DRC 1'b: From EQ
sel_dac1	10:8	R/W	0'h	DACL Source Selection 1 000'b: IF1_DAC_0/1 001'b: IF2_DAC_0/1 010'b: IF3_DAC_L/R 011'b: IF4_DAC_L/R 100'b: IF5_DAC_L/R 101'b: SLB_DAC_0/1 110'b: OutBound0/1 Others: Reserved
mu_adda_mixer1_r	7	R/W	1'h	Mute ADC Filter to DAC1 Filter Right Channel 0'b:UnMute 1'b:Mute
mu_dac1_r	6	R	0'h	Mute IF1 DAC Right Channel 0'b:UnMute 1'b:Mute
reserved	5:2	R	0'h	Reserved
sel_adda1	1:0	R/W	0'h	DAC1L/R Source Selection 00'b: Stereo1_ADC_Mixer_L/R 01'b: Stereo2_ADC_Mixer_L/R 10'b: OutBound0/1 11'b: OutBound0/1_Mini

9.54. MX-0047h: Digital DAC2 Source Control

Default: 0000'h

Table 136. MX-0047h: Digital DAC2 Source Control

DSP Address: 0x1800_C08E **I2C Address: 0x0047**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:14	R	0'h	Reserved
mu_dac2_l	13	R	0'h	Digital Mute DAC2 Left Volume 0: Un-Mute 1: Mute (-∞ dB)
mu_dac2_r	12	R	0'h	Digital Mute DAC2 Right Volume 0: Un-Mute 1: Mute (-∞ dB)
reserved	11:8	R	0'h	Reserved
Sel_dacl2	7:4	R/W	0'h	Select Source Data to DACL2 0000'b: IF1_DAC_2 0001'b: IF2_DAC_2 0010'b: IF3_DAC_L 0011'b: IF4_DAC_L 0100'b: IF5_DAC_L 0101'b: SLB_DAC_2 0110'b: OutBound2 0111'b: OutBound4 1000'b: VAD_ADC 1001'b: Mono_ADC_Mixer_L Others: Reserved
Sel_dacr2	3:0	R/W	0'h	Select Source Data to DACR2 0000'b: IF1_DAC_3 0001'b: IF2_DAC_3 0010'b: IF3_DAC_R 0011'b: IF4_DAC_R 0100'b: IF5_DAC_R 0101'b: SLB_DAC_3 0110'b: OutBound3 0111'b: OutBound5 1000'b: Haptic_Gen 1001'b: Mono_ADC_Mixer_R Others: Reserved

9.55. MX-0048h: Digital DAC3 Source Control

Default: 0000'h

Table 137. MX-0048h: Digital DAC3 Source Control

DSP Address: 0x1800_C090 **I2C Address: 0x0048**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:10	R	0'h	Reserved
mu_dac3_l	9	R/W	0'h	Digital Mute DAC3 Left Volume 0: Un-Mute 1: Mute (-∞ dB)
mu_dac3_r	8	R/W	0'h	Digital Mute DAC3 Right Volume 0: Un-Mute 1: Mute (-∞ dB)
Sel_dacl3	7:4	R/W	0'h	Select Source Data to DACL3 0000'b: IF1_DAC_4 0001'b: IF2_DAC_4 0010'b: IF3_DAC_L 0011'b: IF4_DAC_L 0100'b: IF5_DAC_L 0101'b: IF1_DAC_6 0110'b: IF2_DAC_6 0111'b: SLB_DAC_4 1000'b: SLB_DAC_6 1001'b: OutBound2 1010'b: OutBound4 1011'b: Stereo3_ADC_Mixer_L Others: Reserved
Sel_dacr3	3:0	R/W	0'h	Select Source Data to DACR3 0000'b: IF1_DAC_5 0001'b: IF2_DAC_5 0010'b: IF3_DAC_R 0011'b: IF4_DAC_R 0100'b: IF5_DAC_R 0101'b: IF1_DAC_7 0110'b: IF2_DAC_7 0111'b: SLB_DAC_5 1000'b: SLB_DAC_7 1001'b: OutBound3 1010'b: OutBound5 1011'b: Stereo3_ADC_Mixer_R Others: Reserved

9.56. MX-0049h: Analog DAC Source Control

Default: 0000'h

Table 138. MX-0049h: Analog DAC Source Control

DSP Address: 0x1800_C092 **I2C Address: 0x0049**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_dac12_source	15:14	R/W	0'h	Analog DAC1/2 Source Selection 00'b: Stereo_DAC_MIXL/R 01'b: Mono_DAC_MIXL/R 10'b: DD_MIXL/R 11'b: Reserved
Sel_dac3_source	13:12	R/W	0'h	Analog DAC3 Source Selection 00'b: Stereo_DAC_MIXL 01'b: Mono_DAC_MIXL 10'b: DD_MIXL 11'b: Reserved
Sel_dac4_source	11:10	R/W	0'h	Analog DAC4 Source Selection 00'b: Stereo_DAC_MIXR 01'b: Mono_DAC_MIXR 10'b: DD_MIXR 11'b: Reserved
Sel_dac5_source	9:8	R/W	0'h	Analog DAC5 Source Selection 00'b: Stereo_DAC_MIXL 01'b: Mono_DAC_MIXL 10'b: Mono_DAC_MIXR 11'b: Reserved
Reserved	7:0	R	0'h	Reserved

9.57. MX-004Ah: Stereo1 ADC Mixer Control

Default: C0C0'h

Table 139. MX-004Ah: Stereo1 ADC Mixer Control

DSP Address: 0x1800_C094 **I2C Address: 0x004A**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_stereo1_adcl1	15	R/W	1'h	Mute Source 1 to Stereo1 ADC Left Channel 0'b:UnMute 1'b:Mute
mu_stereo1_adcl2	14	R/W	1'h	Mute Source 2 to Stereo1 ADC Left Channel 0'b:UnMute 1'b:Mute
sel_stereo1_adc1	13	R/W	0'h	Select DataSource1 to Stereo1 ADC 0'b: From ADC1/2 or ADC3/4 1'b: From DD_MIXL/R or Stereo_DAC_MIXL/R
sel_stereo1_adc2	12	R/W	0'h	Select DataSource2 to Stereo1 ADC 0'b: From DMIC1_L/R or DMIC2_L/R or DMIC3_L/R or DMIC4_L/R 1'b: From DD_MIXL/R or Stereo_DAC_MIXL/R or Mono_DAC_MIXL/R
Sel_stereo1_ana_adc	11:10	R/W	0'h	Select Data Source1_1 to Stereo1 ADC 00'b: ADC_1/ADC_2 01'b: ADC_3/ADC_4 10'b: ADC_2/ADC_3 11'b: ADC_6/ADC_7
Sel_stereo1_dd1	9:8	R/W	0'h	Select Data Source1_2 to Stereo1 ADC 00'b: DD_MIXL/R 01'b: Stereo_DAC_MIXL/R 10'b: Reserved 11'b: Reserved
mu_stereo1_adcr1	7	R/W	1'h	Mute Source 1 to Stereo1 ADC Right Channel 0'b:UnMute 1'b:Mute
mu_stereo1_adcr2	6	R/W	1'h	Mute Source 2 to Stereo1 ADC Right Channel 0'b:UnMute 1'b:Mute
Sel_stereo1_dmic	5:4	R/W	0'h	Select Data Source2_1 to Stereo1 ADC 00'b: DMIC1_L/R 01'b: DMIC2_L/R 10'b: DMIC3_L/R 11'b: DMIC4_L/R
Sel_stereo1_dd2	3:2	R/W	0'h	Select Data Source2_2 to Stereo1 ADC 00'b: DD_MIXL/R 01'b: Stereo_DAC_MIXL/R 10'b: Mono_DAC_MIXL/R 11'b: reserved
reserved	1:0	R	0'h	Reserved

9.58. MX-004Bh: Mono ADC Mixer Control 1

Default: C0C0'h

Table 140. MX-004Bh: Mono ADC Mixer Control 1

DSP Address: 0x1800_C096 I2C Address: 0x004B				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_mono_adcl1	15	R/W	1'h	Mute Source 1 to Mono ADC Left channel 0'b:UnMute 1'b:Mute
mu_mono_adcl2	14	R/W	1'h	Mute Source 2 to Mono ADC Left channel 0'b:UnMute 1'b:Mute
sel_mono_adcl1	13	R/W	0'h	Select DataSourceL1 to Mono ADC 0'b: From ADC1 or ADC3 1'b: From DD_MIXL or Mono_DAC_MIXL
sel_mono_adcl2	12	R/W	0'h	Select DataSourceL2 to Mono ADC 0'b: From DMIC1_L or DMIC2_L or DMIC3_L or DMIC4_L 1'b: From DD_MIXL or Stereo_DAC_MIXL or Mono_DAC_MIXL
Reserved	11:8	R	0'h	Reserved
mu_mono_adcr1	7	R/W	1'h	Mute Source 1 to Mono ADC Right channel 0'b:UnMute 1'b:Mute
mu_mono_adcr2	6	R/W	1'h	Mute Source 2 to Mono ADC Right channel 0'b:UnMute 1'b:Mute
sel_mono_adcr1	5	R/W	0'h	Select DataSourceR1 to Mono ADC 0'b: From ADC2 or ADC4 1'b: From DD_MIXR or Mono_DAC_MIXR
sel_mono_adcr2	4	R/W	0'h	Select DataSourceR2 to Mono ADC 0'b: From DMIC1_R or DMIC2_R or DMIC3_R or DMIC4_R 1'b: From DD_MIXR or Stereo_DAC_MIXR or Mono_DAC_MIXR
Reserved	3:0	R	0'h	Reserved

9.59. MX-004Ch: Mono ADC Mixer Control 2

Default: 0000'h

Table 141. MX-004Ch: Mono ADC Mixer Control 2

DSP Address: 0x1800_C098 I2C Address: 0x004C				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_monol_ana_adc	15:14	R/W	0'h	Select Data SourceL1_1 to Mono ADC_L 00'b: ADC1 01'b: ADC3 10'b: Reserved 11'b: Reserved
Sel_monol_dd1	13:12	R/W	0'h	Select Data SourceL1_2 to Mono ADC_L 00'b: DD_MIXL 01'b: Mono_DAC_MIXL 10'b: Reserved 11'b: Reserved
Sel_monol_dmic	11:10	R/W	0'h	Select Data SourceL2_1 to Mono ADC_L 00'b: DMIC1_L 01'b: DMIC2_L 10'b: DMIC3_L 11'b: DMIC4_L
Sel_monol_dd2	9:8	R/W	0'h	Select Data SourceL2_2 to Mono ADC_L 00'b: DD_MIXL 01'b: Stereo_DAC_MIXL 10'b: Mono_DAC_MIXL 11'b: reserved
Sel_monor_ana_adc	7:6	R/W	0'h	Select Data SourceR1_1 to Mono ADC_R 00'b: ADC2 01'b: ADC4 10'b: Reserved 11'b: Reserved
Sel_monor_dd1	5:4	R/W	0'h	Select Data SourceR1_2 to Mono ADC_R 00'b: DD_MIXR 01'b: Mono_DAC_MIXR 10'b: Reserved 11'b: Reserved
Sel_monor_dmic	3:2	R/W	0'h	Select Data SourceR2_1 to Mono ADC_R 00'b: DMIC1_R 01'b: DMIC2_R 10'b: DMIC3_R 11'b: DMIC4_L
Sel_monor_dd2	1:0	R/W	0'h	Select Data SourceR2_2 to Mono ADC_R 00'b: DD_MIXR 01'b: Stereo_DAC_MIXR 10'b: Mono_DAC_MIXR 11'b: reserved

9.60. MX-004Dh: Stereo2 ADC Mixer Control

Default: C0C0'h

Table 142. MX-004Dh: Stereo2 ADC Mixer Control

DSP Address: 0x1800_C09A **I2C Address: 0x004D**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_stereo2_adcl1	15	R/W	1'h	Mute Source1 to Stereo2 ADC Left Channel 0'b:UnMute 1'b:Mute
mu_stereo2_adcl2	14	R/W	1'h	Mute Source2 to Stereo2 ADC Left Channel 0'b:UnMute 1'b:Mute
sel_stereo2_adc1	13	R/W	0'h	Select DataSource1 to Stereo2 ADC 0'b: From ADC1/2 or ADC3/4 1'b: From DD_MIXL/R or Stereo_DAC_MIXL/R
sel_stereo2_adc2	12	R/W	0'h	Select DataSource2 to Stereo2 ADC 0'b: From DMIC1_L/R or DMIC2_L/R or DMIC3_L/R or DMIC4_L/R 1'b: From DD_MIXL/R or Stereo_DAC_MIXL/R or Mono_DAC_MIXL/R
sel_stereo2_ana_adc	11:10	R/W	0'h	Select Data Source1_1 to Stereo2 ADC 00'b: ADC_1/ADC_2 01'b: ADC_3/ADC_4 10'b: ADC_2/ADC_3 11'b: ADC_6/ADC_7
sel_stereo2_dd1	9:8	R/W	0'h	Select Data Source1_2 to Stereo2 ADC 00'b: DD_MIXL/R 01'b: Stereo_DAC_MIXL/R 10'b: Reserved 11'b: Reserved
mu_stereo2_adcr1	7	R/W	1'h	Mute Source1 to Stereo2 ADC Right Channel 0'b:UnMute 1'b:Mute
mu_stereo2_adcr2	6	R/W	1'h	Mute Source2 to Stereo2 ADC Right Channel 0'b:UnMute 1'b:Mute
sel_stereo2_dmic	5:4	R/W	0'h	Select Data Source2_1 to Stereo2 ADC 00'b: DMIC1_L/R 01'b: DMIC2_L/R 10'b: DMIC3_L/R 11'b: DMIC4_L/R
sel_stereo2_dd2	3:2	R/W	0'h	Select Data Source2_2 to Stereo2 ADC 00'b: DD_MIXL/R 01'b: Stereo_DAC_MIXL/R 10'b: Mono_DAC_MIXL/R 11'b: reserved
reserved	1	R	0'h	reserved
sel_stereo2_lr_mix	0	R/W	0'h	Mixing Control for Stereo2 ADC Left channel 0'b: L 1'b: L+R

9.61. MX-004Eh: Stereo3 ADC Mixer Control

Default: C0C0’h

Table 143. MX-004Eh: Stereo3 ADC Mixer Control

DSP Address: 0x1800_C09C **I2C Address: 0x004E**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_stereo3_adcl1	15	R/W	1’h	Mute Source1 to Stereo3 ADC Left Channel 0’b:UnMute 1’b:Mute
mu_stereo3_adcl2	14	R/W	1’h	Mute Source2 to Stereo3 ADC Left Channel 0’b:UnMute 1’b:Mute
sel_stereo3_adc1	13	R/W	0’h	Select DataSource1 to Stereo3 ADC 0’b: From ADC1/2 or ADC3/4 1’b: From DD_MIXL/R or Stereo_DAC_MIXL/R
sel_stereo3_adc2	12	R/W	0’h	Select DataSource2 to Stereo3 ADC 0’b: From DMIC1_L/R or DMIC2_L/R or DMIC3_L/R or DMIC4_L/R 1’b: From DD_MIXL/R or Stereo_DAC_MIXL/R or Mono_DAC_MIXL/R
sel_stereo3_ana_adc	11:10	R/W	0’h	Select Data Source1_1 to Stereo3 ADC 00’b: ADC_1/2 01’b: ADC3/4 10’b: Reserved 11’b: Reserved
sel_stereo3_dd1	9:8	R/W	0’h	Select Data Source1_2 to Stereo3 ADC 00’b: DD_MIXL/R 01’b: Stereo_DAC_MIXL/R 10’b: Reserved 11’b: Reserved
mu_stereo3_adcr1	7	R/W	1’h	Mute Source1 to Stereo3 ADC Right Channel 0’b:UnMute 1’b:Mute
mu_stereo3_adcr2	6	R/W	1’h	Mute Source2 to Stereo3 ADC Right Channel 0’b:UnMute 1’b:Mute
sel_stereo3_dmic	5:4	R/W	0’h	Select Data Source2_1 to Stereo3 ADC 00’b: DMIC1_L/R 01’b: DMIC2_L/R 10’b: DMIC3_L/R 11’b: DMIC4_L/R
sel_stereo3_dd2	3:2	R/W	0’h	Select Data Source2_2 to Stereo3 ADC 00’b: DD_MIXL/R 01’b: Stereo_DAC_MIXL/R 10’b: Mono_DAC_MIXL/R 11’b: reserved
reserved	1:0	R	0’h	Reserved

9.62. MX-0050h: Digital Microphone Control 1

Default: 0550'h

Table 144. MX-0050h: Digital Microphone Control 1

DSP Address: 0x1800_C0A0 I2C Address: 0x0050				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_dmic1	15	R/W	0'h	Enable DMIC1 Interface 0'b: Disable 1'b: Enable (Output DMIC1 clock)
en_dmic2	14	R/W	0'h	Enable DMIC2 Interface 0'b: Disable 1'b: Enable (Output DMIC2 clock)
en_dmic3	13	R/W	0'h	Enable DMIC3 Interface 0'b: Disable 1'b: Enable (Output DMIC3 clock)
en_dmic4	12	R/W	0'h	Enable DMIC4 Interface 0'b: Disable 1'b: Enable (Output DMIC3 clock)
sel_dmic_l_edge_stereo1	11	R/W	0'h	DMIC ADC Left Channel to Stereo1 Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_r_edge_stere1	10	R/W	1'h	DMIC ADC Right Channel to Stereo1 Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_l_edge_stereo2	9	R/W	0'h	DMIC ADC Left Channel to Stereo2 Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_r_edge_stereo2	8	R/W	1'h	DMIC ADC Right Channel to Stereo2 Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_l_edge_stereo3	7	R/W	0'h	DMIC ADC Left Channel to Stereo3 Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_r_edge_stereo3	6	R/W	1'h	DMIC ADC Right Channel to Stereo3 Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_l_edge_mono	5	R/W	0'h	DMIC ADC Left Channel to Mono Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge

DSP Address: 0x1800_C0A0 I2C Address: 0x0050				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_dmic_r_edge_mono	4	R/W	1'h	DMIC ADC Right Channel to Mono Filter Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
Reserved	3	R	0'h	Reserved
sel_dmic_clk	2:0	R/W	0'h	DMIC clock type Control 000'b: 256*fs/2 001'b: 256*fs/3 010'b: 256*fs/4 011'b: 256*fs/6 100'b: 256*fs/8 101'b: 256*fs/12

9.63. MX-0051h: Digital Microphone Control 2

Default: 0055'h

Table 145. MX-0051h: Digital Microphone Control 2

DSP Address: 0x1800_C0A2 **I2C Address: 0x0051**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:12	R	0'h	Reserved
dmic4_data_pin_share	11	R/W	0'h	Select the Pin share of DMIC4_DATA 0'b: GPIO6 1'b: IN3P
dmic3_data_pin_share	10	R/W	0'h	Select the Pin share of DMIC3_DATA 0'b: GPIO24 1'b: IN3N
dmic2_data_pin_share	9	R/W	0'h	Select the Pin share of DMIC2_DATA 0'b: GPIO23 1'b: IN4P
dmic1_data_pin_share	8	R/W	0'h	Select the Pin share of DMIC1_DATA 0'b: GPIO22 1'b: IN4N
sel_dmic4_lpf_l_edge	7	R/W	0'h	DMIC4 ADC Left Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic4_lpf_r_edge	6	R/W	1'h	DMIC4 ADC Right Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic3_lpf_l_edge	5	R/W	0'h	DMIC3 ADC Left Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic3_lpf_r_edge	4	R/W	1'h	DMIC3 ADC Right Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic2_lpf_l_edge	3	R/W	0'h	DMIC2 ADC Left Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic2_lpf_r_edge	2	R/W	1'h	DMIC2 ADC Right Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic1_lpf_l_edge	1	R/W	0'h	DMIC1 ADC Left Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic1_lpf_r_edge	0	R/W	1'h	DMIC1 ADC Right Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge

9.64. MX-0060h: Power Management 1

Default: 0000’h

Table 146. MX-0060h: Power Management 1

DSP Address: 0x1800_C0C0 I2C Address: 0x0060				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
pow_vref1_vad	15	R/W	0’h	VREF1(0.45V) Output Voltage Fast Mode Control 0'b:Fast Mode 1'b:Slow Mode (Normal Mode)
en_fastb1_vad	14	R/W	0’h	VREF1(0.45V) Output Voltage Fast Mode Control 0’b: Fast Vref 1’b: Slow Vref for good performance
pow_vref2_vad	13	R/W	0’h	Enable Vref voltage for all circuit buffer (VREF2 and VREF4 need to avoid turn of Fast Mode at the same time) 0’b: Power Down 1’b: Power On Vref
en_fastb2_vad	12	R/W	0’h	VREF2(0.9V) Output Voltage Fast Mode Control 0'b:Fast Mode 1'b:Slow Mode (Normal Mode)
Reserved	11:8	R	0’h	Reserved
Pow_inbuf	7	R/W	0’h	Power down control of INPUT_BUF (For ADC5 VAD) 0’b: Power down 1’b: Power up
pow_adc1	6	R/W	0’h	Analog ADC1 Power Down Control 0’b: Power Down 1’b: Power On
pow_adc2	5	R/W	0’h	Analog ADC2 Power Down Control 0’b: Power Down 1’b: Power On
pow_adc3	4	R/W	0’h	Analog ADC3 Power Down Control 0’b: Power Down 1’b: Power On
pow_adc4	3	R/W	0’h	Analog ADC4 Power Down Control 0’b: Power Down 1’b: Power On
Pow_adc5	2	R/W	0’h	Analog ADC5 Power Down Control (For VAD) 0’b: Power Down 1’b: Power On
Reserved	1:0	R	0’h	Reserved

9.65. MX-0061h: Power Management 2

Default: 0000'h

Table 147. MX-0061h: Power Management 2

DSP Address: 0x1800_C0C2 I2C Address: 0x0061				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_i2s1	15	R/W	0'h	I2S1 Digital interface enable 0'b: Power Down 1'b: Power On
en_i2s2	14	R/W	0'h	I2S2 Digital interface enable 0'b: Power Down 1'b: Power On
en_i2s3	13	R/W	0'h	I2S3 Digital interface enable 0'b: Power Down 1'b: Power On
en_i2s4	12	R/W	0'h	I2S4 Digital interface enable 0'b: Power Down 1'b: Power On
en_i2s5	11	R/W	0'h	I2S5 Digital interface enable 0'b: Power Down 1'b: Power On
Reserved	10	R	0'h	Reserved
pow_dac1	9	R/W	0'h	Analog DAC1 Power Down Control 0'b: Power Down 1'b: Power On
pow_dac2	8	R/W	0'h	Analog DAC2 Power Down Control 0'b: Power Down 1'b: Power On
pow_dac3	7	R/W	0'h	Analog DAC3 Power Down Control 0'b: Power Down 1'b: Power On
pow_dac4	6	R/W	0'h	Analog DAC4 Power Down Control 0'b: Power Down 1'b: Power On
pow_dac5	5	R/W	0'h	Analog DAC5 Power Down Control 0'b: Power Down 1'b: Power On
Reserved	4:0	R	0'h	Reserved

9.66. MX-0062h: Power Management 3

Default: 0000’h

Table 148. MX-0062h: Power Management 3

DSP Address: 0x1800_C0C4 I2C Address: 0x0062				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
pow_adc_stereo1_filter	15	R/W	0’h	Power on ADC stereo1 filter 0’b: Power Down 1’b: Power On
pow_adc_stereo2_filter	14	R/W	0’h	Power on ADC stereo2 filter 0’b: Power Down 1’b: Power On
pow_adc_stereo3_filter	13	R/W	0’h	Power on ADC stereo3 filter 0’b: Power Down 1’b: Power On
pow_adc_monol_filter	12	R/W	0’h	Power on ADC Mono Left Filter 0’b: Power Down 1’b: Power On
pow_adc_monor_filter	11	R/W	0’h	Power on ADC Mono Right Filter 0’b: Power Down 1’b: Power On
pow_dac_stereo1_filter	10	R/W	0’h	Power on DAC stereo1 filter 0’b: Power Down 1’b: Power On
pow_dac_mono2l_filter	9	R/W	0’h	Power on DAC mono 2 left filter 0’b: Power Down 1’b: Power On
pow_dac_mono2r_filter	8	R/W	0’h	Power on DAC mono 2 right filter 0’b: Power Down 1’b: Power On
pow_dac_mono3l_filter	7	R/W	0’h	Power on DAC mono 3 left filter 0’b: Power Down 1’b: Power On
pow_dac_mono3r_filter	6	R/W	0’h	Power on DAC mono 3 right filter 0’b: Power Down 1’b: Power On
Reserved	5:2	R	0’h	Reserved
Pow_pdm1	1	R/W	0’h	Power on PDM1 Interface 0’b: Power down 1’b: Power on
Pow_pdm2	0	R/W	0’h	Power on PDM2 Interface 0’b: Power down 1’b: Power on

9.67. MX-0063h: Power Management 4

Default: 0040'h

Table 149. MX-0063h: Power Management 4

DSP Address: 0x1800_C0C6 I2C Address: 0x0063				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
pow_vref1	15	R/W	0'h	VREF1(0.45V) Output Voltage Fast Mode Control 0'b:Fast Mode 1'b:Slow Mode (Normal Mode)
en_fastb1	14	R/W	0'h	VREF1(0.45V) Output Voltage Fast Mode Control 0'b: Fast Vref 1'b: Slow Vref for good performance
pow_main_bias	13	R/W	0'h	MBIAS On/Off Control 0'b: Power Down 1'b: Power On Main bias of analog circuit
pow_bg_mbias	12	R/W	0'h	MBIAS Bandgap power 0'b: Power Down 1'b: Power On
pow_lout1	11	R/W	0'h	LOUT1 Power Control 0'b: Power Down 1'b: Power On
pow_lout2	10	R/W	0'h	LOUT2 Power Control 0'b: Power Down 1'b: Power On
pow_vref2	9	R/W	0'h	Enable Vref voltage for all circuit buffer (VREF2 and VREF4 need to avoid turn of Fast Mode at the same time) 0'b: Power Down 1'b: Power On Vref
en_fastb2	8	R/W	0'h	VREF2(0.9V) Output Voltage Fast Mode Control 0'b:Fast Mode 1'b:Slow Mode (Normal Mode)
Pow_vref4	7	R/W	0'h	VREF4 On/Off Control 0'b: Power Down 1'b: Power On Vref
En_fastb4	6	R/W	1'h	VREF4 Output Voltage Fast Mode Control (VREF2 and VREF4 need to avoid turn of Fast Mode at the same time) 0'b: Fast Mode 1'b: Slow Mode (Normal Mode)
Rstb_pll1	5	R/W	0'h	PLL1 Reset Control 0'b: Reset 1'b: Normal
Rstb_pll2	4	R/W	0'h	PLL2 Reset Control 0'b: Reset 1'b: Normal

DSP Address: 0x1800_C0C6 I2C Address: 0x0063				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
pow_pll1	3	R/W	0'h	PLL1 Power/Reset Control 0'b: Power Down and Reset 1'b: Power On PLL
pow_pll2	2	R/W	0'h	PLL2 Power/Reset Control 0'b: Power Down and Reset 1'b: Power On PLL
pow_clk25m	1	R/W	0'h	Digital 25MHz clock power 0'b : Power off 1'b : Power on
pow_clk1m	0	R/W	0'h	Digital 1MHz clock power 0'b : Power off 1'b : Power on

9.68. MX-0064h: Power Management 5

Default: 0000'h

Table 150. MX-0064h: Power Management 5

DSP Address: 0x1800_C0C8 I2C Address: 0x0064				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
pow_bst1	15	R/W	0'h	MIC Boost 1 Power Control 0'b: Power Down 1'b: Power On
pow_bst2	14	R/W	0'h	MIC Boost 2 Power Control 0'b: Power Down 1'b: Power On
pow_bst3	13	R/W	0'h	MIC Boost 3 Power Control 0'b: Power Down 1'b: Power On
pow_bst4	12	R/W	0'h	MIC Boost 4 Power Control 0'b: Power Down 1'b: Power On
Reserved	11:8	R	0'h	Reserved
Pow_vref3_micbias1	7	R/W	0'h	VREF3_MICBIAS On/Off Control 0'b: Power Down 1'b: Power On
En_fastb3	6	R/W	0'h	VREF3 Output Voltage (2.7V) Fast Mode Control 0'b: Fast Mode 1'b: Slow Mode (Normal Mode)
Reserved	5	R	0'h	Reserved
pow_micbias1	4	R/W	0'h	MICBIAS1 Power Control 0'b: Power Down 1'b: Power On microphone bias-1 pin voltage
Reserved	3:2	R	0'h	Reserved
Pow_mic_in_det	1	R/W	0'h	MIC detection power control 0'b: Power down 1'b: Power on
Pow_mono	0	R/W	0'h	Power Control for Mono Amp 0'b: Power down 1'b: Power on

9.69. MX-0065h: Power Management 6

Default: 0181'h

Table 151. MX-0065h: Power Management 6

DSP Address: 0x1800_C0CA I2C Address: 0x0065				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:9	R	0'h	Reserved
hifi3_bclk_enable	8	R/W	1'h	HIFI-3 DSP BCLK Gating Control 0'b: Gating BCLK 1'b: Enable BCLK
hifi3_clk_enable	7	R/W	1'h	HIFI-3 DSP Clock Gating Control 0'b: Gating clock 1'b: Enable clock
pow_dcvdd9_iso	6	R/W	0'h	SRAM, Mini I/DRAM and VAD SRAM Isolation Control 0'b: Isolation 1'b: Normal
pow_dcvdd3_iso	5	R/W	0'h	HIFI-3 DSP Isolation Control 0'b: Isolation 1'b: Normal
sram_reg_pow	4	R/W	0'h	SRAM Power Control 0'b: Power down 1'b: Power on
mini_dsp_reg_pow	3	R/W	0'h	Mini DSP Power Control 0'b: Power down 1'b: Power on
hifi3_dsp_reg_pow	2	R/W	0'h	HIFI-3 DSP Power Control 0'b: Power down 1'b: Power on
hifi3_reset	1	R/W	0'h	HIFI-3 DSP Reset Control 0'b: Normal 1'b: Reset
runstall_hifi3	0	R/W	1'h	HIFI-3 DSP CPU Control 0'b: Run 1'b: Stop

9.70. MX-0066h: Power Management 7

Default: 0000'h

Table 152. MX-0066h: Power Management 7

DSP Address: 0x1800_C0CC I2C Address: 0x0066				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
pow_ldo_dacref1	15	R/W	0'h	LDO_DACREF1 (LDO6_2) Power Control 0'b: Power off 1'b: Power on
pow_ldo_dacref2	14	R/W	0'h	LDO_DACREF2 (LDO6_3) Power Control 0'b: Power off 1'b: Power on
pow_ldo_addaref	13	R/W	0'h	LDO_ADDAREF (LDO6_1) Power Control 0'b: Power off 1'b: Power on
Pow_vref5_l	12	R/W	0'h	VREF5_L On/Off Control (For LDO_DACREF1) 0'b: Power off 1'b: Power on
En_fastb5_l	11	R/W	0'h	VREF5_L(1.6V) Output Voltage Fast Mode Control 0'b:Fast Mode 1'b:Slow Mode (Normal Mode)
Pow_bg_vref5_l	10	R/W	0'h	Bandgap_VREF5_L On/Off Control 0'b: Power off 1'b: Power on
Pow_vref5_r	9	R/W	0'h	VREF5_R On/Off Control (For LDO_DACREF2) 0'b: Power off 1'b: Power on
En_fastb5_r	8	R/W	0'h	VREF5_R(1.6V) Output Voltage Fast Mode Control 0'b:Fast Mode 1'b:Slow Mode (Normal Mode)
Pow_bg_vref5_r	7	R/W	0'h	Bandgap_VREF5_R On/Off Control 0'b: Power off 1'b: Power on
Reserved	6	R	0'h	Reserved
Pow_ldo4_2	5	R/W	0'h	LDO4_2 Power Control (For MICBIAS3) 0'b: Power off 1'b: Power on
Pow_ldo4_1	4	R/W	0'h	LDO4_1 Power Control (For MICBIAS2) 0'b: Power off 1'b: Power on
Pow_bg_ldo4	3	R/W	0'h	LDO4 Bandgap On/Off Control (If want to turn on LDO4_1/2, the pow_bg_ldo4 need be turn on) 0'b: Power off 1'b: Power on
Reserved	2	R	0'h	Reserved
Pow_ldo3_onoff	1	R/W	0'h	LDO_3 Power/I-Limit Control (For HIFI-3 DSP) 0'b: Power off 1'b: Power on
Bps_dldo1	0	R/W	0'h	LDO1 Bypass Control (For Codec Core & Mini DSP Core) 0'b: Pass LDO 1'b: Bypass LDO

9.71. MX-0067h: Power Management 8

Default: 0002'h

Table 153. MX-0067h: Power Management 8

DSP Address: 0x1800_C0CE I2C Address: 0x0067				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
Pow_ldo7_1	12	R/W	0'h	LDO_AVDD1 Power/I-Limit/BG Control 0'b: Power off 1'b: Power on
en_ldo_pll2	11	R/W	0'h	LDO_PLL Power Control (For PLL2) 0'b: Power off 1'b: Power on
en_ldo_pll1	10	R/W	0'h	LDO_PLL Power Control (For PLL1) 0'b: Power off 1'b: Power on
Pow_ldo_mono_2	9	R/W	0'h	LDO_HV2 Power Control 0'b: Power off 1'b: Power on
Pow_ldo_mono_1	8	R/W	0'h	LDO_HV1 Power Control 0'b: Power off 1'b: Power on
Reserved	7:4	R	0'h	Reserved
Pow_dldo9	3	R/W	0'h	LDO9 Power Control (For Mini DSP I/DRAM and SRAM) 0'b: Power off 1'b: Power on
Bps_dldo9	2	R/W	0'h	LDO9 Bypass Control (For Mini DSP I/DRAM and SRAM) 0'b: Pass LDO 1'b: Bypass LDO
Pow_dldo8	1	R/W	1'h	LDO8 Power Control (For LDO1 / LDO9, 1.8V to 1.2V) 0'b: Power off 1'b: Power on
Reserved	0	R	0'h	Reserved

9.72. MX-0068h: Power Management 9

Default: 3703'h

Table 154. MX-0068h: Power Management 9

DSP Address: 0x1800_C0D0 I2C Address: 0x0068				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
dvo9	14:12	R/W	3'h	LDO9 output voltage selection 000'b: 0.75V 001'b: 0.8V 010'b: 0.85V 011'b: 0.9V 100'b: 0.95V 101'b: 1.0V 110'b: 1.05V 111'b: 1.1V
dvo_ldo3	11:8	R/W	7'h	Select LDO3 Output (1.8V Input LDO) 0000'b: 0.85V 0001'b: 0.90V 0010'b: 0.95V 0011'b: 1.0V 0100'b: 1.05V 0101'b: 1.1V 0110'b: 1.15V 0111'b: 1.2V 1000'b: 1.25V 1001'b: 1.3V 1010'b: 1.35V Others: Reserved
reserved	7:3	R	0'h	Reserved
dvo1	2:0	R/W	3'h	LDO1 output voltage selection 000'b: 0.75V 001'b: 0.8V 010'b: 0.85V 011'b: 0.9V 100'b: 0.95V 101'b: 1V 110'b: 1.05V 111'b: 1.1V

9.73. MX-0069h: Power Management 10

Default: 0100'h

Table 155. MX-0069h: Power Management 10

DSP Address: 0x1800_C0D2 **I2C Address: 0x0069**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:14	R	0'h	Reserved
dvo_ldo7_1	13:12	R/W	0'h	AVDD18_1 Voltage Selection: 00: 1.82257V 01: 1.86V 10: 1.92V 11: 2.00477V
reserved	11:10	R	0'h	Reserved
dvo_dldo8	9:8	R/W	1'h	Selection of the LDO8 output, 00'b: 1.1V 01'b: 1.2V 10'b: 1.3V 11'b: 1.4V
reserved	7:6	R	0'h	Reserved
dvo_ldo4_1	5:4	R/W	0'h	LDO4_1 Output Voltage (MICBIAS2) 00'b: 1.8V 01'b: 1.9V 10'b: 2.0V 11'b: 2.7V
dvo_ldo4_2	3:2	R/W	0'h	LDO4_2 Output Voltage (MICBIAS3) 00'b: 1.8V 01'b: 1.9V 10'b: 2.0V 11'b: 2.7V
reserved	1:0	R	0'h	Reserved

9.74. MX-006Ah: Power Management 11

Default: 0000'h

Table 156. MX-006Ah: Power Management 11

DSP Address: 0x1800_C0D4 **I2C Address: 0x006A**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:12	R	0'h	Reserved
dvo_ldo_hv2	11:10	R/W	0'h	LDO_HV2 Output Voltage 00'b: 3.10V 01'b: 3.15V 10'b: 3.20V 11'b: 3.30V
dvo_ldo_hv1	9:8	R/W	0'h	LDO_HV1 Output Voltage 00'b: 3.10V 01'b: 3.15V 10'b: 3.20V 11'b: 3.30V
reserved	7:0	R	0'h	Reserved

9.75. MX-0070h: I2S1 Audio Serial Data Port Control

Default: 8000'h

Table 157. MX-0070h: I2S1 Audio Serial Data Port Control

DSP Address: 0x1800_C0E0 **I2C Address: 0x0070**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s1_ms	15	R/W	1'h	I2S1 Serial Data Port Mode Selection 0'b: Master 1'b: Slave
sel_adcdat1	14	R/W	0'h	I2S1 ADCDAT pin Type 0'b: Output 1'b: Input
reserved	13:10	R	0'h	Reserved
sel_adcdat1_sour	9	R/W	0'h	Select the ADCDAT1 source 0'b: I2S1 DACDAT1 1'b: I2S2 DACDAT2
inv_i2s1_bclk	8	R/W	0'h	I2S1 BCLK Polarity Control 0'b: Normal 1'b: Invert
reserved	7	R	0'h	Reserved
en_i2s1_mono	6	R/W	0'h	Enable I2S1 PCM 17FS Mono Mode 0'b: Disable 1'b: Enable
sel_i2s1_len	5:4	R/W	0'h	I2S1 Data Length Selection 00'b: 16 bits 01'b: 20 bits 10'b: 24 bits 11'b: 8 bits
reserved	3	R	0'h	Reserved
sel_i2s1_format	2:0	R/W	0'h	I2S1 PCM Data Format Selection 000'b: I^2S format 001'b: Left justified 010'b: PCM Mode A (LRCK One Plus at Master Mode) 011'b: PCM Mode B (LRCK One Plus at Master Mode) 100'b: Reserved 101'b: Reserved 110'b: PCM Mode A-N (LRCK One Plus at Master Mode) 111'b: PCM Mode B-N (LRCK One Plus at Master Mode)

9.76. MX-0071h: I2S2 Audio Serial Data Port Control

Default: 8000'h

Table 158. MX-0071h: I2S2 Audio Serial Data Port Control

DSP Address: 0x1800_C0E2 **I2C Address: 0x0071**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s2_ms	15	R/W	1'h	I2S2 Serial Data Port Mode Selection 0'b: Master 1'b: Slave
sel_adcdat2	14	R/W	0'h	I2S2 ADCDAT pin Type 0'b: Output 1'b: Input
reserved	13:9	R	0'h	Reserved
inv_i2s2_bclk	8	R/W	0'h	I2S2 BCLK Polarity Control 0'b: Normal 1'b: Invert
reserved	7	R	0'h	Reserved
en_i2s2_mono	6	R/W	0'h	Enable I2S2 PCM 17FS Mono Mode 0'b: Disable 1'b: Enable
sel_i2s2_len	5:4	R/W	0'h	I2S2 Data Length Selection 00'b: 16 bits 01'b: 20 bits 10'b: 24 bits 11'b: 8bits
reserved	3	R	0'h	Reserved
sel_i2s2_format	2:0	R/W	0'h	I2S2 PCM Data Format Selection 000'b: I^2S format 001'b: Left justified 010'b: PCM Mode A (LRCK One Plus at Master Mode) 011'b: PCM Mode B (LRCK One Plus at Master Mode) 100'b: Reserved 101'b: Reserved 110'b: PCM Mode A-N (LRCK One Plus at Master Mode) 111'b: PCM Mode B-N (LRCK One Plus at Master Mode)

9.77. MX-0072h: I2S3 Audio Serial Data Port Control

Default: 8000'h

Table 159. MX-0072h: I2S3 Audio Serial Data Port Control

DSP Address: 0x1800_C0E4 **I2C Address: 0x0072**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s3_ms	15	R/W	1'h	I2S3 Serial Data Port Mode Selection 0'b: Master 1'b: Slave
reserved	14:9	R	0'h	Reserved
inv_i2s3_bclk	8	R/W	0'h	I2S3 BCLK Polarity Control 0'b: Normal 1'b: Invert
reserved	7	R	0'h	Reserved
en_i2s3_mono	6	R/W	0'h	Enable I2S3 PCM 17FS Mono Mode 0'b: Disable 1'b: Enable
sel_i2s3_len	5:4	R/W	0'h	I2S3 Data Length Selection 00'b: 16 bits 01'b: 20 bits 10'b: 24 bits 11'b: 8bits
reserved	3	R	0'h	Reserved
sel_i2s3_format	2:0	R/W	0'h	I2S3 PCM Data Format Selection 000'b: I^2S format 001'b: Left justified 010'b: PCM Mode A (LRCK One Plus at Master Mode) 011'b: PCM Mode B (LRCK One Plus at Master Mode) 100'b: Reserved 101'b: Reserved 110'b: PCM Mode A-N (LRCK One Plus at Master Mode) 111'b: PCM Mode B-N (LRCK One Plus at Master Mode)

9.78. MX-0073h: I2S4 Audio Serial Data Port Control

Default: 8000'h

Table 160. MX-0073h: I2S4 Audio Serial Data Port Control

DSP Address: 0x1800_C0E6 **I2C Address: 0x0073**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s4_ms	15	R/W	1'h	I2S4 Serial Data Port Mode Selection 0'b: Master 1'b: Slave
reserved	14:9	R	0'h	Reserved
inv_i2s4_bclk	8	R/W	0'h	I2S4 BCLK Polarity Control 0'b: Normal 1'b: Invert
reserved	7	R	0'h	Reserved
en_i2s4_mono	6	R/W	0'h	Enable I2S4 PCM 17FS Mono Mode 0'b: Disable 1'b: Enable
sel_i2s4_len	5:4	R/W	0'h	I2S4 Data Length Selection 00'b: 16 bits 01'b: 20 bits 10'b: 24 bits 11'b: 8bits
reserved	3	R	0'h	Reserved
sel_i2s4_format	2:0	R/W	0'h	I2S4 PCM Data Format Selection 000'b: I^2S format 001'b: Left justified 010'b: PCM Mode A (LRCK One Plus at Master Mode) 011'b: PCM Mode B (LRCK One Plus at Master Mode) 100'b: Reserved 101'b: Reserved 110'b: PCM Mode A-N (LRCK One Plus at Master Mode) 111'b: PCM Mode B-N (LRCK One Plus at Master Mode)

9.79. MX-0074h: I2S5 Audio Serial Data Port Control

Default: 8000'h

Table 161. MX-0074h: I2S5 Audio Serial Data Port Control

DSP Address: 0x1800_C0E8 **I2C Address: 0x0074**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s5_ms	15	R/W	1'h	I2S5 Serial Data Port Mode Selection 0'b: Master 1'b: Slave
reserved	14:9	R	0'h	Reserved
inv_i2s5_bclk	8	R/W	0'h	I2S5 BCLK Polarity Control 0'b: Normal 1'b: Invert
reserved	7	R	0'h	Reserved
en_i2s5_mono	6	R/W	0'h	Enable I2S5 PCM 17FS Mono Mode 0'b: Disable 1'b: Enable
sel_i2s5_len	5:4	R/W	0'h	I2S5 Data Length Selection 00'b: 16 bits 01'b: 20 bits 10'b: 24 bits 11'b: 8bits
reserved	3	R	0'h	Reserved
sel_i2s5_format	2:0	R/W	0'h	I2S5 PCM Data Format Selection 000'b: I^2S format 001'b: Left justified 010'b: PCM Mode A (LRCK One Plus at Master Mode) 011'b: PCM Mode B (LRCK One Plus at Master Mode) 100'b: Reserved 101'b: Reserved 110'b: PCM Mode A-N (LRCK One Plus at Master Mode) 111'b: PCM Mode B-N (LRCK One Plus at Master Mode)

9.80. MX-0075h: I2S LRCK/BCLK Source Selection

Default: 0000'h

Table 162. MX-0075h: I2S LRCK/BCLK Source Selection

DSP Address: 0x1800_C0EA I2C Address: 0x0075				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
Sel_i2s5_clk	14:12	R/W	0'h	I2S5 LRCK and BCLK Selection when Master Mode 000'b: Itself (LRCK5 and BCLK5) 001'b: Reserved 010'b: Reserved 011'b: Reserved 100'b: LRCK1 and BCLK1 101'b: LRCK2 and BCLK2 110'b: LRCK3 and BCLK3 111'b: LRCK4 and BCLK4
Sel_i2s4_clk	11:9	R/W	0'h	I2S4 LRCK and BCLK Selection when Master Mode 000'b: Itself (LRCK4 and BCLK4) 001'b: Reserved 010'b: Reserved 011'b: Reserved 100'b: LRCK1 and BCLK1 101'b: LRCK2 and BCLK2 110'b: LRCK3 and BCLK3 111'b: LRCK5 and BCLK5
Sel_i2s3_clk	8:6	R/W	0'h	I2S3 LRCK and BCLK Selection when Master Mode 000'b: Itself (LRCK3 and BCLK3) 001'b: Reserved 010'b: Reserved 011'b: Reserved 100'b: LRCK1 and BCLK1 101'b: LRCK2 and BCLK2 110'b: LRCK4 and BCLK4 111'b: LRCK5 and BCLK5
Sel_i2s2_clk	5:3	R/W	0'h	I2S2 LRCK and BCLK Selection when Master Mode 000'b: Itself (LRCK2 and BCLK2) 001'b: Same as LRCK1 and BCLK1 of Slave I2S1 010'b: Reserved 011'b: Reserved 100'b: LRCK1 and BCLK1 101'b: LRCK3 and BCLK3 110'b: LRCK4 and BCLK4 111'b: LRCK5 and BCLK5
Sel_i2s1_clk	2:0	R/W	0'h	I2S1 LRCK and BCLK Selection when Master Mode 000'b: Itself (LRCK1 and BCLK1) 001'b: Reserved 010'b: Reserved 011'b: Reserved 100'b: LRCK2 and BCLK2 101'b: LRCK3 and BCLK3 110'b: LRCK4 and BCLK4 111'b: LRCK5 and BCLK5

9.81. MX-0076h: Clock Tree Control 1

Default: 7777'h

Table 163. MX-0076h: Clock Tree Control 1

DSP Address: 0x1800_C0EC I2C Address: 0x0076				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15	R	0'h	Reserved
sel_i2s_pre_div1	14:12	R/W	7'h	I2S_Pre_Div1 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16
Reserved	11	R	0'h	Reserved
sel_i2s_pre_div2	10:8	R/W	7'h	I2S_Pre_Div2 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16
sel_i2s_bclk_ms3	7	R/W	0'h	Third Master Mode clock relative of BCLK and LRCK 0'b: 16Bits (32FS) 1'b: 32Bits (64FS)
sel_i2s_pre_div3	6:4	R/W	7'h	I2S_Pre_Div3 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16
sel_i2s_bclk_ms4	3	R/W	0'h	Fourth Master Mode clock relative of BCLK and LRCK 0'b: 16Bits (32FS) 1'b: 32Bits (64FS)
sel_i2s_pre_div4	2:0	R/W	7'h	I2S_Pre_Div4 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16

9.82. MX-0077h: Clock Tree Control 2

Default: 7777'h

Table 164. MX-0077h: Clock Tree Control 2

DSP Address: 0x1800_C0EE **I2C Address: 0x0077**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s_bclk_ms5	15	R/W	0'h	Fifth Master Mode clock relative of BCLK and LRCK 0'b: 16Bits (32FS) 1'b: 32Bits (64FS)
sel_i2s_pre_div5	14:12	R/W	7'h	I2S_Pre_Div5 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16
reserved	11	R	0'h	Reserved
sel_i2s_pre_div6	10:8	R/W	7'h	I2S_Pre_Div6 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16
reserved	7	R	0'h	Reserved
sel_i2s_pre_div7	6:4	R/W	7'h	I2S_Pre_Div7 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16
reserved	3	R	0'h	Reserved
sel_i2s_pre_div8	2:0	R/W	7'h	I2S_Pre_Div8 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16

9.83. MX-0078h: Clock Tree Control 3

Default: 7000’h

Table 165. MX-0078h: Clock Tree Control 3

DSP Address: 0x1800_C0F0 **I2C Address: 0x0078**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0’h	Reserved
sel_i2s_pre_div0	14:12	R/W	7’h	I2S_Pre_Div0 (For I2S1 Master Pre-Divider) 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16
reserved	11:10	R	0’h	Reserved
sel_dsp_asrcout_div	9:8	R/W	0’h	DSP ASRCOUT Divider 000b: ÷ 1 001b: ÷ 1.5 010b: ÷ 2 011b: ÷ 3
reserved	7:6	R	0’h	Reserved
sel_dsp_asrcin_div	5:4	R/W	0’h	DSP ASRCIN Divider 000b: ÷ 1 001b: ÷ 1.5 010b: ÷ 2 011b: ÷ 3
reserved	3	R	0’h	Reserved
i2s3_lrck_sel_mst	2	R/W	0’h	I2S3 LRCK Divider Control for Master Mode 0’b: ÷ 256 1’b: ÷ 128
i2s4_lrck_sel_mst	1	R/W	0’h	I2S4 LRCK Divider Control for Master Mode 0’b: ÷ 256 1’b: ÷ 128
i2s5_lrck_sel_mst	0	R/W	0’h	I2S5 LRCK Divider Control for Master Mode 0’b: ÷ 256 1’b: ÷ 128

9.84. MX-0079h: Clock Tree Control 4

Default: 3000'h

Table 166. MX-0079h: Clock Tree Control 4

DSP Address: 0x1800_C0F2 I2C Address: 0x0079				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:14	R	0'h	Reserved
sel_spdif_div	13:12	R/W	3'h	SPDIF Input Clock Divider 00b: ÷ 1 01b: ÷ 2 10b: ÷ 3 11b: ÷ 4
Reserved	11:0	R	0'h	Reserved

9.85. MX-007Ah: PLL1 Control 1

Default: 0000'h

Table 167. MX-007Ah: PLL1 Control 1

DSP Address: 0x1800_C0F4 I2C Address: 0x007A				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Div_n_pll1	15:7	R/W	0'h	N[8:0] code for analog PLL1 000000000'b: Div 2 000000001'b: Div 3 …….. 111111111'b: Div 513
reserved	6	R	0'h	Reserved
Bpk_pll1	5	R/W	0'h	Bypass PLL1 K 0'b : No bypass 1'b : Bypass
Div_k_pll1	4:0	R/W	0'h	K[4:0] code for analog PLL1 00000'b: Div 2 00001'b: Div 3 …… 11111'b: Div 33

9.86. MX-007Bh: PLL1 Control 2

Default: 0000'h

Table 168. MX-007Bh: PLL1 Control 2

DSP Address: 0x1800_C0F6 I2C Address: 0x007B				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Div_m_pll1	15:12	R/W	0'h	M[3:0] code for analog PLL1 0000'b: Div 2 0001'b: Div 3 …….. 1111'b: Div 17
Bpm_pll1	11	R/W	0'h	Bypass PLL1 M 0'b : No bypass 1'b : Bypass
reserved	10:2	R	0'h	Reserved
En_update_pll1	1	R	0'h	Simultaneous Update PLL1 M/N/K Code, BPK_PLL1 and BPM_PLL1 Write 1'b to Update
reserved	0	R	0'h	Reserved

9.87. MX-007Ch: PLL2 Control 1

Default: 0000'h

Table 169. MX-007Ch: PLL2 Control 1

DSP Address: 0x1800_C0F8 I2C Address: 0x007C				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Div_n_pll2	15:7	R/W	0'h	N[8:0] code for analog PLL2 000000000'b: Div 2 000000001'b: Div 3 …….. 111111111'b: Div 513
Reserved	6	R	0'h	Reserved
Bpk_pll2	5	R/W	0'h	Bypass PLL2 K 0'b : No bypass 1'b : Bypass
Div_k_pll2	4:0	R/W	0'h	K[4:0] code for analog PLL2 00000'b: Div 2 00001'b: Div 3 …… 11111'b: Div 33

9.88. MX-007Dh: PLL2 Control 2

Default: 0000'h

Table 170. MX-007Dh: PLL2 Control 2

DSP Address: 0x1800_C0FA I2C Address: 0x007D				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Div_m_pll2	15:12	R/W	0'h	M[3:0] code for analog PLL2 0000'b: Div 2 0001'b: Div 3 …….. 1111'b: Div 17
Bpm_pll2	11	R/W	0'h	Bypass PLL2 M 0'b : No bypass 1'b : Bypass
reserved	10:2	R	0'h	Reserved
En_update_pll2	1	R	0'h	Simultaneous Update PLL2 M/N/K Code, BPK_PLL2 and BPM_PLL2 Write 1'b to Update
reserved	0	R	0'h	Reserved

9.89. MX-007Eh: DSP Clock Source Selection 1

Default: 0111'h

Table 171. MX-007Eh: DSP Clock Source Selection 1

DSP Address: 0x1800_C0FC I2C Address: 0x007E				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:11	R	0'h	Reserved
Sel_clk2_hifi3	10:8	R/W	1'h	Select HIFI3 DSP Clock2 Source 000'b: PLL1 001'b: PLL2 010'b: PLL3 011'b: Internal RC Clock 1 (25MHz) 100'b: Internal RC Clock 2 (1MHz) 101'b: MCLK1 110'b: MCLK2 111'b: Reserved
Reserved	7	R	0'h	Reserved
Sel_clk1_hifi3	6:4	R/W	1'h	Select HIFI3 DSP Clock1 Source 000'b: PLL1 001'b: PLL2 010'b: PLL3 011'b: Internal RC Clock 1 (25MHz) 100'b: Internal RC Clock 2 (1MHz) 101'b: MCLK1 110'b: MCLK2 111'b: Reserved
Reserved	3	R	0'h	Reserved

DSP Address: 0x1800_C0FC I2C Address: 0x007E				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_clk0_hifi3	2:0	R/W	1'h	Select HIFI3 DSP Clock0 Source 000'b: PLL1 001'b: PLL2 010'b: PLL3 011'b: Internal RC Clock 1 (25MHz) 100'b: Internal RC Clock 2 (1MHz) 101'b: MCLK1 110'b: MCLK2 111'b: Reserved

9.90. MX-007Fh: DSP Clock Source Selection 2

Default: 0333'h

Table 172. MX-007Fh: DSP Clock Source Selection 2

DSP Address: 0x1800_C0FE I2C Address: 0x007F				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:14	R	0'h	Reserved
En_mini_dsp_clk_gating	13	R/W	0'h	Enable MINI DSP Clock Gating Control for Power Saving (when sel_clk0~2_mini=010'b) 0'b: Disable 1'b: Enable
Reserved	12:11	R	0'h	Reserved
Sel_clk2_mini	10:8	R/W	3'h	Select MINI DSP Clock2 Source 000'b: PLL1 001'b: PLL2 010'b: PLL3 011'b: Internal RC Clock 1 (25MHz) 100'b: Internal RC Clock 2 (1MHz) 101'b: MCLK1 110'b: MCLK2 111'b: Reserved
Reserved	7	R	0'h	Reserved
Sel_clk1_mini	6:4	R/W	3'h	Select MINI DSP Clock1 Source 000'b: PLL1 001'b: PLL2 010'b: PLL3 011'b: Internal RC Clock 1 (25MHz) 100'b: Internal RC Clock 2 (1MHz) 101'b: MCLK1 110'b: MCLK2 111'b: Reserved
Reserved	3	R	0'h	Reserved

DSP Address: 0x1800_C0FE I2C Address: 0x007F				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_clk0_mini	2:0	R/W	3'h	Select MINI DSP Clock0 Source 000'b: PLL1 001'b: PLL2 010'b: PLL3 011'b: Internal RC Clock 1 (25MHz) 100'b: Internal RC Clock 2 (1MHz) 101'b: MCLK1 110'b: MCLK2 111'b: Reserved

9.91. MX-0080h: Global Clock Control 1

Default: 0000'h

Table 173. MX-0080h: Global Clock Control 1

DSP Address: 0x1800_C100 I2C Address: 0x0080				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
sel_sysclk1	14:12	R/W	0'h	System Clock Source MUX Control 000'b: MCLK1 001'b: MCLK2 010'b: PLL1 Out 011'b: PLL2 Out 100'b: PLL3 Out 101'b: Reserved 110'b: Internal Clock Others: Reserved
sel_pll1_sour	11:8	R/W	0'h	PLL1 Source Select 0000'b: From MCLK1 or MCLK2 0001'b: From BCLK1 0010'b: From BCLK2 0011'b: From BCLK3 0100'b: From BCLK4 0101'b: From BCLK5 0110'b: Reserved 0111'b: From RC 25MHz 1000'b: From RC 1MHz Other: Reserved
Sel_pll2_pre	7:6	R/W	0'h	PLL2 Pre-Source Mux Control 00'b: MCLK1 01'b: MCLK1 Div 2 10'b: MCLK2 11'b: Reserved

DSP Address: 0x1800_C100 I2C Address: 0x0080				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_pll1_pre	5:4	R/W	0'h	Pll-1 pre_selection 00'b: MCLK1 01'b: MCLK1 Div 2 10'b: MCLK2 11'b: MCLK1 Div 5
sel_dac_osr	3:2	R/W	0'h	Stereo DAC Over Sample Rate Select 00'b:128Fs 01'b:64Fs 10'b:32Fs 11'b:Reserved
sel_adc_osr	1:0	R/W	0'h	Stereo1 ADC Over Sample Rate Select 00'b:128Fs 01'b:64Fs 10'b:32Fs 11'b:Reserved

9.92. MX-0081h: Global Clock Control 2

Default: 0000'h

Table 174. MX-0081h: Global Clock Control 2

DSP Address: 0x1800_C102 I2C Address: 0x0081				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_pll2_sour	15:12	R/W	0'h	PLL2 Source Select 0000'b: From MCLK1 or MCLK2 0001'b: From BCLK1 0010'b: From BCLK2 0011'b: From BCLK3 0100'b: From BCLK4 0101'b: From BCLK5 0110'b: Reserved 0111'b: From RC 25MHz 1000'b: From RC 1MHz Other: Reserved
Reserved	11	R	0'h	Reserved
Sel_dsp_asrcout_sour	10:8	R/W	0'h	DSP ASRCOUT Clock Source Select 000'b: From MCLK 001'b: From PLL1 010'b: Reserved 011'b: From RC 25M clock 100'b: From DFLL Other: Reserved
Reserved	7	R	0'h	Reserved

DSP Address: 0x1800_C102 I2C Address: 0x0081				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_dsp_asrcin_sour	6:4	R/W	0'h	DSP ASRCIN Clock Source Select 000'b: From MCLK 001'b: From PLL1 010'b: Reserved 011'b: From RC 25M clock 100'b: From DFLL Other: Reserved
Reserved	3:2	R	0'h	Reserved
Sel_clk_sys_pre	1	R/W	0'h	Select the Clk_sys_pre source 0'b: No Pass through Fraction Divider 1'b: Pass through Fraction Divider
Sel_hclk_sram_source	0	R/W	0'h	Select hclk_sram source (SRAM clock) 0'b: From HIFI-Mini hclk 1'b: From HIFI-3 hclk

9.93. MX-0083h: ASRC Control 1

Default: 0000'h

Table 175. MX-0083h: ASRC Control 1

DSP Address: 0x1800_C106 I2C Address: 0x0083				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_mono_da_3l_mode	15	R/W	0'h	Enable DAC ASRC for DD1_L 0'b: Disable 1'b: Enable
sel_mono_da_3r_mode	14	R/W	0'h	Enable DAC ASRC for DD1_R 0'b: Disable 1'b: Enable
reserved	13:7	R	0'h	Reserved
en_i2s7_asrc	6	R/W	0'h	Enable I2S7 ASRC Function 0'b: Disable 1'b: Enable
en_i2s6_asrc	5	R/W	0'h	Enable I2S6 ASRC Function 0'b: Disable 1'b: Enable
en_i2s5_asrc	4	R/W	0'h	Enable I2S5 ASRC Function 0'b: Disable 1'b: Enable
en_i2s4_asrc	3	R/W	0'h	Enable I2S4 ASRC Function 0'b: Disable 1'b: Enable
en_i2s3_asrc	2	R/W	0'h	Enable I2S3 ASRC Function 0'b: Disable 1'b: Enable

DSP Address: 0x1800_C106 I2C Address: 0x0083				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_i2s2_asrc	1	R/W	0'h	Enable I2S2 ASRC Function 0'b: Disable 1'b: Enable
en_i2s1_asrc	0	R/W	0'h	Enable I2S1 ASRC Function 0'b: Disable 1'b: Enable

9.94. MX-0084h: ASRC Control 2

Default: 0000'h

Table 176. MX-0084h: ASRC Control 2

DSP Address: 0x1800_C108 I2C Address: 0x0084				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
Sel_stereo_dac_mode	14	R/W	0'h	Enable DAC ASRC for Stereo DAC 0'b : Disable 1'b : Enable
Sel_mono_dac_l_mode	13	R/W	0'h	Enable DAC ASRC for mono left path 0'b : Disable 1'b : Enable
Sel_mono_dac_r_mode	12	R/W	0'h	Enable DAC ASRC for mono right path 0'b : Disable 1'b : Enable
en_dmic_asrc_stereo1	11	R/W	0'h	Enable DMIC ASRC for stereo1 ADC path 0'b : Disable 1'b : Enable
en_dmic_asrc_stereo2	10	R/W	0'h	Enable DMIC ASRC for stereo2 ADC path 0'b : Disable 1'b : Enable
en_dmic_asrc_stereo3	9	R/W	0'h	Enable DMIC ASRC for stereo3 ADC path 0'b : Disable 1'b : Enable
Reserved	8	R	0'h	Reserved
en_dmic_asrc_monol	7	R/W	0'h	Enable DMIC ASRC for mono left ADC path 0'b : Disable 1'b : Enable
en_dmic_asrc_monor	6	R/W	0'h	Enable DMIC ASRC for mono right ADC path 0'b : Disable 1'b : Enable
en_adc_asrc_stereo1	5	R/W	0'h	Enable ADC ASRC for stereo1 ADC path 0'b : Disable 1'b : Enable
en_adc_asrc_stereo2	4	R/W	0'h	Enable ADC ASRC for stereo2 ADC path 0'b : Disable 1'b : Enable

DSP Address: 0x1800_C108 I2C Address: 0x0084				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_adc_asrc_stereo3	3	R/W	0'h	Enable ADC ASRC for stereo3 ADC path 0'b : Disable 1'b : Enable
Reserved	2	R	0'h	Reserved
en_adc_asrc_monol	1	R/W	0'h	Enable ADC ASRC for mono left ADC path 0'b : Disable 1'b : Enable
en_adc_asrc_monor	0	R/W	0'h	Enable ADC ASRC for mono right ADC path 0'b : Disable 1'b : Enable

9.95. MX-0085h: ASRC Control 3

Default: 0000'h

Table 177. MX-0085h: ASRC Control 3

DSP Address: 0x1800_C10A I2C Address: 0x0085				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_da_filter_stereo_asrc	15:12	R/W	0'h	Select the ASRC clock source for da stereo filter 0000'b : CLK_sys_div_out 0001'b : clk_i2s1_asrc 0010'b : clk_i2s2_asrc 0011'b : clk_i2s3_asrc 0100'b : clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_i2s7_asrc 1000'b : clk_sys2 1001'b : clk_sys3 1010'b : clk_sys4 1011'b : clk_sys5 1100'b : clk_sys6 1101'b : clk_sys7 1110'b : clk_sys8 Others: Reserved
Reserved	11:8	R	0'h	RESERVED

DSP Address: 0x1800_C10A I2C Address: 0x0085				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_da_filter_mono2l_asrc	7:4	R/W	0'h	Select the ASRC clock source for da mono left filter 0000'b : CLK_sys_div_out 0001'b : clk_i2s1_asrc 0010'b : clk_i2s2_asrc 0011'b : clk_i2s3_asrc 0100'b : clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_i2s7_asrc 1000'b : clk_sys2 1001'b : clk_sys3 1010'b : clk_sys4 1011'b : clk_sys5 1100'b : clk_sys6 1101'b : clk_sys7 1110'b : clk_sys8 Others: Reserved
sel_da_filter_mono2r_asrc	3:0	R/W	0'h	Select the ASRC clock source for da mono right filter 0000'b : CLK_sys_div_out 0001'b : clk_i2s1_asrc 0010'b : clk_i2s2_asrc 0011'b : clk_i2s3_asrc 0100'b : clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_i2s7_asrc 1000'b : clk_sys2 1001'b : clk_sys3 1010'b : clk_sys4 1011'b : clk_sys5 1100'b : clk_sys6 1101'b : clk_sys7 1110'b : clk_sys8 Others: Reserved

9.96. MX-0086h: ASRC Control 4

Default: 0000'h

Table 178. MX-0086h: ASRC Control 4

DSP Address: 0x1800_C10C **I2C Address: 0x0086**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_da_filter_mono3l_asrc	15:12	R/W	0'h	Select the ASRC clock source for da mono left filter 0000'b : CLK_sys_div_out 0001'b : clk_i2s1_asrc 0010'b : clk_i2s2_asrc 0011'b : clk_i2s3_asrc 0100'b : clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_i2s7_asrc 1000'b : clk_sys2 1001'b : clk_sys3 1010'b : clk_sys4 1011'b : clk_sys5 1100'b : clk_sys6 1101'b : clk_sys7 1110'b : clk_sys8 Others: Reserved
sel_da_filter_mono3r_asrc	11:8	R/W	0'h	Select the ASRC clock source for da mono right filter 0000'b : CLK_sys_div_out 0001'b : clk_i2s1_asrc 0010'b : clk_i2s2_asrc 0011'b : clk_i2s3_asrc 0100'b : clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_i2s7_asrc 1000'b : clk_sys2 1001'b : clk_sys3 1010'b : clk_sys4 1011'b : clk_sys5 1100'b : clk_sys6 1101'b : clk_sys7 1110'b : clk_sys8 Others: Reserved
Reserved	7:0	R	0'h	Reserved

9.97. MX-0087h: ASRC Control 5

Default: 0000'h

Table 179. MX-0087h: ASRC Control 5

DSP Address: 0x1800_C10E I2C Address: 0x0087				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_ad_filter_stereo1_asrc	15:12	R/W	0'h	Select the ASRC clock source for ad stereo1 filter 0000'b : CLK_sys_div_out 0001'b : clk_i2s1_asrc 0010'b : clk_i2s2_asrc 0011'b : clk_i2s3_asrc 0100'b : clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_i2s7_asrc 1000'b : clk_sys2 1001'b : clk_sys3 1010'b : clk_sys4 1011'b : clk_sys5 1100'b : clk_sys6 1101'b : clk_sys7 1110'b : clk_sys8 Others: Reserved
sel_ad_filter_stereo2_asrc	11:8	R/W	0'h	Select the ASRC clock source for ad stereo2 filter 0000'b : CLK_sys_div_out 0001'b : clk_i2s1_asrc 0010'b : clk_i2s2_asrc 0011'b : clk_i2s3_asrc 0100'b : clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_i2s7_asrc 1000'b : clk_sys2 1001'b : clk_sys3 1010'b : clk_sys4 1011'b : clk_sys5 1100'b : clk_sys6 1101'b : clk_sys7 1110'b : clk_sys8 Others: Reserved

DSP Address: 0x1800_C10E I2C Address: 0x0087				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_ad_filter_stereo3_asrc	7:4	R/W	0'h	Select the ASRC clock source for ad stereo3 filter 0000'b : CLK_sys_div_out 0001'b : clk_i2s1_asrc 0010'b : clk_i2s2_asrc 0011'b : clk_i2s3_asrc 0100'b : clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_i2s7_asrc 1000'b : clk_sys2 1001'b : clk_sys3 1010'b : clk_sys4 1011'b : clk_sys5 1100'b : clk_sys6 1101'b : clk_sys7 1110'b : clk_sys8 Others: Reserved
reserved	3:0	R	0'h	Reserved

9.98. MX-0088h: ASRC Control 6

Default: 0000'h

Table 180. MX-0088h: ASRC Control 6

DSP Address: 0x1800_C110 I2C Address: 0x0088				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_ad_filter_monol_asrc	15:12	R/W	0'h	Select the ASRC clock source for ad monol filter 0000'b : CLK_sys_div_out 0001'b : clk_i2s1_asrc 0010'b : clk_i2s2_asrc 0011'b : clk_i2s3_asrc 0100'b : clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_i2s7_asrc 1000'b : clk_sys2 1001'b : clk_sys3 1010'b : clk_sys4 1011'b : clk_sys5 1100'b : clk_sys6 1101'b : clk_sys7 1110'b : clk_sys8 Others: Reserved

DSP Address: 0x1800_C110 I2C Address: 0x0088				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_ad_filter_monor_asrc	11:8	R/W	0'h	Select the ASRC clock source for ad monor filter 0000'b : CLK_sys_div_out 0001'b : clk_i2s1_asrc 0010'b : clk_i2s2_asrc 0011'b : clk_i2s3_asrc 0100'b : clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_i2s7_asrc 1000'b : clk_sys2 1001'b : clk_sys3 1010'b : clk_sys4 1011'b : clk_sys5 1100'b : clk_sys6 1101'b : clk_sys7 1110'b : clk_sys8 Others: Reserved
Sel_sd_adc_clock	7:4	R/W	0'h	Select the clock source for VAD_ADC 0000'b : CLK_sys_div_out 1000'b : clk_sys2 1001'b : clk_sys3 1010'b : clk_sys4 1011'b : clk_sys5 1100'b : clk_sys6 1101'b : clk_sys7 1110'b : clk_sys8 Others: Reserved
sel_dsp_mini_out_fs	3:0	R/W	0'h	Select the ASRC clock source for Mini DSP OutBound0/1 0000'b : CLK_sys_div_out 0001'b : clk_i2s1_asrc 0010'b : clk_i2s2_asrc 0011'b : clk_i2s3_asrc 0100'b : clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_i2s7_asrc 1000'b : clk_sys2 1001'b : clk_sys3 1010'b : clk_sys4 1011'b : clk_sys5 1100'b : clk_sys6 1101'b : clk_sys7 1110'b : clk_sys8 Others: Reserved

9.99. MX-0089h: ASRC Control 7

Default: 0000'h

Table 181. MX-0089h: ASRC Control 7

DSP Address: 0x1800_C112 I2C Address: 0x0089				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_dsp_out_fs_sec1	15:12	R/W	0'h	Select the ASRC clock source for DSP OutBound0 ~ 3 0000'b : CLK_sys_div_out 0001'b : clk_i2s1_asrc 0010'b : clk_i2s2_asrc 0011'b : clk_i2s3_asrc 0100'b : clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_i2s7_asrc 1000'b : clk_sys2 1001'b : clk_sys3 1010'b : clk_sys4 1011'b : clk_sys5 1100'b : clk_sys6 1101'b : clk_sys7 1110'b : clk_sys8 Others: Reserved
sel_dsp_out_fs_sec2	11:8	R/W	0'h	Select the ASRC clock source for DSP OutBound4 ~ 7 0000'b : CLK_sys_div_out 0001'b : clk_i2s1_asrc 0010'b : clk_i2s2_asrc 0011'b : clk_i2s3_asrc 0100'b : clk_i2s4_asrc 0101'b: clk_i2s5_asrc 0110'b: clk_i2s6_asrc 0111'b: clk_i2s7_asrc 1000'b : clk_sys2 1001'b : clk_sys3 1010'b : clk_sys4 1011'b : clk_sys5 1100'b : clk_sys6 1101'b : clk_sys7 1110'b : clk_sys8 Others: Reserved
sel_dsp_out_fs_src_sec1	7:4	R/W	0'h	Select the ASRC clock source for DSP OutBound0 ~ 1 SRC OUT FS 0000'b: Stereo DA Filter 0001'b : I2S1_ADC1 0010'b : I2S2_ADC1 0011'b : I2S3 0100'b : I2S4 0101'b: I2S5 0110'b: Reserved Others: Reserved

DSP Address: 0x1800_C112 I2C Address: 0x0089				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	3	R	0'h	Reserved
sel_dsp_out_fs_src_sec2	2:0	R/W	0'h	Select the ASRC clock source for DSP OutBound2 ~ 3 SRC OUT FS 000'b : Mono DA Filter 001'b : I2S1_ADC2 010'b : I2S2_ADC2 011'b : I2S3 100'b : I2S4 101'b: I2S5 110'b: Reserved 111'b: Reserved

9.100. MX-008Ah: ASRC Control 8

Default: 0000'h

Table 182. MX-008Ah: ASRC Control 8

DSP Address: 0x1800_C114 I2C Address: 0x008A				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
sel_i2s1_asrc	14:12	R/W	0'h	Select the ASRC source of I2S1 000'b: LRCK1 001'b: LRCK2 010'b: LRCK3 011'b: LRCK4 100'b: LRCK5 101'b: Reserved 110'b: Reserved 111'b: SPDIF
Reserved	11	R	0'h	Reserved
sel_i2s2_asrc	10:8	R/W	0'h	Select the ASRC source of I2S2 000'b: LRCK1 001'b: LRCK2 010'b: LRCK3 011'b: LRCK4 100'b: LRCK5 101'b: Reserved 110'b: Reserved 111'b: SPDIF
Reserved	7	R	0'h	Reserved

DSP Address: 0x1800_C114 I2C Address: 0x008A				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s3_asrc	6:4	R/W	0'h	Select the ASRC source of I2S3 000'b: LRCK1 001'b: LRCK2 010'b: LRCK3 011'b: LRCK4 100'b: LRCK5 101'b: Reserved 110'b: Reserved 111'b: SPDIF
Reserved	3	R	0'h	Reserved
sel_i2s4_asrc	2:0	R/W	0'h	Select the ASRC source of I2S4 000'b: LRCK1 001'b: LRCK2 010'b: LRCK3 011'b: LRCK4 100'b: LRCK5 101'b: Reserved 110'b: Reserved 111'b: SPDIF

9.101. MX-008Bh: ASRC Control 9

Default: 0000'h

Table 183. MX-008Bh: ASRC Control 9

DSP Address: 0x1800_C116 I2C Address: 0x008B				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
sel_i2s5_asrc	14:12	R/W	0'h	Select the ASRC source of I2S5 000'b: LRCK1 001'b: LRCK2 010'b: LRCK3 011'b: LRCK4 100'b: LRCK5 101'b: Reserved 110'b: Reserved 111'b: SPDIF
Reserved	11	R	0'h	Reserved

DSP Address: 0x1800_C116 I2C Address: 0x008B				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_i2s6_asrc	10:8	R/W	0'h	Select the ASRC source of I2S6 000'b: LRCK1 001'b: LRCK2 010'b: LRCK3 011'b: LRCK4 100'b: LRCK5 101'b: Reserved 110'b: Reserved 111'b: SPDIF
Reserved	7	R	0'h	Reserved
sel_i2s7_asrc	6:4	R/W	0'h	Select the ASRC source of I2S7 000'b: LRCK1 001'b: LRCK2 010'b: LRCK3 011'b: LRCK4 100'b: LRCK5 101'b: Reserved 110'b: Reserved 111'b: SPDIF
Reserved	3:0	R	0'h	Reserved

9.102. MX-008Ch: ASRC Control 10

Default: 0000'h

Table 184. MX-008Ch: ASRC Control 10

DSP Address: 0x1800_C118 I2C Address: 0x008C				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
i2s1_asrc_prediv	15:14	R/W	0'h	Set the i2s1 clock division for ASRC mode 00'b: div1 01'b: div2 10'b: div3 11'b: reserved
i2s2_asrc_prediv	13:12	R/W	0'h	Set the i2s2 clock division for ASRC mode 00'b: div1 01'b: div2 10'b: div3 11'b: Reserved
i2s3_asrc_prediv	11:10	R/W	0'h	Set the i2s3 clock division for ASRC mode 00'b: div1 01'b: div2 10'b: div3 11'b: Reserved

DSP Address: 0x1800_C118 I2C Address: 0x008C				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
i2s4_asrc_prediv	9:8	R/W	0'h	Set the i2s4 clock division for ASRC mode 00'b: div1 01'b: div2 10'b: div3 11'b: Reserved
i2s5_asrc_prediv	7:6	R/W	0'h	Set the i2s5 clock division for ASRC mode 00'b: div1 01'b: div2 10'b: div3 11'b: Reserved
i2s6_asrc_prediv	5:4	R/W	0'h	Set the i2s6 clock division for ASRC mode 00'b: div1 01'b: div2 10'b: div3 11'b: Reserved
i2s7_asrc_prediv	3:2	R/W	0'h	Set the i2s7 clock division for ASRC mode 00'b: div1 01'b: div2 10'b: div3 11'b: Reserved
Reserved	1:0	R	0'h	Reserved

9.103. MX-009Ch: Fractional Divider for System Clock Control 1

Default: 0002'h

Table 185. MX-009Ch: Fractional Divider for System Clock Control 1

DSP Address: 0x1800_C138 I2C Address: 0x009C				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Frac_mi	15:0	R/W	2'h	Parameter of fractional divider (range : 0~65535)

9.104. MX-009Dh: Fractional Divider for System Clock Control 2

Default: 0001'h

Table 186. MX-009Dh: Fractional Divider for System Clock Control 2

DSP Address: 0x1800_C13A I2C Address: 0x009D				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Frac_mi_ni_update	15	R	0'h	Fractional divider parameter update
Frac_ni	14:0	R/W	1'h	Parameter of fractional divider (range : 0~65535)

9.105. MX-00A0h: Jack and Microphone Detection Control 1

Default: 7080'h

Table 187. MX-00A0h: Jack and Microphone Detection Control 1

DSP Address: 0x1800_C140 I2C Address: 0x00A0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
En_jack_mic_det	15	R/W	0'h	Enable the Jack and Type Detection Function 0'b: Disable 1'b: Enable
Reg_mode	14	R/W	1'h	Select Auto or Register control for Jack and Type Detection 0'b: Auto mode 1'b: Register mode
Reserved	13:12	R	3'h	Reserved
En_ext_jd	11	R/W	0'h	Enable the external Jack detection trigger 0'b: Disable 1'b: Enable
Polarity_ext_jd	10	R/W	0'h	Select the polarity trigger of the external JD 0'b: High trigger 1'b: Low trigger
Reserved	9:7	R	1'h	Reserved
Ctrl_mb1_path1	6	R/W	0'h	Select the Micbias1 control path 0'b: Turn On/Off by Auto Detection Sequence 1'b: From Register (Pow_micbias1_Digital)
Manual_trig_ext_jd	5	R/W	0'h	Manual trigger the external JD 0'b: Low 1'b: High
Reserved	4:0	R	0'h	Reserved

9.106. MX-00A1h: Jack and Microphone Detection Control 2

Default: 4A00'h

Table 188. MX-00A1h: Jack and Microphone Detection Control 2

DSP Address: 0x1800_C142 I2C Address: 0x00A1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:7	R	94'h	Reserved
Sel_ext_jd_source	6:4	R/W	0'h	Select the external JD trigger source 000'b: Sta_gpio_jd1 001'b: Sta_gpio_jd2 010'b: Sta_gpio_jd3 011'b: Sta_gpio_jd4 100'b: Sta_gpio_jd5 101'b: Sta_gpio_jd6 110'b: Manual trigger (MX0010[5]) 111'b: Reserved
Reserved	3:2	R	0'h	Reserved

DSP Address: 0x1800_C142 I2C Address: 0x00A1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Jack_type	1:0	R	0'h	Detected result of the jack type 00'b: Have not detected 01'b: Headset type (w/ Mic) 10'b: Headphone type (w/o Mic) 11'b: Reserved

9.107. MX-00A3h: Jack and Microphone Detection Control 3

Default: A000'h

Table 189. MX-00A3h: Jack and Microphone Detection Control 3

DSP Address: 0x1800_C146 I2C Address: 0x00A3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Ctrl_vref_bias_path	15	R/W	1'h	Vref1/2, Mbias control signal source selection: 0'b: Power On/Off by Auto Sequence 1'b: Register Control Directly
Reserved	14:12	R	2'h	Reserved
Vo_micdet_cmp	11:8	R	0'h	MIC_IN Detection Comparator Output 0 : Under Threshold 1 : Over Threshold VO_MICDET_CMP<3> : Comparator_4 VO_MICDET_CMP<2> : Comparator_3 VO_MICDET_CMP<1> : Comparator_2 VO_MICDET_CMP<0> : Comparator_1
Reserved	7	R	0'h	Reserved
Sel_jd_avoid_pop	6:4	R/W	0'h	Select the JD source to avoid pop when jack unplug 000'b: Pad_gpio3 001'b: Pad_gpio5 010'b: Pad_gpio8 011'b: Pad_gpio11 100'b: Pad_gpio16 101'b: Pad_gpio18 110'b: JD Status 111'b: JD Status
Reserved	3	R	0'h	Reserved
Polarity_jd_avoid_pop	2	R/W	0'h	Select the Polarity JD source to avoid pop when jack unplug 0'b: Turn off when JD Status= Low 1'b: Turn off when JD Status= High
En_jd_avoid_pop	1	R/W	0'h	Enable the avoid pop function 0'b: Disable 1'b: Enable
Jd_done	0	R	0'h	Status of the Jack and Mic Detection 0'b: Plug Out 1'b: Plug In and Type Detection Done

9.108. MX-00B0h: Jack Detection Control 1

Default: 0000'h

Table 190. MX-00B0h: Jack Detection Control 1

DSP Address: 0x1800_C160 I2C Address: 0x00B0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_gpio_jd1	15:14	R/W	0'h	GPIO Jack Detect – 1 Source Selection 00'b: OFF 01'b: GPIO2 or GPIO27 or GPIO28 10'b: GPIO3 11'b: GPIO4 or GPIO20
sel_gpio_jd2	13:12	R/W	0'h	GPIO Jack Detect – 2 Source Selection 00'b: OFF 01'b: GPIO5 10'b: GPIO6 11'b: GPIO7 or GPIO21
sel_gpio_jd3	11:10	R/W	0'h	GPIO Jack Detect – 3 Source Selection 00'b: OFF 01'b: GPIO8 10'b: GPIO9 11'b: GPIO10 or GPIO22
sel_gpio_jd4	9:8	R/W	0'h	GPIO Jack Detect – 4 Source Selection 00'b: OFF 01'b: GPIO11 10'b: GPIO12 11'b: GPIO13 or GPIO23
sel_gpio_jd5	7:6	R/W	0'h	GPIO Jack Detect – 5 Source Selection 00'b: OFF 01'b: GPIO14 10'b: GPIO15 11'b: GPIO16 or GPIO24
sel_gpio_jd6	5:4	R/W	0'h	GPIO Jack Detect – 6 Source Selection 00'b: OFF 01'b: GPIO17 10'b: GPIO18 11'b: GPIO19 or GPIO25 or GPIO26
Sel_gpio_jd1_pre	3	R/W	0'h	GPIO Jack Detect – 1 Source Pre-Selection 0'b: GPIO4 1'b: GPIO20
Sel_gpio_jd2_pre	2	R/W	0'h	GPIO Jack Detect – 2 Source Pre-Selection 0'b: GPIO7 1'b: GPIO21
Sel_gpio_jd3_pre	1	R/W	0'h	GPIO Jack Detect – 3 Source Pre-Selection 0'b: GPIO10 1'b: GPIO22
Sel_gpio_jd4_pre	0	R/W	0'h	GPIO Jack Detect – 4 Source Pre-Selection 0'b: GPIO13 1'b: GPIO23

9.109. MX-00B1h: Jack Detection Control 2

Default: 0000'h

Table 191. MX-00B1h: Jack Detection Control 2

DSP Address: 0x1800_C162 I2C Address: 0x00B1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_gpio_jd5_pre	15	R/W	0'h	GPIO Jack Detect – 5 Source Pre-Selection 0'b: GPIO16 1'b: GPIO24
Reserved	14:0	R	0'h	Reserved

9.110. MX-00B4h: Jack Detection Control 3

Default: 0000'h

Table 192. MX-00B4h: Jack Detection Control 3

DSP Address: 0x1800_C168 I2C Address: 0x00B4				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_gpio_jd6_pre	15:14	R/W	0'h	Select sta_gpio_jd6 pre-source 00'b: GPIO19 01'b: GPIO25 10'b: GPIO26 11'b: Reserved
Sel_gpio_jd1_pre2	13:12	R/W	0'h	Select sta_gpio_jd1 pre-source 00'b: GPIO2 01'b: Analog JD Status 10'b: Analog JD Status 11'b: Reserved
Reserved	11:4	R	0'h	Reserved
Sel_vad_flag_source	3:0	R/W	0'h	Select VAD Flag Source 0000'b: pitch_det_flag_hold 0001'b: pitch_det_flag 0010'b: hello_det_flag_hold 0011'b: hello_det_flag 0100'b: ok_flag_hold 0101'b: ok_flag 0110'b: ext_det_flag_hold 0111'b: ext_det_flag 1000'b: pitch_det_debounce_flag 1001'b: pitch_det_debounce_edge_flag Other: Reserved

9.111. MX-00B5h: Internal Status 1

Default: 0000'h

Table 193. MX-00B5h: Internal Status 1

DSP Address: 0x1800_C16A I2C Address: 0x00B5				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sta_gpio_jd1	15	R	0'h	Status of GPIO Jack detection 1 Read: Return status of Jack Detect Select output Write: Write '0' to clear stick bit
sta_gpio_jd2	14	R	0'h	Status of GPIO Jack detection 2 Read: Return status of Jack Detect Select output Write: Write '0' to clear stick bit
sta_gpio_jd3	13	R	0'h	Status of GPIO Jack detection 3 Read: Return status of Jack Detect Select output Write: Write '0' to clear stick bit
sta_gpio_jd4	12	R	0'h	Status of GPIO Jack detection 4 Read: Return status of Jack Detect Select output Write: Write '0' to clear stick bit
sta_gpio_jd5	11	R	0'h	Status of GPIO Jack detection 5 Read: Return status of Jack Detect Select output Write: Write '0' to clear stick bit
sta_gpio_jd6	10	R	0'h	Status of GPIO Jack detection 6 Read: Return status of Jack Detect Select output Write: Write '0' to clear stick bit
sta_pitch_det	9	R	0'h	Status of Pitch Detection Flag Read: Return status of Pitch Detection Flag Write: Write '0' to clear stick bit
Sta_micbias1_ovcd	8	R	0'h	MICBIAS1 over current status Read: return status of each status pin Write: Write '0' to clear stick bit
sta_inline_cmd_fg	7	R	0'h	Status of Inline Command Flag Read: Return status Write: Write '0' to clear stick bit
Reserved	6:2	R	0'h	Reserved
sta_long_press	1	R	0'h	Status of Long Press Detection Read: Return status Write: Write '0' to clear stick bit
Reserved	0	R	0'h	Reserved

9.112. MX-00B6h: Internal Status 2

Default: 0000'h

Table 194. MX-00B6h: Internal Status 2

DSP Address: 0x1800_C16C I2C Address: 0x00B6				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:14	R	0'h	Reserved

DSP Address: 0x1800_C16C I2C Address: 0x00B6				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sta_wakeup_click_irq	13	R	0'h	Status of Wakeup Click Detection Read: Return status Write: Write '0' to clear stick bit
sta_hifi3_dsp_watchdog_fg	12	R	0'h	Status of HIFI3 DSP Watch Dog Flag Read: Return status Write: Write '0' to clear stick bit
sta_mini_dsp_watchdog_fg	11	R	0'h	Status of Mini DSP Watch Dog Flag Read: Return status Write: Write '0' to clear stick bit
sta_crc_error_fg	10	R	0'h	Status of CRC Error Flag Read: Return status Write: Write '0' to clear stick bit
Reserved	9:8	R	0'h	Reserved
sta_hifi3_to_host	7	R	0'h	Status of HIFI3 to Host Interrupt Read: Return status Write: Write '0' to clear stick bit
sta_mini_to_host	6	R	0'h	Status of Mini to Host Interrupt Read: Return status Write: Write '0' to clear stick bit
Reserved	5:0	R	0'h	Reserved

9.113. MX-00B7h: IRQ Control 1

Default: 0000'h

Table 195. MX-00B7h: IRQ Control 1

DSP Address: 0x1800_C16E I2C Address: 0x00B7				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_irq_gpio_jd1	15	R/W	0'h	IRQ output source configure of GPIO jack detection 1 status 0'b: Bypass 1'b: Normal
en_tridsp_gpio_jd1	14	R/W	0'h	Trigger HIFI3 DSP source configure of GPIO jack detection 1 status 0'b: Bypass 1'b: Enable
en_triminidsp_gpio_jd1	13	R/W	0'h	Trigger Mini DSP source configure of GPIO jack detection 1 status 0'b: Disable 1'b: Enable
en_gpio_jd1_sticky	12	R/W	0'h	Sticky Control for Jack Detect 1 0'b: Disable 1'b: Enable
inv_gpio_jd1	11	R/W	0'h	GPIO Jack Detection 1 Status Polarity 0'b: Normal 1'b: Output Invert

DSP Address: 0x1800_C16E I2C Address: 0x00B7				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_irq_gpio_jd2	10	R/W	0'h	IRQ output source configure of GPIO jack detection 2 status 0'b: Bypass 1'b: Normal
en_tridsp_gpio_jd2	9	R/W	0'h	Trigger HIFI3 DSP source configure of GPIO jack detection 2 status 0'b: Bypass 1'b: Enable
en_triminidsp_gpio_jd2	8	R/W	0'h	Trigger Mini DSP source configure of GPIO jack detection 2 status 0'b: Disable 1'b: Enable
en_gpio_jd2_sticky	7	R/W	0'h	Sticky Control for Jack Detect 2 0'b: Disable 1'b: Enable
inv_gpio_jd2	6	R/W	0'h	GPIO Jack Detection 2 Status Polarity 0'b: Normal 1'b: Output Invert
en_irq_gpio_jd3	5	R/W	0'h	IRQ output source configure of GPIO jack detection 3 status 0'b: Bypass 1'b: Normal
en_tridsp_gpio_jd3	4	R/W	0'h	Trigger HIFI3 DSP source configure of GPIO jack detection 3 status 0'b: Bypass 1'b: Enable
en_triminidsp_gpio_jd3	3	R/W	0'h	Trigger Mini DSP source configure of GPIO jack detection 3 status 0'b: Disable 1'b: Enable
en_gpio_jd3_sticky	2	R/W	0'h	Sticky Control for Jack Detect 3 0'b: Disable 1'b: Enable
inv_gpio_jd3	1	R/W	0'h	GPIO Jack Detection 3 Status Polarity 0'b: Normal 1'b: Output Invert
En_dual_jd	0	R/W	0'h	Enable the dual JD trigger IRQ function 0'b: Disable 1'b: Enable

9.114. MX-00B8h: IRQ Control 2

Default: 0000'h

Table 196. MX-00B8h: IRQ Control 2

DSP Address: 0x1800_C170 I2C Address: 0x00B8				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_irq_gpio_jd4	15	R/W	0'h	IRQ output source configure of GPIO jack detection 4 status 0'b: Bypass 1'b: Normal
en_tridsp_gpio_jd4	14	R/W	0'h	Trigger HIFI3 DSP source configure of GPIO jack detection 4 status 0'b: Bypass 1'b: Enable
en_triminidsp_gpio_jd4	13	R/W	0'h	Trigger Mini DSP source configure of GPIO jack detection 4 status 0'b: Disable 1'b: Enable
en_gpio_jd4_sticky	12	R/W	0'h	Sticky Control for Jack Detect 4 0'b: Disable 1'b: Enable
inv_gpio_jd4	11	R/W	0'h	GPIO Jack Detection 4 Status Polarity 0'b: Normal 1'b: Output Invert
en_irq_gpio_jd5	10	R/W	0'h	IRQ output source configure of GPIO jack detection 5 status 0'b: Bypass 1'b: Normal
en_tridsp_gpio_jd5	9	R/W	0'h	Trigger HIFI3 DSP source configure of GPIO jack detection 5 status 0'b: bypass 1'b: Enable
en_triminidsp_gpio_jd5	8	R/W	0'h	Trigger Mini DSP source configure of GPIO jack detection 5 status 0'b: Disable 1'b: Enable
en_gpio_jd5_sticky	7	R/W	0'h	Sticky Control for Jack Detect 5 0'b: Disable 1'b: Enable
inv_gpio_jd5	6	R/W	0'h	GPIO Jack Detection 5 Status Polarity 0'b: Normal 1'b: Output Invert
en_irq_gpio_jd6	5	R/W	0'h	IRQ output source configure of GPIO jack detection 6 status 0'b: Bypass 1'b: Normal
en_tridsp_gpio_jd6	4	R/W	0'h	Trigger HIFI3 DSP source configure of GPIO jack detection 6 status 0'b: Bypass 1'b: Enable

DSP Address: 0x1800_C170 I2C Address: 0x00B8				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_triminidsp_gpio_jd6	3	R/W	0'h	Trigger Mini DSP source configure of GPIO jack detection 6 status 0'b: Disable 1'b: Enable
en_gpio_jd6_sticky	2	R/W	0'h	Sticky Control for Jack Detect 6 0'b: Disable 1'b: Enable
inv_gpio_jd6	1	R/W	0'h	GPIO Jack Detection 6 Status Polarity 0'b: Normal 1'b: Output Invert
Reserved	0	R	0'h	Reserved

9.115. MX-00B9h: IRQ Control 3

Default: 0000'h

Table 197. MX-00B9h: IRQ Control 3

DSP Address: 0x1800_C172 I2C Address: 0x00B9				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_irq_pitch_det	15	R/W	0'h	IRQ output source configure of Pitch Detect Flag status 0'b: Bypass 1'b: Normal
en_tridsp_pitch_det	14	R/W	0'h	Trigger HIFI3 DSP output source configure of Pitch Detect Flag status 0'b: Bypass 1'b: Normal
en_triminidsp_pitch_det	13	R/W	0'h	Trigger Mini DSP output source configure of Pitch Detect Flag status 0'b: Disable 1'b: Enable
en_pitch_det_sticky	12	R/W	0'h	Sticky Control for Pitch Detect Flag 0'b: Disable 1'b: Enable
inv_vad_fg_hold	11	R/W	0'h	Pitch Detect Flag Status Polarity 0'b: Normal 1'b: Output Invert
en_irq_micbias1_ovcd	10	R/W	0'h	IRQ output source configure of MICBIAS1 over current status 0'b: Bypass 1'b: Normal
en_tridsp_micbias1_ovcd	9	R/W	0'h	Trigger HIFI3 DSP output source configure of MICBIAS over current status 0'b: Bypass 1'b: Normal

DSP Address: 0x1800_C172 I2C Address: 0x00B9				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_triminidsp_micbias1_ovcd	8	R/W	0'h	Trigger Mini DSP output source configure of MICBIAS over current status 0'b: Disable 1'b: Enable
en_micbias1_ovcd_sticky	7	R/W	0'h	Sticky Control for MICBIAS1 Over Current 0'b: Disable 1'b: Enable
inv_micbias1_ovcd	6	R/W	0'h	MICBIAS1 over current status polarity 0'b: Normal 1'b: Output Invert
en_irq_inline_cmd_fg	5	R/W	0'h	IRQ output source configure of Inline Command Flag 0'b: Bypass 1'b: Normal
en_tridsp_inline_cmd_fg	4	R/W	0'h	Trigger HIFI3 DSP output source configure of Inline Command Flag 0'b: Bypass 1'b: Normal
en_triminidsp_inline_cmd_fg	3	R/W	0'h	Trigger Mini DSP output source configure of Inline Command Flag 0'b: Disable 1'b: Enable
en_inline_cmd_fg_sticky	2	R/W	0'h	Sticky Control for Inline Command Flag 0'b: Disable 1'b: Enable
inv_inline_cmd_fg	1	R/W	0'h	Inline Command Flag Polarity 0'b: Normal 1'b: Output Invert
Reserved	0	R	0'h	Reserved

9.116. MX-00BBh: IRQ Control 4

Default: 0000'h

Table 198. MX-00BBh: IRQ Control 4

DSP Address: 0x1800_C176 I2C Address: 0x00BB				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:14	R	0'h	Reserved
en_irq_long_press	5	R/W	0'h	IRQ output source configure of Long Press Detection 0'b: Bypass 1'b: Normal
en_tridsp_long_press	4	R/W	0'h	Trigger HIFI3 DSP output source configure of Long Press 0'b: Bypass 1'b: Normal
en_triminidsp_long_press	3	R/W	0'h	Trigger Mini DSP output source configure of Long Press 0'b: Bypass 1'b: Normal

DSP Address: 0x1800_C176 I2C Address: 0x00BB				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_long_press_sticky	2	R/W	0'h	Sticky Control for Long Press Detection 0'b: Disable 1'b: Enable
inv_long_press	1	R/W	0'h	Long Press Polarity 0'b: Normal 1'b: Output Invert
Reserved	0	R	0'h	Reserved

9.117. MX-00BDh: IRQ Control 5

Default: 0000'h

Table 199. MX-00BDh: IRQ Control 5

DSP Address: 0x1800_C17A I2C Address: 0x00BD				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_irq_wakeup_click	15	R/W	0'h	IRQ output source configure of Wake up Click Detection 0'b: Bypass 1'b: Normal
en_tridsp_wakeup_click	14	R/W	0'h	Trigger HIFI3 DSP output source configure of Wake up Click Detection 0'b: Bypass 1'b: Normal
en_triminidsp_wakeup_click	13	R/W	0'h	Trigger Mini DSP output source configure of Wake up Click Detection 0'b: Bypass 1'b: Normal
en_wakeup_click_sticky	12	R/W	0'h	Sticky Control for Wake up Click Detection 0'b: Disable 1'b: Enable
inv_wakeup_click	11	R/W	0'h	Wake up Click Detection Polarity 0'b: Normal 1'b: Output Invert
en_irq_hifi3_dsp_watchdog_fg	10	R/W	0'h	IRQ output source configure of HIFI3 DSP Watch Dog Flag 0'b: Bypass 1'b: Normal
en_tri_hifi3_dsp_watchdog_fg	9	R/W	0'h	Trigger HIFI3 DSP output source configure of DSP Watch Dog Flag 0'b: Bypass 1'b: Normal
Reserved	8	R	0'h	Reserved
en_hifi3_dsp_watchdog_fg_sticky	7	R/W	0'h	Sticky Control for HIFI3 DSP Watch Dog Flag 0'b: Disable 1'b: Enable
inv_hifi3_dsp_watchdog_fg	6	R/W	0'h	HIFI3 DSP Watch Dog Flag Polarity 0'b: Normal 1'b: Output Invert

DSP Address: 0x1800_C17A I2C Address: 0x00BD				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_irq_mini_dsp_watchdog_fg	5	R/W	0'h	IRQ output source configure of Mini DSP Watch Dog Flag 0'b: Bypass 1'b: Normal
Reserved	4	R	0'h	Reserved
en_tri_mini_dsp_watchdog_fg	3	R/W	0'h	Trigger Mini DSP output source configure of DSP Watch Dog Flag 0'b: Bypass 1'b: Normal
en_mini_dsp_watchdog_fg_sticky	2	R/W	0'h	Sticky Control for Mini DSP Watch Dog Flag 0'b: Disable 1'b: Enable
inv_mini_dsp_watchdog_fg	1	R/W	0'h	Mini DSP Watch Dog Flag Polarity 0'b: Normal 1'b: Output Invert
Reserved	0	R	0'h	Reserved

9.118. MX-00BEh: IRQ Control 6

Default: 0000'h

Table 200. MX-00BEh: IRQ Control 6

DSP Address: 0x1800_C17C I2C Address: 0x00BE				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_irq_crc_error_fg	15	R/W	0'h	IRQ output source configure of CRC Error Flag 0'b: Bypass 1'b: Normal
reserved	14:13	R	0'h	Reserved
en_crc_error_fg_sticky	12	R/W	0'h	Sticky Control for CRC Error Flag 0'b: Disable 1'b: Enable
inv_crc_error_fg	11	R/W	0'h	CRC Error Flag Polarity 0'b: Normal 1'b: Output Invert
en_irq_jd_done	10	R/W	0'h	IRQ output source configure of Jack and Type Detection Done 0'b: Bypass 1'b: Normal
en_tridsp_jd_done	9	R/W	0'h	Trigger HIFI3 DSP output source configure of Jack and Type Detection Done 0'b: Bypass 1'b: Normal
en_triminidsp_jd_done	8	R/W	0'h	Trigger Mini DSP output source configure of Jack and Type Detection Done 0'b: Bypass 1'b: Normal

DSP Address: 0x1800_C17C I2C Address: 0x00BE				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_jd_done_sticky	7	R/W	0'h	Sticky Control for Jack and Type Detection Done 0'b: Disable 1'b: Enable
inv_jd_done	6	R/W	0'h	JD Done Polarity 0'b: Normal 1'b: Output Invert
reserved	5:0	R	0'h	Reserved

9.119. MX-00BFh: IRQ Control 7

Default: 0000'h

Table 201. MX-00BFh: IRQ Control 7

DSP Address: 0x1800_C17E I2C Address: 0x00BF				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
En_irq2_gpio_jd1	15	R/W	0'h	IRQ2 output source configure of GPIO JD1 0'b: Bypass 1'b: Normal
En_irq2_gpio_jd2	14	R/W	0'h	IRQ2 output source configure of GPIO JD2 0'b: Bypass 1'b: Normal
En_irq2_gpio_jd3	13	R/W	0'h	IRQ2 output source configure of GPIO JD3 0'b: Bypass 1'b: Normal
En_irq2_gpio_jd4	12	R/W	0'h	IRQ2 output source configure of GPIO JD4 0'b: Bypass 1'b: Normal
En_irq2_gpio_jd5	11	R/W	0'h	IRQ2 output source configure of GPIO JD5 0'b: Bypass 1'b: Normal
En_irq2_gpio_jd6	10	R/W	0'h	IRQ2 output source configure of GPIO JD6 0'b: Bypass 1'b: Normal
Reg_hifi3_dsp_irq	9	R/W	0'h	Manual interrupt control bit to HIFI-3 DSP
Reg_mini_dsp_irq	8	R/W	0'h	Manual interrupt control bit to HIFI-Mini DSP
en_irq_hifi3_to_host	7	R/W	0'h	IRQ output source configure of HIFI-3 to HOST Interrupt 0'b: Bypass 1'b: Normal
en_hifi3_to_host_sticky	6	R/W	0'h	Sticky Control for HIFI-3 to HOST Interrupt 0'b: Disable 1'b: Enable
inv_hifi3_to_host	5	R/W	0'h	HIFI-3 to HOST Interrupt Polarity 0'b: Normal 1'b: Output Invert

DSP Address: 0x1800_C17E I2C Address: 0x00BF				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_irq_mini_to_host	4	R/W	0'h	IRQ output source configure of MINI to HOST Interrupt 0'b: Bypass 1'b: Normal
en_mini_to_host_sticky	3	R/W	0'h	Sticky Control for MINI to HOST Interrupt 0'b: Disable 1'b: Enable
inv_mini_to_host	2	R/W	0'h	MINI to HOST Interrupt Polarity 0'b: Normal 1'b: Output Invert
Reserved	1:0	R	0'h	Reserved

9.120. MX-00C0h: Multi-Function Pin Control 1

Default: 2008'h

Table 202. MX-00C0h: Multi-Function Pin Control 1

DSP Address: 0x1800_C180 I2C Address: 0x00C0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_gpio1_type	15	R/W	0'h	GPIO1 Pin Select 0'b: GPIO1 1'b: IRQ1 output
sel_gpio14_15_type	14	R/W	0'h	GPIO14/15 Pin Select 0'b: GPIO function GPIO14 GPIO15 1'b: I2S4 GPIO14 => DACDAT4 or Master_SCL3 GPIO15 => ADCDAT4 or Master_SDA3
Sel_gpio2_type	13	R/W	1'h	GPIO2 Pin Control 0'b: GPIO2 1'b: JTRST or SPI_SCL_Flash or DMIC1_SCL
Sel_gpio3_type	12	R/W	0'h	GPIO3 Pin Control 0'b: GPIO3 1'b: DMIC2_SCL
Sel_gpio4_type	11	R/W	0'h	GPIO4 Pin Control 0'b: GPIO4 1'b: DMIC2_SCL or DACDAT5 or PDM_SCL2
Sel_gpio5_type	10	R/W	0'h	GPIO5 Pin Control 0'b: GPIO5 1'b: DMIC3_SCL or ADCDAT5 or PDM_SDA2
Sel_gpio7_type	9:8	R/W	0'h	GPIO7 Pin Control 00'b: GPIO7 01'b: PDM1_DAT or LRCK5 10'b: DMIC4_SCL 11'b: Reserved

DSP Address: 0x1800_C180 I2C Address: 0x00C0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_gpio_i2s3	7	R/W	0'h	GPIO8/9/10/11 Pin Control 0'b: GPIO8/9/10/11 1'b: GPIO8/9/10/11 Pre-Type
Sel_gpio4_pre_type	6:5	R/W	0'h	GPIO4 Type Pre-Control 00'b: GPIO4 as DMIC2_SCL 01'b: GPIO4 as I2S5 – DACDAT5 10'b: GPIO4 as PDM_SCL2 11'b: GPIO4 as IRQ2
sel_gpio12_13_type	4	R/W	0'h	GPIO12/13 Pin Select 0'b: GPIO function GPIO12 GPIO13 1'b: I2S4 GPIO12 => BCLK4 or Master_SCL2 GPIO13 => LRCK4 or Master_SDA2
Sel_gpio16_type	3:2	R/W	2'h	GPIO16 Pin Select 00'b: GPIO16 01'b: DMIC3_SCL 10'b: SPI_SCL_FLASH 11'b: Reserved
Sel_gpio20_spdifin	1	R/W	0'h	GPIO20 Pin Select 0'b: GPIO20 1'b: SPDIFIN
sel_gpio17_18_19_20_type	0	R/W	0'h	GPIO17/18/19/20 Pin Select 0'b: GPIO function GPIO17 GPIO18 GPIO19 GPIO20 1'b: I2S2 GPIO17 => BCLK2 GPIO18 => LRCK2 GPIO19 => DACDAT2 GPIO20 => ADCDAT2

9.121. MX-00C1h: Multi-Function Pin Control 2

Default: 8600'h

Table 203. MX-00C1h: Multi-Function Pin Control 2

DSP Address: 0x1800_C182 I2C Address: 0x00C1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_gpio2_pre_type	15:14	R/W	2'h	GPIO2 Type Pre-Control 00'b: GPIO2 as JTRST 01'b: GPIO2 as DMIC1_SCL 10'b: GPIO2 as SPI_SCL_Flash 11'b: Reserved
Sel_gpio5_pre_type	13:12	R/W	0'h	GPIO5 Type Pre-Control 00'b: GPIO5 as DMIC3_SCL 01'b: GPIO5 as I2S5 – ADCDAT5 10'b: GPIO5 as PDM_SDA2 11'b: GPIO5 as IRQ2
Sel_gpio6_7_pre_type	11	R/W	0'h	GPIO6/7 Type Pre-Control 0'b: GPIO6 as PDM1_SCL GPIO7 as PDM1_SDA 1'b: GPIO6 as I2S5-BCLK5 GPIO7 as I2S5-LRCK5
Sel_master_i2c1_spi_flash	10	R/W	1'h	Master I2C1/SPI Flash Control 0'b: Master_SCL1/Master_SDA1 1'b: SPI_SDI_Flash/SPI_SDO_Flash
Sel_mclk2_type	9:8	R/W	2'h	MCLK2 Pin Control 00'b: MCLK2 input function 01'b: DMIC2_SCL output function 10'b: SPI_CS_Flash 11'b: reserved
Sel_gpio8_9_10_11_pre_type	7:6	R/W	0'h	GPIO8/9/10/11 Type Pre-Control 00'b: I2S3 Function GPIO8 as I2S3-BCLK3 GPIO9 as I2S3-LRCK3 GPIO10 as I2S3-DACDAT3 GPIO11 as I2S3-ADCDAT3 01'b: SPI Master 1 Function GPIO8 as SPI_SCL_M1 GPIO9 as SPI_CS_M1 GPIO10 as SPI_SDI_M1 GPIO11 as SPI_SDO_M1 10'b: UART Function GPIO8 as Tx_UART GPIO9 as Rx_UART GPIO10 as RTS#_UART GPIO11 as CTS#_UART 11'b: Selecti Bonding Function GPIO8 No Function GPIO9 No Function GPIO10 as Sel_bonding0 GPIO11 as Sel_bonding1

DSP Address: 0x1800_C182 I2C Address: 0x00C1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_gpio12_13_pre_type	5	R/W	0'h	GPIO12/13 Type Pre-Control 0'b: GPIO12 as I2S4-BCLK4 GPIO13 as I2S4-LRCK4 1'b: GPIO12 as Master_SCL2 GPIO13 as Master_SDA2
Sel_gpio14_15_pre_type	4	R/W	0'h	GPIO14/15 Type Pre-Control 0'b: GPIO14 as I2S4-DACDAT4 GPIO15 as I2S4-ADCDAT4 1'b: GPIO14 as Master_SCL3 GPIO15 as Master_SDA3
Sel_spi_jtag_gpio	3:2	R/W	0'h	Select SPI or JTAG or GPIO Control 00'b: Slave SPI Function SPI_SCL_S SPI_CS_S SPI_SDI_S SPI_SDO_S 01'b: JTAG Function JTCK JTMS JTDI JTDO 10'b: GPIO Function GPIO25 GPIO26 GPIO27 GPIO28 11'b: Reserved
Sel_gpio6_type	1:0	R/W	0'h	GPIO6 Pin Control 00'b: GPIO6 01'b: PDM1_SCL or BCLK5 10'b: DMIC4_SDA 11'b: Reserved

9.122. MX-00C2h: Multi-Function Pin Control 3

Default: 0000'h

Table 204. MX-00C2h: Multi-Function Pin Control 3

DSP Address: 0x1800_C184 I2C Address: 0x00C2				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_gpio21_type	15:14	R/W	0'h	GPIO21 Type Control 00'b: GPIO21 01'b: GPIO21 as DMIC1_SCL 10'b: GPIO21 as SPI_SCL_M2 11'b: Reserved
Sel_gpio22_type	13:12	R/W	0'h	GPIO22 Type Control 00'b: GPIO22 01'b: GPIO22 as DMIC1_SDA 10'b: GPIO22 as SPI_CS_M2 11'b: Reserved
Sel_gpio23_type	11:10	R/W	0'h	GPIO23 Type Control 00'b: GPIO23 01'b: GPIO23 as DMIC2_SDA 10'b: GPIO23 as SPI_SDI_M2 11'b: Reserved
Sel_gpio24_type	9:8	R/W	0'h	GPIO24 Type Control 00'b: GPIO24 01'b: GPIO24 as DMIC3_SDA 10'b: GPIO24 as SPI_SDO_M2 11'b: Reserved
Reserved	7:0	R	0'h	Reserved

9.123. MX-00C3h: GPIO Control 1

Default: 0000'h

Table 205. MX-00C3h: GPIO Control 1

DSP Address: 0x1800_C186 I2C Address: 0x00C3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
sel_gpio1	14	R/W	0'h	GPIO1 Pin Configuration 0'b: Input 1'b: Output
sel_gpio1_logic	13	R/W	0'h	GPIO1 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio1	12	R/W	0'h	GPIO1 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio2	11	R/W	0'h	GPIO2 Pin Configuration 0'b: Input 1'b: Output

DSP Address: 0x1800_C186 I2C Address: 0x00C3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_gpio2_logic	10	R/W	0'h	GPIO2 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio2	9	R/W	0'h	GPIO2 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio3	8	R/W	0'h	GPIO3 Pin Configuration 0'b: Input 1'b: Output
sel_gpio3_logic	7	R/W	0'h	GPIO3 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio3	6	R/W	0'h	GPIO3 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio4	5	R/W	0'h	GPIO4 Pin Configuration 0'b: Input 1'b: Output
sel_gpio4_logic	4	R/W	0'h	GPIO4 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio4	3	R/W	0'h	GPIO4 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio5	2	R/W	0'h	GPIO5 Pin Configuration 0'b: Input 1'b: Output
sel_gpio5_logic	1	R/W	0'h	GPIO5 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio5	0	R/W	0'h	GPIO5 Pin Polarity 0'b: Normal 1'b: Output Invert

9.124. MX-00C4h: GPIO Control 2

Default: 0000'h

Table 206. MX-00C4h: GPIO Control 2

DSP Address: 0x1800_C188 I2C Address: 0x00C4				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15	R	0'h	Reserved
sel_gpio6	14	R/W	0'h	GPIO6 Pin Configuration 0'b: Input 1'b: Output
sel_gpio6_logic	13	R/W	0'h	GPIO6 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio6	12	R/W	0'h	GPIO6 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio7	11	R/W	0'h	GPIO7 Pin Configuration 0'b: Input 1'b: Output
sel_gpio7_logic	10	R/W	0'h	GPIO7 Output Pin Control 0'b: Drive Low 1'b: Drive High

DSP Address: 0x1800_C188 I2C Address: 0x00C4				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
inv_gpio7	9	R/W	0'h	GPIO7 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio8	8	R/W	0'h	GPIO8 Pin Configuration 0'b: Input 1'b: Output
sel_gpio8_logic	7	R/W	0'h	GPIO8 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio8	6	R/W	0'h	GPIO8 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio9	5	R/W	0'h	GPIO9 Pin Configuration 0'b: Input 1'b: Output
sel_gpio9_logic	4	R/W	0'h	GPIO9 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio9	3	R/W	0'h	GPIO9 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio10	2	R/W	0'h	GPIO10 Pin Configuration 0'b: Input 1'b: Output
sel_gpio10_logic	1	R/W	0'h	GPIO10 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio10	0	R/W	0'h	GPIO10 Pin Polarity 0'b: Normal 1'b: Output Invert

9.125. MX-00C5h: GPIO Control 3

Default: 0000'h

Table 207. MX-00C5h: GPIO Control 3

DSP Address: 0x1800_C18A I2C Address: 0x00C5				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15	R	0'h	Reserved
sel_gpio11	14	R/W	0'h	GPIO11 Pin Configuration 0'b: Input 1'b: Output
sel_gpio11_logic	13	R/W	0'h	GPIO11 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio11	12	R/W	0'h	GPIO11 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio12	11	R/W	0'h	GPIO12 Pin Configuration 0'b: Input 1'b: Output
sel_gpio12_logic	10	R/W	0'h	GPIO12 Output Pin Control 0'b: Drive Low 1'b: Drive High

DSP Address: 0x1800_C18A I2C Address: 0x00C5				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
inv_gpio12	9	R/W	0'h	GPIO12 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio13	8	R/W	0'h	GPIO13 Pin Configuration 0'b: Input 1'b: Output
sel_gpio13_logic	7	R/W	0'h	GPIO13 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio13	6	R/W	0'h	GPIO13 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio14	5	R/W	0'h	GPIO14 Pin Configuration 0'b: Input 1'b: Output
sel_gpio14_logic	4	R/W	0'h	GPIO14 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio14	3	R/W	0'h	GPIO14 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio15	2	R/W	0'h	GPIO15 Pin Configuration 0'b: Input 1'b: Output
sel_gpio15_logic	1	R/W	0'h	GPIO15 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio15	0	R/W	0'h	GPIO15 Pin Polarity 0'b: Normal 1'b: Output Invert

9.126. MX-00C6h: GPIO Control 4

Default: 0000'h

Table 208. MX-00C6h: GPIO Control 4

DSP Address: 0x1800_C18C I2C Address: 0x00C6				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_gpio16	15	R/W	0'h	GPIO16 Pin Configuration 0'b: Input 1'b: Output
sel_gpio16_logic	14	R/W	0'h	GPIO16 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio16	13	R/W	0'h	GPIO16 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio17	12	R/W	0'h	GPIO17 Pin Configuration 0'b: Input 1'b: Output
sel_gpio17_logic	11	R/W	0'h	GPIO17 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio17	10	R/W	0'h	GPIO17 Pin Polarity 0'b: Normal 1'b: Output Invert

DSP Address: 0x1800_C18C I2C Address: 0x00C6				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_gpio18	9	R/W	0'h	GPIO18 Pin Configuration 0'b: Input 1'b: Output
sel_gpio18_logic	8	R/W	0'h	GPIO18 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio18	7	R/W	0'h	GPIO18 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio19	6	R/W	0'h	GPIO19 Pin Configuration 0'b: Input 1'b: Output
sel_gpio19_logic	5	R/W	0'h	GPIO19 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio19	4	R/W	0'h	GPIO19 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio20	3	R/W	0'h	GPIO20 Pin Configuration 0'b: Input 1'b: Output
sel_gpio20_logic	2	R/W	0'h	GPIO20 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio20	1	R/W	0'h	GPIO20 Pin Polarity 0'b: Normal 1'b: Output Invert
reserved	0	R	0'h	Reserved

9.127. MX-00C7h: GPIO Control 5

Default: 0000'h

Table 209. MX-00C7h: GPIO Control 5

DSP Address: 0x1800_C18E I2C Address: 0x00C7				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_gpio21	15	R/W	0'h	GPIO21 Pin Configuration 0'b: Input 1'b: Output
sel_gpio21_logic	14	R/W	0'h	GPIO21 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio21	13	R/W	0'h	GPIO21 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio22	12	R/W	0'h	GPIO22 Pin Configuration 0'b: Input 1'b: Output
sel_gpio22_logic	11	R/W	0'h	GPIO22 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio22	10	R/W	0'h	GPIO22 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio23	9	R/W	0'h	GPIO23 Pin Configuration 0'b: Input 1'b: Output

DSP Address: 0x1800_C18E I2C Address: 0x00C7				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_gpio23_logic	8	R/W	0'h	GPIO23 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio23	7	R/W	0'h	GPIO23 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio24	6	R/W	0'h	GPIO24 Pin Configuration 0'b: Input 1'b: Output
sel_gpio24_logic	5	R/W	0'h	GPIO24 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio24	4	R/W	0'h	GPIO24 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio25	3	R/W	0'h	GPIO25 Pin Configuration 0'b: Input 1'b: Output
sel_gpio25_logic	2	R/W	0'h	GPIO25 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio25	1	R/W	0'h	GPIO25 Pin Polarity 0'b: Normal 1'b: Output Invert
reserved	0	R	0'h	Reserved

9.128. MX-00C8h: GPIO Control 6

Default: 0000'h

Table 210. MX-00C8h: GPIO Control 6

DSP Address: 0x1800_C190 I2C Address: 0x00C8				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sel_gpio26	15	R/W	0'h	GPIO26 Pin Configuration 0'b: Input 1'b: Output
sel_gpio26_logic	14	R/W	0'h	GPIO26 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio26	13	R/W	0'h	GPIO26 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio27	12	R/W	0'h	GPIO27 Pin Configuration 0'b: Input 1'b: Output
sel_gpio27_logic	11	R/W	0'h	GPIO27 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio27	10	R/W	0'h	GPIO27 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio28	9	R/W	0'h	GPIO28 Pin Configuration 0'b: Input 1'b: Output
sel_gpio28_logic	8	R/W	0'h	GPIO28 Output Pin Control 0'b: Drive Low 1'b: Drive High

DSP Address: 0x1800_C190 I2C Address: 0x00C8				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
inv_gpio28	7	R/W	0'h	GPIO28 Pin Polarity 0'b: Normal 1'b: Output Invert
reserved	6:0	R	0'h	Reserved

9.129. MX-00C9h: GPIO Status 1

Default: 0000'h

Table 211. MX-00C9h: GPIO Status 1

DSP Address: 0x1800_C192 I2C Address: 0x00C9				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sta_gpio15	15	R	0'h	GPIO15 Pin Status 0'b: Low 1'b: High
sta_gpio14	14	R	0'h	GPIO14 Pin Status 0'b: Low 1'b: High
sta_gpio13	13	R	0'h	GPIO13 Pin Status 0'b: Low 1'b: High
sta_gpio12	12	R	0'h	GPIO12 Pin Status 0'b: Low 1'b: High
sta_gpio11	11	R	0'h	GPIO11 Pin Status 0'b: Low 1'b: High
sta_gpio10	10	R	0'h	GPIO10 Pin Status 0'b: Low 1'b: High
sta_gpio9	9	R	0'h	GPIO9 Pin Status 0'b: Low 1'b: High
sta_gpio8	8	R	0'h	GPIO8 Pin Status 0'b: Low 1'b: High
sta_gpio7	7	R	0'h	GPIO7 Pin Status 0'b: Low 1'b: High
sta_gpio6	6	R	0'h	GPIO6 Pin Status 0'b: Low 1'b: High
sta_gpio5	5	R	0'h	GPIO5 Pin Status 0'b: Low 1'b: High

DSP Address: 0x1800_C192 I2C Address: 0x00C9				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sta_gpio4	4	R	0'h	GPIO4 Pin Status 0'b: Low 1'b: High
sta_gpio3	3	R	0'h	GPIO3 Pin Status 0'b: Low 1'b: High
sta_gpio2	2	R	0'h	GPIO2 Pin Status 0'b: Low 1'b: High
sta_gpio1	1	R	0'h	GPIO1 Pin Status 0'b: Low 1'b: High
sta_gpio16	0	R	0'h	GPIO16 Pin Status 0'b: Low 1'b: High

9.130. MX-00CAh: GPIO Status 2

Default: 0000'h

Table 212. MX-00CAh: GPIO Status 2

DSP Address: 0x1800_C194 I2C Address: 0x00CA				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sta_gpio17	15	R	0'h	GPIO17 Pin Status 0'b: Low 1'b: High
sta_gpio18	14	R	0'h	GPIO18 Pin Status 0'b: Low 1'b: High
sta_gpio19	13	R	0'h	GPIO19 Pin Status 0'b: Low 1'b: High
sta_gpio20	12	R	0'h	GPIO20 Pin Status 0'b: Low 1'b: High
sta_gpio21	11	R	0'h	GPIO21 Pin Status 0'b: Low 1'b: High
sta_gpio22	10	R	0'h	GPIO22 Pin Status 0'b: Low 1'b: High
sta_gpio23	9	R	0'h	GPIO23 Pin Status 0'b: Low 1'b: High

DSP Address: 0x1800_C194 I2C Address: 0x00CA				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sta_gpio24	8	R	0'h	GPIO24 Pin Status 0'b: Low 1'b: High
sta_gpio25	7	R	0'h	GPIO25 Pin Status 0'b: Low 1'b: High
sta_gpio26	6	R	0'h	GPIO26 Pin Status 0'b: Low 1'b: High
sta_gpio27	5	R	0'h	GPIO27 Pin Status 0'b: Low 1'b: High
sta_gpio28	4	R	0'h	GPIO28 Pin Status 0'b: Low 1'b: High
Reserved	3:0	R	0'h	Reserved

9.131. MX-00CFh: Long Press Detection Control

Default: 0300'h

Table 213. MX-00CFh: Long Press Detection Control

DSP Address: 0x1800_C19E I2C Address: 0x00CF				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
En_press_det	15	R/W	0'h	Enable long press behavior detection control 0'b: Disable 1'b: Enable
Sel_gpio16_edge	14	R/W	0'h	GPIO16 Input Pin edge trigger control 0'b: Rising edge trigger 1'b: Falling edge trigger
reserved	13:12	R	0'h	Reserved

DSP Address: 0x1800_C19E I2C Address: 0x00CF				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_press_time	11:8	R/W	3'h	Set long press time 4'h0 : Press time=0.5 s 4'h1 : Press time= 1 s 4'h2 : Press time= 2 s 4'h3 : Press time= 3 s 4'h4 : Press time= 4 s 4'h5 : Press time= 5 s 4'h6 : Press time= 6 s 4'h7 : Press time= 7 s 4'h8 : Press time= 8 s 4'h9 : Press time= 9 s 4'hA : Press time= 10 s 4'hB : Press time= 11 s 4'hC : Press time= 12 s 4'hD : Press time= 13 s 4'hE : Press time= 14 s 4'hF : Press time= 15 s
reserved	7:0	R	0'h	Reserved

9.132. MX-00D0h: Stereo1 ADC Wind Filter Control 1

Default: B320'h

Table 214. MX-00D0h: Stereo1 ADC Wind Filter Control 1

DSP Address: 0x1800_C1A0 I2C Address: 0x00D0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_stereo1_wind_filter	15	R/W	1'h	Enable Stereo1 ADC Filter 0'b : Disable 1'b : Enable
adj_hpf_coef_l_sel_stereo1	14:12	R/W	3'h	Left channel coefficient coarse select for Stereo1 Filter (If fs = 48kHz) 000'b : fc = 120.3~12000Hz 001'b : fc = 59.9~4915.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 14.9~1017Hz 100'b : fc = 7.46~492.7Hz 101'b : Reserved 110'b : Reserved 111'b : Reserved
Reserved	11	R	0'h	Reserved

DSP Address: 0x1800_C1A0 I2C Address: 0x00D0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
adj_hpf_coef_r_sel_stereo1	10:8	R/W	3'h	Right channel coefficient coarse select for Stereo1 Filter (If fs = 48kHz) 000'b : fc = 120.3~12000Hz 001'b : fc = 59.9~4915.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 14.9~1017Hz 100'b : fc = 7.46~492.7Hz 101'b : Reserved 110'b : Reserved 111'b : Reserved
reserved	7:0	R	20'h	Reserved

9.133. MX-00D1h: Stereo1 ADC Wind Filter Control 2

Default: 0000'h

Table 215. MX-00D1h: Stereo1 ADC Wind Filter Control 2

DSP Address: 0x1800_C1A2 I2C Address: 0x00D1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:14	R	0'h	Reserved
adj_hpf_coef_l_num_stereo1	13:8	R/W	0'h	Left channel coefficient fine select for Stereo1 Filter (0~63)
reserved	7:6	R	0'h	Reserved
adj_hpf_coef_r_num_stereo1	5:0	R/W	0'h	Right channel coefficient fine select for Stereo1 Filter (0~63)

9.134. MX-00D2h: MONO ADC Wind Filter Control 1

Default: B320'h

Table 216. MX-00D2h: MONO ADC Wind Filter Control 1

DSP Address: 0x1800_C1A4 I2C Address: 0x00D2				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_mono_wind_filter	15	R/W	1'h	Enable MONO ADC Filter 0'b : Disable 1'b : Enable

DSP Address: 0x1800_C1A4 I2C Address: 0x00D2				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
adj_hpf_coef_l_sel_mono	14:12	R/W	3'h	Left channel coefficient coarse select for MONO Filter (If fs = 48kHz) 000'b : fc = 120.3~12000Hz 001'b : fc = 59.9~4915.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 14.9~1017Hz 100'b : fc = 7.46~492.7Hz 101'b : Reserved 110'b : Reserved 111'b : Reserved
Reserved	11	R	0'h	Reserved
adj_hpf_coef_r_sel_mono	10:8	R/W	3'h	Right channel coefficient coarse select for MONO Filter (If fs = 48kHz) 000'b : fc = 120.3~12000Hz 001'b : fc = 59.9~4915.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 14.9~1017Hz 100'b : fc = 7.46~492.7Hz 101'b : Reserved 110'b : Reserved 111'b : Reserved
reserved	7:0	R	20'h	Reserved

9.135. MX-00D3h: MONO ADC Wind Filter Control 2

Default: 0000'h

Table 217. MX-00D3h: MONO ADC Wind Filter Control 2

DSP Address: 0x1800_C1A6 I2C Address: 0x00D3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:14	R	0'h	Reserved
adj_hpf_coef_l_num_mono	13:8	R/W	0'h	Left channel coefficient fine select for Mono Filter (0~63)
Reserved	7:6	R	0'h	Reserved
adj_hpf_coef_r_num_mono	5:0	R/W	0'h	Right channel coefficient fine select for Mono Filter (0~63)

9.136. MX-00D4h: Stereo2 ADC Wind Filter Control 1

Default: B320'h

Table 218. MX-00D4h: Stereo2 ADC Wind Filter Control 1

DSP Address: 0x1800_C1A8 **I2C Address: 0x00D4**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_stereo2_wind_filter	15	R/W	1'h	Enable Stereo2 ADC Filter 0'b : Disable 1'b : Enable
adj_hpf_coef_l_sel_stereo2	14:12	R/W	3'h	Left channel coefficient coarse select for Stereo2 Filter (If fs = 48kHz) 000'b : fc = 120.3~12000Hz 001'b : fc = 59.9~4915.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 14.9~1017Hz 100'b : fc = 7.46~492.7Hz 101'b : Reserved 110'b : Reserved 111'b : Reserved
Reserved	11	R	0'h	Reserved
adj_hpf_coef_r_sel_stereo2	10:8	R/W	3'h	Right channel coefficient coarse select for Stereo2 Filter (If fs = 48kHz) 000'b : fc = 120.3~12000Hz 001'b : fc = 59.9~4915.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 14.9~1017Hz 100'b : fc = 7.46~492.7Hz 101'b : Reserved 110'b : Reserved 111'b : Reserved
reserved	7:0	R	20'h	Reserved

9.137. MX-00D5h: Stereo2 ADC Wind Filter Control 2

Default: 0000'h

Table 219. MX-00D5h: Stereo2 ADC Wind Filter Control 2

DSP Address: 0x1800_C1AA **I2C Address: 0x00D5**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:14	R	0'h	Reserved
adj_hpf_coef_l_num_stereo2	13:8	R/W	0'h	Left channel coefficient fine select for Stereo2 Filter (0~63)
Reserved	7:6	R	0'h	Reserved
adj_hpf_coef_r_num_stereo2	5:0	R/W	0'h	Right channel coefficient fine select for Stereo2 Filter (0~63)

9.138. MX-00D6h: Stereo3 ADC Wind Filter Control 1

Default: B320'h

Table 220. MX-00D6h: Stereo3 ADC Wind Filter Control 1

DSP Address: 0x1800_C1AC **I2C Address: 0x00D6**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
en_stereo3_wind_filter	15	R/W	1'h	Enable Stereo3 ADC Filter 0'b : Disable 1'b : Enable
adj_hpf_coef_l_sel_stereo3	14:12	R/W	3'h	Left channel coefficient coarse select for Stereo3 Filter (If fs = 48kHz) 000'b : fc = 120.3~12000Hz 001'b : fc = 59.9~4915.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 14.9~1017Hz 100'b : fc = 7.46~492.7Hz 101'b : Reserved 110'b : Reserved 111'b : Reserved
Reserved	11	R	0'h	Reserved
adj_hpf_coef_r_sel_stereo3	10:8	R/W	3'h	Right channel coefficient coarse select for Stereo3 Filter (If fs = 48kHz) 000'b : fc = 120.3~12000Hz 001'b : fc = 59.9~4915.9Hz 010'b : fc = 29.8~2168Hz 011'b : fc = 14.9~1017Hz 100'b : fc = 7.46~492.7Hz 101'b : Reserved 110'b : Reserved 111'b : Reserved
reserved	7:0	R	20'h	Reserved

9.139. MX-00D7h: Stereo3 ADC Wind Filter Control 2

Default: 0000'h

Table 221. MX-00D7h: Stereo3 ADC Wind Filter Control 2

DSP Address: 0x1800_C1AE **I2C Address: 0x00D7**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:14	R	0'h	Reserved
adj_hpf_coef_l_num_stereo3	13:8	R/W	0'h	Left channel coefficient fine select for Stereo3 Filter (0~63)
Reserved	7:6	R	0'h	Reserved
adj_hpf_coef_r_num_stereo3	5:0	R/W	0'h	Right channel coefficient fine select for Stereo3 Filter (0~63)

9.140. MX-00DBh: 3 Push Buttons Detect Control 1

Default: 0008'h

Table 222. MX-00DBh: 3 Push Buttons Detect Control 1

DSP Address: 0x1800_C1B6 **I2C Address: 0x00DB**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sta_one_up_button	15	R	0'h	Status of One Click Command for Up Button Write "1" to clear it
sta_double_up_button	14	R	0'h	Status of Double Click Command for Up Button Write "1" to clear it
sta_hold_up_button	13	R	0'h	Status of Hold Command for Up Button Write "1" to clear it
sta_one_center_button	12	R	0'h	Status of One Click Command for Center Button Write "1" to clear it
sta_double_center_button	11	R	0'h	Status of Double Click Command for Center Button Write "1" to clear it
sta_hold_center_button	10	R	0'h	Status of Hold Command for Center Button Write "1" to clear it
sta_one_down_button	9	R	0'h	Status of One Click Command for Down Button Write "1" to clear it
sta_double_down_button	8	R	0'h	Status of Double Click Command for Down Button Write "1" to clear it
sta_hold_down_button	7	R	0'h	Status of Hold Command for Down Button Write "1" to clear it
reserved	6:5	R	0'h	Reserved
irq_inline	4	R	0'h	Irq triggered by inline command button
Sel_clk_mic	3:2	R/W	2'h	Select InLine Command Debounce Clock 00'b: 1MHz/2^{13} (8.192ms) 01'b: 1MHz/2^{14} (16.38ms) 10'b: 1MHz/2^{15} (32.7ms) 11'b: 1MHz/2^{16} (65.5ms)
Sel_clk_tw	1:0	R/W	0'h	Select Inline command time window clock 00'b: 1MHz/2^{13} (8.192ms) 01'b: 1MHz/2^{12} (4.096ms) 10'b: 1MHz/2^{11} (2.048ms) 11'b: 1MHz/2^{10} (1.024ms)

9.141. MX-00DCh: 3 Push Buttons Detect Control 2

Default: 00C0'h

Table 223. MX-00DCh: 3 Push Buttons Detect Control 2

DSP Address: 0x1800_C1B8 I2C Address: 0x00DC				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
En_3button_det	15	R/W	0'h	Enable 3 Buttons Detection 0'b: Disable 1'b: Enable
Reserved	14:0	R	C0'h	Reserved

9.142. MX-00DDh: Push Buttons Detect Control

Default: 6724'h

Table 224. MX-00DDh: Push Buttons Detect Control

DSP Address: 0x1800_C1BA I2C Address: 0x00DD				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_vth1_md	15:12	R/W	6'h	MIC IN Detection Low Voltage Threshold Control 0'h : 25mV 1'h : 30mV 2'h : 40mV 3'h : 60mV 4'h : 85mV 5'h : 90mV 6'h : 100mV 7'h : 110mV 8'h : 120mV 9'h : 125mV A'h : 130mV B'h : 140mV C'h : 160mV D'h : 180mV E'h : 200mV F'h : 215mV

DSP Address: 0x1800_C1BA I2C Address: 0x00DD				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_vth2_md	11:8	R/W	7'h	MIC in detection Level 2 voltage threshold control 0'h : 185mV 1'h : 190mV 2'h : 195mV 3'h : 200mV 4'h : 205mV 5'h : 210mV 6'h : 215mV 7'h : 220mV 8'h : 225mV 9'h : 230mV A'h : 235mV B'h : 240mV C'h : 245mV D'h : 250mV E'h : 255mV F'h : 260mV
Sel_vth3_md	7:4	R/W	2'h	MIC in detection Level 3 voltage threshold control 0'h : 325mV 1'h : 335mV 2'h : 345mV 3'h : 355mV 4'h : 365mV 5'h : 375mV 6'h : 395mV 7'h : 415mV 8'h : 425mV 9'h : 435mV A'h : 445mV B'h : 465mV C'h : 475mV D'h : 485mV E'h : 505mV F'h : 515mV

DSP Address: 0x1800_C1BA I2C Address: 0x00DD				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_vth4_md	3:0	R/W	4'h	MIC in detection Level 4 voltage threshold control 0'h : 630mV 1'h : 640mV 2'h : 700mV 3'h : 740mV 4'h : 780mV 5'h : 820mV 6'h : 860mV 7'h : 900mV 8'h : 1135mV 9'h : 1190mV A'h : 1240mV B'h : 1300mV C'h : 1350mV D'h : 1400mV E'h : 1460mV F'h : 1515mV

9.143. MX-00DEh: 3 Push Buttons Detect Control 3

Default: 3131'h

Table 225. MX-00DEh: 3 Push Buttons Detect Control 3

DSP Address: 0x1800_C1BC I2C Address: 0x00DE				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
in_hold_det_window	14:8	R/W	31'h	In-line command (microphone button) hold window control If Reg00DB[1:0]=00_(1/1MHz)* 2^{13} *n If Reg00DB[1:0]=01_(1/1MHz)* 2^{12} *n If Reg00DB[1:0]=10_(1/1MHz)* 2^{11} *n If Reg00DB[1:0]=11_(1/1MHz)* 2^{10} *n (n=0~127)
Reserved	7	R	0'h	Reserved
in_click_det_window	6:0	R/W	31'h	In-line command (microphone button) click window control If Reg00DB[1:0]=00_(1/1MHz)* 2^{13} *n If Reg00DB[1:0]=01_(1/1MHz)* 2^{12} *n If Reg00DB[1:0]=10_(1/1MHz)* 2^{11} *n If Reg00DB[1:0]=11_(1/1MHz)* 2^{10} *n (n=0~127)

9.144. MX-00DFh: 4 Push Buttons Detect Control 1

Default: 0008'h

Table 226. MX-00DFh: 4 Push Buttons Detect Control 1

DSP Address: 0x1800_C1BE **I2C Address: 0x00DF**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
sta_one_button1	15	R	0'h	Status of One Click Command for Button1 Write "1" to clear it
sta_double_button1	14	R	0'h	Status of Double Click Command for Button1 Write "1" to clear it
sta_hold_button1	13	R	0'h	Status of Hold Command for Button1 Write "1" to clear it
sta_one_button2	12	R	0'h	Status of One Click Command for Button2 Write "1" to clear it
sta_double_button2	11	R	0'h	Status of Double Click Command for Button2 Write "1" to clear it
sta_hold_button2	10	R	0'h	Status of Hold Command for Button2 Write "1" to clear it
sta_one_button3	9	R	0'h	Status of One Click Command for Button3 Write "1" to clear it
sta_double_button3	8	R	0'h	Status of Double Click Command for Button3 Write "1" to clear it
sta_hold_button3	7	R	0'h	Status of Hold Command for Button3 Write "1" to clear it
sta_one_button4	6	R	0'h	Status of One Click Command for Button4 Write "1" to clear it
sta_double_button4	5	R	0'h	Status of Double Click Command for Button4 Write "1" to clear it
sta_hold_button4	4	R	0'h	Status of Hold Command for Button4 Write "1" to clear it
Sel_4button_clk_mic	3:2	R/W	2'h	Select 4 Buttons InLine Command Debounce Clock 00'b: 1MHz/2^{13} (8.192ms) 01'b: 1MHz/2^{14} (16.38ms) 10'b: 1MHz/2^{15} (32.7ms) 11'b: 1MHz/2^{16} (65.5ms)
Sel_4button_clk_tw	1:0	R/W	0'h	Select 4 Buttons Inline command time window clock 00'b: 1MHz/2^{13} (8.192ms) 01'b: 1MHz/2^{12} (4.096ms) 10'b: 1MHz/2^{11} (2.048ms) 11'b: 1MHz/2^{10} (1.024ms)

9.145. MX-00E0h: 4 Push Buttons Detect Control 2

Default: 4000'h

Table 227. MX-00E0h: 4 Push Buttons Detect Control 2

DSP Address: 0x1800_C1C0 I2C Address: 0x00E0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
En_4button_inline	15	R/W	0'h	Enable 4 buttons InLine Command 0'b: Disable 1'b: Enable
Reserved	14:0	R	4000'h	Reserved

9.146. MX-00E1h: 4 Push Buttons Detect Control 3

Default: 3131'h

Table 228. MX-00E1h: 4 Push Buttons Detect Control 3

DSP Address: 0x1800_C1C2 I2C Address: 0x00E1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
in_4button_hold_det_window	14:8	R/W	31'h	4 Buttons In-line command (microphone button) hold window control If Reg00DF[1:0]=00_(1/1MHz)* 2^{13} *n If Reg00DF[1:0]=01_(1/1MHz)* 2^{12} *n If Reg00DF[1:0]=10_(1/1MHz)* 2^{11} *n If Reg00DF[1:0]=11_(1/1MHz)* 2^{10} *n (n=0~127)
Reserved	7	R	0'h	Reserved
in_4button_click_det_window	6:0	R/W	31'h	4 Buttons In-line command (microphone button) click window control If Reg00DF[1:0]=00_(1/1MHz)* 2^{13} *n If Reg00DF[1:0]=01_(1/1MHz)* 2^{12} *n If Reg00DF[1:0]=10_(1/1MHz)* 2^{11} *n If Reg00DF[1:0]=11_(1/1MHz)* 2^{10} *n (n=0~127)

9.147. MX-00E1h: 4 Push Buttons Detect Control 3

Default: 3131'h

Table 229. MX-00E1h: 4 Push Buttons Detect Control 3

DSP Address: 0x1800_C1C2 I2C Address: 0x00E1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved

DSP Address: 0x1800_C1C2 I2C Address: 0x00E1				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
in_4button_hold_det_window	14:8	R/W	31'h	4 Buttons In-line command (microphone button) hold window control If Reg00DF[1:0]=00_(1/1MHz)* 2^{13} *n If Reg00DF[1:0]=01_(1/1MHz)* 2^{12} *n If Reg00DF[1:0]=10_(1/1MHz)* 2^{11} *n If Reg00DF[1:0]=11_(1/1MHz)* 2^{10} *n (n=0~127)

9.148. MX-00E4h: Power Saving Push Button Detect Control

Default: 402C'h

Table 230. MX-00E4h: Power Saving Push Button Detect Control

DSP Address: 0x1800_C1C8 I2C Address: 0x00E4				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
En_pow_save_inline	15	R/W	0'h	Enable power saving inline command 0'b: Disable 1'b: Enable
Reserved	14:13	R	2'h	Reserved
sta_wakeup_click	12	R	0'h	Status of One Click Button when power save mode Write "1" to clear it
Reserved	11:0	R	02C'h	Reserved

9.149. MX-00FAh: System Clock Enable Control

Default: 0000'h

Table 231. MX-00FAh: System Clock Enable Control

DSP Address: 0x1800_C1F4 I2C Address: 0x00FA				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:1	R	0'h	Reserved
Sys_clk_en_ctrl	0	R/W	0'h	Enable gate mode with System Clock for power saving 0'b: Disable 1'b: Enable

9.150. MX-00FEh: Vender ID

Default: 10EC'h

Table 232. MX-00FEh: Vender ID

DSP Address: 0x1800_C1FC I2C Address: 0x00FE				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
vender_id	15:0	R	10EC'h	Vender ID "10EC"

9.151. MX-0100h: PDM Output Control

Default: C0C0'h

Table 233. MX-0100h: PDM Output Control

DSP Address: 0x1800_C200 I2C Address: 0x0100				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_pdm1_l	15	R/W	1'h	Mute PDM 1 Left channel data 0'b: UnMute 1'b: Mute
mu_pdm1_r	14	R/W	1'h	Mute PDM 1 Right channel data 0'b: UnMute 1'b: Mute
sel_pdm1_l	13:12	R/W	0'h	Select PDM 1 Left channel source 00'b: Stereo_DAC_MIXL 01'b: Mono_DAC_MIXL 10'b: DD_MIXL 11'b: Reserved
sel_pdm1_r	11:10	R/W	0'h	Select PDM 1 Right channel source 00'b: Stereo_DAC_MIXR 01'b: Mono_DAC_MIXR 10'b: DD_MIXR 11'b: Reserved
Swap_pdm1	9	R/W	0'h	Swap PDM1 L/R Channel 0'b: Normal 1'b: Swap
Swap_pdm2	8	R/W	0'h	Swap PDM2 L/R Channel 0'b: Normal 1'b: Swap
mu_pdm2_l	7	R/W	1'h	Mute PDM 2 Left channel data 0'b: UnMute 1'b: Mute
mu_pdm2_r	6	R/W	1'h	Mute PDM 2 Right channel data 0'b: UnMute 1'b: Mute
sel_pdm2_l	5:4	R/W	0'h	Select PDM 2 Left channel source 00'b: Stereo_DAC_MIXL 01'b: Mono_DAC_MIXL 10'b: DD_MIXL 11'b: Reserved
sel_pdm2_r	3:2	R/W	0'h	Select PDM 2 Right channel source 00'b: Stereo_DAC_MIXR 01'b: Mono_DAC_MIXR 10'b: DD_MIXR 11'b: Reserved
Reserved	1:0	R	0'h	Reserved

9.152. MX-011Ah: Sidetone Control

Default: 000B'h

Table 234. MX-011Ah: Sidetone Control

DSP Address: 0x1800_C234 **I2C Address: 0x011A**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sidetone_hpf_fc_sel	15:13	R/W	0'h	Sidetone HPF Fc Selection 000'b: 120Hz 001'b: 239Hz 010'b: 358Hz 011'b: 477Hz 100'b: 597Hz 101'b: 716hz 110'b: 835Hz 111'b: 955Hz
Sidetone_hpf_en	12	R/W	0'h	2nd HPF for Sidetone Path 0'b: Bypass HPF 1'b: Enable HPF
Sel_sidetone_source	11:9	R/W	0'h	Select Sidetone Source 000'b: DMIC_L1 001'b: DMIC_L2 010'b: DMIC_L3 011'b: DMIC_L4 100'b: ADC_1 101'b: ADC_2 110'b: ADC_3 111'b: ADC_4
Reserved	8:7	R	0'h	Reserved
En_sidetone	6	R/W	0'h	Sidetone Enabe Control 0'b: Disable 1'b: Enable
Sidetone_boost_sel	5	R/W	0'h	Sidetone gain control 0'b: 0dB 1'b: +12dB
Sidetone_vol_sel	4:0	R/W	B'h	Sidetone volume in 1.5 dB step❶
For❶	*00h*	*-46.5 dB*		
	1fh	*0 dB*		

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-46.5/-34.5	7	7	-36/-24	14	E	-25.5/-13.5	21	15	-15/-3	28	1C	-4.5/7.5
1	1	-45/-33	8	8	-34.5/-22.5	15	F	-24/-12	22	16	-13.5/-1.5	29	1D	-3/9
2	2	-43.5/-31.5	9	9	-33/-21	16	10	-22.5/-10.5	23	17	-12/0	30	1E	-1.5/10.5
3	3	-42/-30	10	A	-31.5/-19.5	17	11	-21/-9	24	18	-10.5/1.5	31	1F	0/12
4	4	-40.5/-28.5	11	B	-30/-18	18	12	-19.5/-7.5	25	19	-9/3			
5	5	-39/-27	12	C	-28.5/-16.5	19	13	-18/-6	26	1A	-7.5/4.5			
6	6	-37.5/-25.5	13	D	-27/-15	20	14	-16.5/-4.5	27	1B	-6/6			

9.153. MX-011Dh: System Clock Detection

Default: 0000'h

Table 235. MX-011Dh: System Clock Detection

DSP Address: 0x1800_C23A I2C Address: 0x011D				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
En_auto_pd_ana_out	15	R/W	0'h	Enable Auto Power Down Analog Output When SYSCLK Off 0'b: Disable 1'b: Enable (Auto power down HPO, LOUT, MONO when SYSCLK off)
Pow_mclk_wd	14	R/W	0'h	Power Control for SYSCLK detection 0'b: Disable 1'b: Enable
Reserved	13:1	R	0'h	Reserved
Mclk_wd_out	0	R	0'h	MCLK Status 0'b: No Clock 1'b: Clock is exist

9.154. MX-0150h: Stereo1 DAC Path Noise Gate Control

Default: 4131'h

Table 236. MX-0150h: Stereo1 DAC Path Noise Gate Control

DSP Address: 0x1800_C2A0 I2C Address: 0x0150				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Noise_gate_en_stereo1_dac	15	R/W	0'h	Stereo1 DAC Noise Gate Enable Control 0'b: Disable 1'b: Enable
Reserved	14:0	R	4131'h	Reserved

9.155. MX-0151h: MONO2 DAC Lch Path Noise Gate Control

Default: 4131'h

Table 237. MX-0151h: MONO2 DAC Lch Path Noise Gate Control

DSP Address: 0x1800_C2A2 I2C Address: 0x0151				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Noise_gate_en_mono2_dacl	15	R/W	0'h	Mono2 DAC Lch Noise Gate Enable Control 0'b: Disable 1'b: Enable
Reserved	14:0	R	4131'h	Reserved

9.156. MX-0152h: MONO2 DAC Rch Path Noise Gate Control

Default: 4131'h

Table 238. MX-0152h: MONO2 DAC Rch Path Noise Gate Control

DSP Address: 0x1800_C2A4 I2C Address: 0x0152				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Noise_gate_en_mono2_dacr	15	R/W	0'h	Mono2 DAC Rch Noise Gate Enable Control 0'b: Disable 1'b: Enable
Reserved	14:0	R	4131'h	Reserved

9.157. MX-0153h: MONO3 DAC Lch Path Noise Gate Control

Default: 4131'h

Table 239. MX-0153h: MONO3 DAC Lch Path Noise Gate Control

DSP Address: 0x1800_C2A6 I2C Address: 0x0153				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Noise_gate_en_mono3_dacl	15	R/W	0'h	Mono3 DAC Lch Noise Gate Enable Control 0'b: Disable 1'b: Enable
Reserved	14:0	R	4131'h	Reserved

9.158. MX-0154h: MONO3 DAC Rch Path Noise Gate Control

Default: 4131'h

Table 240. MX-0154h: MONO3 DAC Rch Path Noise Gate Control

DSP Address: 0x1800_C2A8 I2C Address: 0x0154				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Noise_gate_en_mono3_dacr	15	R/W	0'h	Mono3 DAC Rch Noise Gate Enable Control 0'b: Disable 1'b: Enable
Reserved	14:0	R	4131'h	Reserved

9.159. MX-0155h: Noise Gate for Output Port

Default: 0000'h

Table 241. MX-0155h: Noise Gate for Output Port

DSP Address: 0x1800_C2AA I2C Address: 0x0155				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
En_noise_gate_hpamp	15	R/W	0'h	Enable Noise Gate Function for HP Amp 0'b: Disable 1'b: Enable
En_noise_gate_lout1	14	R/W	0'h	Enable Noise Gate Function for LOUT1 0'b: Disable 1'b: Enable
En_noise_gate_lout2	13	R/W	0'h	Enable Noise Gate Function for LOUT2 0'b: Disable 1'b: Enable
En_noise_gate_mono	12	R/W	0'h	Enable Noise Gate Function for MONO Amp 0'b: Disable 1'b: Enable
En_noise_gate_pdm1	11	R/W	0'h	Enable Noise Gate Function for PDM1 0'b: Disable 1'b: Enable
En_noise_gate_pdm2	10	R/W	0'h	Enable Noise Gate Function for PDM2 0'b: Disable 1'b: Enable
En_noise_gate_digital_dac1	9	R/W	0'h	Enable Noise Gate Function for Digital DAC1 0'b: Disable 1'b: Enable
En_noise_gate_digital_dac2	8	R/W	0'h	Enable Noise Gate Function for Digital DAC2 0'b: Disable 1'b: Enable
En_noise_gate_i2s1_dataout	7	R/W	0'h	Enable Noise Gate Function for I2S1 Data Output 0'b: Disable 1'b: Enable
En_noise_gate_i2s2_dataout	6	R/W	0'h	Enable Noise Gate Function for I2S2 Data Output 0'b: Disable 1'b: Enable
En_noise_gate_i2s3_dataout	5	R/W	0'h	Enable Noise Gate Function for I2S3 Data Output 0'b: Disable 1'b: Enable
En_noise_gate_i2s4_dataout	4	R/W	0'h	Enable Noise Gate Function for I2S4 Data Output 0'b: Disable 1'b: Enable
En_noise_gate_i2s5_dataout	3	R/W	0'h	Enable Noise Gate Function for I2S5 Data Output 0'b: Disable 1'b: Enable
Reserved	2:0	R	0'h	Reserved

9.160. MX-0160h: ADC EQ Control 1

Default: 6000'h

Table 242. MX-0160h: ADC EQ Control 1

DSP Address: 0x1800_C2C0 I2C Address: 0x0160				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'b	Reserved
ad_eq_param_update	14	R/W	1'h	ADC Path EQ parameter update control 0'b: Disable 1'b: Update
reserved	13:0	R	2000'h	Reserved

9.161. MX-0161h: ADC EQ Control 2

Default: 0000'h

Table 243. MX-0161h: ADC EQ Control 2

DSP Address: 0x1800_C2C2 I2C Address: 0x0161				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ad_eq_hpf1_tpy_l	15	R/W	0'h	ADC_L Path 1st EQ High Pass Filter1 Mode Control (HPF1) 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)
ad_eq_hpf1_tpy_r	14	R/W	0'h	ADC_R Path 1st EQ High Pass Filter1 Mode Control (HPF1) 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)
ad_eq_lpf1_tpy_l	13	R/W	0'h	ADC_L Path 1st EQ Low Pass Filter Mode Control (LPF) 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)
ad_eq_lpf1_tpy_r	12	R/W	0'h	ADC_R Path 1st EQ Low Pass Filter Mode Control (LPF) 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)
ad_eq_lpf1_en	11:10	R/W	0'h	ADC Path 1st EQ Low Pass Filter (LPF) Filter Control. 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel
ad_eq_bpf4_en	9:8	R/W	0'h	ADC Path 2nd EQ Band-4 (BP4) shelving Filter Control 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel

DSP Address: 0x1800_C2C2 I2C Address: 0x0161				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ad_eq_bpf3_en	7:6	R/W	0'h	ADC Path 2nd EQ Band-3 (BP3) shelving Filter Control 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel
ad_eq_bpf2_en	5:4	R/W	0'h	ADC Path 2nd EQ Band-2 (BP2) shelving Filter Control 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel
ad_eq_bpf1_en	3:2	R/W	0'h	ADC Path 2nd EQ Band-1 (BP1) shelving Filter Control 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel
ad_eq_hpf1_en	1:0	R/W	0'h	ADC Path EQ 1st High Pass Filter (HPF1) Control 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel

9.162. MX-0164h: DAC EQ Control 1

Default: C000'h

Table 244. MX-0164h: DAC EQ Control 1

DSP Address: 0x1800_C2C8 I2C Address: 0x0164				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
da_eq_param_update	15	R/W	1'h	DAC Path EQ parameter update control 0'b: Disable 1'b: Enable
Reserved	14:0	R	4000'h	Reserved

9.163. MX-0166h: DAC EQ Control 2

Default: 0000'h

Table 245. MX-0166h: DAC EQ Control 2

DSP Address: 0x1800_C2CC I2C Address: 0x0166				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_lpf1_tpy_r	15	R/W	0'h	DAC Path Right Channel 1st EQ Low Pass Filter Mode Control (LPF1) 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)

DSP Address: 0x1800_C2CC I2C Address: 0x0166				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Da_eq_lpf1_tpy_l	14	R/W	0'h	DAC Path Left Channel 1st EQ Low Pass Filter Mode Control (LPF1) 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)
Da_eq_lpf2_tpy_r	13	R/W	0'h	DAC Path Right Channel 1st EQ Low Pass Filter Mode Control (LPF2) 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)
Da_eq_lpf2_tpy_l	12	R/W	0'h	DAC Path Left Channel 1st EQ Low Pass Filter Mode Control (LPF2) 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)
Da_eq_hpf1_tpy_r	11	R/W	0'h	DAC Path Right Channel 1st EQ High Pass Filter1 Mode Control 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)
Da_eq_hpf1_tpy_l	10	R/W	0'h	DAC Path Left Channel 1st EQ High Pass Filter1 Mode Control 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)
Da_eq_hpf3_tpy_r	9	R/W	0'h	DAC Path Right Channel 1st EQ High Pass Filter3 Mode Control 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)
Da_eq_hpf3_tpy_l	8	R/W	0'h	DAC Path Left Channel 1st EQ High Pass Filter3 Mode Control 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)
Eq_biquad_en	7:6	R/W	0'h	DAC Path 2nd EQ Band-1 (Biquad Type) shelving Filter Control 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel
Da_eq_hpf3_en	5:4	R/W	0'h	DAC Path EQ 1st High Pass Butterworth Filter (HPF3) Control. 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel
Da_eq_hpf2_en	3:2	R/W	0'h	DAC Path EQ 2nd High Pass Filter (HPF2) Control 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel
Da_eq_hpf1_en	1:0	R/W	0'h	DAC Path EQ 1st High Pass Filter (HPF1) Control 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel

9.164. MX-0167h: DAC EQ Control 3

Default: 0000'h

Table 246. MX-0167h: DAC EQ Control 3

DSP Address: 0x1800_C2CE **I2C Address: 0x0167**				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:14	R	0'h	Reserved
Da_eq_lpf2_en	13:12	R/W	0'h	DAC Path 1st EQ Low Pass Filter (LPF2) Filter Control 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel
Da_eq_lpf1_en	11:10	R/W	0'h	DAC Path 1st EQ Low Pass Filter (LPF1) Filter Control 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel
Da_eq_bpf5_en	9:8	R/W	0'h	DAC Path 2nd EQ Band-4 (BP5) shelving Filter Control 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel
Da_eq_bpf4_en	7:6	R/W	0'h	DAC Path 2nd EQ Band-3 (BP4) shelving Filter Control 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel
Da_eq_bpf3_en	5:4	R/W	0'h	DAC Path 2nd EQ Band-2 (BP3) shelving Filter Control 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel
Da_eq_bpf2_en	3:2	R/W	0'h	DAC Path 2nd EQ Band-2 (BP2) shelving Filter Control 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel
Da_eq_bpf1_en	1:0	R/W	0'h	DAC Path 2nd EQ Band-2 (BP1) shelving Filter Control 00'b: Disabled and reset (stereo bypass) 01'b: Enable mono R channel (all band sync) 10'b: Enable mono L channel (all band sync) 11'b: Enable L & R channel

9.165. MX-0170h: I2S Master Mode Clock Control 1

Default: 0000'h

Table 247. MX-0170h: I2S Master Mode Clock Control 1

DSP Address: 0x1800_C2E0 I2C Address: 0x0170				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:14	R	0'h	Reserved
Sel_master_clk_i2s1	13:12	R/W	0'h	I2S1 Master Mode Clock Source Selection 00b: MCLK 01b: PLL1 10b: Fractional Divider 11b: Reserved
Reserved	11	R	0'h	Reserved
Sel_master_i2s_div1	10:8	R/W	0'h	I2S1 Master Mode Divider Selection 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16
Reserved	7:6	R	0'h	Reserved
Sel_master_clk_i2s2	5:4	R/W	0'h	I2S2 Master Mode Clock Source Selection 00b: MCLK 01b: PLL1 10b: Fractional Divider 11b: Reserved
Reserved	3	R	0'h	Reserved
Sel_master_i2s_div2	2:0	R/W	0'h	I2S2 Master Mode Divider Selection 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16

9.166. MX-0171h: I2S Master Mode Clock Control 2

Default: 0000'h

Table 248. MX-0171h: I2S Master Mode Clock Control 2

DSP Address: 0x1800_C2E2 I2C Address: 0x0171				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:14	R	0'h	Reserved
Sel_master_clk_i2s3	13:12	R/W	0'h	I2S3 Master Mode Clock Source Selection 00b: MCLK 01b: PLL1 10b: Fractional Divider 11b: 25MHz RC Clock
Reserved	11	R	0'h	Reserved
Sel_master_i2s_div3	10:8	R/W	0'h	I2S3 Master Mode Divider Selection 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16
Reserved	7:6	R	0'h	Reserved
Sel_master_clk_i2s4	5:4	R/W	0'h	I2S4 Master Mode Clock Source Selection 00b: MCLK 01b: PLL1 10b: Fractional Divider 11b: 25MHz RC Clock
Reserved	3	R	0'h	Reserved
Sel_master_i2s_div4	2:0	R/W	0'h	I2S4 Master Mode Divider Selection 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16

9.167. MX-0172h: I2S Master Mode Clock Control 3

Default: 0000'h

Table 249. MX-0172h: I2S Master Mode Clock Control 3

DSP Address: 0x1800_C2E4 I2C Address: 0x0172				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:14	R	0'h	Reserved
Sel_master_clk_i2s5	13:12	R/W	0'h	I2S5 Master Mode Clock Source Selection 00b: MCLK 01b: PLL1 10b: Fractional Divider 11b: 25MHz RC Clock
Reserved	11	R	0'h	Reserved
Sel_master_i2s_div5	10:8	R/W	0'h	I2S5 Master Mode Divider Selection 000b: ÷ 1 001b: ÷ 2 010b: ÷ 3 011b: ÷ 4 100b: ÷ 6 101b: ÷ 8 110b: ÷ 12 111b: ÷ 16
Reserved	7:0	R	0'h	Reserved

9.168. MX-0173h: I2S Master Mode Clock Control 4

Default: 0002'h

Table 250. MX-0173h: I2S Master Mode Clock Control 4

DSP Address: 0x1800_C2E6 I2C Address: 0x0173				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Frac_mi_i2s1	15:0	R/W	2'h	Parameter of fractional divider (range : 0~65535)

9.169. MX-0174h: I2S Master Mode Clock Control 5

Default: 0001'h

Table 251. MX-0174h: I2S Master Mode Clock Control 5

DSP Address: 0x1800_C2E8 I2C Address: 0x0174				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Frac_mi_ni_i2s1_update	15	R	0'h	Fractional divider parameter update
Frac_ni_i2s1	14:0	R/W	1'h	Parameter of fractional divider (range : 0~65535)

9.170. MX-0175h: I2S Master Mode Clock Control 6

Default: 0002'h

Table 252. MX-0175h: I2S Master Mode Clock Control 6

DSP Address: 0x1800_C2EA I2C Address: 0x0175				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Frac_mi_i2s2	15:0	R/W	2'h	Parameter of fractional divider (range : 0~65535)

9.171. MX-0176h: I2S Master Mode Clock Control 7

Default: 0001'h

Table 253. MX-0176h: I2S Master Mode Clock Control 7

DSP Address: 0x1800_C2EC I2C Address: 0x0176				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Frac_mi_ni_i2s2_update	15	R	0'h	Fractional divider parameter update
Frac_ni_i2s2	14:0	R/W	1'h	Parameter of fractional divider (range : 0~65535)

9.172. MX-0177h: I2S Master Mode Clock Control 8

Default: 0002'h

Table 254. MX-0177h: I2S Master Mode Clock Control 8

DSP Address: 0x1800_C2EE I2C Address: 0x0177				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Frac_mi_i2s3	15:0	R/W	2'h	Parameter of fractional divider (range : 0~65535)

9.173. MX-0178h: I2S Master Mode Clock Control 9

Default: 0001'h

Table 255. MX-0178h: I2S Master Mode Clock Control 9

DSP Address: 0x1800_C2F0 I2C Address: 0x0178				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Frac_mi_ni_i2s3_update	15	R	0'h	Fractional divider parameter update
Frac_ni_i2s3	14:0	R/W	1'h	Parameter of fractional divider (range : 0~65535)

9.174. MX-0179h: I2S Master Mode Clock Control 10

Default: 0002'h

Table 256. MX-0179h: I2S Master Mode Clock Control 10

DSP Address: 0x1800_C2F2 I2C Address: 0x0179				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Frac_mi_i2s4	15:0	R/W	2'h	Parameter of fractional divider (range : 0~65535)

9.175. MX-017Ah: I2S Master Mode Clock Control 11

Default: 0001'h

Table 257. MX-017Ah: I2S Master Mode Clock Control 11

DSP Address: 0x1800_C2F4 I2C Address: 0x017A				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Frac_mi_ni_i2s4_update	15	R	0'h	Fractional divider parameter update
Frac_ni_i2s4	14:0	R/W	1'h	Parameter of fractional divider (range : 0~65535)

9.176. MX-017Bh: I2S Master Mode Clock Control 12

Default: 0002'h

Table 258. MX-017Bh: I2S Master Mode Clock Control 12

DSP Address: 0x1800_C2F6 I2C Address: 0x017B				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Frac_mi_i2s5	15:0	R/W	2'h	Parameter of fractional divider (range : 0~65535)

9.177. MX-017Ch: I2S Master Mode Clock Control 13

Default: 0001'h

Table 259. MX-017Ch: I2S Master Mode Clock Control 13

DSP Address: 0x1800_C2F8 I2C Address: 0x017C				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Frac_mi_ni_i2s5_update	15	R	0'h	Fractional divider parameter update
Frac_ni_i2s5	14:0	R/W	1'h	Parameter of fractional divider (range : 0~65535)

9.178. MX-0192h: VAD ADC Filter Control 1

Default: 882F'h

Table 260. MX-0192h: VAD ADC Filter Control 1

DSP Address: 0x1800_C324 I2C Address: 0x0192				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ad_hpf_en	15	R/W	1'h	High pass filter enable control 0'b: Disable 1'b: Enable
reserved	14:10	R	2'h	Reserved
ad_boost_gain	9:8	R/W	0'h	ADC digital boost gain 00'b : 0dB 01'b: 12dB 10'b : 24dB 11'b : 36dB
ad_mute	7	R/W	0'h	Digital Mute 0'b: Unmute 1'b: Mute
ad_gain	6:0	R/W	2F'h	ADC volume in 0.375 dB step❶

❶ *00'h -17.625dB*
2F'h 0dB
7F'h +30 dB, with 0.75dB/step

9.179. MX-0193h: VAD ADC Filter Control 2

Default: 0000'h

Table 261. MX-0193h: VAD ADC Filter Control 2

DSP Address: 0x1800_C326 I2C Address: 0x0193				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
reserved	15:8	R	0'h	Reserved
sel_vad_dmic_data	7:6	R/W	0'h	Select DMIC Data Input for VAD 00'b: DMIC1 01'b: DMIC2 10'b: DMIC3 11'b: DMIC4
reserved	5	R	0'h	Reserved
sel_vad_dmic_edge	4	R/W	0'h	DMIC Data Latching control 0'b: Rise latch 1'b: Fall latch
reserved	3:1	R	0'h	Reserved
ad_input_sel	0	R/W	0'h	VAD Source Selection 0'b: AMIC 1'b: DMIC

9.180. MX-01A0h: Headphone Impedance Sensing Control 1

Default: 433D'h

Table 262. MX-01A0h: Headphone Impedance Sensing Control 1

DSP Address: 0x1800_C340 I2C Address: 0x01A0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
rldet_trig	15	R	0'h	Impedance sense trigger signal Write '1' to start impedance sense
Reserved	14:6	R	10C'h	Reserved
sel_sensing_range	5:4	R/W	3'h	Select Rs for impedance sensing 2'b00: Reserved 2'b01: Only sense 0~1kOhm impedance 2'b10: Only sense 1k~50kOhm impedance 2'b11: Sense 0~50kOhm impedance
sel_sensing_lr	3:2	R/W	3'h	Select channel(s) to perform impedance sensing 2'b00: Reserved 2'b01: Only sensing Lch Impedance 2'b10: Only sensing Rch Impedance 2'b11: Sensing Lch+Rch Impedance
Reserved	1:0	R	1'h	Reserved

9.181. MX-01A2h: Headphone Impedance Sensing Control 2

Default: 0000'h

Table 263. MX-01A2h: Headphone Impedance Sensing Control 2

DSP Address: 0x1800_C344 I2C Address: 0x01A2				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:8	R	0'h	Reserved
hp_rl_l	7:4	R	0'h	Final voltage type impedance sense result (Left) 0000'b: 0~8 ohm 0001'b: 9~23 ohm 0010'b: 24~41 ohm 0011'b: 42~75 ohm 0100'b: 76~150 ohm 0101'b: 151~450 ohm 0110'b: 451~1000 ohm 0111'b: 1001~5000 ohm 1000'b: 5001~50000 ohm 1001'b: >50000 ohm Other: Reserved

DSP Address: 0x1800_C344 I2C Address: 0x01A2				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
hp_rl_r	3:0	R	0'h	Final voltage type impedance sense result (Right) 0000'b: 0~8 ohm 0001'b: 9~23 ohm 0010'b: 24~41 ohm 0011'b: 42~75 ohm 0100'b: 76~150 ohm 0101'b: 151~450 ohm 0110'b: 451~1000 ohm 0111'b: 1001~5000 ohm 1000'b: 5001~50000 ohm 1001'b: >50000 ohm Other: Reserved

9.182. MX-01B3h: Headphone Impedance Sensing Control 3

Default: 40AF'h

Table 264. MX-01B3h: Headphone Impedance Sensing Control 3

DSP Address: 0x1800_C366 I2C Address: 0x01B3				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Rldet_en	15	R/W	0'h	HP Impedance Sensing Control 0'b: Disable 1'b: Enable
Reserved	14:0	R	40AF'h	Reserved

9.183. MX-01F0h: IRQ De-bounce Clock Control

Default: 0000'h

Table 265. MX-01F0h: IRQ Debounce Clock Control

DSP Address: 0x1800_C3E0 I2C Address: 0x01F0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
En_irq_clock	14	R/W	0'h	Enable IRQ De-bounce Clock 0'b: Disable 1'b: Enable
Reserved	13:0	R	0'h	Reserved

9.184. MX-0280h: Pitch Detection Control 1

Default: 7681'h

Table 266. MX-0280h: Pitch Detection Control 1

DSP Address: 0x1800_C500 I2C Address: 0x0280				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
pitch_det_en	15	R/W	0'h	Pitch Detection Enable Control 0'b: Disable 1'b: Enable
reserved	14:8	R	76'h	Reserved
pitch_det_clr	7	R/W	1'h	Clear pitch_det_flag & pitch_det_flag_hold 0'b: Bypass pitch detect flags 1'b: Clear pitch detect flags (force output = 0)
pitch_det_flag_hold	6	R	0'h	Pitch detect hold flag 0'b: Detection on-going 1'b: Detected
pitch_det_flag	5	R	0'h	Pitch detect flag 0'b: Detection on-going 1'b: Detected
pitch_det_debounce_flag	4	R	0'h	The debounce flag of pitch_det_flag 0'b: Non-speech audio input 1'b: Speech audio input
pitch_det_debounce_edge_flag	3	R	0'h	The edge event of pitch_det_debounce_flag 0'b: Nothing 1'b: Edge event occurred
hello_flag_hold	2	R	0'h	Hello detect flag hold 0'b: Detection on-going 1'b: Detected
hello_flag	1	R	0'h	Hello detect flag 0'b: Detection on-going 1'b: Detected
pitch_det_debounce_edge_flag_clr	0	R/W	1'h	Clear pitch_det_debounce_edge_flag 0'b: Bypass pitch_det_debounce_edge_flag 1'b: Clear pitch_det_debounce_edge_flag (force output = 0)

9.185. MX-02A0h: Pitch Detection Control 2

Default: 4089'h

Table 267. MX-02A0h: Pitch Detection Control 2

DSP Address: 0x1800_C540 I2C Address: 0x02A0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ok_det_en	15	R/W	0'h	Enable signal of ok detection 0'b: Disable OK Detection system 1'b: Enable OK Detection system
Reserved	14:8	R	40'h	Reserved

DSP Address: 0x1800_C540 I2C Address: 0x02A0				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
ok_det_clr	7	R/W	1'h	Clear ok_flag & ok_flag_hold 0'b: Bypass ok detect flags 1'b: Clear ok detect flags (force output = 0)
ok_flag_hold	6	R	0'h	Ok detect flag hold 0'b: Detection on-going 1'b: Detected
ok_flag	5	R	0'h	Ok detect flag 0'b: Detection on-going 1'b: Detected
Reserved	4:0	R	9'h	Reserved

9.186. MX-0300h: Multi-Band DRC Control 1

Default: 3C10'h

Table 268. MX-0300h: Multi-Band DRC Control 1

DSP Address: 0x1800_C600 I2C Address: 0x0300				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
mu_alc_hb_out_l	15	R/W	0'h	Mute Control for ALC High Band Output_L 0'b: Un-mute 1'b: Mute
mu_alc_hb_out_r	14	R/W	0'h	Mute Control for ALC High Band Output_R 0'b: Un-mute 1'b: Mute
mu_alc_mb_out_l	13	R/W	1'h	Mute Control for ALC Middle Band Output_L 0'b: Un-mute 1'b: Mute
mu_alc_mb_out_r	12	R/W	1'h	Mute Control for ALC Middle Band Output_R 0'b: Un-mute 1'b: Mute
mu_alc_bb_out_l	11	R/W	1'h	Mute Control for ALC Bass Band Output_L 0'b: Un-mute 1'b: Mute
mu_alc_bb_out_r	10	R/W	1'h	Mute Control for ALC Bass Band Output_R 0'b: Un-mute 1'b: Mute
reserved	9:4	R	1'h	Reserved
threeband_en	3	R/W	0'h	Three Band Filter Clock Gating Control 0'b: Disable (Clock gating and reset) 1'b: Enable
threeband_hpf_en	2	R/W	0'h	Three Band High Pass Filter Control 0'b: Disable 1'b: Enable 4th order HPF
threeband_bpf_en	1	R/W	0'h	Three Band Band Pass Filter Control 0'b: Disable 1'b: Enable 4th order BPF

DSP Address: 0x1800_C600 I2C Address: 0x0300				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
threeband_lpf_en	0	R/W	0'h	Three Band Low Pass Filter Control 0'b: Disable 1'b: Enable 4th order LPF

9.187. MX-0310h: Multi-Band DRC Control 2

Default: 5254'h

Table 269. MX-0310h: Multi-Band DRC Control 2

DSP Address: 0x1800_C620 I2C Address: 0x0310				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
alc_hb_en	15	R/W	0'h	HB ALC + DRC Enable Control 0'b: Disable 1'b: Enable
Reserved	14:0	R	5254'h	Reserved

9.188. MX-0311h: Multi-Band DRC Control 3

Default: 0300'h

Table 270. MX-0311h: Multi-Band DRC Control 3

DSP Address: 0x1800_C622 I2C Address: 0x0311				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
alc_hb_atk_rate	12:8	R/W	3'h	ALC_HB attack time (attack time = (4 * 2^n) /48k, n = alc_hb_atk_rate[4:0]) 5'h00: 83us 5'h01: 166us 5'h02: 332us ... 5'h12: 21.85 s
Reserved	7:5	R	0'h	Reserved
alc_hb_atk_speed_up_rate	4:0	R/W	0'h	ALC_HB attack time for speed up mode (attack time = (2 * 2^n) /48k, n = alc_hb_atk_speed_up_rate[4:0]) 5'h00: 42us 5'h01: 83us 5'h02: 166us ... 5'h13: 21.85 s

9.189. MX-0312h: Multi-Band DRC Control 4

Default: 5F5F'h

Table 271. MX-0312h: Multi-Band DRC Control 4

DSP Address: 0x1800_C624 I2C Address: 0x0312				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
alc_hb_bk_gain_l	14:8	R/W	5F'h	ALC_HB back boost gain control (0.375dB/step) 7'h00: -35.625 dB 7'h01: -35.250 dB ..... 7'h5F: 0.000 dB ..... 7'h7F: 12.000dB
Reserved	7	R	0'h	Reserved
alc_hb_bk_gain_r	6:0	R/W	5F'h	ALC_HB back boost gain control (0.375dB/step) 7'h00: -35.625 dB 7'h01: -35.250 dB ..... 7'h5F: 0.000 dB ..... 7'h7F: 12.000dB

9.190. MX-0313h: Multi-Band DRC Control 4

Default: 133E'h

Table 272. MX-0313h: Multi-Band DRC Control 4

DSP Address: 0x1800_C626 I2C Address: 0x0313				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
alc_hb_rate_sel	14:12	R/W	1'h	ALC_HB rate control for sample rate change 3'b001: 48 kHz 3'b010: 96 kHz 3'b011: 192 kHz 3'b011: 44.1kHz 3'b100: 88.2kHz 3'b101: 176.4kHz
Reserved	11:10	R	0'h	Reserved
alc_hb_ft_boost	9:0	R/W	33E'h	Front boost for ALC_HB(24db~-103.75db, 0p125db/step) 10'h000: -103.75dB 10'h001: -103.625dB 10'h33E: 0 dB … 10'h3FD:23.875dB 10'h3FE: 24.000dB

9.191. MX-0315h: Multi-Band DRC Control 5

Default: 040C'h

Table 273. MX-0315h: Multi-Band DRC Control 5

DSP Address: 0x1800_C62A I2C Address: 0x0315				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
alc_hb_rc_fast_rate	12:8	R/W	4'h	ALC_HB fast recovery time (attack time = (4 * 2^n) /48k, n = alc_hb_atk_rate[4:0]) 5'h00: 83us 5'h01: 166us 5'h02: 332us ... 5'h12: 21.85 s
Reserved	7:5	R	0'h	Reserved
alc_hb_rc_slow_rate	4:0	R/W	C'h	ALC_HB slow recovery time (attack time = (2 * 2^n) /48k, n = alc_hb_atk_speed_up_rate[4:0]) 5'h00: 42us 5'h01: 83us 5'h02: 166us ... 5'h13: 21.85 s

9.192. MX-0320h: Multi-Band DRC Control 6

Default: 5254'h

Table 274. MX-0320h: Multi-Band DRC Control 6

DSP Address: 0x1800_C640 I2C Address: 0x0320				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
alc_mb_en	15	R/W	0'h	MB ALC + DRC Enable Control 0'b: Disable 1'b: Enable
Reserved	14:0	R	5254'h	Reserved

9.193. MX-0321h: Multi-Band DRC Control 7

Default: 0300'h

Table 275. MX-0321h: Multi-Band DRC Control 7

DSP Address: 0x1800_C642 I2C Address: 0x0321				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved

DSP Address: 0x1800_C642 I2C Address: 0x0321				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
alc_mb_atk_rate	12:8	R/W	3'h	ALC_MB attack time (attack time = (4 * 2^n) /48k, n = alc_hb_atk_rate[4:0]) 5'h00: 83us 5'h01: 166us 5'h02: 332us ... 5'h12: 21.85 s
Reserved	7:5	R	0'h	Reserved
alc_mb_atk_speed_up_rate	4:0	R/W	0'h	ALC_MB attack time for speed up mode (attack time = (2 * 2^n) /48k, n = alc_hb_atk_speed_up_rate[4:0]) 5'h00: 42us 5'h01: 83us 5'h02: 166us ... 5'h13: 21.85 s

9.194. MX-0322h: Multi-Band DRC Control 8

Default: 5F5F'h

Table 276. MX-0322h: Multi-Band DRC Control 8

DSP Address: 0x1800_C644 I2C Address: 0x0322				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
alc_mb_bk_gain_l	14:8	R/W	5F'h	ALC_MB back boost gain control (0.375dB/step) 7'h00: -35.625 dB 7'h01: -35.250 dB ..... 7'h5F: 0.000 dB ..... 7'h7F: 12.000dB
Reserved	7	R	0'h	Reserved
alc_mb_bk_gain_r	6:0	R/W	5F'h	ALC_MB back boost gain control (0.375dB/step) 7'h00: -35.625 dB 7'h01: -35.250 dB ..... 7'h5F: 0.000 dB ..... 7'h7F: 12.000dB

9.195. MX-0323h: Multi-Band DRC Control 9

Default: 133E'h

Table 277. MX-0323h: Multi-Band DRC Control 9

DSP Address: 0x1800_C646 I2C Address: 0x0323				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
alc_mb_rate_sel	14:12	R/W	1'h	ALC_MB rate control for sample rate change 3'b001: 48 kHz 3'b010: 96 kHz 3'b011: 192 kHz 3'b011: 44.1kHz 3'b100: 88.2kHz 3'b101: 176.4kHz
Reserved	11:10	R	0'h	Reserved
alc_mb_ft_boost	9:0	R/W	33E'h	Front boost for ALC_MB(24db~-103.75db, 0p125db/step) 10'h000: -103.75dB 10'h001: -103.625dB 10'h33E: 0 dB … 10'h3FD:23.875dB 10'h3FE: 24.000dB

9.196. MX-0325h: Multi-Band DRC Control 10

Default: 040C'h

Table 278. MX-0325h: Multi-Band DRC Control 10

DSP Address: 0x1800_C64A I2C Address: 0x0325				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
alc_mb_rc_fast_rate	12:8	R/W	4'h	ALC_MB fast recovery time (attack time = (4 * 2^n) /48k, n = alc_hb_atk_rate[4:0]) 5'h00: 83us 5'h01: 166us 5'h02: 332us ... 5'h12: 21.85 s
Reserved	7:5	R	0'h	Reserved
alc_mb_rc_slow_rate	4:0	R/W	C'h	ALC_MB slow recovery time (attack time = (2 * 2^n) /48k, n = alc_hb_atk_speed_up_rate[4:0]) 5'h00: 42us 5'h01: 83us 5'h02: 166us ... 5'h13: 21.85 s

9.197. MX-0330h: Multi-Band DRC Control 11

Default: 5254'h

Table 279. MX-0330h: Multi-Band DRC Control 11

DSP Address: 0x1800_C660 I2C Address: 0x0330				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
alc_bb_en	15	R/W	0'h	BB ALC + DRC Enable Control 0'b: Disable 1'b: Enable
Reserved	14:0	R	5254'h	Reserved

9.198. MX-0331h: Multi-Band DRC Control 12

Default: 0300'h

Table 280. MX-0331h: Multi-Band DRC Control 12

DSP Address: 0x1800_C662 I2C Address: 0x0331				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
alc_bb_atk_rate	12:8	R/W	3'h	ALC_BB attack time (attack time = (4 * 2^n) /48k, n = alc_hb_atk_rate[4:0]) 5'h00: 83us 5'h01: 166us 5'h02: 332us ... 5'h12: 21.85 s
Reserved	7:5	R	0'h	Reserved
alc_bb_atk_speed_up_rate	4:0	R/W	0'h	ALC_BB attack time for speed up mode (attack time = (2 * 2^n) /48k, n = alc_hb_atk_speed_up_rate[4:0]) 5'h00: 42us 5'h01: 83us 5'h02: 166us ... 5'h13: 21.85 s

9.199. MX-0332h: Multi-Band DRC Control 13

Default: 5F5F'h

Table 281. MX-0332h: Multi-Band DRC Control 13

DSP Address: 0x1800_C664 I2C Address: 0x0332				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved

DSP Address: 0x1800_C664 I2C Address: 0x0332				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
alc_bb_bk_gain_l	14:8	R/W	5F'h	ALC_BB back boost gain control (0.375dB/step) 7'h00: -35.625 dB 7'h01: -35.250 dB ..... 7'h5F: 0.000 dB ..... 7'h7F: 12.000dB
Reserved	7	R	0'h	Reserved
alc_bb_bk_gain_r	6:0	R/W	5F'h	ALC_BB back boost gain control (0.375dB/step) 7'h00: -35.625 dB 7'h01: -35.250 dB ..... 7'h5F: 0.000 dB ..... 7'h7F: 12.000dB

9.200. MX-0333h: Multi-Band DRC Control 14

Default: 133E'h

Table 282. MX-0333h: Multi-Band DRC Control 14

DSP Address: 0x1800_C666 I2C Address: 0x0333				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
alc_bb_rate_sel	14:12	R/W	1'h	ALC_BB rate control for sample rate change 3'b001: 48 kHz 3'b010: 96 kHz 3'b011: 192 kHz 3'b011: 44.1kHz 3'b100: 88.2kHz 3'b101: 176.4kHz
Reserved	11:10	R	0'h	Reserved
alc_bb_ft_boost	9:0	R/W	33E'h	Front boost for ALC_BB(24db~-103.75db, 0p125db/step) 10'h000: -103.75dB 10'h001: -103.625dB 10'h33E: 0 dB … 10'h3FD:23.875dB 10'h3FE: 24.000dB

9.201. MX-0335h: Multi-Band DRC Control 15

Default: 040C'h

Table 283. MX-0335h: Multi-Band DRC Control 15

DSP Address: 0x1800_C66A I2C Address: 0x0335				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
alc_bb_rc_fast_rate	12:8	R/W	4'h	ALC_BB fast recovery time (attack time = (4 * 2^n) /48k, n = alc_hb_atk_rate[4:0]) 5'h00: 83us 5'h01: 166us 5'h02: 332us ... 5'h12: 21.85 s
Reserved	7:5	R	0'h	Reserved
alc_bb_rc_slow_rate	4:0	R/W	C'h	ALC_BB slow recovery time (attack time = (2 * 2^n) /48k, n = alc_hb_atk_speed_up_rate[4:0]) 5'h00: 42us 5'h01: 83us 5'h02: 166us ... 5'h13: 21.85 s

9.202. MX-0340h: Multi-Band DRC Control 16

Default: 4951'h

Table 284. MX-0340h: Multi-Band DRC Control 16

DSP Address: 0x1800_C680 I2C Address: 0x0340				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
alc_pos_drc_en	15	R/W	0'h	Post DRC enable control 0'b: Disable 1'b: Enable
Reserved	14:8	R	49'h	Reserved
alc_pos_drc_ratio_sel	7:6	R/W	1'h	ALC_POS DRC compression ratio select control 2'b00: 1:1 2'b01: 1:2 2'b10: 1:4 2'b11: 1:8
alc_pos_drc_ratio_sel2	5:4	R/W	1'h	ALC_POS DRC compression ratio select control 2'b00: 1:1 2'b01: 1:2 2'b10: 1:4 2'b11: 1:8
Reserved	3	R	0'h	Reserved

DSP Address: 0x1800_C680 I2C Address: 0x0340				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
alc_pos_rate_sel	2:0	R/W	1'h	ALC_POS rate control for sample rate change 3'b001: 48 kHz 3'b010: 96 kHz 3'b011: 192 kHz 3'b011: 44.1kHz 3'b100: 88.2kHz 3'b101: 176.4kHz

9.203. MX-0341h: Multi-Band DRC Control 17

Default: 1860'h

Table 285. MX-0341h: Multi-Band DRC Control 17

DSP Address: 0x1800_C682 I2C Address: 0x0341				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
alc_pos_atk_noise_rate	14:10	R/W	6'h	ALC_POS attack time in noise gate mode (attack time = (4 * 2^n) /48k, n = alc_pos_atk_noise_rate[4:0]) 5'h00: 83us 5'h01:166us 5'h02:332us ... 5'h12: 21.85 s
alc_pos_atk_rate	9:5	R/W	3'h	ALC_POS attack time (attack time = (4 * 2^n) /48k, n = alc_pos_atk_rate[4:0]) 5'h00: 83us 5'h01:166us 5'h02:332us ... 5'h12: 21.85 s
alc_pos_atk_speed_up_rate	4:0	R/W	0'h	ALC_POS attack time for spped up mode (attack time = (2 * 2^n) /48k, n = alc_pos_atk_rate[4:0]) 5'h00: 42us 5'h01: 83us 5'h02: 166us ... 5'h13: 21.85 s

9.204. MX-0342h: Multi-Band DRC Control 18

Default: 5F5F'h

Table 286. MX-0342h: Multi-Band DRC Control 18

DSP Address: 0x1800_C684 I2C Address: 0x0342				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
alc_pos_bk_gain_l	14:8	R/W	5F'h	ALC_POS back boost gain control (0.375dB/step) 7'h00: -35.625 dB 7'h01: -35.250 dB ..... 7'h5F: 0.000 dB ..... 7'h7F: 12.000dB
Reserved	7	R	0'h	Reserved
alc_pos_bk_gain_r	6:0	R/W	5F'h	ALC_POS back boost gain control (0.375dB/step) 7'h00: -35.625 dB 7'h01: -35.250 dB ..... 7'h5F: 0.000 dB ..... 7'h7F: 12.000dB

9.205. MX-0344h: Multi-Band DRC Control 19

Default: 0450'h

Table 287. MX-0344h: Multi-Band DRC Control 19

DSP Address: 0x1800_C688 I2C Address: 0x0344				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
alc_pos_noise_gate_en	15	R/W	0'h	ALC_POS noise_gate mode control 0'b: Disable noise_gate mode 1'b: Enable noise_gate mode
alc_pos_noise_gain_hd	14	R/W	0'h	ALC_POS hold gain when noise gate mode 0'b: Do not hold gain when noise gate mode(depend on noise gate threshold to do noise gate's AGC) 1'b: Hold gain when noise gate mode
alc_pos_noise_gate_drop_en	13	R/W	0'h	ALC_POS noise_gate drop mode control 0'b: Disable noise_gate_drop mode 1'b: Enable noise_gate_drop mode
Reserved	12	R	0'h	reserved

DSP Address: 0x1800_C688 I2C Address: 0x0344				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
alc_pos_noise_gate_exp	11:8	R/W	4'h	ALC_POS noise_gate boost control 4'b0000: 0dB 4'b0001: 3dB 4'b0010: 6dB ..... 4'b1111: 45dB (3dB/step)
alc_pos_noise_gate_ratio_sel	7:6	R/W	1'h	ALC_POS DRC expansion ratio select control, when noise gate is enabled 2'b00: 1:1 2'b01: 2:1 2'b10: 4:1 2'b11: 8:1
alc_pos_noise_range	5:4	R/W	1'h	Noise gate threshold margin control in ALC_POS 2'b00: +-0 dB 2'b01: +-1.5 dB 2'b10: +-3.0 dB 2'b11: +-4.5 dB
Reserved	3:0	R	0'h	reserved

9.206. MX-0345h: Multi-Band DRC Control 20

Default: 00FF'h

Table 288. MX-0345h: Multi-Band DRC Control 20

DSP Address: 0x1800_C68A I2C Address: 0x0345				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
alc_pos_thnoise	12:8	R/W	0'h	AGC noise gate threshold level (at amplitude domain) control 5'h00: -24.00dB 5'h01: -25.50dB 5'h02: -27.00dB ..... 5'h1f : -70.50dB (-1.5dB/step)
Reserved	7:0	R	FF'h	Reserved

9.207. MX-0346h: Multi-Band DRC Control 21

Default: 040C'h

Table 289. MX-0346h: Multi-Band DRC Control 21

DSP Address: 0x1800_C68C I2C Address: 0x0346				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
alc_pos_rc_fast_en	15	R/W	0'h	ALC_POS force fast recovery control for special cases (window) 0'b: Disable force fast recovery for special cases 1'b: Enable force fast recovery for normal use
Reserved	14:13	R	0'h	Reserved
alc_pos_rc_fast_rate	12:8	R/W	4'h	ALC_POS fast recovery time (recovery time = (4 * 2^n) /48k, n = alc_pos_rc_fast_rate[4:0]) 5'h00: 83us 5'h01:166us 5'h02:332us ... 5'h12: 21.85 s
Reserved	7:5	R	0'h	Reserved
alc_pos_rc_slow_rate	4:0	R/W	C'h	ALC_POS slow recovery time (recovery time = (4 * 2^n) /48k, n = alc_pos_rc_slow_rate[4:0]) 5'h00: 83us 5'h01:166us 5'h02:332us ... 5'h12: 21.85 s

9.208. MX-0348h: Multi-Band DRC Control 22

Default: 0000'h

Table 290. MX-0348h: Multi-Band DRC Control 22

DSP Address: 0x1800_C690 I2C Address: 0x0348				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:14	R	0'h	Reserved
alc_pos_thmax	13:8	R/W	0'h	ALC_POS main-limiter threshold level (at amplitude domain) control 6'h00: 0dB 6'h01: - 0.375dB 6'h02: - 0.750dB ..... 6'h3f: -23.625dB (-0.375dB/step)
Reserved	7:6	R	0'h	Reserved
alc_pos_thmax2	5:0	R/W	0'h	ALC_POS second-limiter threshold level (at amplitude domain) control 6'h00: 0dB 6'h01: - 0.75dB 6'h02: - 1.5dB ..... 6'h3c: -45 dB (-0.75dB/step)

9.209. MX-0350h: ADC ALC/DRC Control 1

Default: 4905'h

Table 291. MX-0350h: ADC ALC/DRC Control 1

DSP Address: 0x1800_C6A0 I2C Address: 0x0350				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
alc_adc_en	15	R/W	0'h	ALC_ADC enable control 1'b0: Disable ALC_ADC 1'b1: Enable ALC_ADC
Reserved	14:7	R	92'h	Reserved
alc_adc_noise_gate_en	6	R/W	0'h	ALC_ADC noise_gate mode control 1'b0: Disable noise_gate mode 1'b1: Enable noise_gate mode
alc_adc_noise_gate_drop_en	5	R/W	0'h	ALC_ADC noise_gate drop mode control 1'b0: Disable noise_gate_drop mode 1'b1: Enable noise_gate_drop mode
Reserved	4	R	0'h	Reserved
alc_adc_drc_ratio_sel	3:2	R/W	1'h	ALC_ADC DRC compression ratio select control 2'b00: 1:1 2'b01: 1:2 2'b10: 1:4 2'b11: 1:8
alc_adc_drc_ratio_sel2	1:0	R/W	1'h	ALC_ADC DRC compression ratio select control 2'b00: 1:1 2'b01: 1:2 2'b10: 1:4 2'b11: 1:8

9.210. MX-0352h: ADC ALC/DRC Control 2

Default: 0100'h

Table 292. MX-0351h: ADC ALC/DRC Control 2

DSP Address: 0x1800_C6A2 I2C Address: 0x0351				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:11	R	0'h	Reserved
alc_adc_rate_sel	10:8	R/W	1'h	ALC_ADC rate control for sample rate change 3'b001: 48kHz 3'b010: 96kHz 3'b011: 192kHz 3'b011: 44.1kHz 3'b100: 88.2kHz 3'b101: 176.4kHz Others: Reserved
Reserved	7:6	R	0'h	Reserved

DSP Address: 0x1800_C6A2 I2C Address: 0x0351				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
alc_adc_ft_boost	5:0	R/W	0'h	ALC_ADC front boost gain control (0.75dB/step) 6'h00: 0 dB 6'h01: 0.75 dB ..... 6'27h: 29.25 dB

9.211. MX-0353h: ADC ALC/DRC Control 3

Default: 5F5F'h

Table 293. MX-0353h: ADC ALC/DRC Control 3

DSP Address: 0x1800_C6A6 I2C Address: 0x0353				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
alc_adc_bk_gain_l	14:8	R/W	5F'h	ALC_ADC back boost gain control (0.375dB/step) 7'h00: -35.625 dB 7'h01: -35.250 dB ..... 7'h5f: 0.000 dB ..... 7'h7f: 12.000dB
Reserved	7	R	0'h	Reserved
alc_adc_bk_gain_r	6:0	R/W	5F'h	ALC_ADC back boost gain control (0.375dB/step) 7'h00: -35.625 dB 7'h01: -35.250 dB ..... 7'h5f: 0.000 dB ..... 7'h7f: 12.000dB

9.212. MX-0354h: ADC ALC/DRC Control 4

Default: 5F5F'h

Table 294. MX-0353h: ADC ALC/DRC Control 3

DSP Address: 0x1800_C6A6 I2C Address: 0x0353				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved

DSP Address: 0x1800_C6A6 I2C Address: 0x0353				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
alc_adc_atk_noise_rate	12:8	R/W	6'h	ALC_ADC attack time in noise gate mode (attack time = (4 * 2^n) /48k, n = alc_adc_atk_noise_rate[4:0]) 5'h00: 83us 5'h01:166us 5'h02:332us ... 5'h12: 21.85 s
Reserved	7:5	R	0'h	Reserved
alc_adc_atk_rate	4:0	R/W	3'h	ALC_ADC attack time (attack time = (4 * 2^n) /48k, n = alc_adc_atk_rate[4:0]) 5'h00: 83us 5'h01:166us 5'h02:332us ... 5'h12: 21.85 s

9.213. MX-0355h: ADC ALC/DRC Control 5

Default: 0022'h

Table 295. MX-0355h: ADC ALC/DRC Control 5

DSP Address: 0x1800_C6AA I2C Address: 0x0355				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
alc_adc_atk_speed_up_rate	12:8	R/W	0'h	ALC_ADC attack time for spped up mode (attack time = (2 * 2^n) /48k, n = alc_adc_atk_rate[4:0]) 5'h00: 42us 5'h01: 83us 5'h02: 166us ... 5'h13: 21.85 s
Reserved	7:0	R	22'h	Reserved

9.214. MX-0356h: ADC ALC/DRC Control 6

Default: 45FF'h

Table 296. MX-0356h: ADC ALC/DRC Control 6

DSP Address: 0x1800_C6AC I2C Address: 0x0356				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
alc_adc_noise_gate_exp	15:12	R/W	4'h	ALC_ADC noise_gate boost control 0'h: 0dB 1'h: 3dB 2'h: 6dB ... F'h: 45dB, 3dB/step
alc_adc_noise_gate_ratio_sel	11:10	R/W	1'h	ALC_ADC DRC expansion ratio select control, when noise gate is enabled 00'b: 1:1 01'b: 2:1 10'b: 4:1 11'b: 8:1
alc_adc_noise_range	9:8	R/W	1'h	Noise gate threshold margin control in ALC_ADC 2'b00: +-0 dB 2'b01: +-1.5 dB 2'b10: +-3.0 dB 2'b11: +-4.5 dB
Reserved	7:0	R	FF'h	Reserved

9.215. MX-0357h: ADC ALC/DRC Control 7

Default: 040C'h

Table 297. MX-0357h: ADC ALC/DRC Control 7

DSP Address: 0x1800_C6AE I2C Address: 0x0357				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
alc_adc_rc_fast_rate	12:8	R/W	4'h	ALC_ADC fast recovery time (recovery time = (4 * 2^n) /48k, n = alc_adc_rc_fast_rate[4:0]) 5'h00: 83us 5'h01:166us 5'h02:332us ... 5'h12: 21.85 s
Reserved	7:5	R	0'h	Reserved

DSP Address: 0x1800_C6AE I2C Address: 0x0357				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
alc_adc_rc_slow_rate	4:0	R/W	C'h	ALC_ADC slow recovery time (recovery time = (4 * 2^n) /48k, n = alc_adc_rc_slow_rate[4:0]) 5'h00: 83us 5'h01:166us 5'h02:332us ... 5'h12: 21.85 s

9.216. MX-0359h: ADC ALC/DRC Control 8

Default: 0000'h

Table 298. MX-0359h: ADC ALC/DRC Control 8

DSP Address: 0x1800_C6B2 I2C Address: 0x0359				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:14	R	0'h	Reserved
alc_adc_thmax	13:8	R/W	0'h	ALC_ADC main-limiter threshold level (at amplitude domain) control 00'h= 0dBFS 01'h= -0.375dBFS 02'h= -0.75dBFS 03'h= -1.125dBFS …….. 3F'h= -23.625dBFS
Reserved	7:6	R	0'h	Reserved
alc_adc_thmax2	5:0	R/W	0'h	ALC_ADC second-limiter threshold level (at amplitude domain) control 00'h= 0dBFS 01'h= -0.75dBFS 02'h= -1.5dBFS 03'h= -2.25dBFS …….. 3F'h= -45dBFS

9.217. MX-035Ah: ADC ALC/DRC Control 9

Default: 0000'h

Table 299. MX-035Ah: ADC ALC/DRC Control 9

DSP Address: 0x1800_C6B4 I2C Address: 0x035A				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:5	R	0'h	Reserved

DSP Address: 0x1800_C6B4 I2C Address: 0x035A				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
alc_adc_thnoise	4:0	R/W	0'h	AGC noise gate threshold level (at amplitude domain) control 00'h: -24dBFS 01'h: -25.5dBFS …….. 1F'h: -70.5 dBFS

9.218. MX-0500h: DSP Inbound/Outbound Control 1

Default: 0000'h

Table 300. MX-0500h: DSP Inbound/Outbound Control 1

DSP Address: 0x1800_CA00 I2C Address: 0x0500				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_ib01	15:12	R/W	0'h	Select InBound0/1 Source 0000'b: IF1_DAC_0/1 0001'b: IF2_DAC_0/1 0010'b: SLB_DAC_0/1 0011'b: Stereo1_ADC_Mixer_L/R 0100'b: Mono_ADC_Mixer_L/R 0101'b: VAD_ADC/VAD_ADC 0110'b: DAC1_FS/DAC1_FS 0111'b: VAD_ADC_Filter 1000'b: SPDIF_IN_L/R
Sel_ib23	11:8	R/W	0'h	Select InBound2/3 Source 0000'b: IF1_DAC_2/3 0001'b: IF2_DAC_2/3 0010'b: Reserved 0011'b: SLB_DAC_2/3 0100'b: Stereo2_ADC_Mixer_L/R 0101'b: Stereo3_ADC_Mixer_L/R 0110'b: DACL1_FS/DACR1_FS 0111'b: Mono_ADC_Mixer_L/R 1000'b: SPDIF_IN_L/R
Reserved	7	R	0'h	Reserved
Sel_ib45	6:4	R/W	0'h	Select InBound4/5 Source 000'b: IF1_DAC_4/5 001'b: IF2_DAC_4/5 010'b: IF3_DAC_L/R 011'b: IF4_DAC_L/R 100'b: SLB_DAC_4/5 101'b: Stereo1_ADC_Mixer_L/R 110'b: Mono_ADC_Mixer_L/R 111'b: Stereo3_ADC_Mixer_L/R
Reserved	3	R	0'h	Reserved

DSP Address: 0x1800_CA00 I2C Address: 0x0500				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Sel_ib6	2:0	R/W	0'h	Select InBound6 Source 000'b: IF1_DAC_6 001'b: IF2_DAC_6 010'b: IF4_DAC_L 011'b: IF5_DAC_L 100'b: SLB_DAC_6 101'b: Mono_ADC_Mixer_L 110'b: Stereo2_ADC_Mixer_L 111'b: Stereo3_ADC_Mixer_L

9.219. MX-0501h: DSP Inbound/Outbound Control 2

Default: 0000'h

Table 301. MX-0501h: DSP Inbound/Outbound Control 2

DSP Address: 0x1800_CA02 I2C Address: 0x0501				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
Sel_ib7	14:12	R/W	0'h	Select InBound7 Source 000'b: IF1_DAC_7 001'b: IF2_DAC_7 010'b: IF4_DAC_R 011'b: IF5_DAC_R 100'b: SLB_DAC_7 101'b: Mono_ADC_Mixer_R 110'b: Stereo2_ADC_Mixer_R 111'b: Stereo3_ADC_Mixer_R
Reserved	11:3	R	0'h	Reserved
Sel_mini_ib01	2:0	R/W	0'h	Select Mini DSP InBound0/1 Source 000'b: VAD_ADC 001'b: IF1_DAC_0/1 010'b: IF3_DAC_L/R 011'b: SLB_DAC_0/1 100'b: Mono_ADC_Mixer_L/R 101'b: Stereo1_ADC_Mixer_L/R 110'b: VAD_ADC_Filter 111'b: DAC1_FS

9.220. MX-0502h: DSP Inbound/Outbound Control 3

Default: 0000'h

Table 302. MX-0502h: DSP Inbound/Outbound Control 3

DSP Address: 0x1800_CA04 I2C Address: 0x0502				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:5	R	0'h	Reserved
Sel_src_ob23	4	R/W	0'h	Select OutBound2/3 Source Pass SRC Control 0'b: Bypass 1'b: Pass SRC
Sel_src_ob01	3	R/W	0'h	Select OutBound0/1 Source Pass SRC Control 0'b: Bypass 1'b: Pass SRC
Sel_src_ib45	2	R/W	0'h	Select InBound4/5 Source Pass SRC Control 0'b: Bypass 1'b: Pass SRC
Sel_src_ib23	1	R/W	0'h	Select InBound2/3 Source Pass SRC Control 0'b: Bypass 1'b: Pass SRC
Sel_src_ib01	0	R/W	0'h	Select InBound0/1 Source Pass SRC Control 0'b: Bypass 1'b: Pass SRC

9.221. MX-0503h: DSP Inbound/Outbound Control 4

Default: 2F2F'h

Table 303. MX-0503h: DSP Inbound/Outbound Control 4

DSP Address: 0x1800_CA06 I2C Address: 0x0503				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
Vol_ob0	14:8	R/W	2F'h	DSP OutBound0 digital volume in 0.375 dB step❶
Reserved	7	R	0'h	Reserved
Vol_ob1	6:0	R/W	2F'h	DSP OutBound1 digital volume in 0.375 dB step❶

❶ *00'h -17.625dB*
2F'h 0dB
7F'h +30 dB, with 0.375dB/step

9.222. MX-0504h: DSP Inbound/Outbound Control 5

Default: 2F2F'h

Table 304. MX-0504h: DSP Inbound/Outbound Control 5

DSP Address: 0x1800_CA08 I2C Address: 0x0504				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
Vol_ob2	14:8	R/W	2F'h	DSP OutBound2 digital volume in 0.375 dB step❶
Reserved	7	R	0'h	Reserved
Vol_ob3	6:0	R/W	2F'h	DSP OutBound3 digital volume in 0.375 dB step❶

❶ *00'h -17.625dB*
2F'h 0dB
7F'h +30 dB, with 0.375dB/step

9.223. MX-0505h: DSP Inbound/Outbound Control 6

Default: 2F2F'h

Table 305. MX-0505h: DSP Inbound/Outbound Control 6

DSP Address: 0x1800_CA0A I2C Address: 0x0505				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
Vol_ob4	14:8	R/W	2F'h	DSP OutBound4 digital volume in 0.375 dB step❶
Reserved	7	R	0'h	Reserved
Vol_ob5	6:0	R/W	2F'h	DSP OutBound5 digital volume in 0.375 dB step❶

❶ *00'h -17.625dB*
2F'h 0dB
7F'h +30 dB, with 0.375dB/step

9.224. MX-0506h: DSP Inbound/Outbound Control 7

Default: 2F2F'h

Table 306. MX-0506h: DSP Inbound/Outbound Control 7

DSP Address: 0x1800_CA0C I2C Address: 0x0506				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
Vol_ob6	14:8	R/W	2F'h	DSP OutBound6 digital volume in 0.375 dB step❶
Reserved	7	R	0'h	Reserved
Vol_ob7	6:0	R/W	2F'h	DSP OutBound7 digital volume in 0.375 dB step❶

❶ *00'h -17.625dB*
2F'h 0dB
7F'h +30 dB, with 0.375dB/step

9.225. MX-0507h: DSP Inbound/Outbound Control 8

Default: 2F2F'h

Table 307. MX-0507h: DSP Inbound/Outbound Control 8

DSP Address: 0x1800_CA0E I2C Address: 0x0507				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15	R	0'h	Reserved
Vol_ob0_mini	14:8	R/W	2F'h	Mini DSP OutBound0 digital volume in 0.375 dB step❶
Reserved	7	R	0'h	Reserved
Vol_ob1_mini	6:0	R/W	2F'h	Mini DSP OutBound1 digital volume in 0.375 dB step❶

❶ *00'h -17.625dB*
2F'h 0dB
7F'h +30 dB, with 0.375dB/step

9.226. MX-0520h: HIFI-Mini DSP Control and Status

Default: 0041'h

Table 308. MX-0520h: HIFI-Mini DSP Control and Status

DSP Address: 0x1800_CA40 I2C Address: 0x0520				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
Mini_pwaitmode	12	R	0'h	0'b: Not idle status 1'b: DSP idle status
Reserved	11:7	R	0'h	Reserved
Reserved	6	R	1'h	Reserved
Mini_bclk_enable	5	R/W	0'h	Mini DSP Bus CLK Gating Control 0'b: Gating BCLK 1'b: Enable BCLK
Mini_clk_enable	4	R/W	0'h	Mini DSP Clock Gating Control 0'b: Gating clock 1'b: Enable clock
Mini_ocdhaltonreset	3	R/W	0'h	Debug mode
Mini_tdebuginterrupt	2	R/W	0'h	Debug mode
Mini_reset	1	R/W	0'h	Mini DSP Reset Control 0'b: Normal 1'b: Reset
Mini_runstall	0	R/W	1'h	Mini DSP Run Stall Control 0'b: Run 1'b: Stop

9.227. MX-0610h: Analog ADC Clock Control 1

Default: A490'h

Table 309. MX-0610h: Analog ADC Clock Control 1

DSP Address: 0x1800_CC20 I2C Address: 0x0610				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	5'h	Reserved
en_ckgen_adc12	12	R/W	0'h	ADC1/2 power on reset 0'b: Reset 1'b: No Reset
Reserved	11:0	R/W	490'h	Reserved

9.228. MX-0611h: Analog ADC Clock Control 2

Default: A490'h

Table 310. MX-0611h: Analog ADC Clock Control 2

DSP Address: 0x1800_CC22 I2C Address: 0x0611				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	5'h	Reserved
en_ckgen_adc34	12	R/W	0'h	ADC3/4 power on reset 0'b: Reset 1'b: No Reset
Reserved	11:0	R/W	490'h	Reserved

9.229. MX-0612h: Analog ADC Clock Control 3

Default: 0210'h

Table 311. MX-0612h: Analog ADC Clock Control 3

DSP Address: 0x1800_CC24 I2C Address: 0x0612				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
en_ckgen_adc5	12	R/W	0'h	ADC5 power on reset 0'b: Reset 1'b: No Reset
Reserved	11:0	R/W	210'h	Reserved

9.230. MX-0657h: DSP Bus Bypass Control

Default: 0000'h

Table 312. MX-0657h: DSP Bus Bypass Control

DSP Address: 0x1800_CCAE I2C Address: 0x0657				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
En_bypass_dsp	15	R/W	0'h	DSP Bus Bypass Mode 0'b: Normal Mode 1'b: Bypass Mode
Reserved	11:0	R/W	0'h	Reserved

9.231. MX-0660h: Analog DAC Clock Control 1

Default: 0010'h

Table 313. MX-0660h: Analog DAC Clock Control 1

DSP Address: 0x1800_CCC0 I2C Address: 0x0660				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
En_ckgen_dac1	12	R/W	0'h	Enable Clock Generation of DAC1 0'b:Disable 1'b:Enable
Reserved	11:0	R	10'h	Reserved

9.232. MX-0661h: Analog DAC Clock Control 2

Default: 0010'h

Table 314. MX-0661h: Analog DAC Clock Control 2

DSP Address: 0x1800_CCC2 I2C Address: 0x0661				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
En_ckgen_dac2	12	R/W	0'h	Enable Clock Generation of DAC2 0'b:Disable 1'b:Enable
Reserved	11:0	R	10'h	Reserved

9.233. MX-0662h: Analog DAC Clock Control 3

Default: 0010'h

Table 315. MX-0662h: Analog DAC Clock Control 3

DSP Address: 0x1800_CCC4 I2C Address: 0x0662				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
En_ckgen_dac3	12	R/W	0'h	Enable Clock Generation of DAC3 0'b:Disable 1'b:Enable
Reserved	11:0	R	10'h	Reserved

9.234. MX-0663h: Analog DAC Clock Control 4

Default: 0010'h

Table 316. MX-0663h: Analog DAC Clock Control 4

DSP Address: 0x1800_CCC6 I2C Address: 0x0663				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
En_ckgen_dac4	12	R/W	0'h	Enable Clock Generation of DAC4 0'b:Disable 1'b:Enable
Reserved	11:0	R	10'h	Reserved

9.235. MX-0664h: Analog DAC Clock Control 5

Default: 0010'h

Table 317. MX-0664h: Analog DAC Clock Control 5

DSP Address: 0x1800_CCC8 I2C Address: 0x0664				
Port Name	**Bits**	**Read/Write**	**Reset State**	**Description**
Reserved	15:13	R	0'h	Reserved
En_ckgen_dac5	12	R/W	0'h	Enable Clock Generation of DAC5 0'b:Disable 1'b:Enable
Reserved	11:0	R	10'h	Reserved

10. Electrical Characteristics

10.1. DC Characteristics

10.1.1. Absolute Maximum Ratings

Table 318. Absolute Maximun Ratings

POWER TYPE	DECSRIPTION	MIN	TYP	MAX	UNIT
DBVDD	Digital I/O Power	-0.3		3.63	V
LDO18_IN	LDOs Power for DSP, RAM and Codec Digital Core	-0.3		1.98	V
AVDD18	Analog Power	-0.3		1.98	V
AVDDHV1	Analog Power for Receiver Amplifier	-0.3		7.1	V
AVDDHV2	Analog Power for ADC/DAC Reference and MICBIAS	-0.3		7.1	V
MONOVDD	Analog Power for Receiver Amplifier	-0.3		3.63	V
AVDD33	Analog Power for ADC/DAC Reference and MICBIAS	-0.3		3.63	V
CPVDD	Analog Power for Charge Pump	-0.3		1.98	V
AVDD18_L_DAC	Analog Power for DAC	-0.3		1.98	V
AVDD18_R_DAC	Analog Power for DAC	-0.3		1.98	V
HPVDD	Analog Power for HP Amplifier	-0.3		1.98	V
HPVDD_AMPL	Analog Power for HP Amplifier	-0.3		1.98	V
HPVDD_AMPL	Analog Power for HP Amplifier	-0.3		1.98	V
DACREF_L	Analog Power for DAC Reference	-0.3		1.98	V
DACREF_R	Analog Power for DAC Reference	-0.3		1.98	V
Ta	Operating Ambient Temperature	-25		85	^{o}C
Ts	Storage Temperature	-55		125	^{o}C

10.1.2. Power/Ground Recommended Operating Conditions

Table 319. Power/Ground Operaton Conditions

POWER TYPE	DECSRIPTION	MIN	TYP	MAX	UNIT
DBVDD	Digital I/O Power	1.71	1.8	3.6 ❶	V
DCVDD1	Digital power for codec core (Supplied by internal LDO2 or external power)	0.9	1.1	1.2	V
DCVDD3	Digital power for DSP (Supplied by internal LDO1 or external power)	1.1	1.2	1.4	V
LDO18_IN	LDOs Power for DSP, RAM and Codec Digital Core	1.71	1.8	1.9	V
AVDD18	Analog Power	1.71	1.8	1.9	V
AVDDHV1	Analog Power for Receiver Amplifier	2.5	4.2	5	V
AVDDHV2	Analog Power for ADC/DAC Reference and MICBIAS	2.5	4.2	5	V
MONOVDD	Analog Power for Receiver Amplifier	3.0	3.3	3.6	V
AVDD33	Analog Power for ADC/DAC Reference and MICBIAS	3.0	3.3	3.6	V
CPVDD	Analog Power for Charge Pump	1.71	1.8	1.9	V
AVDD18_L_DAC	Analog Power for DAC	1.71	1.8	1.9	V
AVDD18_R_DAC	Analog Power for DAC	1.71	1.8	1.9	V
HPVDD	Analog Power for HP Amplifier	1.71	1.8	1.9	V
HPVDD_AMPL	Analog Power for HP Amplifier	1.71	1.8	1.9	V
HPVDD_AMPL	Analog Power for HP Amplifier	1.71	1.8	1.9	V
DACREF_L	Analog Power for DAC Reference	1.71	1.8	1.9	V
DACREF_R	Analog Power for DAC Reference	1.71	1.8	1.9	V
DGND, AGND, MONOGND, AGND_LOUT, DACGND_L, DACGND_R	Ground		0		V

❶When using analog mic input port to receive DMIC's data, the DBVDD only support 1.8V operation voltage.

10.1.3. Static Characteristics

Table 320. Static Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage Range	V_{IN}	-0.30	-	DBVDD+0.30	V
Low Level Input Voltage	V_{IL}	-	-	0.35DBVDD	V
High Level Input Voltage	V_{IH}	0.65DBVDD	-	-	V
High Level Output Voltage	V_{OH}	0.9DBVDD	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.1DBVDD	V
Output Buffer High Drive Current	-	0.6	4	8	mA
Output Buffer Low Drive Current	-	0.7	4	8	mA
Input Buffer Pull-Up Resistor	-	55	110	270	KΩ
Input Buffer Pull-Down Resistor	-	63	130	300	KΩ

Note: DBVDD=1.8V, DCVDD=1.2V, Tambient=40℃.

10.2. Signal Timing

10.2.1. I²C Control Interface

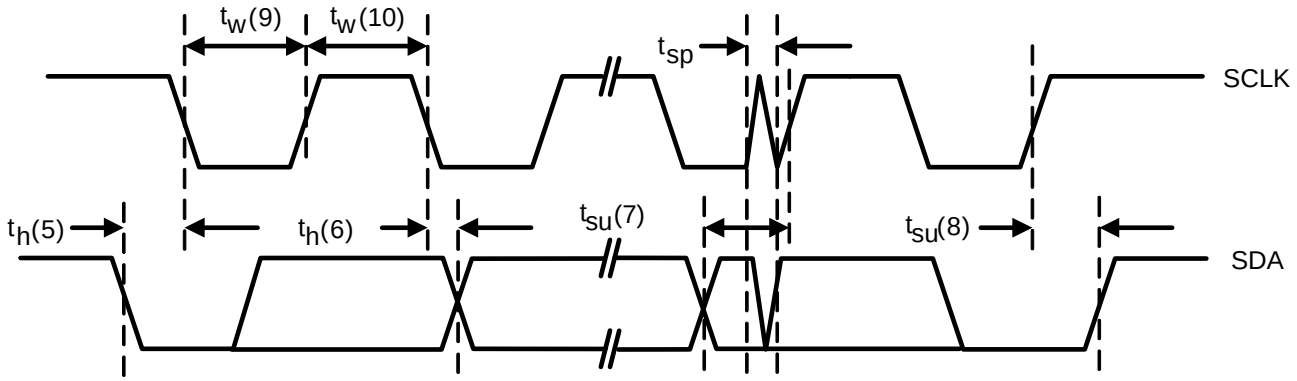


Figure 53. I2C Control Interface

Table 321. I2C Timing

Parameter	Symbol	Min	Typ	Max	Units
Clock Pulse Duration	t_w	1.3	-	-	µs
Clock Pulse Duration	t_w	600	-	-	ns
Clock Frequency	F	0	-	400K	Hz
Start Hold Time	t_h	600	-	-	ns
Data Setup Time	t_{su}	100	-	-	ns
Data Hold Time	t_h	-	-	900	ns
Rising Time	t_r	-	-	300	ns
Falling Time	t_f	-	-	300	ns
Stop Setup Time	t_{su}	600	-	-	ns
Pulse Width of Spikes Suppressed Input Filter	t_{sp}	0	-	50	ns

10.2.2. I²S/PCM Interface Master Mode

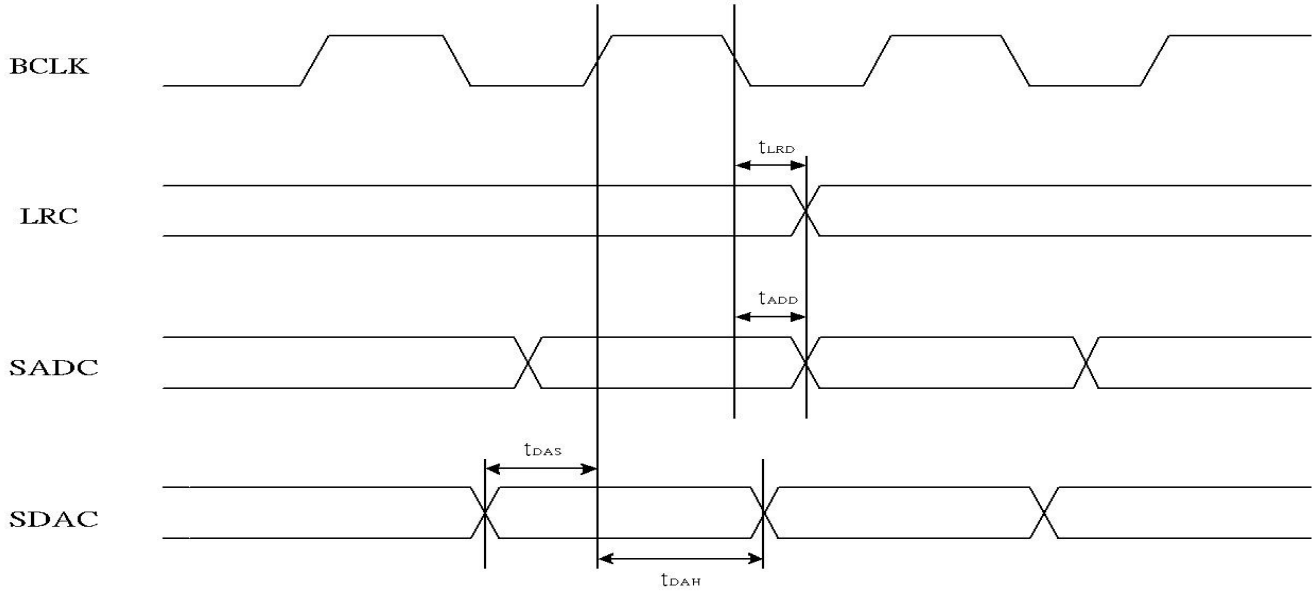


Figure 54. Timing of I2S/PCM Master Mode

Table 322. Timing of I2S/PCM Master Mode

Parameter	Symbol	Min	Typ	Max	Units
LRCK Output to BCLK Delay	t_{LRD}	-	-	30	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

10.2.3. I²S/PCM Interface Slave Mode

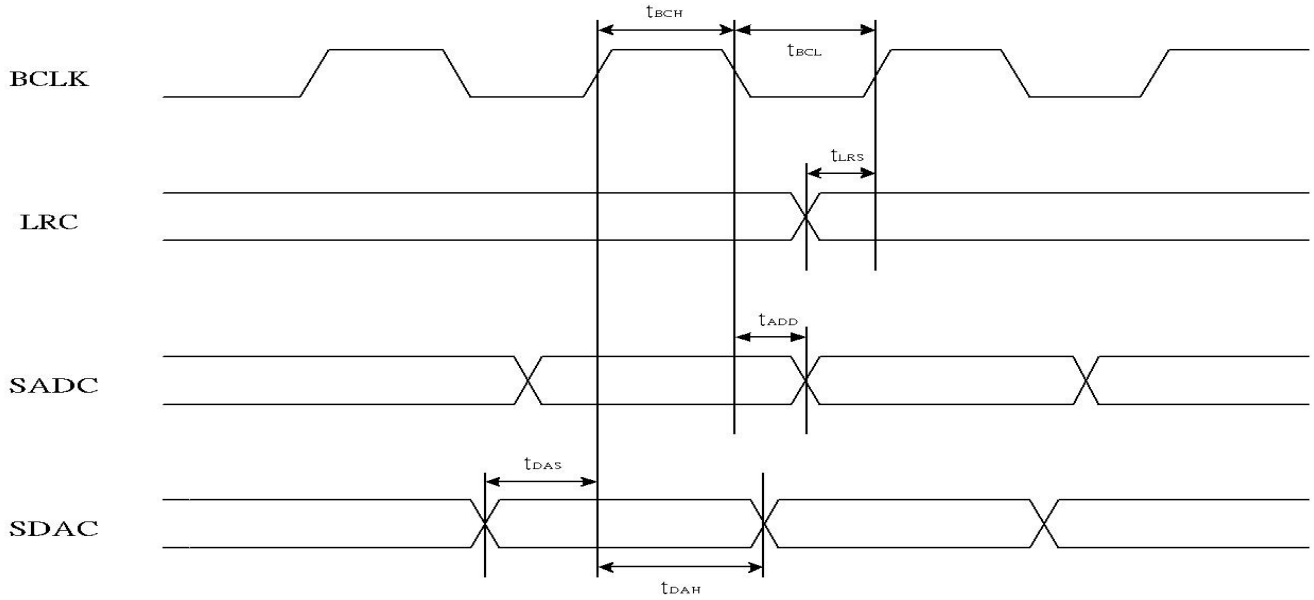


Figure 55. Timing of I2S/PCM Slave Mode

Table 323. Timing of I2S/PCM Slave Mode

Parameter	Symbol	Min	Typ	Max	Units
BCLK High Pulse Width	t_{BCH}	20	-	-	ns
BCLK Low Pulse Width	t_{BCL}	20	-	-	ns
LRCK Input Setup Time	t_{LRS}	30	-	-	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

10.2.4. Digital Microphone Interface

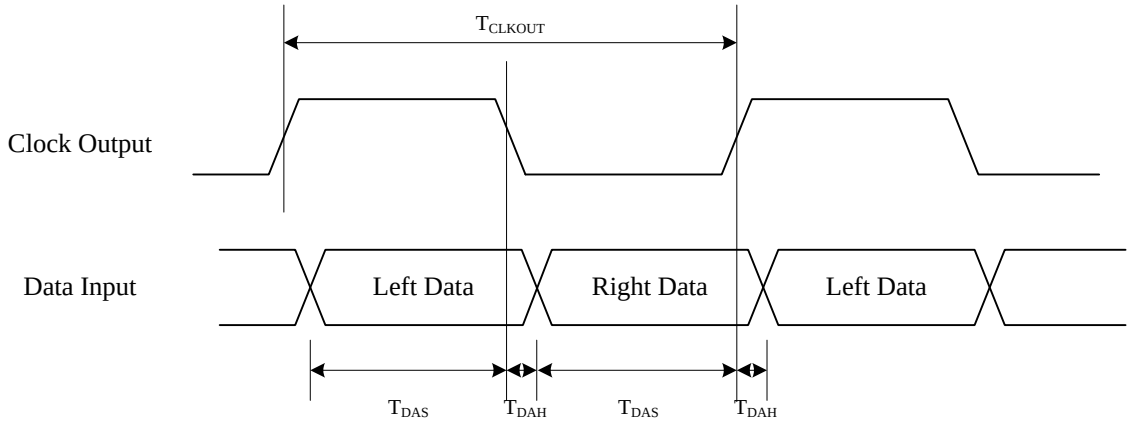


Figure 56. Digital Microphone Interface Timing

Table 324. Digital Microphone Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
Clock Output Rate	T_{CLKOUT}	300	-	-	ns
Clock Duty Cycle	-	45:55	-	55:45	-
Data Input Setup Time	T_{DAS}	20	-	-	ns
Data Input Hold Time	T_{DAH}	10	-	-	ns

10.2.5. MCLK Timing

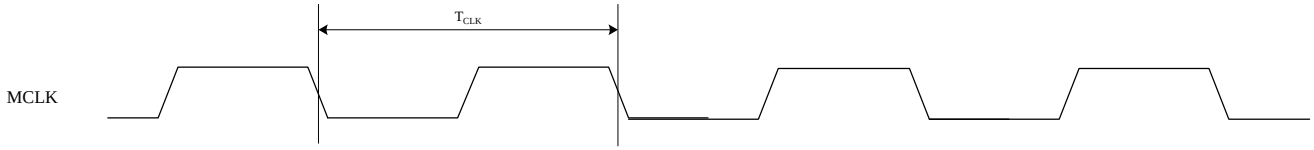
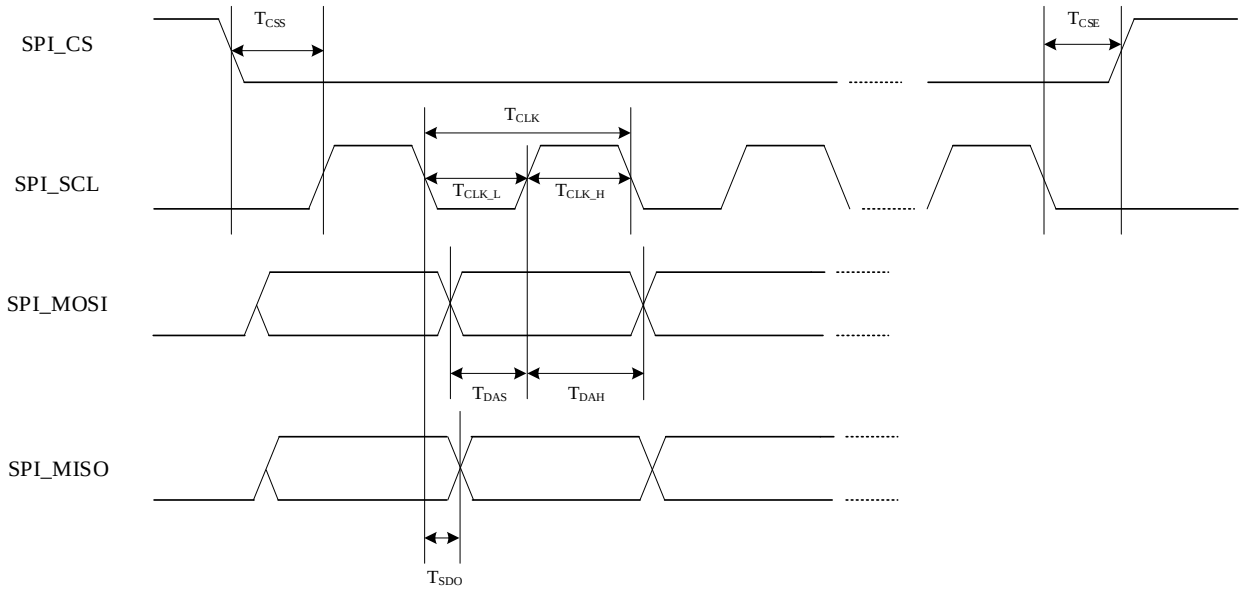


Figure 57. MCLK Timing

Table 325. MCLK Timing

Parameter	Symbol	Min	Typ	Max	Units
MCLK cycle time	T_{CLK}	25	-	-	ns
MCLK duty cycle	-	60:40	-	40:60	-

10.2.6. Slave SPI Interface

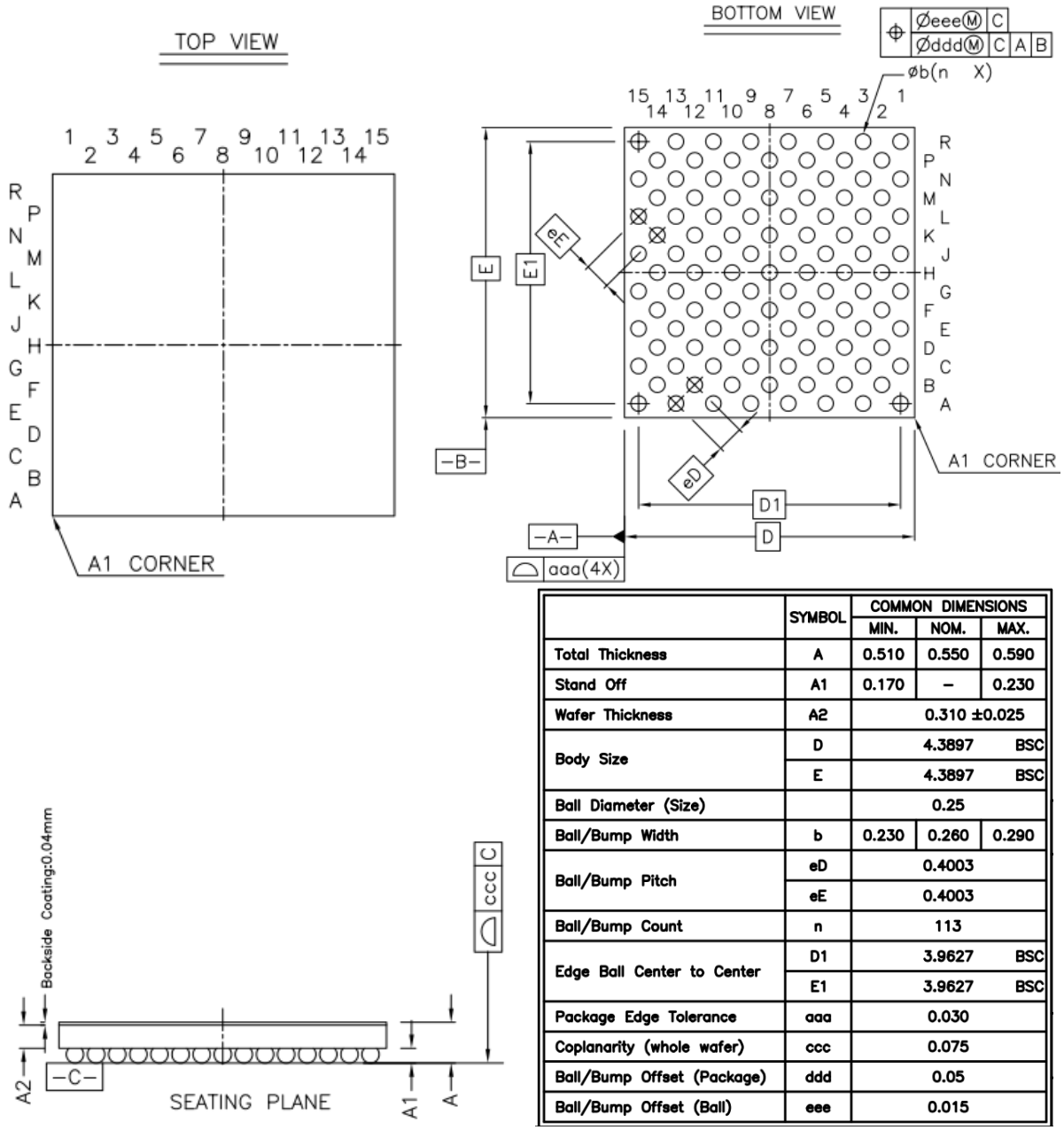


Parameter	Symbol	Min	Typ	Max	Units
SPI_CS falling edge to SPI_SCL rising edge	T_{CSS}	25			ns
SPI_SCL falling edge to SPI_CS rising edge	T_{CSE}	25			ns
SPI_SCL pulse period time	T_{CLK}	50			ns
SPI_SCL pulse high width	T_{CLK_H}	25			ns
SPI_SCL pulse low width	T_{CLK_L}	25			ns
SPI_MOSI setup time	T_{DAS}	13			ns
SPI_MOSI hold time	T_{DAH}	13			ns
SPI_MISO output time	T_{SDO}			13	ns

Figure 58. Slave SPI Interface AC Characteristic

11. Package Information

11.1. Mechanical Dimensions



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
Total Thickness	A	0.510	0.550	0.590
Stand Off	A1	0.170	–	0.230
Wafer Thickness	A2		0.310 ±0.025	
Body Size	D		4.3897 BSC	
	E		4.3897 BSC	
Ball Diameter (Size)			0.25	
Ball/Bump Width	b	0.230	0.260	0.290
Ball/Bump Pitch	eD		0.4003	
	eE		0.4003	
Ball/Bump Count	n		113	
Edge Ball Center to Center	D1		3.9627 BSC	
	E1		3.9627 BSC	
Package Edge Tolerance	aaa		0.030	
Coplanarity (whole wafer)	ccc		0.075	
Ball/Bump Offset (Package)	ddd		0.05	
Ball/Bump Offset (Ball)	eee		0.015	

Figure 59. Package Dimension

12. Ordering Information

Table 326. Ordering Information

Part Number	Package	Status
CM7120-GRT	113-Ball WLCSP (Tape & Reel)	MP