<IGBT Modules>

# CM75DY-34T

**HIGH POWER SWITCHING USE**
**INSULATED TYPE**

**dual switch (half-bridge)**

Collector current $I_C$ ..... **75** A
Collector-emitter voltage $V_{CES}$ ..... **1700** V
Maximum junction temperature $T_{vjmax}$ ..... **175** °C

- Flat base type
- Copper base plate (Nickel-plating)
- Nickel-plating tab terminals
- RoHS Directive compliant
- UL Recognized under UL1557, File No.E323585

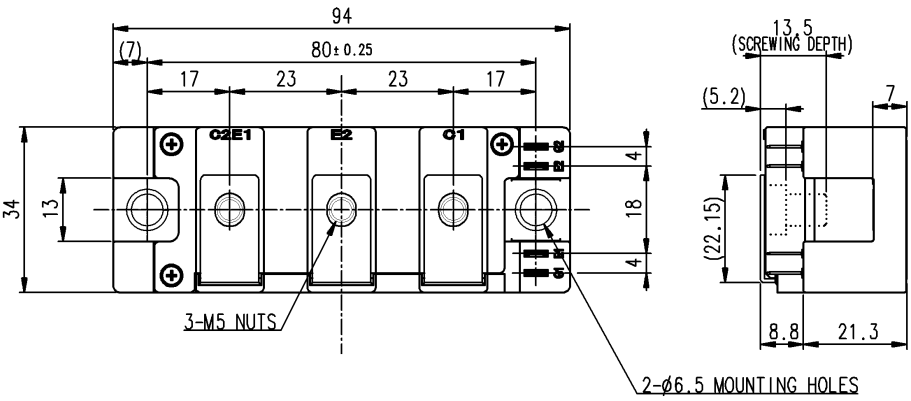
**APPLICATION**

AC Motor Control, Motion/Servo Control, Power supply, etc.

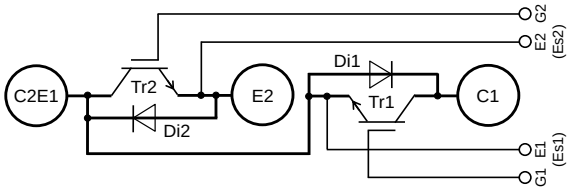
**OPTION** (Below options are available.)

- PC-TIM (Phase Change Thermal Interface Material) pre-apply

**OUTLINE DRAWING & INTERNAL CONNECTION** **Dimension in mm**




INTERNAL CONNECTION




Tolerance otherwise specified

| Division of Dimension | | Tolerance |
|---|---|---|
| 0.5 | to 3 | ±0.2 |
| over 3 | to 6 | ±0.3 |
| over 6 | to 30 | ±0.5 |
| over 30 | to 120 | ±0.8 |
| over 120 | to 400 | ±1.2 |

JIS B 0405 c

**MAXIMUM RATINGS ($T_{vj}$=25 °C, unless otherwise specified)**

| Symbol | Item | Conditions | Rating | Unit |
|---|---|---|---|---|
| $V_{CES}$ | Collector-emitter voltage | G-E short-circuited | 1700 | V |
| $V_{GES}$ | Gate-emitter voltage | C-E short-circuited | ± 20 | V |
| $I_C$ | Collector current | DC, $T_C$=137 °C* (Note2, 4) | 75 | A |
| $I_{CRM}$ | | Pulse, Repetitive (Note3) | 150 | |
| $P_{tot}$ | Total power dissipation | $T_C$=25 °C (Note2, 4) | 930 | W |
| $I_E$ (Note1) | Emitter current | DC (Note2) | 75 | A |
| $I_{ERM}$ (Note1) | | Pulse, Repetitive (Note3) | 150 | |
| $V_{isol}$ | Isolation voltage | Terminals to base plate, RMS, f=60 Hz, AC 1 min | 4000 | V |
| $T_{vjmax}$ | Maximum junction temperature | Instantaneous event (overload) | 175 | °C |
| $T_{Cmax}$ | Maximum case temperature | (Note4) | 150* | |
| $T_{vjop}$ | Operating junction temperature | Continuous operation (under switching) | -40 ~ +150 | °C |
| $T_{stg}$ | Storage temperature | - | -40 ~ +150* | |

**ELECTRICAL CHARACTERISTICS ($T_{vj}$=25 °C, unless otherwise specified)**

| Symbol | Item | Conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $I_{CES}$ | Collector-emitter cut-off current | $V_{CE}$=$V_{CES}$, G-E short-circuited | | - | - | 1.0 | mA |
| $I_{GES}$ | Gate-emitter leakage current | $V_{GE}$=$V_{GES}$, C-E short-circuited | | - | - | 0.5 | μA |
| $V_{GE(th)}$ | Gate-emitter threshold voltage | $I_C$=7.5 mA, $V_{CE}$=10 V | | 5.4 | 6.0 | 6.6 | V |
| $V_{CEsat}$ (Terminal) | Collector-emitter saturation voltage | $I_C$=75 A, $V_{GE}$=15 V, Refer to the figure of test circuit (Note5) | $T_{vj}$=25 °C | - | 2.0 | 2.45 | V |
| | | | $T_{vj}$=125 °C | - | 2.4 | - | |
| | | | $T_{vj}$=150 °C | - | 2.5 | - | |
| $V_{CEsat}$ (Chip) | | $I_C$=75 A, $V_{GE}$=15 V, (Note5) | $T_{vj}$=25 °C | - | 1.95 | 2.35 | V |
| | | | $T_{vj}$=125 °C | - | 2.35 | - | |
| | | | $T_{vj}$=150 °C | - | 2.45 | - | |
| $C_{ies}$ | Input capacitance | $V_{CE}$=10 V, G-E short-circuited | | - | - | 20.6 | nF |
| $C_{oes}$ | Output capacitance | | | - | - | 0.5 | |
| $C_{res}$ | Reverse transfer capacitance | | | - | - | 0.2 | |
| $Q_G$ | Gate charge | $V_{CC}$=1000 V, $I_C$=75 A, $V_{GE}$=15 V | | - | 0.62 | - | μC |
| $t_{d(on)}$ | Turn-on delay time | $V_{CC}$=1000 V, $I_C$=75 A, $V_{GE}$=±15 V, $R_G$=0 Ω, Inductive load | | - | - | 800 | ns |
| $t_r$ | Rise time | | | - | - | 200 | |
| $t_{d(off)}$ | Turn-off delay time | | | - | - | 800 | |
| $t_f$ | Fall time | | | - | - | 600 | |
| $V_{EC}$ (Note.1) (Terminal) | Emitter-collector voltage | $I_E$=75 A, G-E short-circuited, Refer to the figure of test circuit (Note5) | $T_{vj}$=25 °C | - | 2.7 | 3.3 | V |
| | | | $T_{vj}$=125 °C | - | 2.9 | - | |
| | | | $T_{vj}$=150 °C | - | 2.9 | - | |
| $V_{EC}$ (Note.1) (Chip) | | $I_E$=75 A, G-E short-circuited, (Note5) | $T_{vj}$=25 °C | - | 2.65 | 3.20 | V |
| | | | $T_{vj}$=125 °C | - | 2.75 | - | |
| | | | $T_{vj}$=150 °C | - | 2.75 | - | |
| $t_{rr}$ (Note1) | Reverse recovery time | $V_{CC}$=1000 V, $I_E$=75 A, $V_{GE}$=±15 V, $R_G$=0 Ω, Inductive load | | - | - | 300 | ns |
| $Q_{rr}$ (Note1) | Reverse recovery charge | | | - | 3.8 | - | μC |
| $E_{on}$ | Turn-on switching energy per pulse | $V_{CC}$=1000 V, $I_C$=$I_E$=75 A, $V_{GE}$=±15 V, $R_G$=0 Ω, $T_{vj}$=150 °C, Inductive load | | - | 22 | - | mJ |
| $E_{off}$ | Turn-off switching energy per pulse | | | - | 21 | - | |
| $E_{rr}$ (Note1) | Reverse recovery energy per pulse | | | - | 8.57 | - | mJ |
| $R_{CC'+EE'}$ | Internal lead resistance | Main terminals-chip, per switch, $T_C$=25 °C (Note4) | | - | 0.2 | - | mΩ |
| $r_g$ | Internal gate resistance | Per switch | | - | 10 | - | Ω |

*: The value of PC-TIM applied module is limited by the heat resistant temperature of PC-TIM.

## THERMAL RESISTANCE CHARACTERISTICS

| Symbol | Item | Conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $R_{th(j-c)Q}$ | Thermal resistance | Junction to case, per Inverter IGBT (Note4) | | - | - | 161 | K/kW |
| $R_{th(j-c)D}$ | | Junction to case, per Inverter FWD (Note4) | | - | - | 231 | |
| $R_{th(c-s)}$ | Contact thermal resistance | Case to heat sink, per 1 module | Thermal grease applied (Note4, 6) | - | 36.6 | - | K/kW |

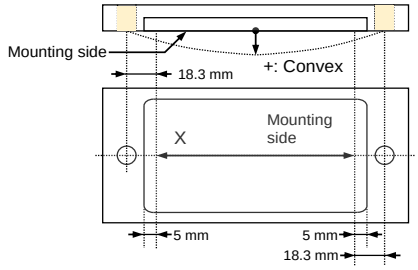
## MECHANICAL CHARACTERISTICS

| Symbol | Item | Conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $M_t$ | Mounting torque | Main terminals | M 5 screw | 2.5 | 3.0 | 3.5 | N·m |
| $M_s$ | Mounting torque | Mounting to heat sink | M 6 screw | 3.5 | 4.0 | 4.5 | N·m |
| $d_s$ | Creepage distance | Terminal to terminal | | 18.4 | - | - | mm |
| | | Terminal to base plate | | 21.1 | - | - | |
| $d_a$ | Clearance | Terminal to terminal | | 9.6 | - | - | mm |
| | | Terminal to base plate | | 16.7 | - | - | |
| $e_c$ | Flatness of base plate | On the centerline X, Y (Note7) | | ±0 | - | +200 | μm |
| m | mass | - | | - | 120 | - | g |

*: This product is compliant with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) directive 2011/65/EU.

Note1. Represent ratings and characteristics of the anti-parallel, emitter-collector free-wheeling diode (FWD).

2. Junction temperature ($T_{vj}$) should not increase beyond $T_{vjmax}$ rating.
3. Pulse width and repetition rate should be such that the device junction temperature ($T_{vj}$) dose not exceed $T_{vjmax}$ rating.
4. Case temperature ($T_C$) and heat sink temperature ($T_S$) are defined on the each surface (mounting side) of base plate and heat sink just under the chips. Refer to the figure of chip location.
5. Pulse width and repetition rate should be such as to cause negligible temperature rise. Refer to the figure of test circuit.
6. Typical value is measured by using thermally conductive grease of $\lambda$=3.0W/(m·K)/$D_{(C-S)}$=50 μm.
7. The base plate (mounting side) flatness measurement points (X, Y) are shown in the following figure.

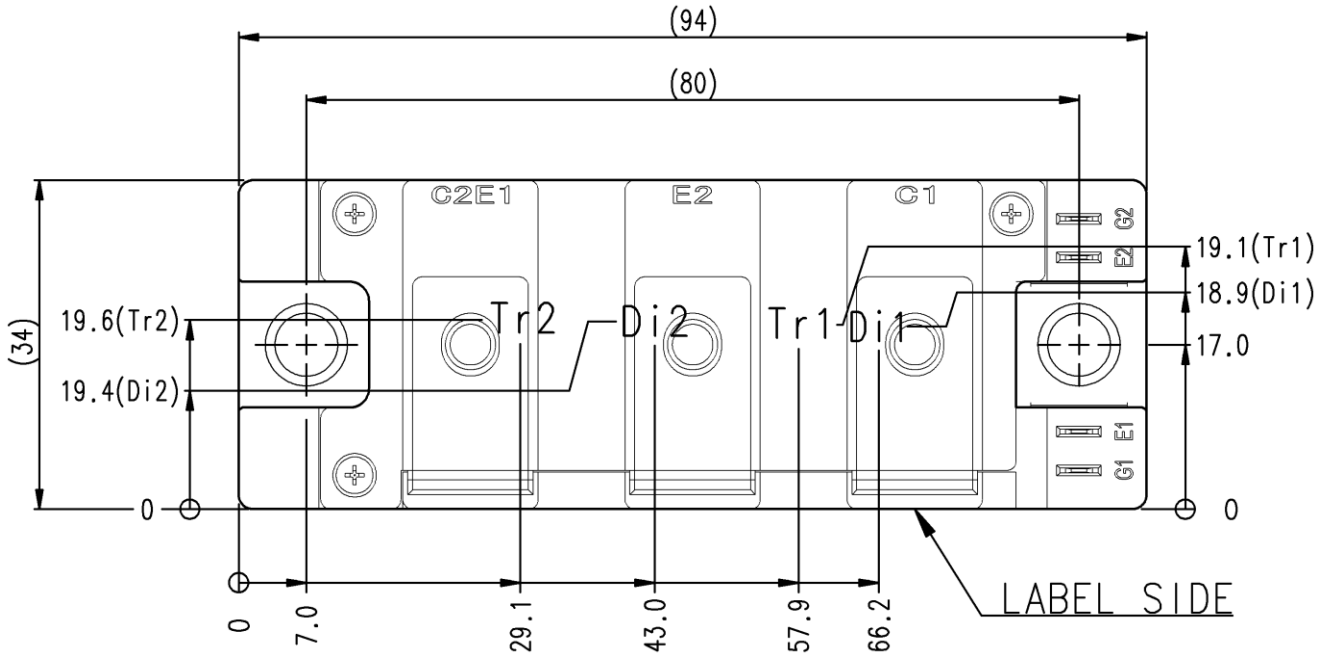


**RECMENDED OPERATING CONDITIONS**

| Symbol | Item | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{CC}$ | (DC) Supply voltage | Applied across C1-E2 terminals | - | 1000 | 1200 | V |
| $V_{GEon}$ | Gate (-emitter drive) voltage | Applied across G1-Es1/G2-Es2 terminals | 13.5 | 15.0 | 16.5 | V |
| $R_G$ | External gate resistance | Per switch | 0 | - | 91 | Ω |

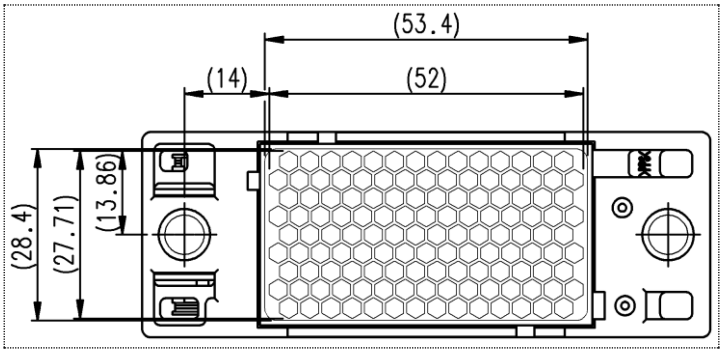
**CHIP LOCATION (Top view)**

Dimension in mm, tolerance: ±1 mm

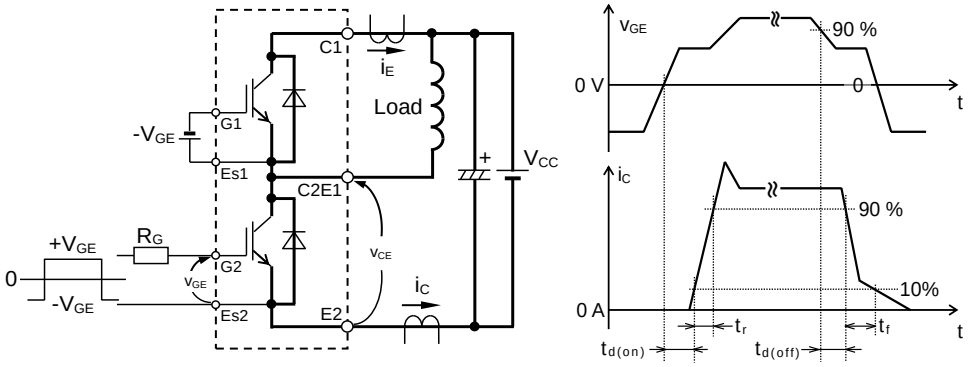



Tr1/Tr2: IGBT, Di1/Di2: FWD

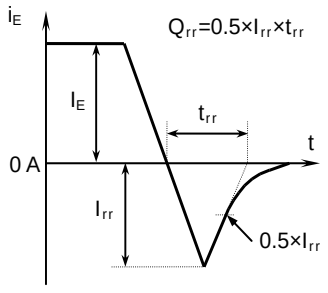
**Option: PC-TIM applied baseplate outline**



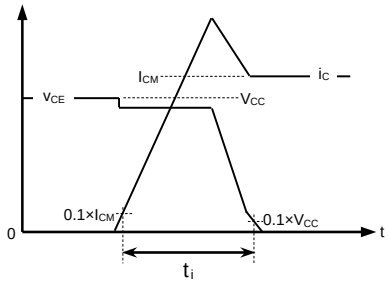
**TEST CIRCUIT AND WAVEFORMS**



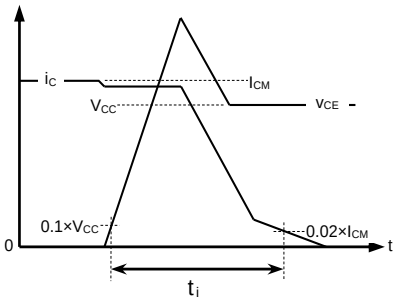

Switching characteristics test circuit and waveforms



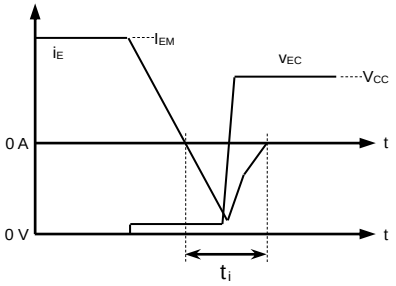

$t_{rr}$, $Q_{rr}$ characteristics test waveform




IGBT Turn-on switching energy



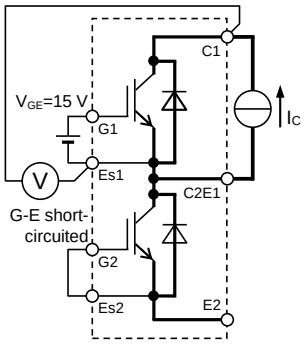

IGBT Turn-off switching energy



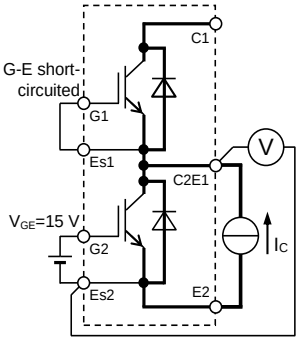

FWD Reverse recovery energy

Turn-on / Turn-off switching energy and Reverse recovery energy test waveforms (Integral time instruction drawing)

**TEST CIRCUIT**

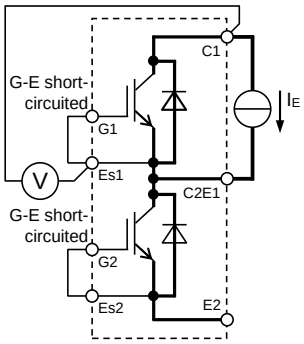



Tr1

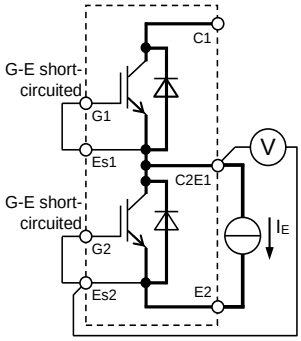



Tr2

$V_{CEsat}$ characteristics test circuit




Di1

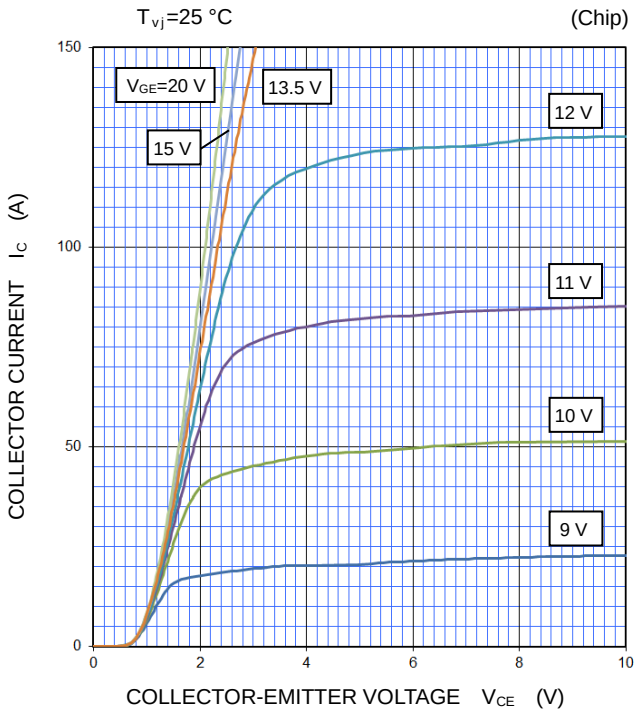



Di2

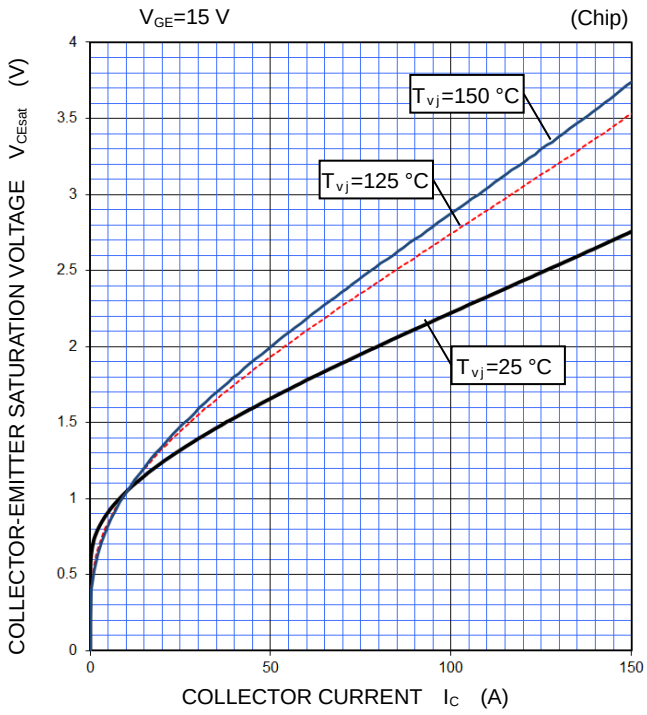
$V_{EC}$ characteristics test circuit

## PERFORMANCE CURVES

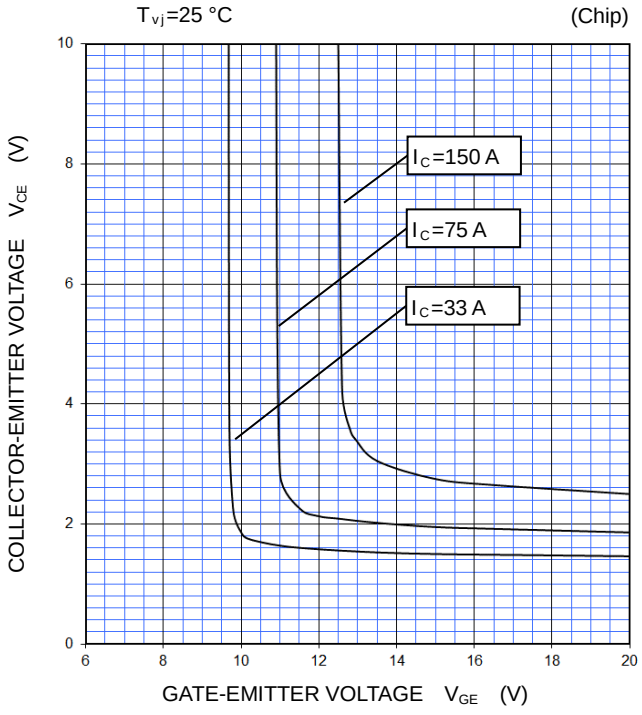
### OUTPUT CHARACTERISTICS (TYPICAL)



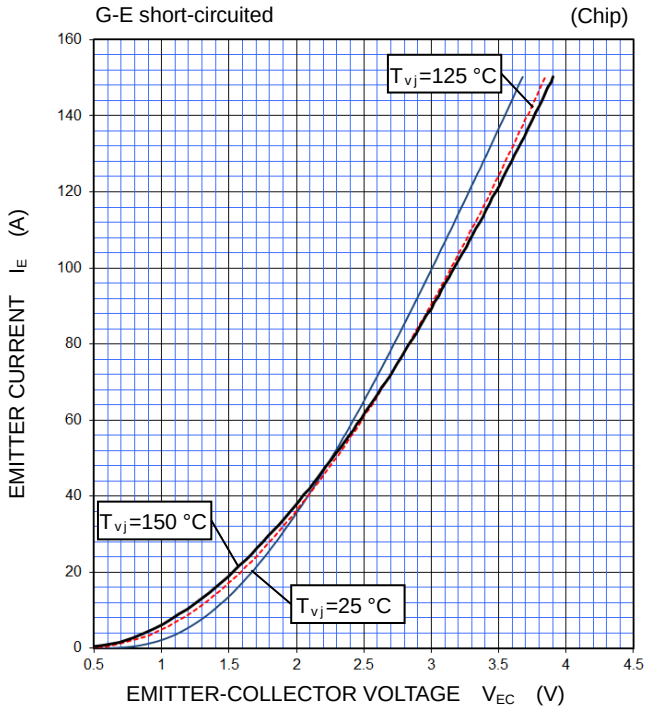

### COLLECTOR-EMITTER SATURATION VOLTAGE CHARACTERISTICS (TYPICAL)




### COLLECTOR-EMITTER VOLTAGE CHARACTERISTICS (TYPICAL)



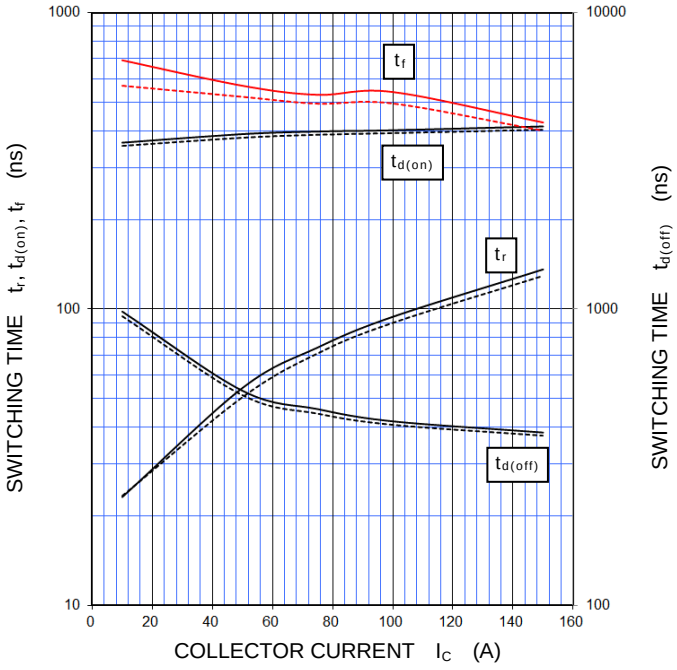

### FREE WHEELING DIODE FORWARD CHARACTERISTICS (TYPICAL)



## PERFORMANCE CURVES

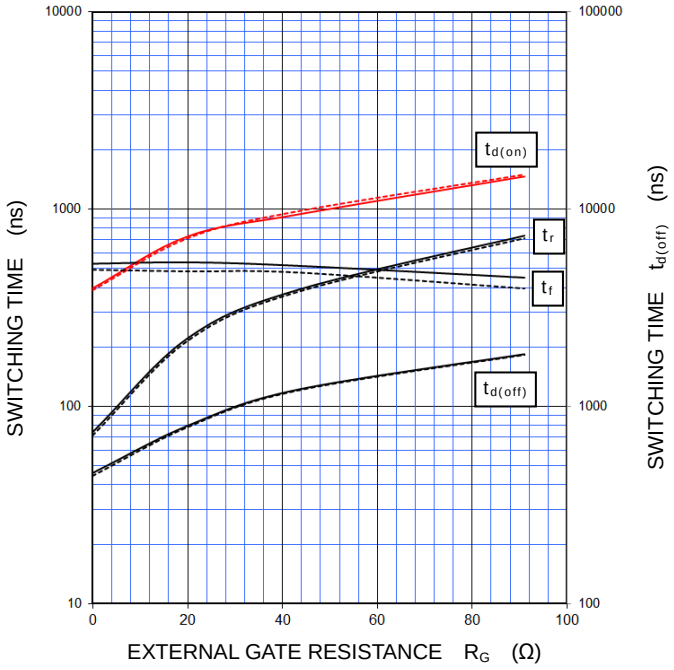
### HALF-BRIDGE SWITCHING CHARACTERISTICS (TYPICAL)

$V_{CC}$=1000 V, $V_{GE}$=±15 V, $R_G$=0 Ω, INDUCTIVE LOAD
———: $T_{vj}$=150 °C, - - - - -: $T_{vj}$=125 °C



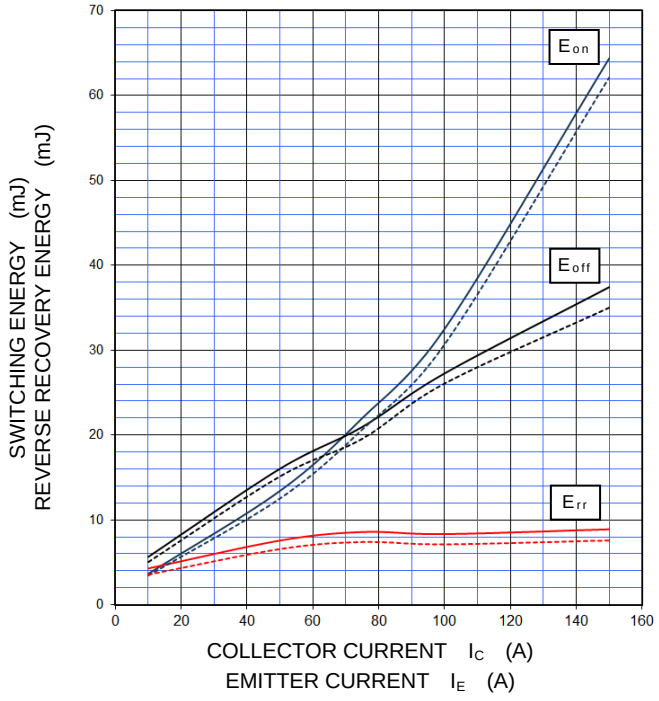

### HALF-BRIDGE SWITCHING CHARACTERISTICS (TYPICAL)

$V_{CC}$=1000 V, $V_{GE}$=±15 V, $I_C$=75 A, INDUCTIVE LOAD
———: $T_{vj}$=150 °C, - - - - -: $T_{vj}$=125 °C



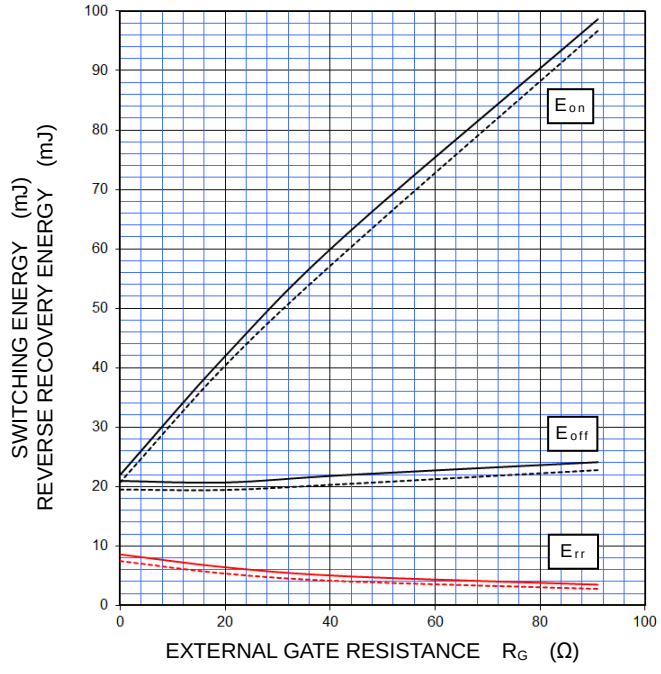

### HALF-BRIDGE SWITCHING CHARACTERISTICS (TYPICAL)

$V_{CC}$=1000 V, $V_{GE}$=±15 V, $R_G$=0 Ω, INDUCTIVE LOAD
———: $T_{vj}$=150 °C, - - - - -: $T_{vj}$=125 °C




### HALF-BRIDGE SWITCHING CHARACTERISTICS (TYPICAL)

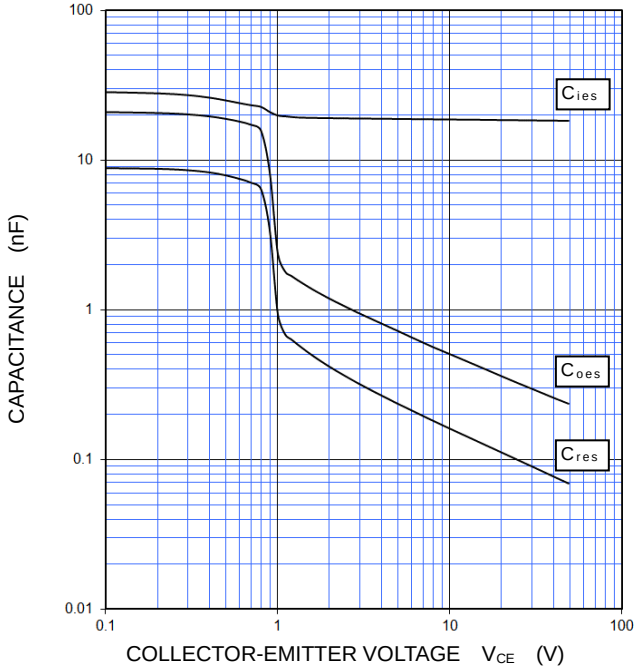
$V_{CC}$=1000 V, $V_{GE}$=±15 V, $I_C$=75 A, INDUCTIVE LOAD
———: $T_{vj}$=150 °C, - - - - -: $T_{vj}$=125 °C



## PERFORMANCE CURVES

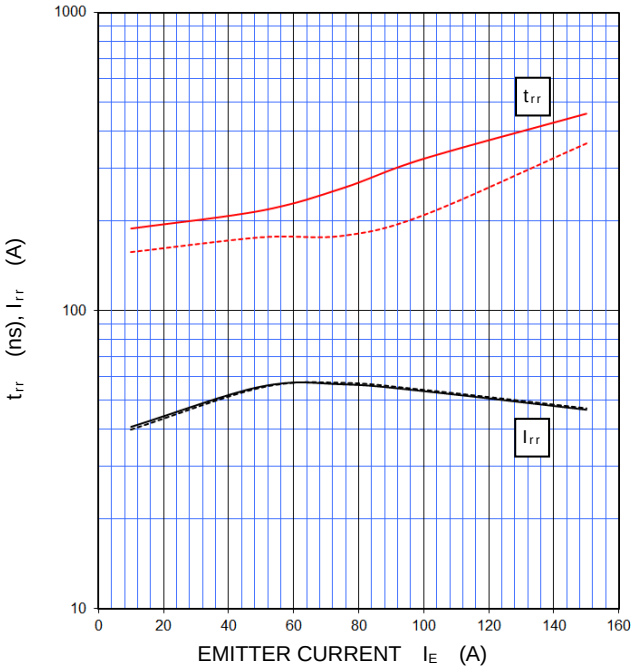
### CAPACITANCE CHARACTERISTICS (TYPICAL)

G-E short-circuited, $T_{vj}$=25 °C



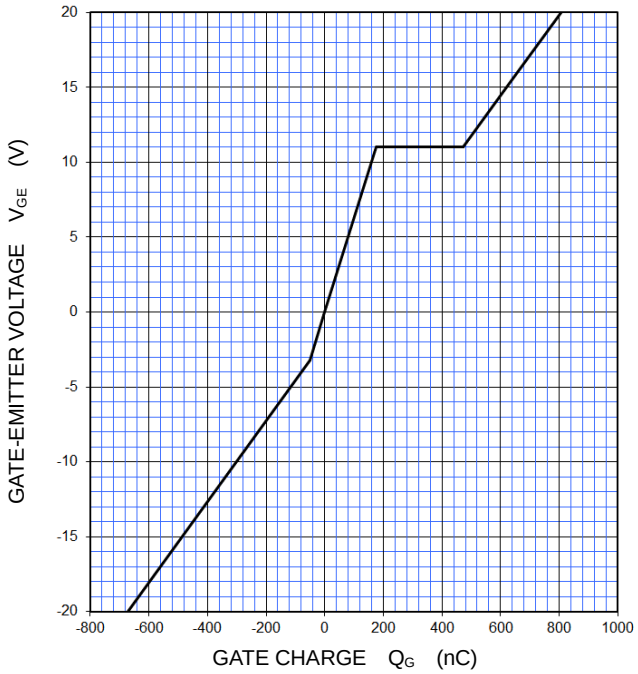

### FREE WHEELING DIODE REVERSE RECOVERY CHARACTERISTICS (TYPICAL)

$V_{CC}$=1000 V, $V_{GE}$=±15 V, $R_G$=0 Ω, INDUCTIVE LOAD
———: $T_{vj}$=150 °C, - - - - -: $T_{vj}$=125 °C



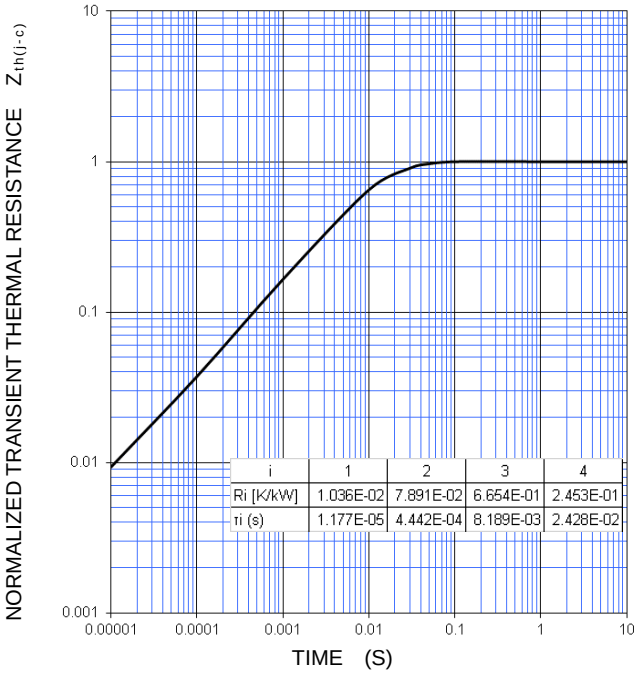

### GATE CHARGE CHARACTERISTICS (TYPICAL)

$V_{CC}$=1000 V, $I_C$=75 A, $T_{vj}$=25 °C




### TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (MAXIMUM)

Single pulse, $T_C$=25 °C
$R_{th(j-c)Q}$=161 K/kW, $R_{th(j-c)D}$=231 K/kW



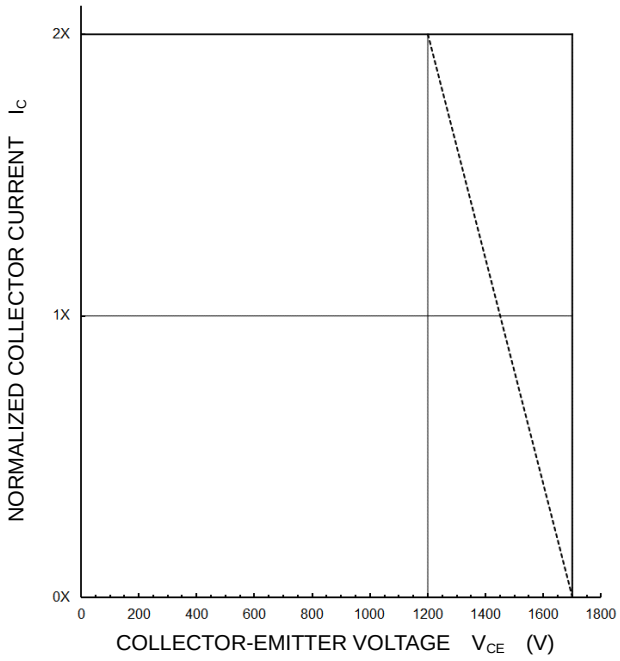

| i | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| Ri [K/kW] | 1.036E-02 | 7.891E-02 | 6.654E-01 | 2.453E-01 |
| ti (s) | 1.177E-05 | 4.442E-04 | 8.189E-03 | 2.428E-02 |

Note: The characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

**PERFORMANCE CURVES**

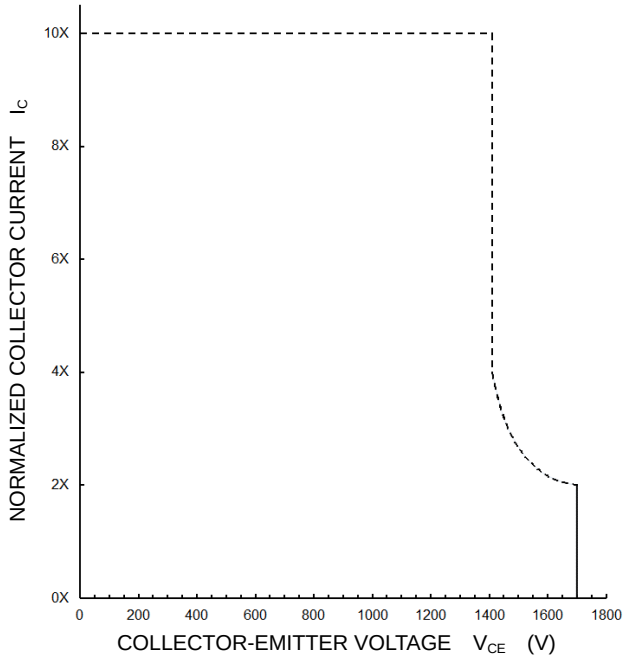
**TURN-OFF SWITCHING SAFE OPERATING AREA (REVERSE BIAS SAFE OPERATING AREA) (MAXIMUM)**

$V_{CC}$≤1200 V, $V_{GE}$=±15 V, $R_G$=0~91 Ω,
———: $T_{vj}$=25~150 °C (Normal load operations (Continuous)
- - - - - -: $T_{vj}$=175 °C (Unusual load operations (Limited period)




**SHORT-CIRCUIT SAFE OPERATING AREA (MAXIMUM)**

$V_{CC}$≤1200 V, $V_{GE}$=±15 V, $R_G$=0~91 Ω,
$T_{vj}$= 25 ~ 150 °C, $t_W$≤8 μs, Non-Repetitive



## Keep safety first in your circuit designs!

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In the customer's research and development, please evaluate it not only with a single semiconductor product but also in the entire system, and judge whether it's applicable. Furthermore, trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits (e.g. appropriate fuse or circuit breaker between a power supply and semiconductor products), (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

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