CM8563

1.5A LINEAR BUS TERMINATION REGULATOR

GENERAL DESCRIPTION

The CM8563 is a low cost linear regulator designed to provide a desired output voltage or termination voltage for various applications. The device contains a high-speed operational amplifier to provide excellent response to load transients. The CM8563 is capable of sourcing or sinking up to 1.5A, and peaks up to 3A of current while regulating an output VOUT voltage to meet the JEDEC SSTL-2 and SSTL-3 specification. .

The CM8563 also incorporates a VFB pin to provide superior load regulation and a VREF output as a reference for the chipset and DDR DIMMS.

The CM8563 provides low profile 8-pin SOIC package to save system space.

FEATURES

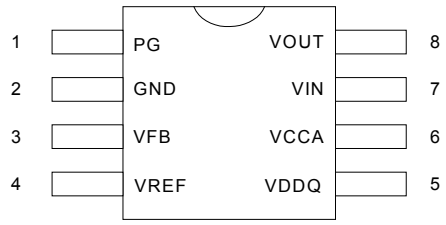
- Ideal for DDR-I and DDR-II
- 8-pin SOIC package
- Source and sink up to 1.5A, no heat sink required
- Integrated power MOSFETs
- No external resistors required
- Minimum external components

APPLICATIONS

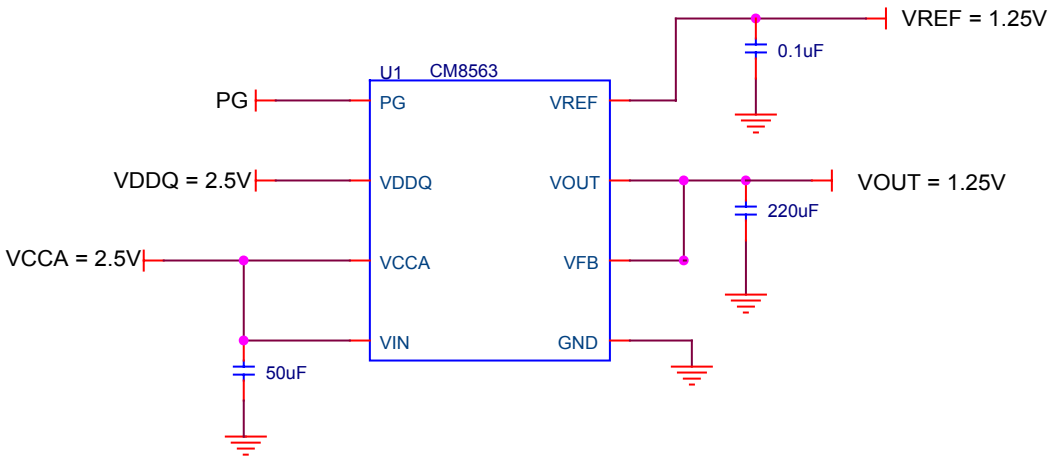
- Mother Board
- PCI/AGP Graphics
- DDR Termination Voltage (SSTL-2 & SSTL-3)

PIN CONFIGURATION

SOP-8 (S08)
Top View



TYPICAL APPLICATION



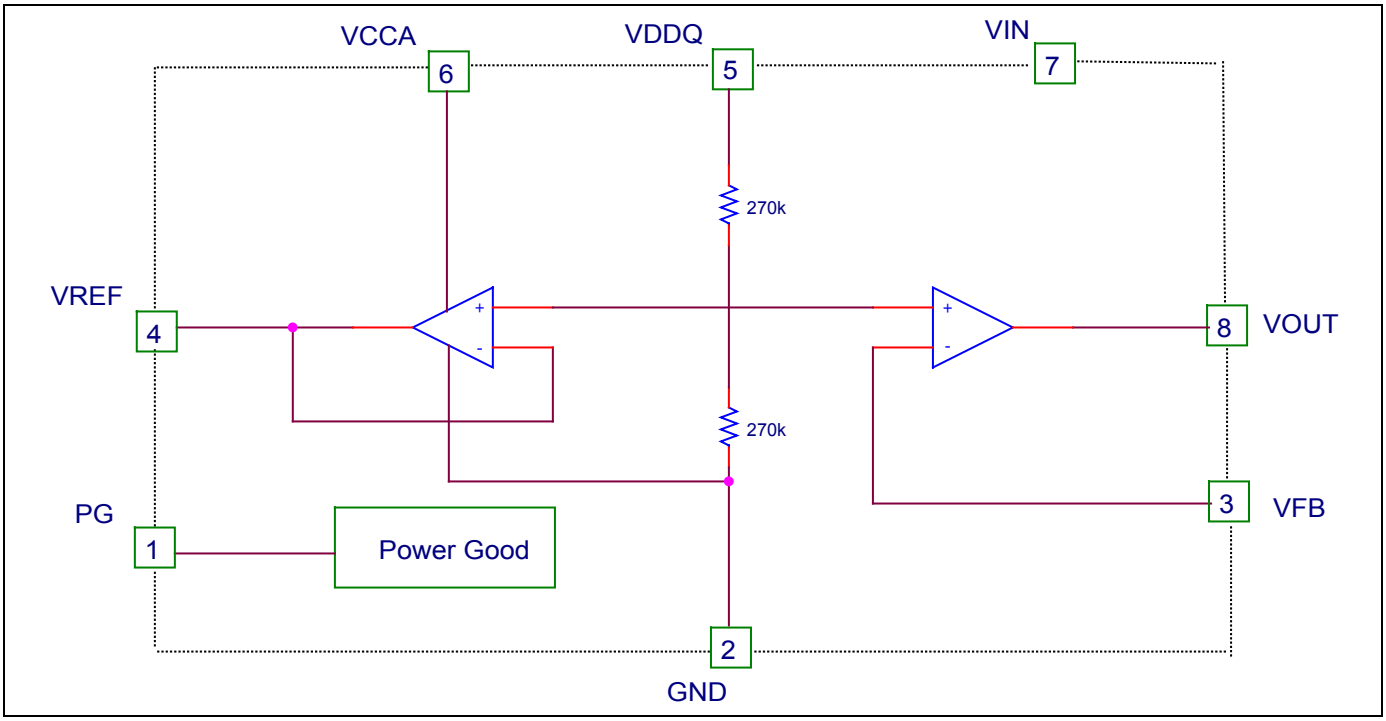
PIN DESCRIPTION

Pin No.	Symbol	Description
1	PG	Power Good
2	GND	Ground
3	VFB	Feedback pin for regulating VOUT
4	VREF	Buffered reference Voltage
5	VDDQ	Input for internal reference equal to VDDQ/2
6	VCCA	Analog input
7	VIN	Power input
8	VOUT	Output voltage for connection to termination resistors

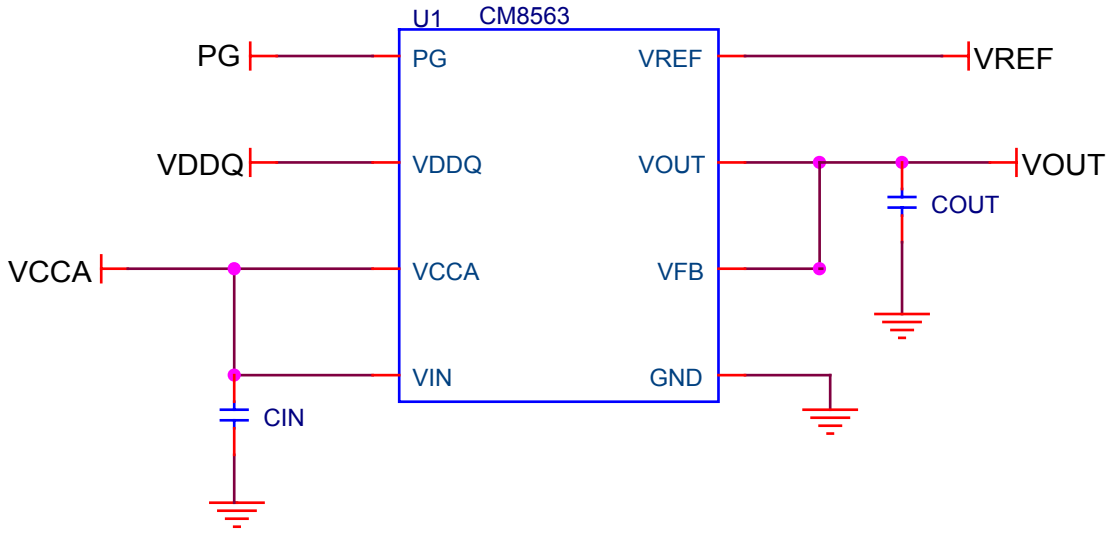
ORDERING INFORMATION

Part Number	Temperature Range	Package
CM8563IS	-40℃ to 85℃	8-Pin SOP (S08)
CM8563PIS	-40℃ to 85℃	8-Pin PSOP (PS08)

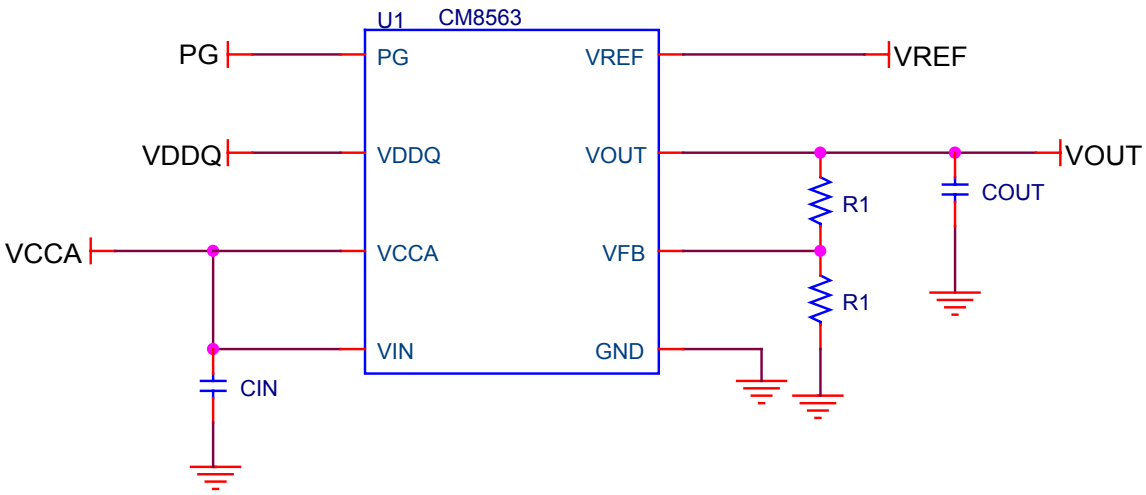
BLOCK DIAGRAM



APPLICATION CIRCUITS



Application Circuit for Bus Termination



Application Circuit for Adjustable Output Voltage

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged.

VIN, VCCA, VDDQ to GND ..... –0.3V to 6V
Storage Temperature ..... -65°C to 150°C
Lead Temperature (Soldering, 5 sec)..... 260°C
Thermal Resistance(θ_{JC})..... .14°C/W (PSOP-8)
Thermal Resistance(θ_{JC})..... 15.7°C/W (SOP-8)

OPERATING RANGE (Note 1)

Junction Temperature Range (Note 2) ..... 0°C to 125°C
VCCA to GND ..... 2.2V to 5.5V
VIN to GND ..... 2.2V to VCCA

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply T_A=25°C; VCCA=VIN=+2.5V and VDDQ=+2.5V (Note 3)) maximum ratings are stress ratings only and functional device operation is not implied.

Symbol	Parameter	Test Conditions	CM8563			Unit
			Min.	Typ.	Max.	
V_{REF}	VREF Voltage	I_{REFOUT}=0mA	1.21	1.235	1.26	V
V_{OS}	VOUT Output Voltage Offset	I_{OUT}=0A (Note 4)	-15 -20	0	15 20	mV
$\lvert \Delta V_{LOAD} \rvert$	Load Regulation (Note 5)	I_{OUT}: 0A -> 1.5A		0.5		%
		I_{OUT}: 0A -> -1.5A		-0.5		%
Z_{VREF}	VREF Output Impedance	I_{REF}= -5uA to +5uA		5		kΩ
Z_{VDDQ}	VDDQ Output Impedance			540		kΩ
I_{CCQ}	Quiescent Current	I_{OUT}=0A (Note 6)		250	400	μA
Power Good (Note 7)						

Note 1: Operating range indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specification and test conditions see Electrical Characteristics.

Note 2: At elevated temperatures, devices must be derated based on the thermal resistance. The SO-8 package must be derated at θ_{JA} = 151℃/W junction to ambient with no heat sink.

Note 3: Limits are 100% production tested at 25℃. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control methods.

Note 4: VOS = VREF – VOUT

Note 5: Load regulation is tested by using a 10ms current pulse and measuring VOUT.

Note 6: Quiescent current defined as the current flow into VCCA.

Note 7: PG function but LP2995 does not have it. PG will be high as VTT is larger than 90% VREF, and PG will change to low as VTT is lower than 85% VREF. PG also will be low as VTT is greater than 115% VREF, and PG will change to high as VTT is lower than 110% VREF. It has both directions PG function.

FUNCTIONAL DESCRIPTION

The CM8563 is a linear bus termination regulator designed to meet the JEDEC requirements of SSTL-2 and SSTL-3. The CM8563 is capable of sinking and sourcing current at the output VOUT, regulating the voltage to equal VDDQ/2. A buffered reference voltage that also tracks VDDQ/2 is generated on the VREF pin for providing a global reference to the DDR-SDRAM and Northbridge Chipset. VOUT is designed to track the VREF voltage with a tight tolerance over the entire current range while preventing shoot through on the output stage.

The CM8563 integrates power MOSFETs that are capable of source and sink 1.5A of current while maintaining excellent voltage regulation. The output voltage can be regulated within 3% or less by using the external feedback. Separate voltage supply inputs have been added to fit applications with various power supplies for the databus and power buses.

Pin Description

VCCA & VIN

VCCA and VIN are the input supply pins for the CM8563. VCCA is used to supply all the internal control circuitry for the two op-amps and the output stage of VREF. VIN is used exclusively to provide the rail voltage for the output stage on the power operational amplifier used to the 2.5V rail for optimal performance. This eliminates the need for bypassing the two supply pins separately.

VDDQ

VDDQ is the input that is used to create the internal reference voltage for regulating VOUT and VREF. This voltage is generated by two internal 270kΩ resistors. This guarantees that VOUT and VREF will track VDDQ/2 precisely.

VFB

The purpose of the VFB pin is to provide improved remote load regulation. In most motherboard applications the termination resistors will connect to VOUT in a long plane. If the output voltage was regulated only at the output of the CM8563, then the long trace will cause a significant IR drop, resulting in a termination voltage lower at one end of the bus than the other. The VFB pin can be used to improve this performance, by connecting it to the middle of the bus. This will provide a better distribution across the entire termination bus.

VREF

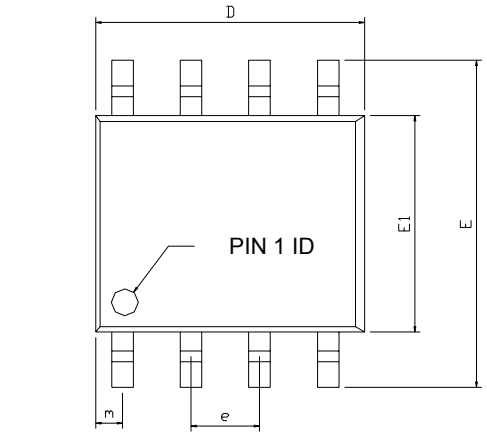
VREF provides the buffered output of the internal reference voltage VDDQ/2. This output should be used to provide the reference voltage of Northbridge chipset and memory.

VOUT

VOUT is the regulated output that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output precisely to VDDQ/2. The CM8563 is designed to handle peak transient currents of up to +/- 3A with a fast transient response. The maximum continuous current is a function of VIN. If a transient is expected to last above the maximum continuous current rating for a significant amount of time then the output capacitor should be sized large enough to prevent an excessive voltage drop.

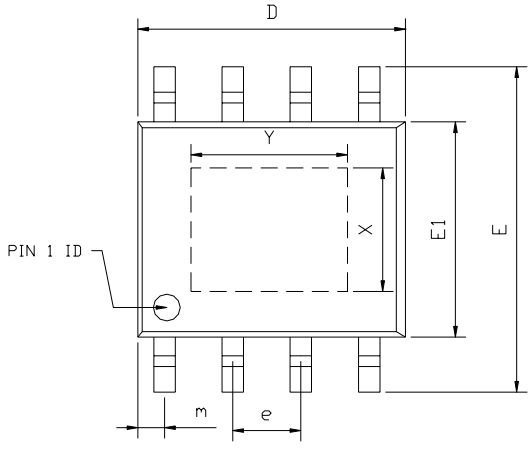
PACKAGE DIMENSION

8-Pin SOP (S08)



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A1	0.10	---	0.25	0.004	---	0.010
A2	1.40	---	1.55	0.055	---	0.061
b	0.30	---	0.51	0.012	---	0.020
C	0.15	---	0.26	0.006	---	0.010
D	4.60	---	5.06	0.169	---	0.199
E	5.79	---	6.20	0.228	---	0.244
E1	3.76	---	4.01	0.148	---	0.158
e	---	1.27	---	---	0.050	---
L	0.38	---	0.69	0.015	---	0.035
m	0.43	---	0.69	0.017	---	0.027
θ	0°	---	8°	0°	---	8°

8-Pin SOP w/ Power Pad (PS08)



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m	0.43	---	0.69	0.017	---	0.027
θ	0°	---	8°	0°	---	8°

EXPOSED PAD DIMENSION : (mm)
PAD SIZE: X=2.34 ; Y=2.92

IMPORTANT NOTICE

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