Oxygen™ Express CM8828

High Performance PCI Express Audio Processor

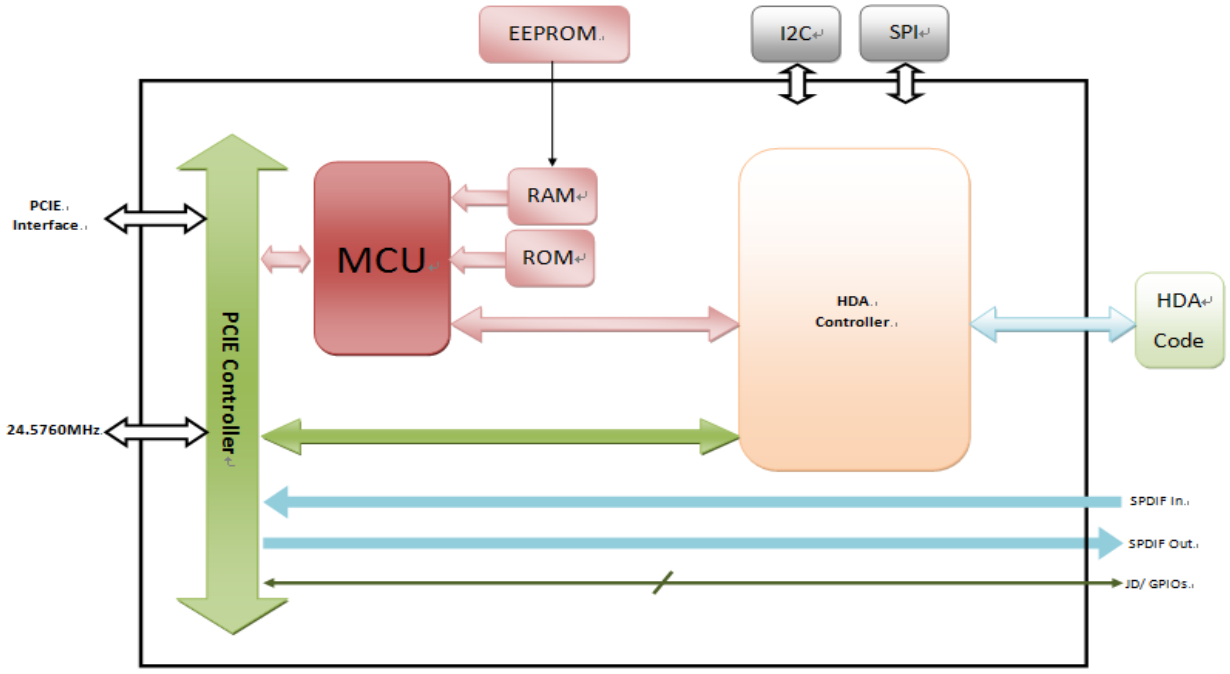
DESCRIPTION

The Oxygen Express™ HD CM8828 is a high quality PCI express multi-channel audio processor that not only an Intel HD Audio specification compatible audio single chip, but also can be a controller which can link HDA codec. CM8828 can be built in the home audio electronics or personal computer to provide high fidelity sound and become a professional audio processing center in your life. It supports up to 10 outgoing channels and 6 ingoing channels. The 10 outgoing channels are composed of 2 playback DMA's, which are multi-channel DMA (24 bits, 8 channels, 192k), Headphone out & S/PDIF (each 24 bits, 2 channels, 192k), and RTC (real-time communication) DMA (24 bits, 2 channels, 192k). The 6 ingoing channels are spread in 3 recording DMA's (up to 24 bits, 192k).

FEATURES

- Compatible with PCI Express 1.1 interface with bus mastering and burst modes
- Embedded an 8051-based MCU to transcode HD Audio command s(An external 4 or 8KB serial EEPROM is required
  Build in HD Audio controller.
  Audio format supports 192K/176.4K/96K/88.2K/48K/44.1K and 16/24bits resolution
- integrated 192K/176.4K/96K/88.2K/48K/44.1K, and 16/24-bit S/PDIF transmitter/Receiver
- Supports SPI/I2C control interface
- 24.576MHz crystal input required with embedded PLL for adaptive clock rate
- Win7/8 WHQL compatible

Block Diagram



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Revision History

Date	Rev.	Release Note
2011/11/11	Rev. 0.9	First release
		-modify 3.3v power range -add power consumption data
2012/05/07	Rev. 0.95	-modify pin definition table -modify block diagram -modify software and features
2013/09/13	Rev. 1.0	Formal release

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1. Description and Overview

The Oxygen Express™ HD CM8828 is a high quality PCI express multi-channel audio processor that not only an Intel HD Audio specification compatible audio single chip, but also can be a controller which can connect HDA codec. CM8828 can be built in the home audio electronics or personal computer to provide high fidelity sound and become a professional audio processing center in your life. It supports up to 10 outgoing channels and 6 ingoing channels. The 10 outgoing channels are composed of 2 playback DMA's, which are multi-channel DMA (24 bits, 8 channels, 192k), Headphone out & S/PDIF DMA (each 24 bits, 2 channels, 192k). The 6 ingoing channels are spread in 3 recording DMA's (up to 24 bits, 192k).

The Oxygen Express™ HD CM8828 is a MCU-based audio processor which can co-work with all the usual HDA codecs. The audio topology for HDA spec. can be flexible by only changing the Firmware. This ability gives customers the flexibility to design their products. The HDA-Link, 2-wire master bus, and SPI interfaces are used to transfer audio data and control data between the CM8828 and codecs. To facilitate the connection with the existing home audio electronics, the CM8828 has incorporated the S/PDIF transmitter with 192k sampling rate in it.

A master I2C interface is built in to connect with the serial EEPROM to store and retrieve the non-evaporable data for firmware code and the customer applications, such as board configuration, sub-vender and sub-system IDs, or any dynamic data that customers want to save for the next power-on to restore.

The Oxygen Express™ HD CM8828 has an independent 2-wire slave bus to communicate with micro control unit (MCU). Strictly speaking, this interface is used as a media for system driver and MCU to talk. There are nine GPIOs pins, which can be used to distinguish if a device is plugged in the phone jack or other purpose.

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2. Features

Bus

- Compatible with PCI Express 1.1 interface with bus mastering and burst modes

Architecture

- Build in HD Audio controller
- Embedded an 8051-based MCU to transcode HD Audio command to accommodate various external HDA codecs (An external 4 or 8KB serial EEPROM is required]
- Embedded ROM code for MCU to transcode HD Audio command to control embedded HDA codecs
- Analog mixer to mix all input data to output streams through HDA codecs

DMA Controller

- Three playback DMAs and three recording DMAs following Vista/Win7 HD Audio controller requirements and to be WaveRT-port-friendly:
- Playback DMA#A supports up to 8ch audio output (2,4,6,8CH configurable by SW driver control)
- Playback DMA#B supports independent 2ch audio output (e.g. Front Headphone Out) or S/PDIF
- Recording DMA#A supports up to 2ch audio input
- Recording DMA#B supports independent 2ch audio input
- Recording DMA#C supports independent 2ch audio input (for S/PDIF input stream or other purpose)
- Sampling rates: all DMA channels support: 192K/176.4K/96K/88.2K/48K/44.1K PCM data
- Resolution (Word-length): all DMA channels support: 16/24bit PCM data transfer modes

Audio I/O

- Intel HD Audio Link supports 1 external HDA codec
- Integrated 192K/176.4K/96K/88.2K/48K/44.1K, and 16/24-bit S/PDIF transmitter

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- All input data can be analog mixed to output streams

Control Interface

- SPI control interfaces
- I^2C Interface supports both Master and Slave mode
- Interrupt pin for external MCU read transaction
- Serial EEPROM programming interface for customizing Sub-VendorID/Sub-DeviceID (and even Vendor/Device IDs as well), storing HDA power-on pin configuration (replacing MB BIOS function) and 8051 ROM-codes (HDA command transcoder)
- Maximum 9 GPIO pins for external devices control and various purposes

General

- Compliant with Microsoft Win7/8 UAA design guideline and driver
- Pass Windows 7 audio logo certification
- 24.576MHz crystal input required with embedded PLL for adaptive clock rate
- Single 3.3V power supply
- 3.3 V digital I/O pads with 5V tolerance
- Package and Pin Number: LQFP-80
- Default target codec: CM9882A

□

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3. Applications

- High Definition PCIe sound cards for retailer market
- Pro-Audio / High-End studio applications
- Gaming audio devices
- Bundle selling with high-profile VGA cards or motherboard
- Embedded system / Industrial computer audio

4. Software and Features

- Xear™ Living 1.1
- Xear™ VoClear
- Xear™ Sonic
- Xear™ Surround
- Xear™ Pro 1.0
- Xear™ SingFX
- Xear™ MagicVoice
- Face Lift UI(including customizable graphics and layout)
- Stereo mix (Line-in, Mic-in and Wave files)

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5. Block Diagram

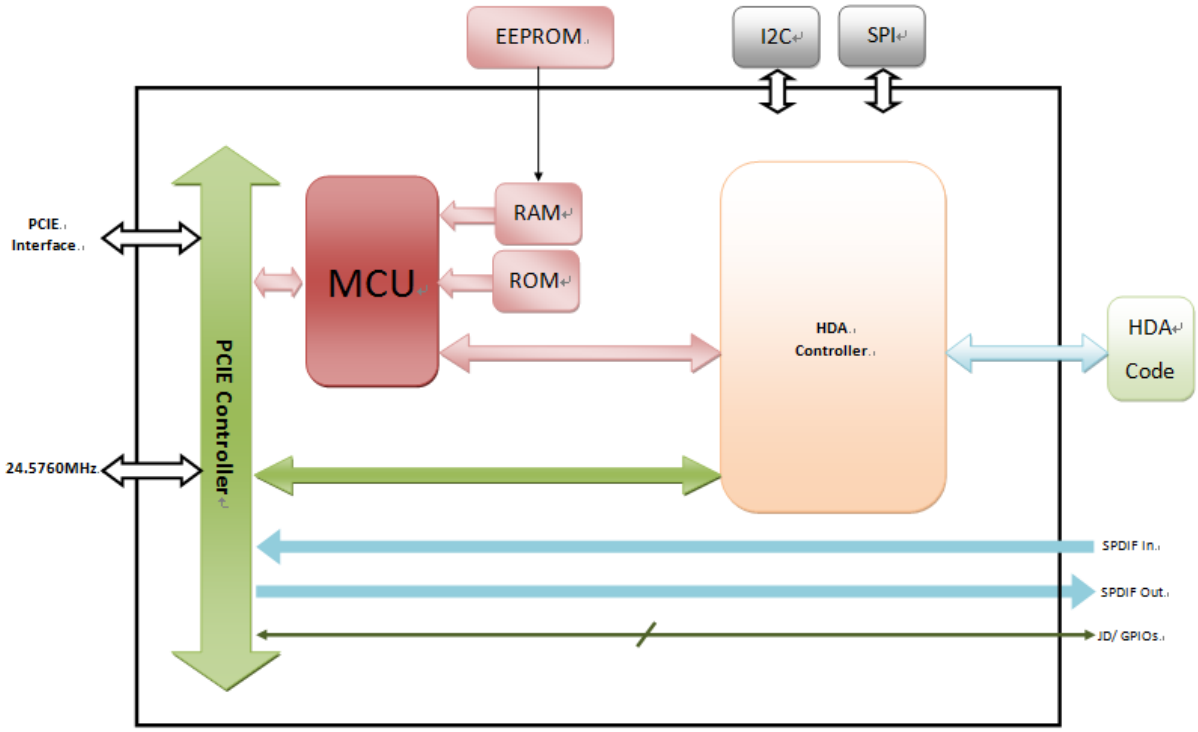

Figure 1. Block Diagram of Oxygen™ Express CM8828

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6. Pin Assignment

6.1 Pin-Out Diagram

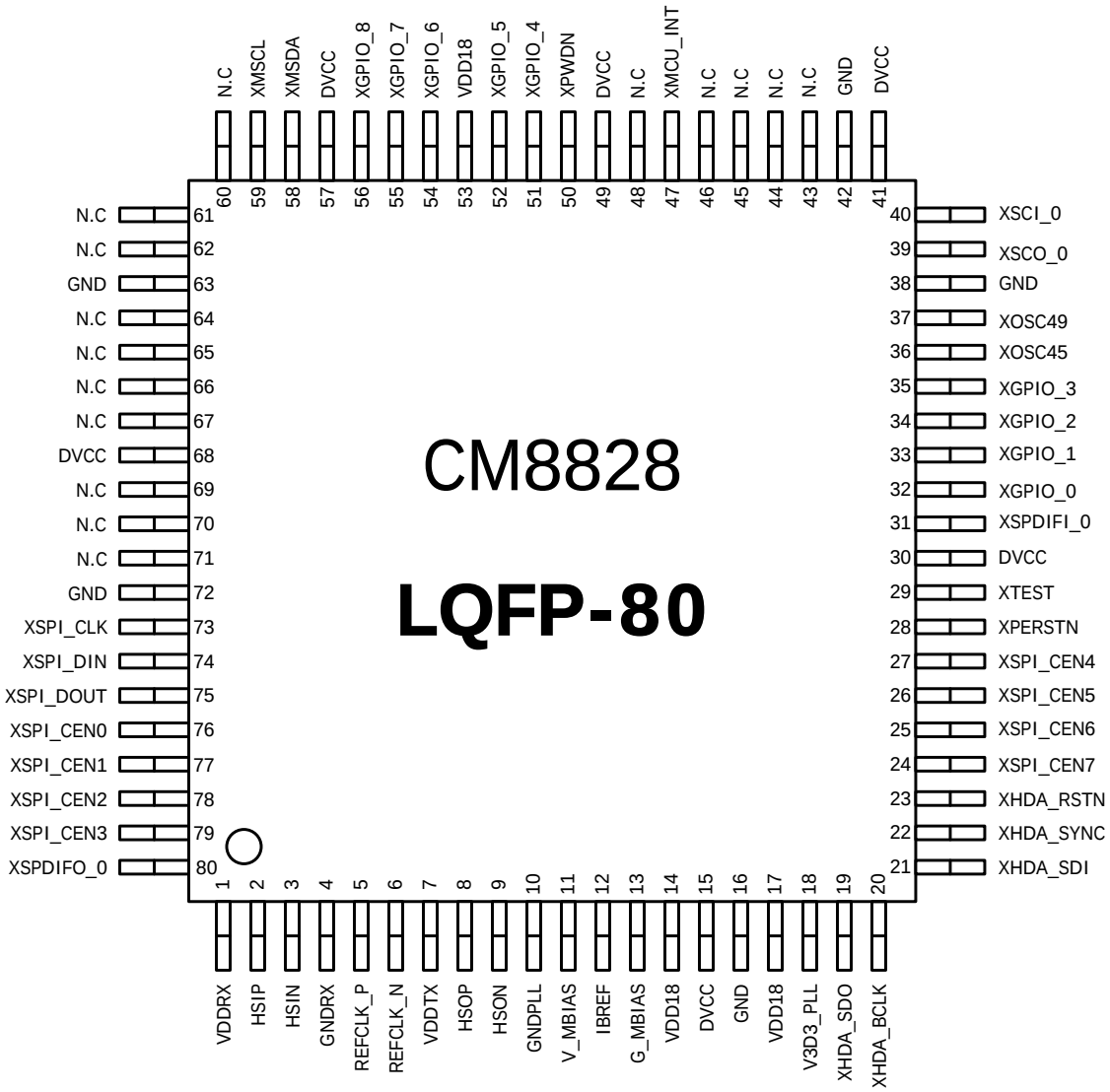

Figure 2. Pin-Out Diagram of Oxygen™ Express CM8828

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Pin Descriptions

The following table gives the pin descriptions for the Oxygen Express™ HD CM8828. The abbreviations used in the pin description table are explained below.

DI: digital input signal
DO: digital output signal
DIO: digital bidirectional signal
AI: analog input
PU: pull-up with 75KΩ resistor
PD: pull-down with 75KΩ resistor
#: low active signal

Table 5.1 Pin description table of Oxygen Experss™ HD CM8828

Pin No.	Pin Name	Type	Description
1	VDDRX	P	PHY VDD
2	HSIP	AI	PHY Signal
3	HSIN	AI	PHY Signal
4	GNDRX	G	PHY GND
5	REFCLK_P	AI	PHY Signal
6	REFCLK_M	AI	PHY Signal
7	VDDPLL / VDDTX	P	PHY VDD
8	HSOP	AO	PHY Signal
9	HSON	AO	PHY Signal
10	GNDPLL / GNDTX	G	PHY GND
11	VDDBIAS	P	PHY VDD
12	IBREF	AO	PHY Signal
13	GNDBIAS	G	PHY GND
14	VDD18	P	Digital 1.8V Power
15	DVCC	P	Digital Core power
16	GND	G	Digital Ground
17	VDD18	P	Digital 1.8V Power

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18	DVCC	P	Digital Core Power
19	XHDA_SDO	DO	HDA serial data output to codec
20	XHDA_BCLK	DO	HDA 24MHz serial clock output
21	XHDA_SDI	DIO,PD	1st HDA serial data input from codec
22	XHDA_SYNC	DO	HDA frame synchronization
23	XHDA_RSTN	DO	HDA codec reset 0
24	XSPI_CEN7	DIO,PU	SPI chip enable, which select the codec #7 to be controlled
25	XSPI_CEN6	DIO,PU	SPI chip enable, which select the codec #6 to be controlled
26	XSPI_CEN5	DIO,PU	SPI chip enable, which select the codec #5 to be controlled
27	XSPI_CEN4	DIO,PU	SPI chip enable, which select the codec #4 to be controlled
28	XPERSTN	DI,PU	PCIe PHY Reset#
29	XTEST	DI,PD	Test mode enable
30	DVCC	P	Digital Core Power
31	XSPDIFI_0	DI	1st S/PDIF input
32	XGPIO_0	DIO,PD	GPIO0, default input
33	XGPIO_1	DIO,PD	GPIO1, default input
34	XGPIO_2	DIO,PD	GPIO2, default input
35	XGPIO_3	DIO,PD	GPIO3, default input
36	XOSC45	DI,PD	45.1584 MHz Osc in
37	XOSC49	DI,PD	49.1520 MHz Osc in
38	GND	G	Digital Ground
39	XSCO_0	DIO	24.576 Crystal out
40	XSCI_0	DIO	24.576 Crystal in
41	DVCC	P	Digital Core Power
42	GND	G	Digital Ground
43	N.C		
44	N.C		

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45	N.C		
46	N.C		
47	XMCU_INT	DIO,PD	2-wire serial bus interrupt
48	N.C		
49	DVCC	P	Digital Core Power
50	XPWDN	DIO,PU	Codec Reset (Low active)
51	XGPIO_4	DIO,PD	GPIO4, default input
52	XGPIO_5	DIO,PD	GPIO5, default input
53	VDD18	P	Digital 1.8V Power
54	XGPIO_6	DIO,PD	GPIO6, default input
55	XGPIO_7	DIO,PD	GPIO7, default input
56	XGPIO_8	DIO,PD	GPIO8, default input
57	DVCC	P	Digital Core Power
58	XMSDA	DIO,PU	2-wire serial bus data
59	XMSCL	DIO,PU	2-wire serial bus clock
60	N.C		
61	N.C		
62	N.C		
63	GND	G	Digital Ground
64	N.C		
65	N.C		
66	N.C		
67	N.C		
68	DVCC	P	Digital Core Power
69	N.C		
70	N.C		
71	N.C		
72	GND	G	Digital Ground
73	XSPI_CLK	DIO,PD	SPI clock output
74	XSPI_DIN	DIO,PD	SPI data input
75	XSPI_DOUT	DIO,PD	SPI data output(master) / data input (slave)
76	XSPI_CEN0	DIO,PU	SPI chip enable, which select the codec #0 to be controlled
77	XSPI_CEN1	DIO,PU	SPI chip enable, which select the codec #1 to be controlled

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78	XSPI_CEN2	DIO,PU	SPI chip enable, which select the codec #2 to be controlled
79	XSPI_CEN3	DIO,PU	SPI chip enable, which select the codec #3 to be controlled
80	XSPDIFO_0	DO	1st S/PDIF transmitter

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7. Electrical Characteristics

7.1 Maximum Ratings

Test Conditions
DVDD = 3.3V, DGND =0V,TA=+25oC

Parameter	Symbol	Min	Typ	Max	Units
Storge temperature	-	-25	-	+120	°C
Operating ambient temperature	-	0	25	70	°C
DC supply voltage(DVCC)	-	3.1	3.3	3.6	V
DC supply voltage(VDD18)		1.62	1.8	1.98	V
I/O pin voltage	-	GND	-	V_{DD}	Vrms
Power dissipation	-	-		-	W

7.2 Recommended Operation Conditions

Test Conditions
DVDD = 3.3V, DGND =0V,TA=+25°C

Parameter	Symbol	Min	Typ	Max	Units
DVDD Input voltage range	-	V_{DD}-0.2	V_{DD}	V_{DD}+0.3	Vrms
DVDD Output voltage range	-	0	-	V_{DD}	Vrms
AVDD Input voltage range		Vavdd-5%	Vavdd	Vavdd+5%	Vrms

7.3 Power Consumption

Test Conditions
DVDD = 3.3V, DGND =0V,TA=+25°C

Parameter	Symbol	Min	Typ	Max	Units
Supply current : power up	-	-	203	-	mA
Supply current : power down	-	-	0.2	-	uA

7.4 DC Characteristics

Test Conditions
DVDD = 3.3V, DGND =0V,TA=+25oC

Parameter	Symbol	Min	Typ	Max	Units
Input voltage range	Vin	V_{DD}-0.2	V_{DD}	V_{DD}+0.3	V
Output voltage range	Vout	0	-	V_{DD}	V
High level input voltage	Vih	0.7V_{DD}	-	-	V
Low level input voltage	Vil	-	-	0.3V_{DD}	V
High level output voitage	Voh	2.4	-	-	V
Low level output voltage	Vol		-	0.4	V
Input leakage current	Iil	-10	-	10	uA

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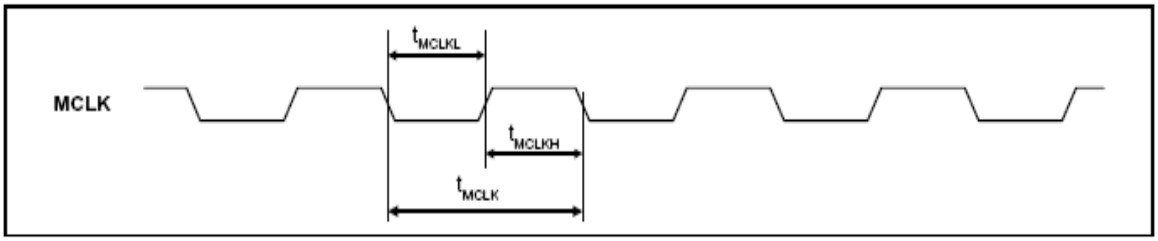
Output leakage current	Iol	-10	-	10	uA
Output buffer driver current	-	-	8	-	mA
SPDIF transmit output driver current	-	-	8	-	mA

7.5 AC Timing Characteristics

7.5.1 I2S Signal Timing

a. System Clock Timing

System Clock Timing Diagram



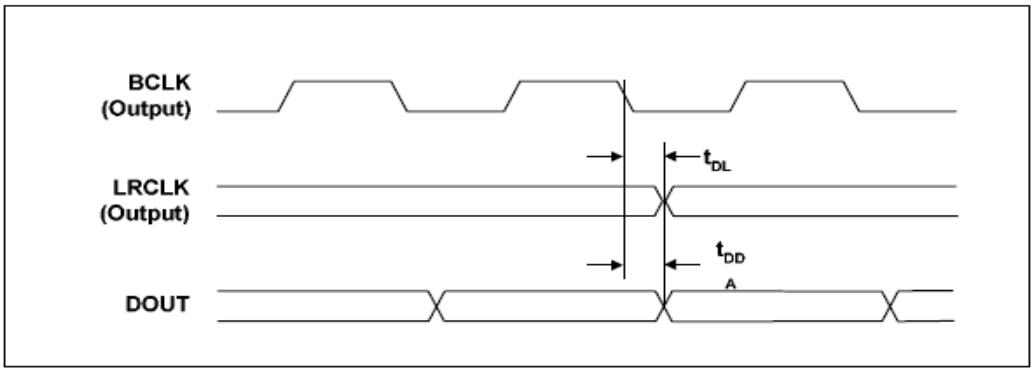
Test Conditions
DVDD = 3.3V, DGND =0V,TA=+25oC,fs=96KHz,MCLK=512fs,24 bit data,unless otherwise stated

System Clock Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
MCLK clock cycle time	tmclk	20	-	-	ns
MCLK pulse width high	tmclkh	10	-	-	ns
MCLK pulse width high	tmclkl	10	-	-	ns
MCLK duty cycle		40	50	60	%

b. Audio Interface Timing

Audio Interface Timing Diagram



Test Conditions
DVDD = 3.3V, DGND =0V,TA=+25oC,fs=96KHz,MCLK=512fs,24 bit data, unless otherwise stated

Audio Interface Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units

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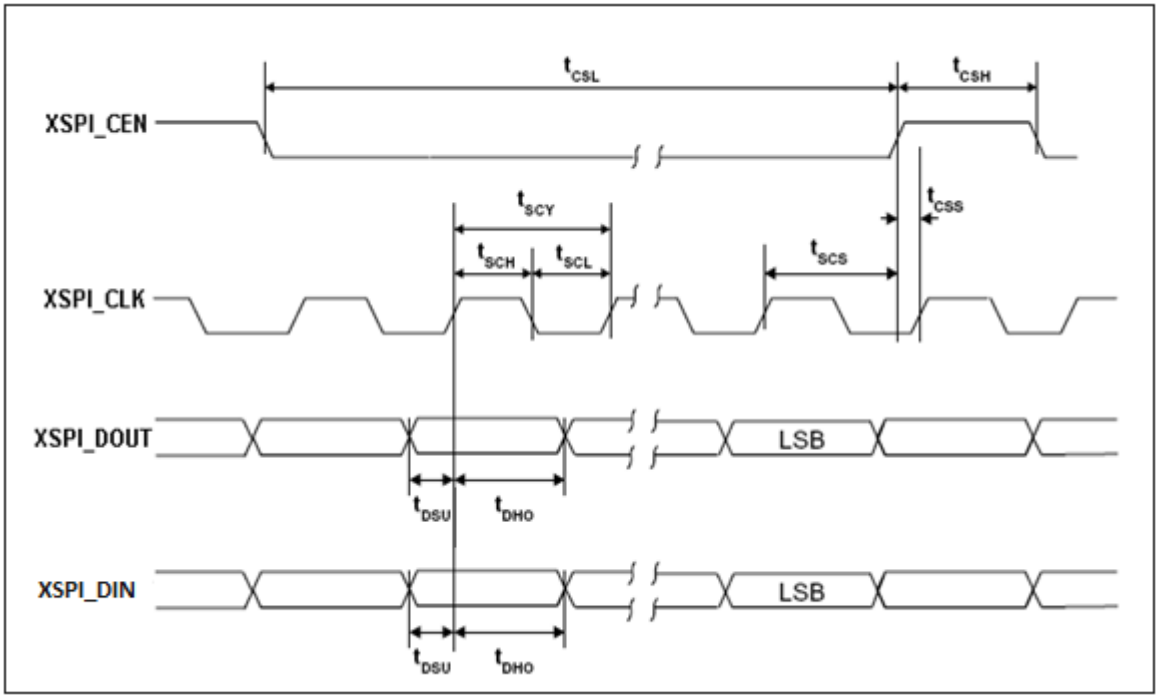
LRCK propagation delay from BCLK falling edge	Tdl	5	-	-	ns
SDOUT propagation delay from BCLK falling edge	Tdd	5	-	-	ns

7.5.2 Control Interface Timing - 3 - Wire Mode

Control Interface Timing -3- Wire Diagram



Note: latch data at XSPI_CEN clock low mode, XSPI_CEN clock can be low or high mode

Test Conditions

DVDD = 3.3V, DGND =0V, TA=+25°C, SPI clock 160 ns, unless otherwise stated

Control Interface Timing -3- Wire Parameters

Parameter	Symbol	Min	Typ	Max	Units
XSPI_CLK rising edge to XSPI_CEN rising edge	Tscs	120	-	-	ns
XSPI_CLK pulse cycle time	Tscy	160	-	-	ns
XSPI_CLK pulse width low	Tscl	80	-	-	ns
XSPI_CLK pulse width high	Tsch	80	-	-	ns
XSPI_DOUT to XSPI_CLK set-up time	Tdsu	40	-	-	ns
XSPI_DOUT to XSPI_CLK hold time	Tdho	40	-	-	ns
XSPI_CEN rising to SCLK rising	Tcss	40	-	-	ns

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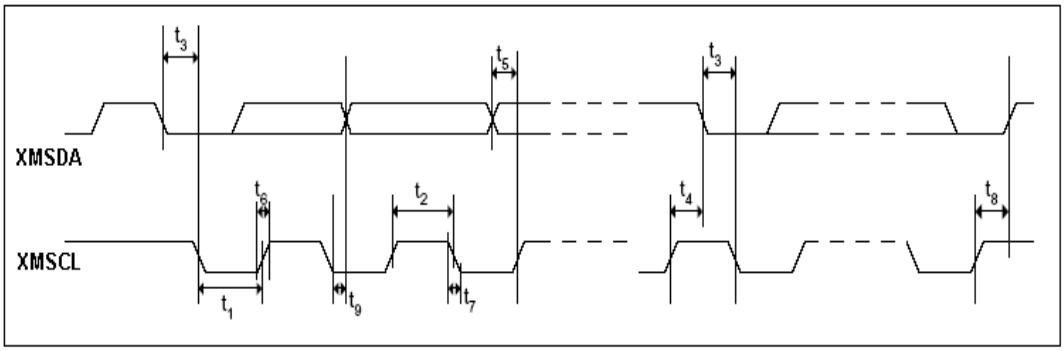
Control Interface Timing - 2 – Wire Mode

Control Interface Timing -2- Wire Diagram



Test Conditions
DVDD = 3.3V, DGND =0V, TA=+25°C, 2 wire, Fast speed mode, unless otherwise stated

Control Interface Timing -2- Wire Parameters

Parameter	Symbol	Min	Typ	Max	Units
XMSCL frequency		400	-	-	KHz
XMSCL pulse width low	t1	650	-	-	ns
XMSCL pulse width high	t2	1.3	-	-	us
Hold time (start condition)	t3	650	-	-	ns
Set-up time (start condition)	t4	650	-	-	ns
Data set-up time	t5	650	-	-	ns
XMSDI,XMSCL rise time	t6	100	-	-	ns
XMSDI,XMSCL fall time	t7	100	-	-	ns
Set-up time (stop condition)	t8	650	-	-	ns
Data hold time	t9	650	-	-	ns

Note: test parameters at 2 wire, Fast speed mode

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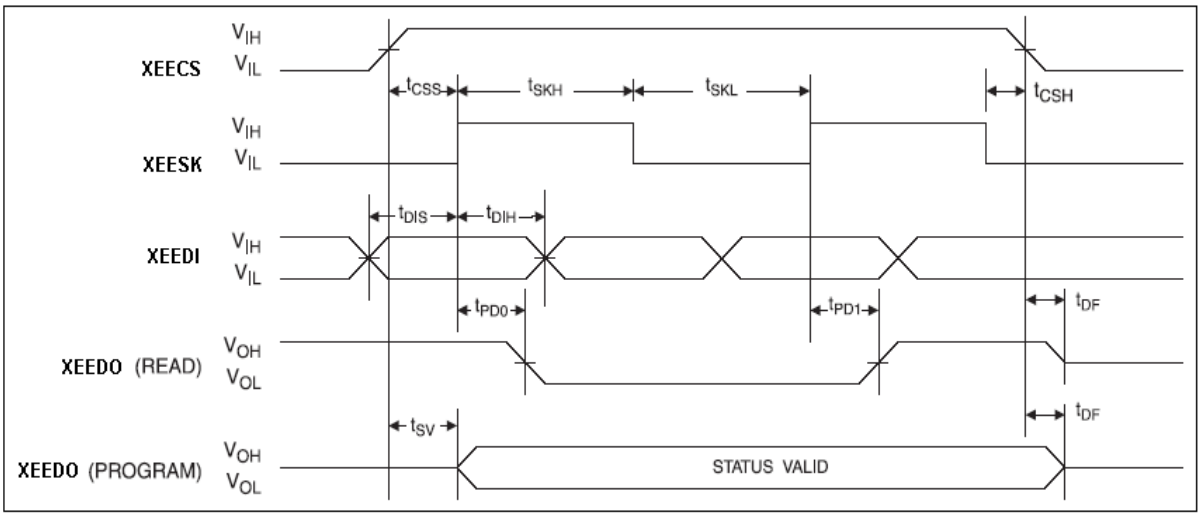
7.5.3 EEPROM Interface Timing

EEPROM Interface Timing Diagram



Test Conditions
DVDD = 3.3V, DGND =0V, TA=+25°C, unless otherwise stated

EEPROM Interface Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
XEESK clock frequency	tsk	555	-	-	KHz
XEESK high time	tskh	900	-	-	ns
XEESK low time	tskl	900	-	-	ns
XEECS setup time	tcss	900	-	-	ns
XEEDI setup time	tdis	900	-	-	ns
XEECS hold time	tcsh	900	-	-	ns
XEEDI hold time	tdih	2	-	-	ns
Output delay to "1"	tpd1	900	-	-	ns
Output delay to "0"	tpd0	30	-	-	ns
XEECS to status valid	tsv	30	-	-	ns
XEECS to XEEDO in high impedance	tdf	30	-	-	ns

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7.5.4 EEPROM AC Timing Characteristics

Symbol	Description	Min	Max	Units
fsk	SK Clock Frequency	0	0.5	MHz
tskh	SK High Time	500		ns
tskl	SK Low Time	500		ns
tcss	CS Setup Time	100		ns
tcsh	CS Hold Time	0		ns
tdis	DI Setup Time	200		ns
tdih	DI Hold Time	200		ns
tpd0	Output Delay to “0”		500	ns
tpd1	Output Delay to “1”		500	ns
tsv	CS to Status Valid		500	ns
tdf	CS to DO High Impedance		200	ns

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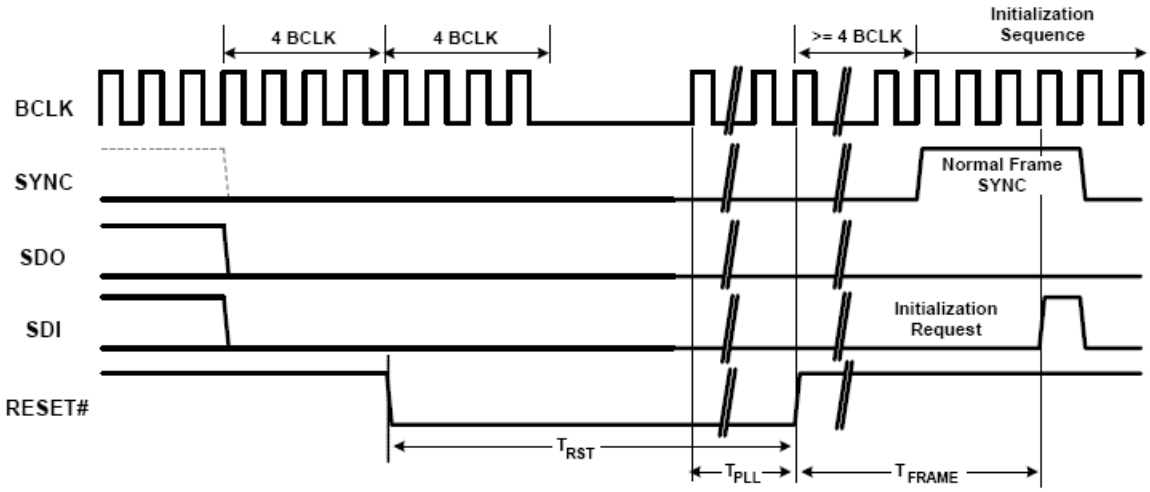
7.5.5 HD Audio-Link Timing Characteristics:

Test Conditions
DVDD = 3.3V, DGND =0V,TA=+25oC ,unless otherwise stated

1 Link Reset and Initialization Timing



Link Reset and Initialization Timing

Link Reset and Initialization Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
RESET#Active Low Pulse Width	Trst	1.0	-	-	us
RESET#Inactive to BCLK Startup delay time for PLL ready	Tpll	20	-	-	us
SDI Initialization Request time	Tframe	-	-	1	FrameTime

2 Link Timing Parameters

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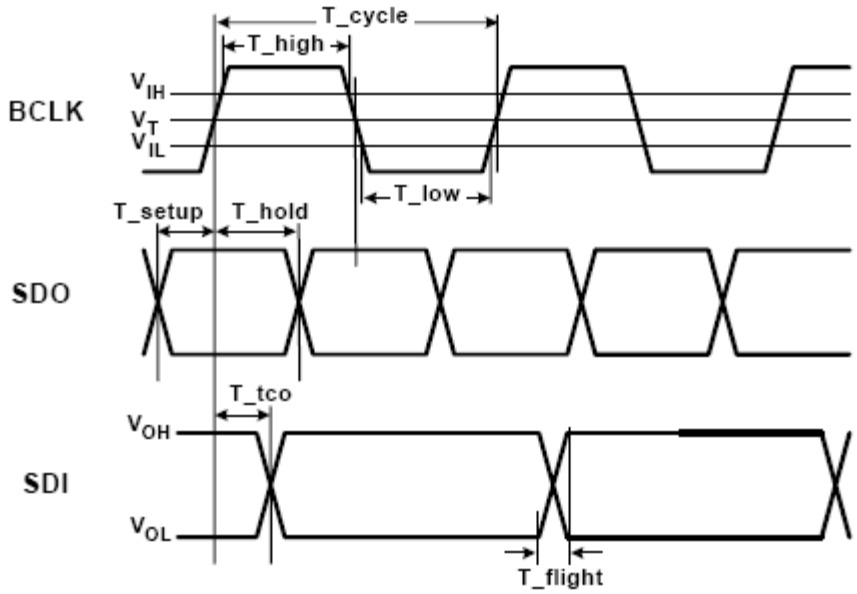

Link Signals Timing

Link Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
BCLK Frequency	-	-	24	-	MHz
BCLK out Period	Tcycle	-	41.67	-	ns
BCLK Jitter	-	-	-	2.0	ns
BCLK High,Low Level Width	Thigh/Tlow	18.75	-	22.91	ns
SDO Setup Time at Rising,Falling Edge of BCLK	Tsetup	2.0	-	-	ns
SDO Hold Time at Rising,Falling Edge of BCLK	Thold	2.0	-	-	ns
SDI Valid Time after Rising Edge of BCLK	Ttco	-	7.5	-	ns
SDI Flight Time	Tflight	-	2.0	-	ns

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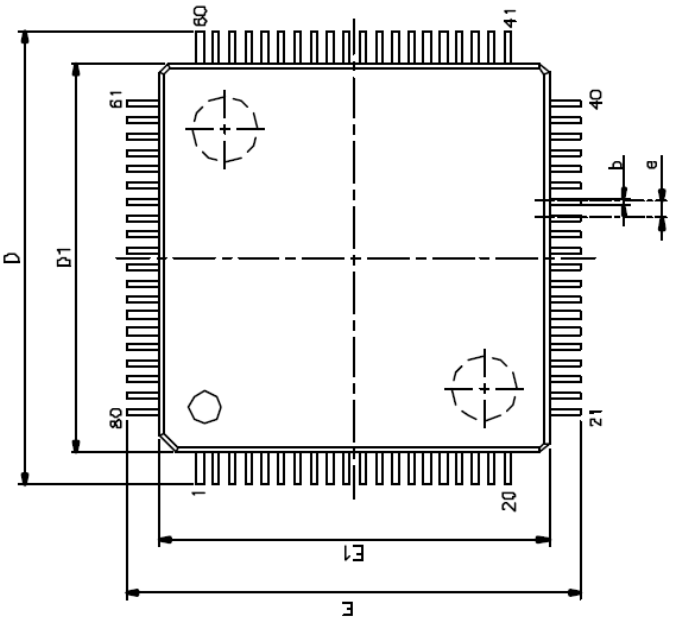
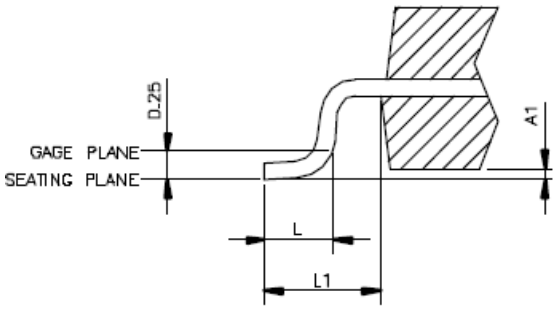
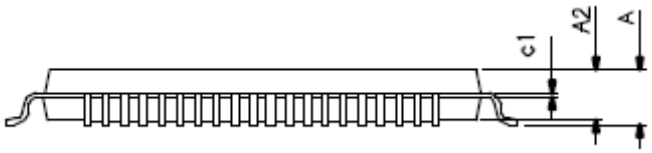
8. Mechanical Specification

8.1 Package Dimension







VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	12 BSC	
D1	10 BSC	
E	12 BSC	
E1	10 BSC	
e	0.4 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:

1. JEDEC OUTLINE:MS-026 BCE
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

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—End of Specifications—

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