Oxygen™ Express-series CM8888

High-Performance PCI Express Audio Processor

DESCRIPTION

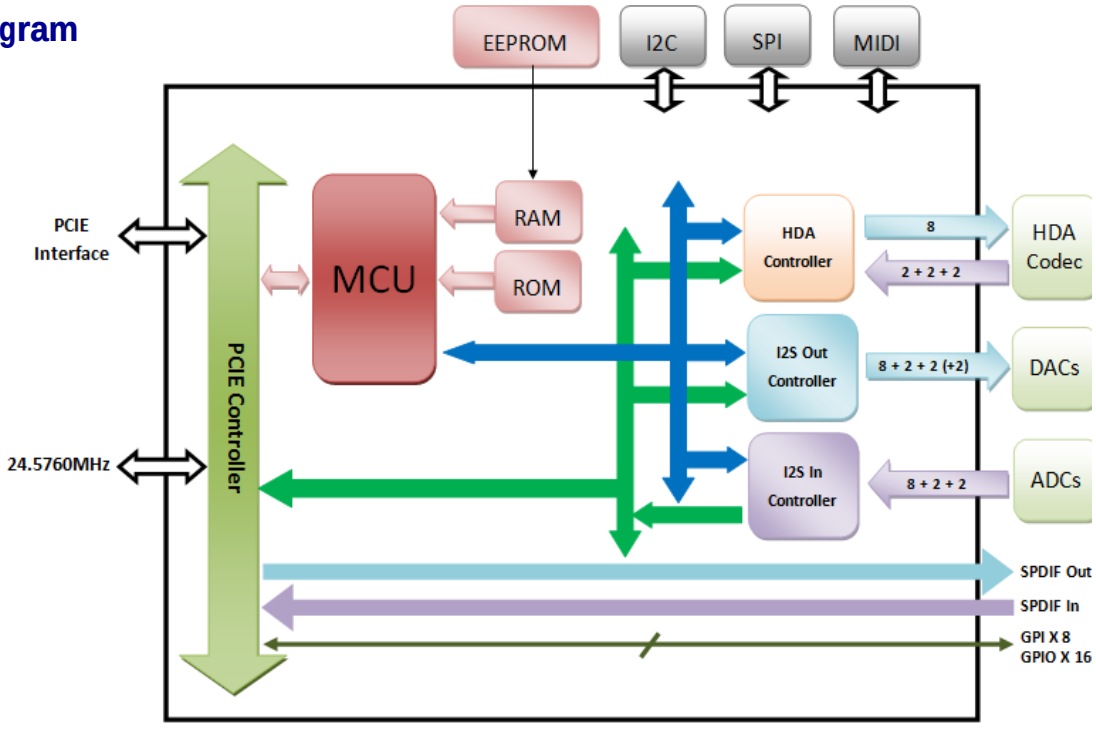
The Oxygen Express™-series HD CM8888 is a high-quality PCI Express multi-channel audio processor with an Intel HD Audio specification-compatible audio chip. It is also a controller that can link HDA codecs or bridge high-quality I2S codecs. The CM8888 can be built into home audio electronics or personal computers to provide high-fidelity sound, providing a professional audio processing center.

It supports up to 14 outgoing channels and 12 ingoing channels. The 14 outgoing channels are composed of 4 playback DMA's, including a multi-channel DMA (32 bits, 8 channels, 192k), a S/PDIF & HDMI DMA (each 32 bits, 2 channels, 192k), and a RTC (real-time communication) DMA (32 bits, 2 channels, 192k) channels. The 12 ingoing channels are spread out in 3 recording DMAs (up to 32 bits, 192k).

FEATURES

- Compatible with PCI Express 1.1 interface, with bus mastering and burst modes
- Embedded 8051-based MCU transcodes HD Audio commands to link various external I2S codecs (external 4 or 8KB serial EEPROM is required)
- Built-in HD Audio and I2S controllers
- I2S interface sample rate supports 192K/176.4K/96K/88.2K/48K/44.1K and 16/24/32-bit resolutions
- Integrated 192K/176.4K/96K/88.2K/48K/44.1K and 16/24-bit S/PDIF transmitter/receiver
- Supports SPI/I2C control interface
- 24.576MHz crystal input required with embedded PLL for adaptive clock rate

Block Diagram



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Revision History

Date	Rev.	Release Note
2011/2/24	Rev. 0.5	First version
2011/2/15	Rev. 0.6	Add software and features option chapter
2011/05/25	Rev 0.7	Remove MIDI support
2011/12/02	Rev 0.92	Update electronic characteristics: modified 3.3v power range
2012/06/20	Rev 0.93	Update recommended components: modified some typos
2012/11/05	Rev 1.00	Formal release
2013/04/24	Rev 1.01	Modify Pin39, 40 and 125 description Modify software features
2013/05/06	Rev 1.02	Modify Pin27, 28, 29, 30 and 31 definition Modify software features
2015/06/30	Rev 1.1	Remove O.S. information

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1 Description and Overview

The Oxygen Express™-series HD CM8888 is a high- quality PCI Express multi-channel audio processor with an Intel HD Audio specification-compatible audio chip. It is also a controller that can link HDA codecs or bridge high-quality I2S codecs. The CM8888 can be built into home audio electronics or personal computers to provide high-fidelity sound, providing a professional audio processing center.

It supports up to 14 outgoing channels and 12 ingoing channels. The 14 outgoing channels are composed of 4 playback DMA's, including a multi-channel DMA (32 bits, 8 channels, 192k), a S/PDIF & HDMI DMA (each 32 bits, 2 channels, 192k), and a RTC (real-time communication) DMA (32 bits, 2 channels, 192k) channels. The 12 ingoing channels are spread out in 3 recording DMAs (up to 32 bits, 192k).

The Oxygen Express™-series HD CM8888 is a MCU-based audio processor that can link all the currently popular codecs, from I2S codecs with over 120dB quality to regular HDA codecs. The audio topology for HDA specifications is flexible only by changing the firmware. The flexibility to change the firmware gives customers added flexibility when designing their products. The I2S, HDA-Link, 2-wire master bus, and SPI interfaces are used to transfer audio data and control data between the CM8888 and codecs. To facilitate the connection with the existing home audio electronics, the CM8888 has incorporated an S/PDIF transmitter and receiver with a 192k sampling rate.

A built-in master I2C interface connects to the serial EEPROM to store and retrieve non-evaporable data for firmware code and the customer applications, including as board configuration, sub-vender and sub-system IDs, or any dynamic data that customers want to save and restore on system power up.

The Oxygen Express™ HD CM8888 series has an independent 2-wire slave bus to communicate with the MCU. Strictly speaking, this interface is used as a medium system driver and MCU communication. An MPU-401 MIDI UART is also integrated. There are eight GPI phone jack detect pins, which can be used to distinguish if a device is plugged into a phone jack. In total there are 10 GPIO pins, however, some of them are shared with other functions.

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2 Features

Bus

- Compatible with PCI Express 1.1 interface, with bus mastering and burst modes

Architecture

- Embedded 8051-based MCU transcodes HD Audio commands to link various external I2S codecs (external 4 or 8KB serial EEPROM is required)
- Embedded ROM code for MCU transcoding of HD Audio commands for embedded DACs and ADCs
- Built-in HD Audio and I2S controllers offer flexibility in choosing external codecs for different product applications
- Digital mixer to mix all input data to output streams

DMA Controller

- Four playback DMAs and three recording DMAs that support MS Vista/Win7 HD Audio controller requirements, and are WaveRT-port-friendly:
  - Cyclic DMA engine with a scatter/gather list
  - Position register is separate from other hardware registers (can be a copy)
  - Ability to loop on buffers without software intervention
- Playback DMA#A supports up to 8-ch audio output (2/4/6/8-ch configurable by SW driver control)
- Playback DMA#B supports independent 2-ch audio output (e.g. front headphone out for RTC)
- Playback DMA#C supports independent 2-ch audio output (e.g. back headphone out) or S/PDIF for HDMI output
- Playback DMA#D supports independent 2-ch audio output (for S/PDIF output or other purposes)
- Recording DMA#A supports up to 8-ch audio input (2/4/6/8-ch configurable by SW driver control)
- Recording DMA#B supports independent 2-ch audio input (for RTC headsets)
- Recording DMA#C supports independent 2-ch audio input (for S/PDIF input stream or other purposes)
- Sampling rates: all DMA channels support 192K/176.4K/96K/88.2K/48K/44.1K PCM data
- Resolution (Word-length): all DMA channels support 16/24/32-bit PCM data transfer modes

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Audio I/O

- Intel HD Audio Link supports 1 external HDA codec
- Six pairs of I^2S serial audio output interfaces (12-ch out)
  - Pair 1~4 use playback DMA#A
  - Pair 5 uses playback DMA#B
  - Pair 6 uses playback DMA#C
- Six pairs of I^2S serial audio input interfaces (12-ch in)
  - Pair 1~4 use recording DMA#A
  - Pair 5 uses recording DMA#B
  - Pair 6 uses recording DMA#C
- Integrated 192K/176.4K/96K/88.2K/48K/44.1K, and 16/24/32-bit S/PDIF transmitter with a 2-source selector/mux (from playback DMA digital mixing, S/PDIF input), including WMA-Pro output support
- Integrated 192K/176.4K/96K/88.2K/48K/44.1K, and 16/24/32-bit S/PDIF receiver with 2-input internal selector/switch for media center/AV receiver features
- Built-in MPU-401 MIDI UART I/O port for pro audio applications
- All input data can be mixed to output streams for low-latency record monitoring/mixing output

Control Interface

- SPI control interfaces with up to 8 external audio devices (5 output devices and 3 input devices)
- I^2C Interface supports both master and slave modes (master for external audio devices and slave for additional MCU applications such as remote controls)
- Interrupt pin for external MCU read transaction
- Serial EEPROM programming interface for customizing sub-vendor and sub-device IDs (and vendor/device IDs as well), storing HDA power-on pin configuration data (replacing the MB BIOS function) and 8051 ROM codes (HDA command transcoder)
- Maximum 8 jack-detection pins (5 for output jacks and 3 for input jacks)
- Maximum 16 GPIO pins for external devices control and other purposes
- LED indicator control pin functions while protected content is playing

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General

- 24.576MHz crystal input required with embedded PLL for adaptive clock rate
- Single 3.3V power supply
- 3.3 V digital I/O pads with 5V tolerance
- Fully compatible with all mainstream southbridges (Intel, nVIDIA, VIA, SiS)
- LQFP-128 package
- Default target codecs: CM9882A for HDA; CS5381 (ADC)+PCM1795(DAC) for I^2S

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3 Applications

- High-definition PCIe sound cards for the high-performance consumer market
- Pro audio/high-end studio applications
- Gaming audio devices
- Bundling with high-profile VGA cards or motherboard
- Embedded system/industrial computer audio
- Embedded with high-quality audio HTPC

4 Software and Features Option

Features	CM8888DHT	CM8888DMS	CM8888
Dolby® Home Theater® V4	Yes		
Dolby® Master Studio		Yes	
DTS® UltraPC II™	Yes		
DTS® Connect		Yes	
Xear™ 3D EX 1.0	Yes	Yes	Yes
Xear™ Living	Yes	Yes	Yes
Xear™ VoClear	Yes	Yes	Yes
Xear™ Sonic	Yes	Yes	Yes
Xear™ SingFX	Yes	Yes	Yes
Xear™ Fidelity	Yes	Yes	Yes
Xear™ Pro	Yes	Yes	Yes
FaceLift II GUI	Yes	Yes	Yes

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5 Block Diagram

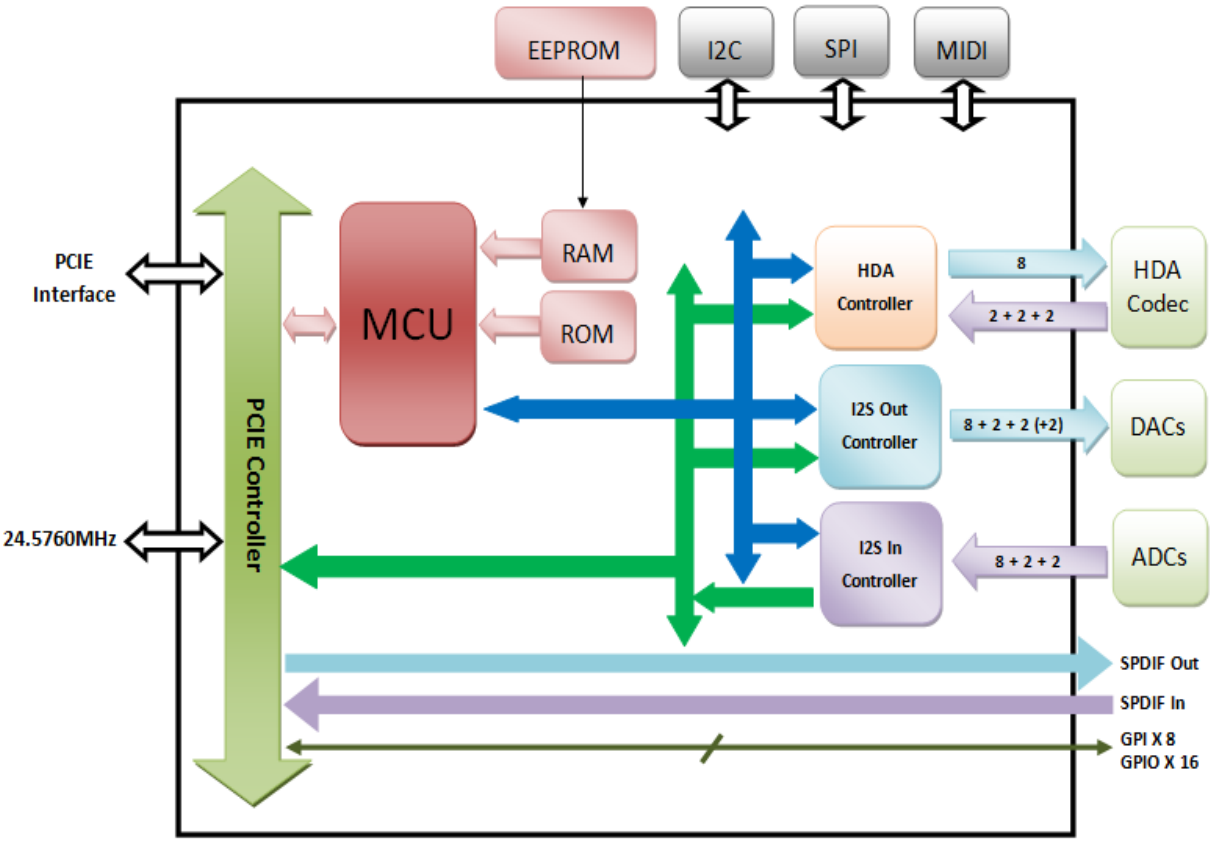

Figure 1. Block Diagram for Oxygen™ Express CM8888

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6 Pin Assignment

6.1 Pin-Out Diagram

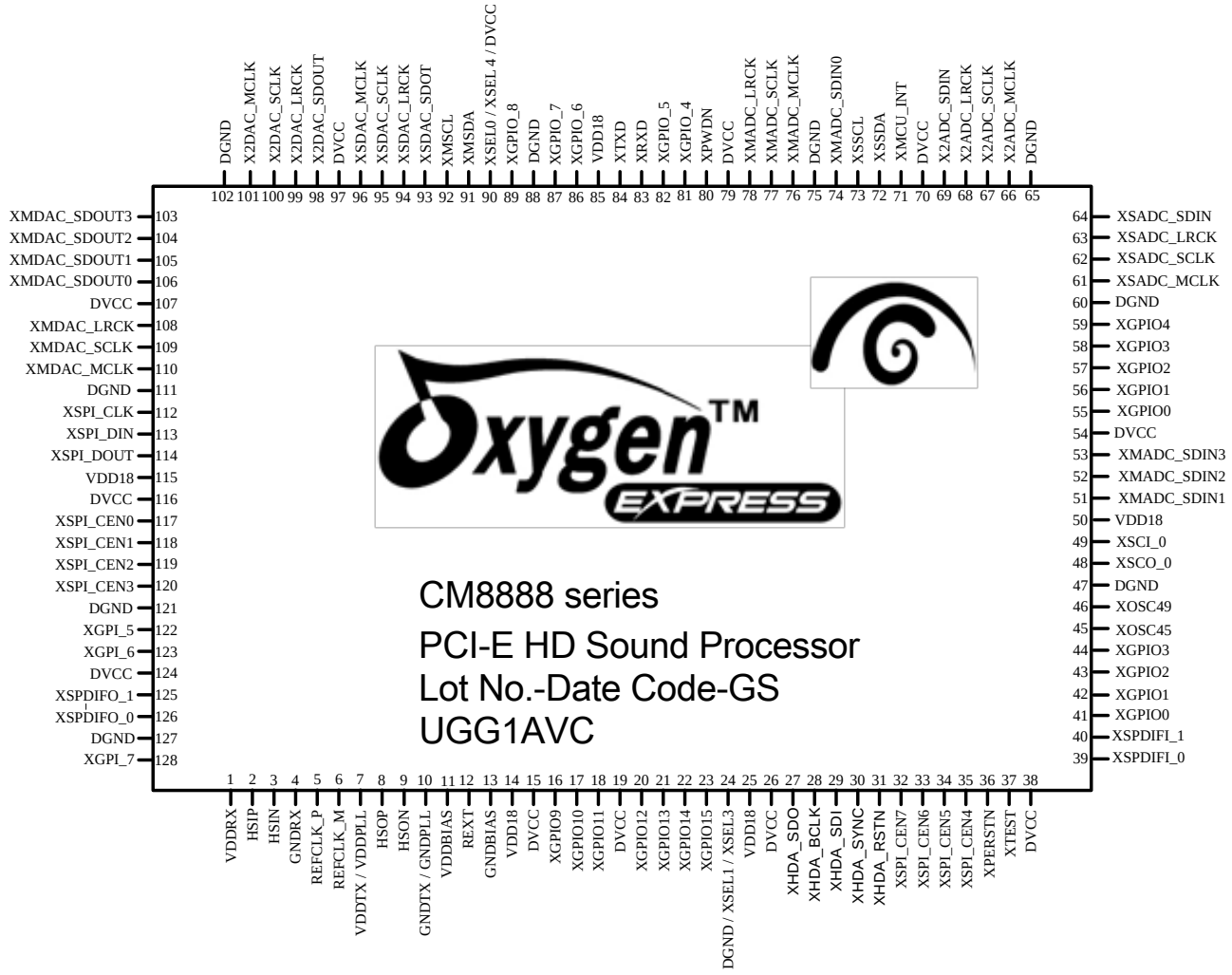

Figure 2. Pin-Out Diagram for Oxygen™ Express-series CM8888

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Pin Descriptions

The following table gives the pin descriptions for the Oxygen Express™-series HD CM8888 series. The abbreviations used in the pin description table are explained here:

DI: digital input signal
DO: digital output signal
DIO: digital bidirectional signal
AI: analog input
PU: pull-up with 75KΩ resistor
PD: pull-down with 75KΩ resistor
#: low active signal

Table 5.1 Pin description table of Oxygen Experss™ HD CM8888 series

Pin No.	Pin Name	Type	Description
1	VDDRX	P	PHY VDD
2	HSIP	AI	PHY Signal
3	HSIN	AI	PHY Signal
4	GNDRX	G	PHY GND
5	REFCLK_P	AI	PHY Signal
6	REFCLK_M	AI	PHY Signal
7	VDDPLL / VDDTX	P	PHY VDD
8	HSOP	AO	PHY Signal
9	HSON	AO	PHY Signal
10	GNDPLL / GNDTX	G	PHY GND
11	VDDBIAS	P	PHY VDD
12	REXT	AO	PHY Signal
13	GNDBIAS	G	PHY GND
14	VDD18	P	Digital 1.8V Power
15	DVCC	P	Digital Core power
16	XGPIO_9	DIO,PD	GPIO9, default Input
17	XGPIO_10	DIO,PD	GPIO10, default Input
18	XGPIO_11	DIO,PD	GPIO11, default Input

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19	DVCC	P	Digital core power
20	XGPIO_12	DIO,PD	GPIO12, default Input
21	XGPIO_13	DIO,PD	GPIO13, default Input
22	XGPIO_14	DIO,PD	GPIO14, default Input
23	XGPIO_15	DIO,PD	GPIO15, default Input
24	GND	G	Digital ground
25	VDD18	P	Digital 1.8V power
26	DVCC	P	Digital core power
27	XHDA_SDO	DO	HDA serial data output to codec
28	XHDA_BCLK	DO	HDA 24MHz serial clock output
29	XHDA_SDI	DIO,PD	1st HDA serial data input from codec
30	XHDA_SYNC	DO	HDA frame synchronization
31	XHDA_RSTN	DO	HDA codec reset 0
32	XSPI_CEN7	DIO,PU	SPI chip enable, which select the codec #7 to be controled
33	XSPI_CEN6	DIO,PU	SPI chip enable, which select the codec #6 to be controled
34	XSPI_CEN5	DIO,PU	SPI chip enable, which select the codec #5 to be controled
35	XSPI_CEN4	DIO,PU	SPI chip enable, which select the codec #4 to be controled
36	XPERSTN	DI,PU	PCIe PHY reset no.
37	XTEST	DI,PD	Test mode enable
38	DVCC	P	Digital core power
39	XSPDIFI_0	DI	1st S/PDIF receiver
40	XSPDIFI_1	DI	2nd S/PDIF receiver
41	XGPIO_0	DIO,PD	GPIO0, default input
42	XGPIO_1	DIO,PD	GPIO1, default input
43	XGPIO_2	DIO,PD	GPIO2, default input
44	XGPIO_3	DIO,PD	GPIO3, default input
45	XOSC45	DI,PD	45.1584 MHz Osc in
46	XOSC49	DI,PD	49.1520 MHz Osc in

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47	GND	G	Digital ground
48	XSCO_0	DIO	24.576 crystal out
49	XSCI_0	DIO	24.576 crystal in
50	VDD18	P	Digital 1.8V power
51	XMADC_SDIN1	DIO,PD	I2S ADC stream A channel 2, channel 3 serial data input
52	XMADC_SDIN2	DIO,PD	I2S ADC stream A channel 4, channel 5 serial data input
53	XMADC_SDIN3	DIO,PD	I2S ADC stream A channel 6, channel 7 serial data input
54	DVCC	P	Digital core power
55	XGPI_0	DIO,PD	JACK A detection input
56	XGPI_1	DIO,PD	JACK B detection input
57	XGPI_2	DIO,PD	JACK C detection input
58	XGPI_3	DIO,PD	JACK D detection input
59	XGPI_4	DIO,PD	JACK E detection input
60	GND	G	Digital ground
61	XSADC_MCLK	DO	I2S stream C master clock output
62	XSADC_SCLK	DIO,PD	I2S ADC stream C bit clock
63	XSADC_LRCK	DIO,PD	I2S ADC stream C left/right sample clock
64	XSADC_SDIN	DI,PD	I2S ADC stream C channel 0/channel 1 serial data input
65	GND	G	Digital ground
66	X2ADC_MCLK	DIO,PD	I2S stream B master clock output
67	X2ADC_SCLK	DIO,PD	I2S ADC stream B bit clock
68	X2ADC_LRCK	DI, PD	I2S ADC stream B left/right sample clock
69	X2ADC_SDIN	DI,PU	I2S ADC stream B channel 0/channel 1 serial data input
70	DVCC	P	Digital core power
71	XMCU_INT	DIO,PD	2-wire serial bus interupt
72	XSSDA	DIO,PU	2-wire serial bus data
73	XSSCL	DIO,PU	2-wire serial bus clock
74	XMADC_SDIN0	DIO,PD	I2S ADC stream A channel 0/channel 1 serial data input
75	GND	G	Digital ground

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76	XMADC_MCLK	DIO,PD	I2S ADC stream A master clock output
77	XMADC_SCLK	DIO,PD	I2S ADC stream A bit clock.
78	XMADC_LRCK	DIO,PD	I2S ADC stream A left/right sample clock
79	DVCC	P	Digital core power
80	XPWDN	DIO,PU	Codec reset (low active)
81	XGPIO_4	DIO,PD	GPIO4, default input
82	XGPIO_5	DIO,PD	GPIO5, default input
83	XRXD	DIO,PD	MPU401 MIDI receiver input (5V tolerance)
84	XTXD	DIO,PD	MPU401 MIDI transmitter output (5V tolerance)
85	VDD18	P	Digital 1.8V power
86	XGPIO_6	DIO,PD	GPIO6, default input
87	XGPIO_7	DIO,PD	GPIO7, default input
88	GND		Digital ground
89	XGPIO_8	DIO,PD	GPIO8, default input
90	DVCC	P	Digital core power
91	XMSDA	DIO,PU	2-wire serial bus data
92	XMSCL	DIO,PU	2-wire serial bus clock
93	XSDAC_SDOUT	DO	I2S DAC stream C channel 0/channel 1 serial data output
94	XSDAC_LRCK	DIO,PD	I2S DAC stream C left/right sample clock
95	XSDAC_SCLK	DIO,PD	I2S DAC stream C bit clock
96	XSDAC_MCLK	DIO,PD	I2S ADC stream A master clock output
97	DVCC	P	Digital core power
98	X2DAC_SDOUT	DIO,PD	I2S DAC stream B channel 0/channel 1 serial data output
99	X2DAC_LRCK	DIO,PD	I2S DAC stream B left/Right sample clock
100	X2DAC_SCLK	DIO,PD	I2S DAC stream B bit clock
101	X2DAC_MCLK	DIO,PD	I2S DAC stream B master clock output
102	GND	G	Digital ground
103	XMDAC_SDOUT3	DIO,PD	I2S DAC stream A channel 6/channel 7 serial data output
104	XMDAC_SDOUT2	DIO,PD	I2S DAC stream A channel 4/channel 5 serial data output
105	XMDAC_SDOUT1	DIO,PD	I2S DAC stream A channel 2/channel 3 serial

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			data output
106	XMDAC_SDOUT0	DIO,PD	I2S DAC stream A channel 0/channel 1 serial data output
107	DVCC	P	Digital core power
108	XMDAC_LRCK	DIO,PD	I2S DAC stream A left/right sample clock
109	XMDAC_SCLK	DIO,PD	I2S DAC stream A bit clock
110	XMDAC_MCLK	DIO,PD	I2S DAC stream A master clock output
111	GND	G	Digital ground
112	XSPI_CLK	DIO,PD	SPI clock output
113	XSPI_DIN	DIO,PD	SPI data input
114	XSPI_DOUT	DIO,PD	SPI data output (master) / data input (slave)
115	VDD18	P	Digital 1.8V power
116	DVCC	P	Digital core power
117	XSPI_CEN0	DIO,PU	SPI chip enable, selects codec #0 to be controlled
118	XSPI_CEN1	DIO,PU	SPI chip enable, selects codec #1 to be controlled
119	XSPI_CEN2	DIO,PU	SPI chip enable, which select the codec #2 to be controlled
120	XSPI_CEN3	DIO,PU	SPI chip enable, which select the codec #3 to be controlled
121	GND	G	Digital ground
122	XGPI_5	DIO,PD	JACK F detection input
123	XGPI_6	DIO,PD	JACK G detection input
124	DVCC	P	Digital core power
125	XSPDIFO_1	DO	2nd S/PDIF transmitter
126	XSPDIFO_0	DO	1st S/PDIF transmitter
127	GND	G	Digital ground
128	XGPI_7	DIO,PD	JACK H detection input

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7 Electrical Characteristics

7.1 Maximum Ratings

Test Conditions: DVCC = 3.3V, DGND =0V, TA=+25oC

Parameter	Symbol	Min	Typ	Max	Units
Storge temperature	-	-25	-	+120	°C
Operating ambient temperature	-	0	25	70	°C
DC supply voltage(DVCC)	-	3.1	3.3	3.6	V
DC supply voltage(AVDD)		1.62	1.8	1.98	V
I/O pin voltage	-	GND	-	V_{DD}	V
Power dissipation	-	-		-	W

7.2 Recommended Operation Conditions

Test Conditions: DVCC = 3.3V, DGND =0V, TA=+25°C

Parameter	Symbol	Min	Typ	Max	Units
DVCC Input voltage range	-	V_{DD}-0.2	V_{DD}	V_{DD}+0.3	V
DVCC Output voltage range	-	0	-	V_{DD}	V
AVDD Input voltage range		Vavdd-5%	Vavdd	Vavdd+5%	V

7.3 Power Consumption

Test Conditions: DVCC = 3.3V, DGND =0V, TA=+25°C

Parameter	Symbol	Min	Typ	Max	Units
Supply current : power up(DVCC+VDD3.3V)	-	-	203	-	mA
Supply current : power down(DVCC+VDD3.3V)	-	-	0.2	-	uA

7.4 DC Characteristics

Test Conditions: DVCC = 3.3V, DGND =0V, TA=+25oC

Parameter	Symbol	Min	Typ	Max	Units
Input voltage range	Vin	V_{DD}-0.2	V_{DD}	V_{DD}+0.3	V
Output voltage range	Vout	0	-	V_{DD}	V
High level input voltage	Vih	0.7V_{DD}	-	-	V
Low level input voltage	Vil	-	-	0.3V_{DD}	V
High level output voitage	Voh	2.4	-	-	V
Low level output voltage	Vol		-	0.4	V
Input leakage current	Iil	-10	-	10	uA

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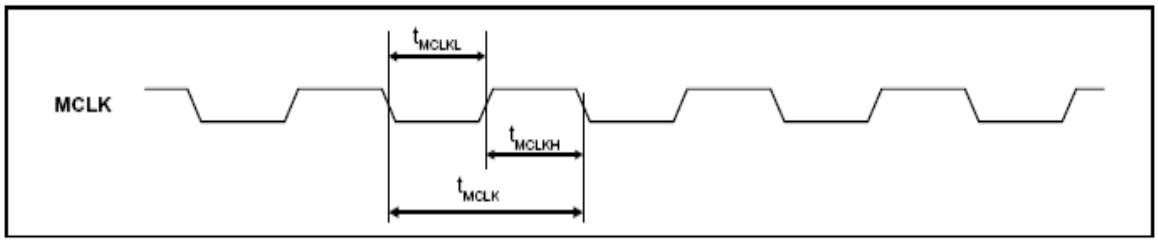
Output leakage current	Iol	-10	-	10	uA
Output buffer driver current	-	-	8	-	mA
SPDIF transmit output driver current	-	-	8	-	mA

7.5 AC Timing Characteristics

7.5.1 I2S Signal Timing

a. **System Clock Timing**

System Clock Timing Diagram



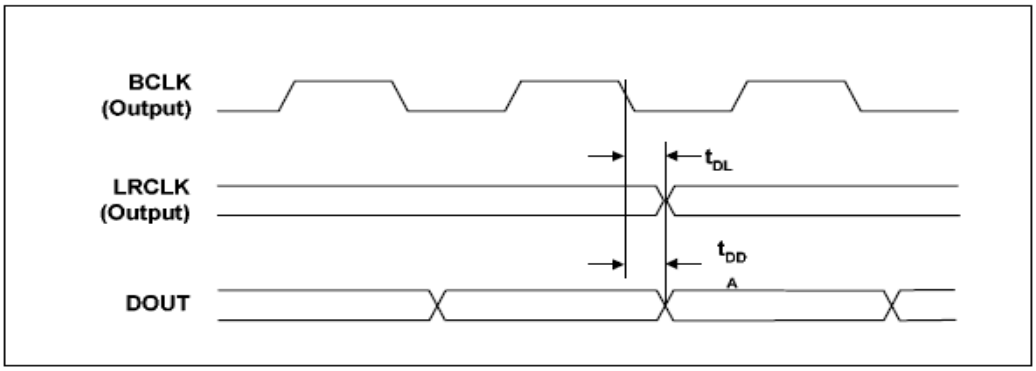
Test Conditions: DVCC = 3.3V, DGND =0V,TA=+25oC,fs=96KHz,MCLK=512fs,24 bit data, unless otherwise stated

System Clock Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
MCLK clock cycle time	tmclk	20	-	-	ns
MCLK pulse width high	tmclkh	10	-	-	ns
MCLK pulse width high	tmclkl	10	-	-	ns
MCLK duty cycle		40	50	60	%

b. **Audio Interface Timing**

Audio Interface Timing Diagram



Test Conditions: DVCC = 3.3V, DGND =0V,TA=+25oC,fs=96KHz,MCLK=512fs,24 bit data, unless otherwise stated

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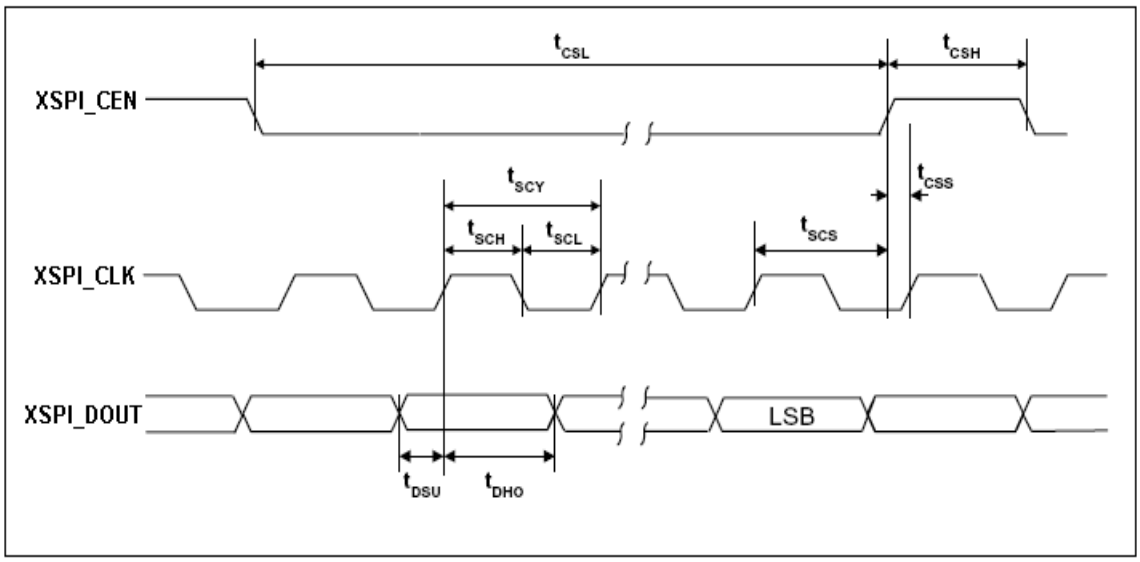
Audio Interface Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
LRCK propagation delay from BCLK falling edge	Tdl	5	-	-	ns
SDOUT propagation delay from BCLK falling edge	Tdd	5	-	-	ns

7.5.2 Control Interface Timing - 3-Wire Mode

Control Interface Timing - 3-Wire Diagram



Note: latch data at XSPI_CEN clock low mode, XSPI_CEN clock can be low or high mode
Test Conditions: DVCC = 3.3V, DGND =0V, TA=+25°C, SPI clock 160 ns, unless otherwise stated

Control Interface Timing - 3-Wire Parameters

Parameter	Symbol	Min	Typ	Max	Units
XSPI_CLK rising edge to XSPI_CEN rising edge	Tscs	120	-	-	ns
XSPI_CLK pulse cycle time	Tscy	160	-	-	ns
XSPI_CLK pulse width low	Tscl	80	-	-	ns
XSPI_CLK pulse width high	Tsch	80	-	-	ns
XSPI_DOUT to XSPI_CLK set-up time	Tdsu	40	-	-	ns
XSPI_DOUT to XSPI_CLK hold time	Tdho	40	-	-	ns
XSPI_CEN rising to SCLK rising	Tcss	40	-	-	ns

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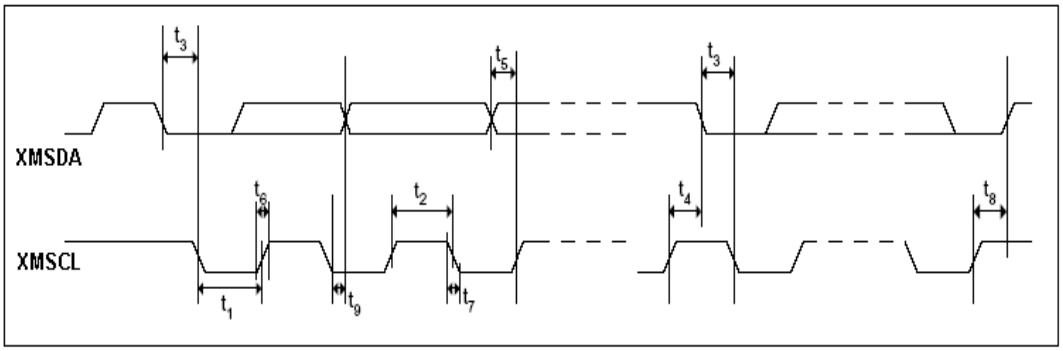
Control Interface Timing - 2-Wire Mode

Control Interface Timing - 2-Wire Diagram



Test Conditions: DVCC = 3.3V, DGND =0V, TA=+25°C, 2-wire, fast-speed mode, unless otherwise stated

Control Interface Timing - 2-Wire Parameters

Parameter	Symbol	Min	Typ	Max	Units
XMSCL frequency		400	-	-	KHz
XMSCL pulse width low	t1	650	-	-	ns
XMSCL pulse width high	t2	1.3	-	-	us
Hold time (start condition)	t3	650	-	-	ns
Set-up time (start condition)	t4	650	-	-	ns
Data set-up time	t5	650	-	-	ns
XMSDI,XMSCL rise time	t6	100	-	-	ns
XMSDI,XMSCL fall time	t7	100	-	-	ns
Set-up time (stop condition)	t8	650	-	-	ns
Data hold time	t9	650	-	-	ns

Note: test parameters at 2 wire, fast-speed mode

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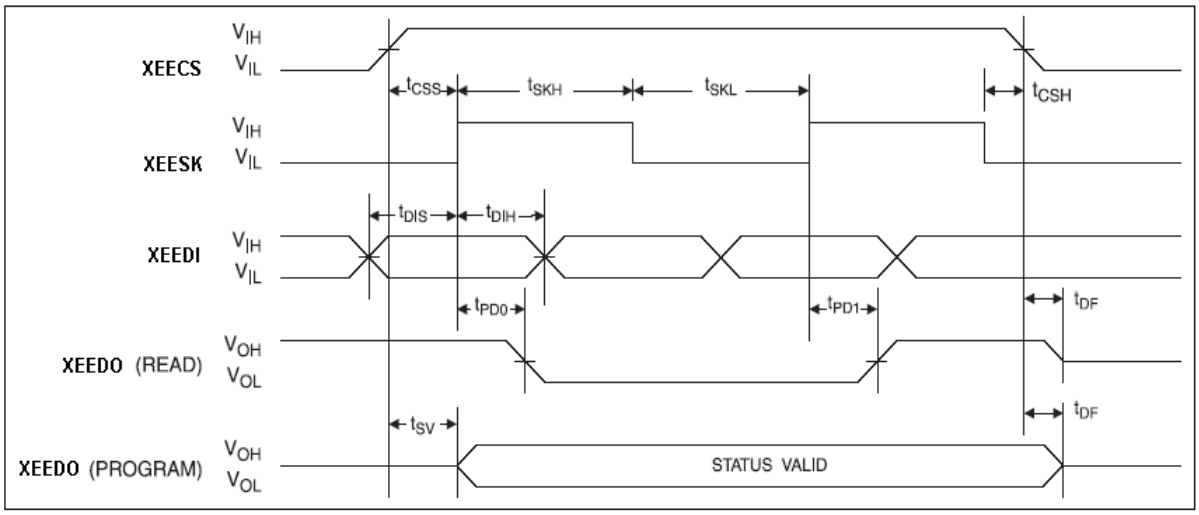
7.5.3 EEPROM Interface Timing

EEPROM Interface Timing Diagram



Test Conditions: DVCC = 3.3V, DGND =0V, TA=+25°C, unless otherwise stated

EEPROM Interface Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
XEESK clock frequency	tsk	555	-	-	KHz
XEESK high time	tskh	900	-	-	ns
XEESK low time	tskl	900	-	-	ns
XEECS setup time	tcss	900	-	-	ns
XEEDI setup time	tdis	900	-	-	ns
XEECS hold time	tcsh	900	-	-	ns
XEEDI hold time	tdih	2	-	-	ns
Output delay to "1"	tpd1	900	-	-	ns
Output delay to "0"	tpd0	30	-	-	ns
XEECS to status valid	tsv	30	-	-	ns
XEECS to XEEDO in high impedance	tdf	30	-	-	ns

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7.5.4 EEPROM AC Timing Characteristics

Symbol	Description	Min.	Max.	Units
fsk	SK clock frequency	0	0.5	MHz
tskh	SK high time	500		ns
tskl	SK low time	500		ns
tcss	CS setup time	100		ns
tcsh	CS hold time	0		ns
tdis	DI setup time	200		ns
tdih	DI hold time	200		ns
tpd0	Output delay to “0”		500	ns
tpd1	Output delay to “1”		500	ns
tsv	CS to status valid		500	ns
tdf	CS to DO high impedance		200	ns

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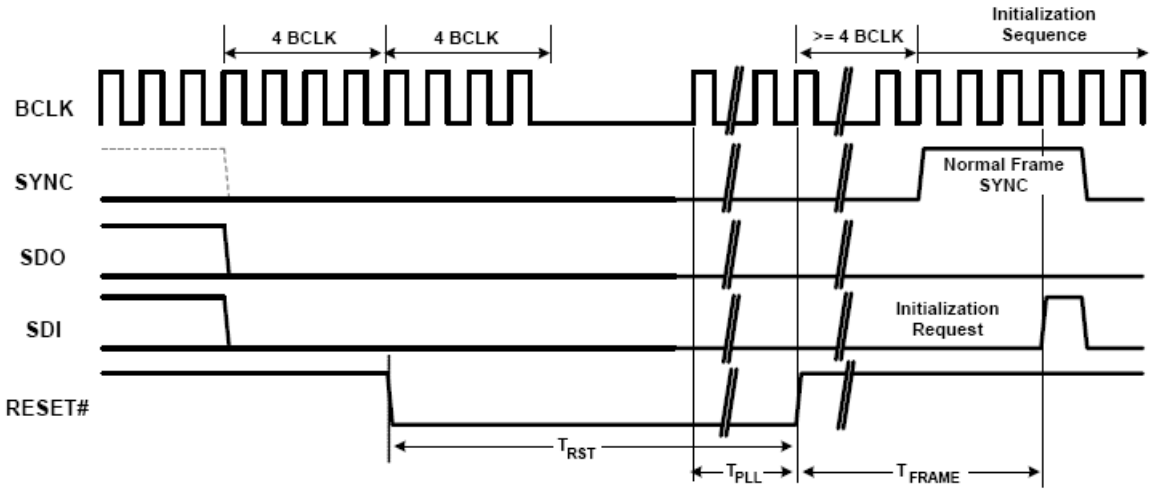
7.5.5 HD Audio-Link Timing Characteristics:

Link Reset and Initialization Timing



Link Reset and Initialization Timing

Link Reset and Initialization Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
RESET#Active Low Pulse Width	Trst	1.0	-	-	us
RESET#Inactive to BCLK Startup delay time for PLL ready	Tpll	20	-	-	us
SDI Initialization Request time	Tframe	-	-	1	FrameTime

Test Conditions: DVCC = 3.3V, DGND =0V,TA=+25oC,unless otherwise stated

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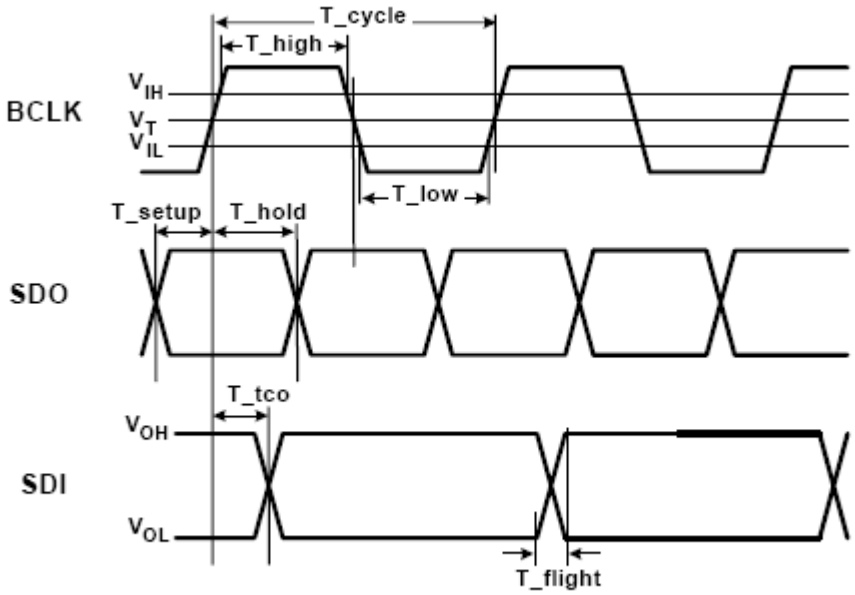
Link Timing Parameters



Link Signals Timing

Link Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
BCLK Frequency	-	-	24	-	MHz
BCLK out Period	Tcycle	-	41.67	-	ns
BCLK Jitter	-	-	-	2.0	ns
BCLK High, Low- Level Width	Thigh/Tlow	18.75	-	22.91	ns
SDO Setup Time at Rising, Falling Edge of BCLK	Tsetup	2.0	-	-	ns
SDO Hold Time at Rising, Falling Edge of BCLK	Thold	2.0	-	-	ns
SDI Valid Time after Rising Edge of BCLK	Ttco	-	7.5	-	ns
SDI Flight Time	Tflight	-	2.0	-	ns

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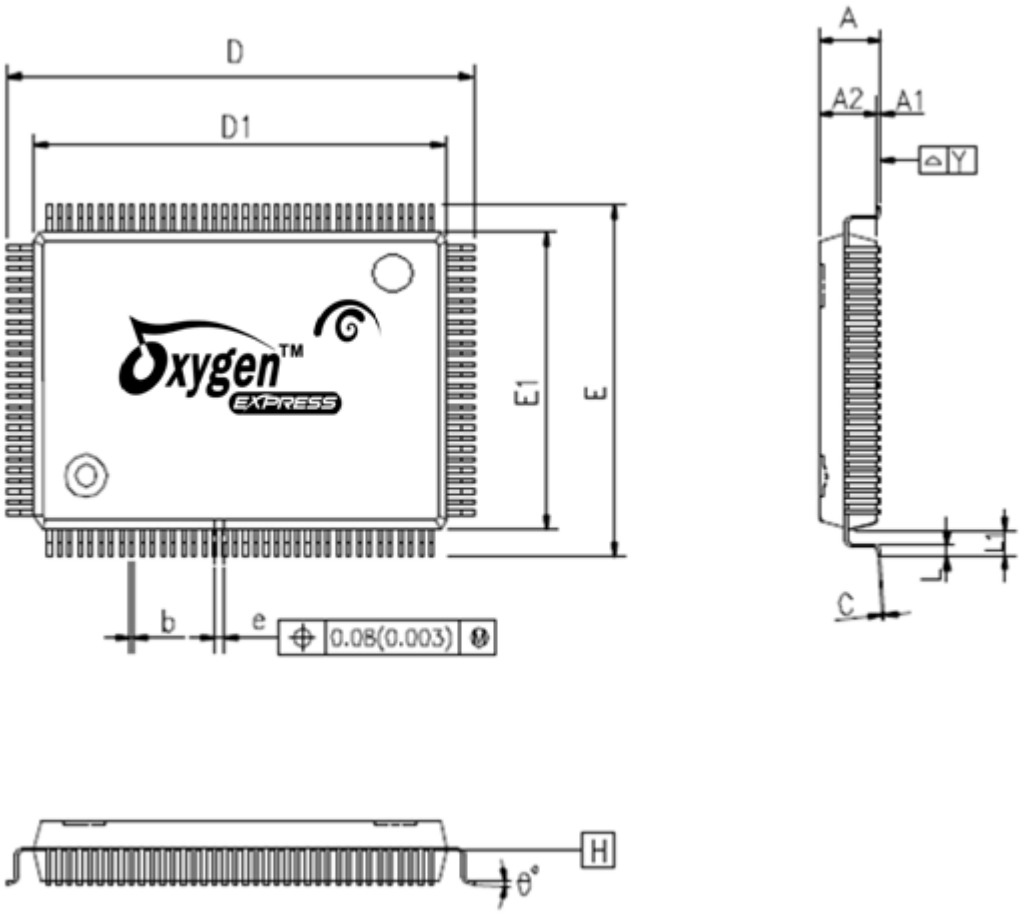
8 Mechanical Specifications

8.1 Package Dimensions



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
C	0 10	0.15	0.20
D1	–	20.00 BSC	–
E1	–	14.00 BSC	–
e	–	0.50 BSC	–
D	–	22.00 BSC	–
E	–	16.00 BSC	–
L	0.45	0.60	0.75
L1	–	1.00 REF	–
Y	–	–	0.08
θ°	0°	3.5°	7°

UNIT : mm

NOTES.

1. JEDEC OUTLINE MS-026 BHB
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS E1 AND D1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS E AND E DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .

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—End of Datasheet—

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