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0. Revision History

Date	Revision	Description
2003/06/30	Rev 1.0	Preliminary Version

1. Features

Basic features:

- Full-duplex 6 channel DAC / 2 channel ADC
- High audio quality much beyond PC 2001 requirements **(A-A SNR > 95 dB)**
- Support 96KHz double sample rate playback for DVD-Audio
- Internal PLL circuit for saving the external crystal

New features of AC'97 2.3 codec:

- **Extensive jack-detection capability** covering front and back panel jacks via patented resistor network method that can save much BOM cost
- **Precise and advanced impedance sensing** for audio device identification, smart configuration, and smart device memorization (with S/W Smart Wizard support)
- **Support 2 stereo microphones recording and playback** to improve telephony and voice recognition applications (via noise reduction & acoustic echo cancellation)
- Integrated **digital PC Beep** for BIOS control.

Versatile I/O functionalities:

- Stereo Line-In jack as Surround-Out.
- Stereo Mic-In jack as Center/LFE output
- Built-in headphone amplifiers at **Line-Out/Surround-Out** pins
- High-quality differential analog CD input and supports **stand-by-power CD playing mode** for consumer systems
- **AUX / Video stereo inputs**
- 2 GPIO (General Purpose I/O) support **additional surround audio bracket detection**
- EAPD (External Amplifier Power Down) support.
- S/PDIF I/O support:
  Output: **96 / 48 kHz with 24 / 20 / 16 bits**
  Input: **48 / 44.1 / 32 kHz with 20 / 16 bits** (**with S/PDIF-In interrupt, auto-lock, anti-noise, and anti-distortion enhancement**)

Valuable software technology:

- Support **Dolby Digital 5.1 RTCE (Real-Time Content Encoder)** output for Dolby-certified MB/Media Center applications (optional)
- **Xear 3D™ sound technology**: 5.1 Virtual SPEAKER SHIFTER and Earphone Plus listening mode (earphone in place of rear speakers)
- Sensaura® CRL3D™ HRTF 3D positional sound and enhancement
- Support Creative EAX™ 1.0/2.0, Microsoft® DirectSound™ 3D (DirectX) H/W&S/W, & A3D™ 1.0 for realistic PC game playing
- **Karaoke functionality** includes unique **Microphone Echo, Key Shifting, and Vocal Cancellation** features
- 10-Band Equalizer with 12 pre-set modes
- 27 listening environment effects plus 3 environmental sizes emulation
- **Dynamic Auto-Gain-Control technology** preventing the volume saturation distortion of playback and recording
- Provide Microsoft WHQL certified drivers compatible with Intel®, SiS®, VIA®, ALi®, and nVidia® SB AC'97 audio controllers

2. Overview

C-Media CMI9761 is a 6 channel, Intel® AC'97 Rev. 2.3 compliant audio codec. It's applicable to extensive chipsets including Intel® ICHx series as well as those supplied by SiS®, VIA®, Ali®, and nVidia®. Its universal driver passed Microsoft WHQL certification on Windows XP, 2000, ME, 98. It also has Windows NT and Linux driver. The excellent audio quality (SNR>95dB), cost-effective design, and powerful/sophisticated driver makes CMI9761 the best solution for designing multimedia desktops, media center, and notebooks.

The versatile features of CMI9761 can satisfy customer's system requirements and create value more than users' expectation. The new jack-detection & impedance-sensing patented technology within CMI9761 can minimize user's intervention and try-and-error effort during the initial setup. With precise advanced sensing technology, CMI9761 can detect most device classes correctly with smart learning ability and make smart configuration accordingly. Therefore, it will reduce a lot of customer service cost and give users very positive impression.

The optional Dolby® Digital Real-Time Content Encoder (RTCE) embedded in the driver can promote much value for end products with Dolby logo on the system. It makes PC able to transmit multi-channel Dolby® Digital audio stream with low distortion and noise to the external decoder via digital S/PDIF link and to utilize users' high-quality Home Theater acoustics. It realizes media center concept and facilitates online audio streaming application to home. The 96 kHz / 24 bits S/PDIF output capability of CMI9761 can easily distribute the premium-quality sound such as DVD-Audio to Consumer Electronics.

Combining with C-Media innovative Xear 3D™ 5.1 Virtual SPEAKER SHIFTER sound technology, even audiophiles will be surprised at the better-than-soundcard features and will enjoy the convenience of 5.1CH sound at 2 speakers and the magic of moving each virtual speaker to anywhere they want.

3. Pin Assignment

PIN #	Signal Name	PIN #	Signal Name
1	DVDD1	25	AVDD1
2	XTL_IN	26	AVSS1
3	XTL_OUT	27	VREF
4	DVSS1	28	VREFOUT1
5	SDATA_OUT	29	VREFOUT2
6	BIT_CLK	30	NC
7	DVSS2	31	NC
8	SDATA_IN	32	NC
9	DVDD2	33	FMIC_R
10	SYNC	34	FMIC_L
11	RESET#	35	LINEOUT_L
12	NC	36	LINEOUT_R
13	JACKSENSE2	37	EXT_R
14	AUX_L	38	AVDD2
15	AUX_R	39	SURR_OUT_L
16	VIDEO_L	40	JACKSENSE1
17	VIDEO_R	41	SURR_OUT_R
18	CD_L	42	AVSS2
19	CD_C	43	CENTER_OUT
20	CD_R	44	LFE_OUT
21	MIC1	45	HP_ON / GPIO0
22	MIC2	46	XTLSEL / GPIO1
23	LINE_IN_L	47	EAPD / SPDIFI
24	LINE_IN_R	48	SPDIFO

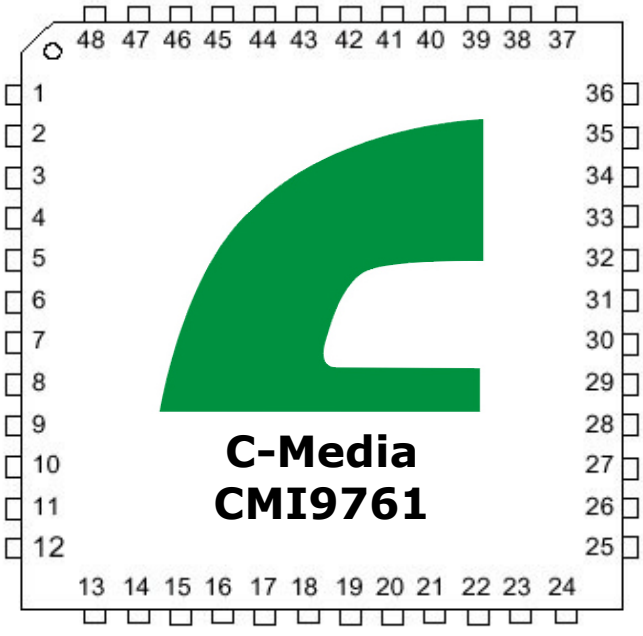

Figure 1. Pin Assignment

4. Pin / Signal Descriptions

4.1 Power / Ground

The digital portion of CMI9761 operates at 3.3V and the analog portion operates at 5V. The grounds should be separated well to assure the best analog audio quality.

Pin No	Signal Name	Type	Description
1	DVDD1	I	Digital VDD (3.3V)
4	DVSS1	I	Digital ground
7	DVSS2	I	Digital ground
9	DVDD2	I	Digital VDD (3.3V)
25	AVDD1	I	Analog VDD (5V)
26	AVSS1	I	Analog ground
38	AVDD2	I	Analog VDD (5V)
42	AVSS2	I	Analog ground

4.2 AC-Link / Clocking

These signals connect CMI9761 to its AC'97 controller counterpart and external crystal / oscillator clock source.

Pin No	Signal Name	Type	Description
2	XTL_IN	I	24.576 MHz crystal input or 14.318 MHz oscillator input
3	XTL_OUT	O	24.576 MHz crystal output or **NC** (for 14.318 MHz oscillator input)
5	SDATA_OUT	I	Serial, time division multiplexed, input stream from the AC'97 controller.
6	BIT_CLK	O	12.288 MHz bit clock output
8	SDATA_IN	O	Serial, time division multiplexed, output stream to the AC'97 controller.
10	SYNC	I	48 kHz sample sync
11	RESET#	I	AC'97 master H/W reset

Note: # denotes active low

4.3 Digital I/O

These signals are digital inputs and outputs of CMI9761 that includes S/PDIF I/O and GPIO.

Pin No	Signal Name	Type	Description
45	HP_ON/GPIO0	I/O	Headphone ON detection / General Purpose I/O #0
46	XTLSEL/GPIO1	I/O	Clock source selection / General Purpose I/O #1
47	EAPD/SPDIFI	I/O	External Amplifier Power Down or S/PDIF input
48	SPDIFO	O	S/PDIF output

4.4 Analog I/O

These signals connect CMI9761 to analog sources and sinks, including microphones and speakers.

Pin No	Signal Name	Type	Description
14	AUX_IN_L	I	Aux input left channel
15	AUX_IN_R	I	Aux input right channel
16	VIDEO_L	I	Video audio input left channel
17	VIDEO_R	I	Video audio input right channel
18	CD_L	I	CD audio input left channel
19	CD_C	I	CD audio common channel
20	CD_R	I	CD audio input right channel
21	MIC1	I/O	Stereo microphone left channel / Alternative center channel output
22	MIC2	I/O	Stereo microphone right channel / Alternative LFE channel output
23	LINE_IN_L	I/O	Line-In input left channel / Alternative rear output left channel
24	LINE_IN_R	I/O	Line-In input right channel / Alternative rear output right channel
33	FMIC_R	I	Front panel stereo microphone right channel
34	FMIC_L	I	Front panel stereo microphone left channel
35	LINEOUT_L	O	Line output left channel

Pin No	Signal Name	Type	Description
36	LINEOUT_R	O	Line output right channel
39	SURR_OUT_L	O	Dedicated rear output left channel
41	SURR_OUT_R	O	Dedicated rear output right channel
43	CENTER_OUT	O	Dedicated center output channel
44	LFE_OUT	O	Dedicated LFE output channel

4.5 Filter / Reference

These signals of CMI9761 connected to resistors or capacitors.

Pin No	Signal Name	Type	Description
27	VREF	O	Reference voltage
28	VREFOUT1	O	Reference voltage out for MIC1 bias
29	VREFOUT2	O	Reference voltage out for MIC2 bias
37	EXT_R	O	For external 1KΩ precision resistor reference

4.6 Configuration

These pins utilize C-Media proprietary parallel resistors method for jack detection.

Pin No	Signal Name	Type	Description
13	JACKSENSE 2	I	Jack sensing pin 2
40	JACKSENSE 1	I	Jack sensing pin 1

Note: For detailed information, please refer to Sec. 5.1 to facilitate the implementation of resistors network.

5. Jack Detection and Configuration Information

In this section, we describe the resistors network method for jack detection and configuration identification. And also, due to the design of CMI9761 with shared audio function and dedicated multi-channel output, the configuration of audio system can be as versatile as possible.

5.1 Resistors Network Method

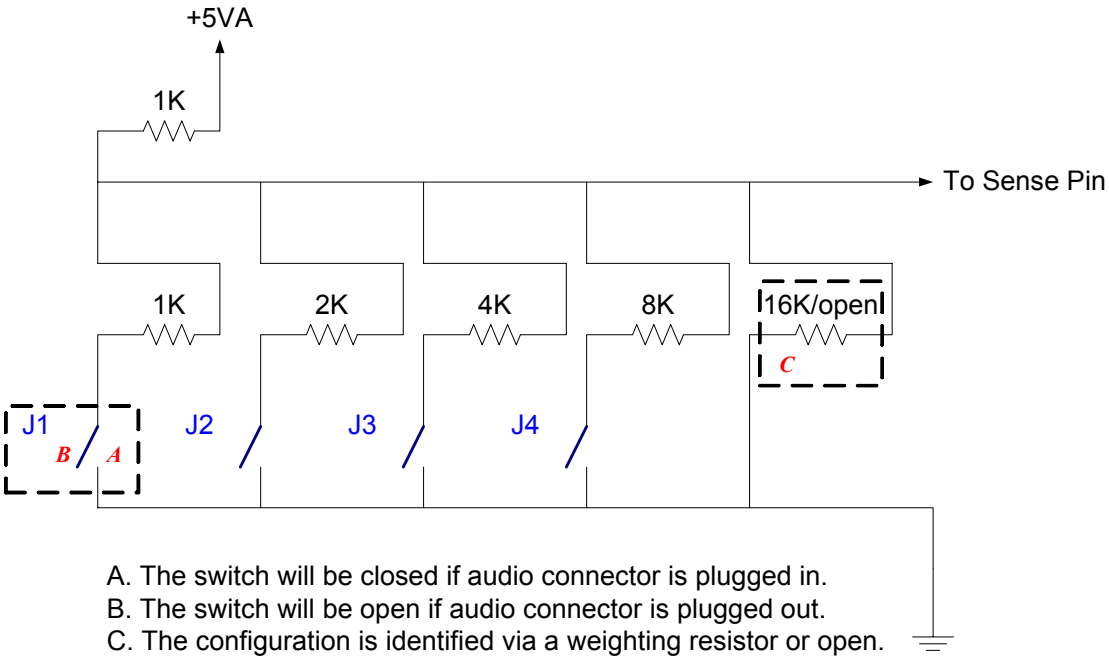

Figure 2. Resistors Network Method for Jack Detection

The sense pin connects to an ADC internally to measure the resistance of the network. CMI9761 is able to monitor the plugging status of each jack according to the resistance measured. To obtain a correct result, the value of each precision resistor should not be modified from the specified schematics provided by C-Media for any reason.

5.2 Configuration Diagram

C-Media CMI9761 - Recommended Configuration Diagram

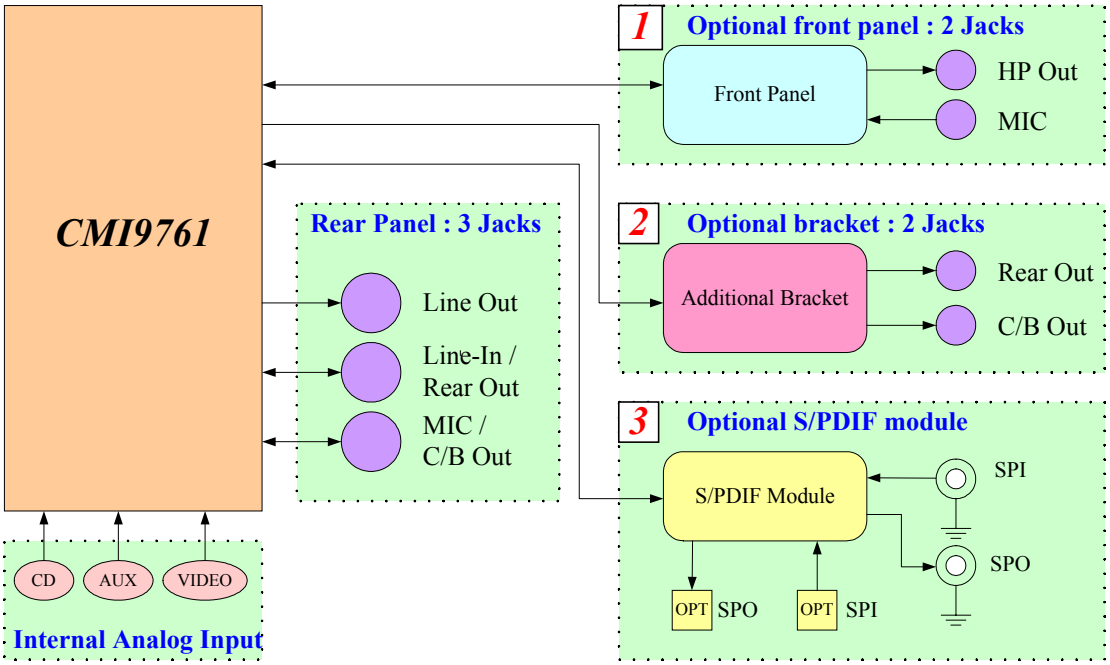

Figure 3. Recommended Configuration Diagram

6. DC Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Digital power supply	DVdd	3.135	3.3	3.465	V
Input voltage range	V_{in}	-0.30	-	DVdd+0.3	V
Low level input voltage	V_{il}	-	-	0.35xDVdd	V
High level input voltage	V_{ih}	0.65xDVdd	-	-	V
High level output voltage	V_{oh}	0.90xDVdd	-	-	V
Low level output voltage	V_{ol}	-	-	0.10xDVdd	V
Input leakage current (AC-Link inputs)	-	-10	-	10	µA
Output leakage current (Hi-Z'd AC-Link outputs)	-	-10	-	10	µA
Input/Output Pin Capacitance	-	-	-	7.5	pF

7. AC-Link Timing Characteristics

7.1 Cold Reset Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	µs
REEST# inactive to SDATA_IN or BIT_CLK active delay	$T_{tri2actv}$	-	-	25	ns
RESET# inactive to BIT_CLK startup delay	$T_{rst2clk}$	162.8	-	-	ns
BITCLK active to RESET# asserted	$T_{clk2rst}$	0.416	-	-	µs

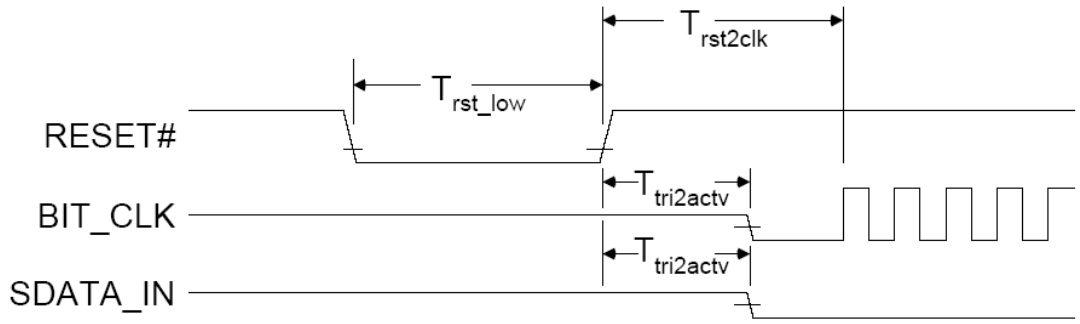

Figure 4. Cold Reset Timing Diagram

7.2 Warm Reset Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
SYNC active high pulse width	T_{sync_high}	1.0	-	-	µs
SYNC inactive to BIT_CLK startup delay	$T_{sync2clk}$	162.8	-	-	ns

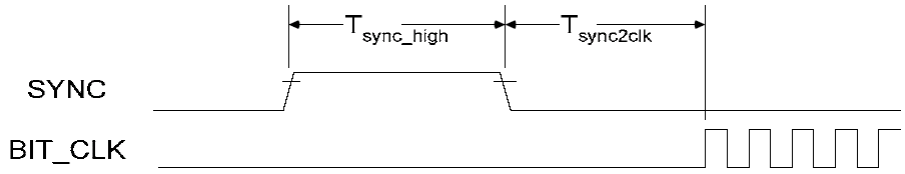

Figure 5. Warm Reset Timing Diagram

7.3 AC-Link Clocks

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter		-	-	750.0	ps
BLT_CLK high pulse width (note 1)	T_{clk_high}	36.0	40.7	45.0	ns
BIT_CLK low pulse width (note 1)	T_{clk_low}	36.0	40.7	45.0	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	T_{sync_period}	-	20.8	-	µs
SYNC high pulse width	T_{sync_high}	-	1.3	-	µs
SYNC low_pulse width	T_{sync_low}	-	19.5	-	µs

Note 1: Worse case duty cycle restricted to 45/55.

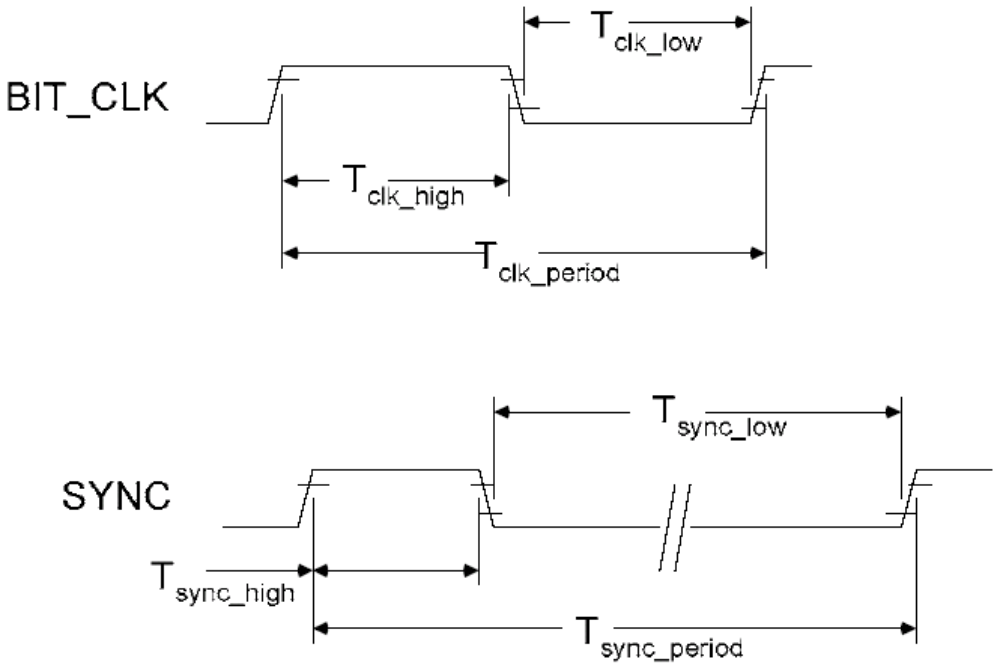

Figure 6. BIT_CLK and SYNC Timing Diagram

7.4 Data Output and Input Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output valid delay from rising edge of BIT_CLK	T_{co}	-	-	15.0	ns

Note: 50pF external load.

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Setup to falling edge of BIT_CLK	T_{setup}	10.0	-	-	ns
Input Hold from falling edge of BIT_CLK	T_{hold}	10.0	-	-	ns

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK combined rise or fall plus flight time	-	-	-	7.0	ns
SDATA combined rise or fall plus flight time	-	-	-	7.0	ns

Note: Combined rise or fall plus flight times are provided for worst case scenario modeling purposes.

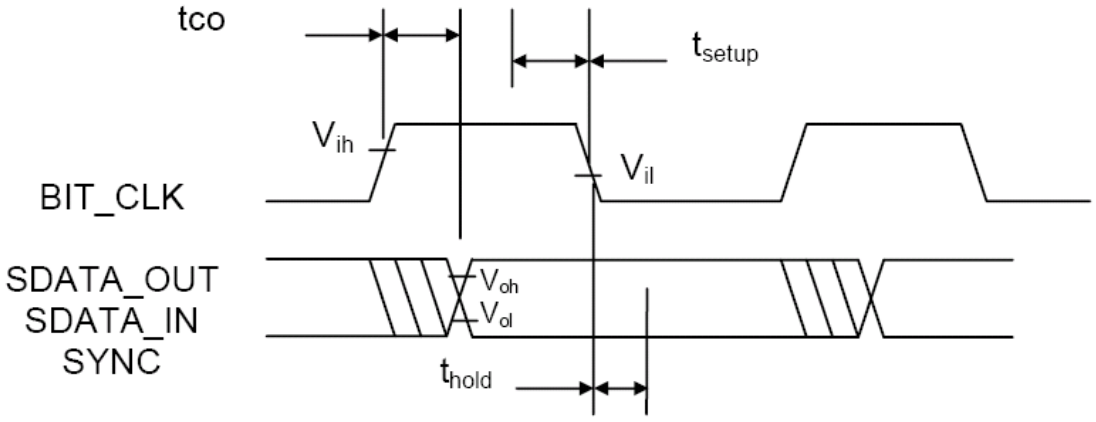

Figure 7. Data Output and Input Timing Diagram

7.5 Signal Rise and Fall Timing

The rise time is from 10% to 90% of VDD (V_{ol} to V_{oh}). The fall time is from 90% to 10% of VDD (V_{oh} to V_{ol}).

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK rise time (note 1)	$Trise_{clk}$	-	-	6.0	ns
BIT_CLK fall time (note 1)	$Tfall_{clk}$	-	-	6.0	ns
SYNC rise time (note 1)	$Trise_{sync}$	-	-	6.0	ns
SYNC fall time (note 1)	$Tfall_{sync}$	-	-	6.0	ns
SDATA_IN rise time (note 2)	$Trise_{din}$	-	-	6.0	ns
SDATA_IN fall time (note 2)	$Tfall_{din}$	-	-	6.0	ns
SDATA_OUT rise time (note 1)	$Trise_{dout}$	-	-	6.0	ns
SDATA_OUT fall time (note 1)	$Tfall_{dout}$	-	-	6.0	ns

Note 1: 75pF external load

Note 2: 60pF external load

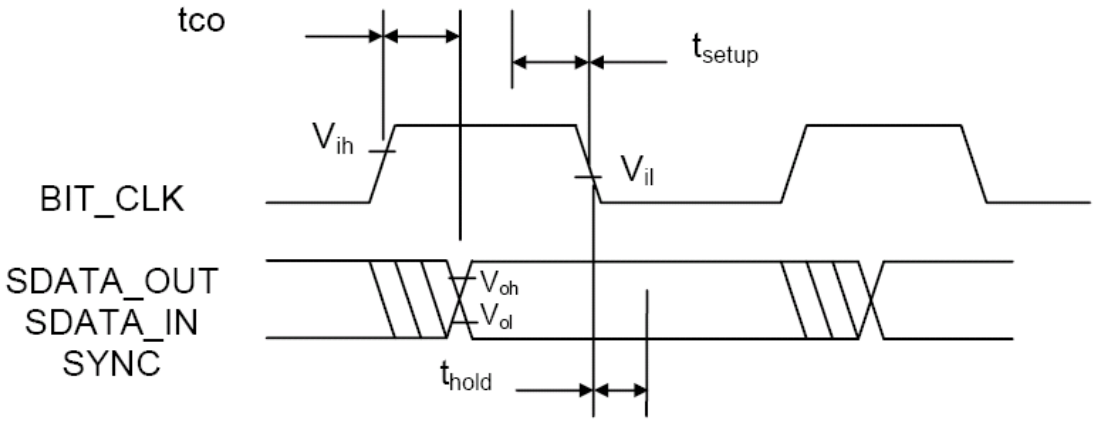

Figure 8. Signal Rise and Fall Timing Diagram

7.6 AC-Link Low Power Mode Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	µs

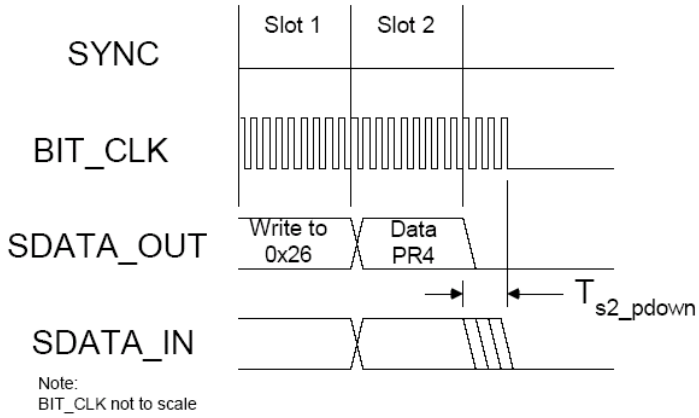

Figure 9. AC-Link Low Power Mode Timing Diagram

7.7 ATE Test Mode

Parameter	Symbol	Minimum	Typical	Maximum	Units
Setup to trailing edge of RESET# (also applies to SYNC)	$T_{setup2rst}$	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	T_{off}	-	-	25.0	ns

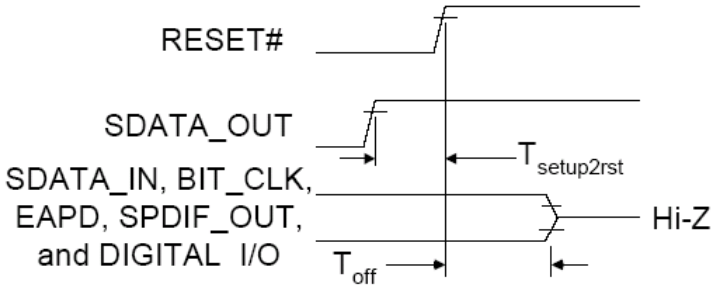

Figure 10. ATE Test Mode Timing Diagram

8. Analog Performance Characteristics

The measurements are performed under the circumstance as: $T_{ambient}$ = 25□, AVdd = 5.0V ± 5%, DVdd = 3.3V ± 5%, 10kΩ/50pF external load. Input is 1 kHz sine wave; Sampling frequency = 48 kHz; Bandwidth = 20 to 20 kHz; 0dB attenuation; All sound effects such as 3D effects are disabled.

Parameter	Minimum	Typical	Maximum	Units
Full Scale Input Voltage:				
Line Inputs	-	1.1	1.4	Vrms
Mic Inputs	-	0.1	-	Vrms
Full Scale Output Voltage:				
LINEOUT	-	1.1	1.4	Vrms
REAROUT	-	1.1	-	Vrms
CENTER_OUT / LFE_OUT	-	1.1	-	Vrms
Frequency Response				
A/A	20	-	20,000	Hz
D/A	20	-	20,000	Hz
A/D	20	-	20,000	Hz
Dynamic Range				
A/A	-	96	-	dB
D/A	-	92	-	dB
A/D	-	85	-	dB
SNR				-
A/A	-	95	-	dB
D/A	-	92	-	dB
A/D	-	90	-	dB
Total Harmonic Distortion Plus Noise				
A/A	-	-92	-	dB
D/A	-	-75	-	dB
A/D	-	-76	-	dB
Cross-talk @ 10KHz	-	92	-	dB
Power Supply Current				
AVDD (5.0V)	-	50	-	mA
DVDD (3.3V)	-	10	-	mA
Vrefout	-	2.25	-	V

9. Package Dimension

Dimensions are shown in inches (mm)

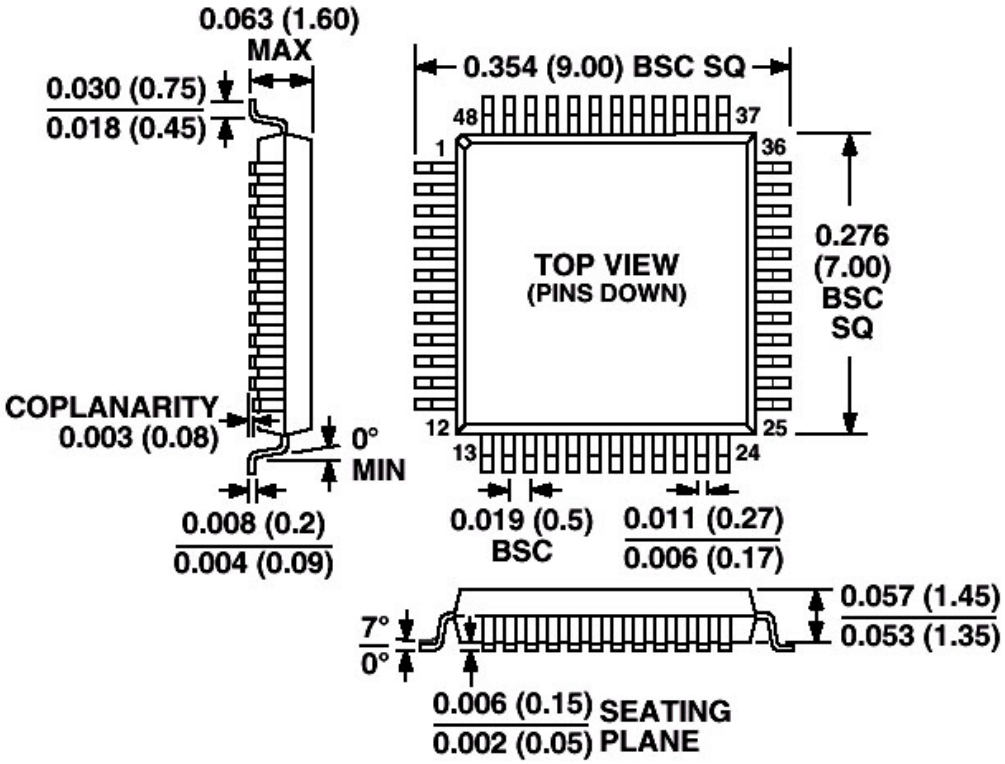

Figure 11. Mechanical Dimension

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