Document Title

256K x 16 bit Super Low Power and Low Voltage Full CMOS RAM

Revision History

Revision No.	History	Draft date	Remark
0.0	Initial Draft	Dec. 22nd, 2003	Preliminary
0.1	Add tCP=10ns in AC characteristics Minor Changes	Mar. 10th, 2004	Final
0.2	Minor Changes	Jul. 6th, 2004	Final
0.3	Modified functional description & MRS update timing Minor Changes	Nov. 8th, 2004	Final
0.4	Added G(Pb-Free) and H(Pb-Free & Halogen Free) descriptions Removed the MRS DPD function Minor Changes	Oct. 26th, 2005	Final
0.5	Removed 60ns descriptions	Aug. 22nd, 2006	Final

256K x 16 bit Super Low Power and Low Voltage Full CMOS RAM

FEATURES

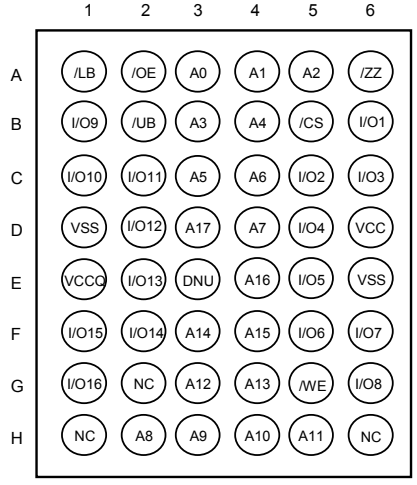
- Process Technology : Full CMOS
- Organization : 256K x 16
- Power Supply Voltage : 2.7~3.3V
- Low Power & Page Modes
  - CMP0417AA1 : support the PASR function
  - CMP0417AA2 : support the DPD function
  - CMP0417AA4 : support the PASR/PAGE function
  - CMP0417AA5 : support the DPD/PAGE function
- Three state output and TTL Compatible
- Package Type : 48-FBGA-6.00x8.00 mm²
- Separated I/O power(VCCQ) & Core Power(VCC)
- Page read/write operation up to 16 words (CMP0417AA4, CMP0417AA5)
- DPD mode when /ZZ goes low (CMP0417AA2, CMP0417AA5)

PRODUCT FAMILY

Product Family	Operating Temperature	Operating Voltage (V)			Speed	Power Dissipation					
						ICC1		ICC2		ISB1 (CMOS Standby Current)	
						f = 1MHz		f = fmax			
		Min.	Typ.	Max.		Typ.	Max.	Typ.	Max.	Typ.	Max.
CMP0417AAx-F70E	Industrial (-25~85℃)	2.7	3.0	3.3	70ns	1.5mA	3mA	12mA	20mA	30uA	70uA

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at Vcc = Vcc (typ) and T_A = 25C.
2. F=FBGA, G=FBGA(Pb-Free), H=FBGA(Pb-Free & Halogen Free), W=WAFER

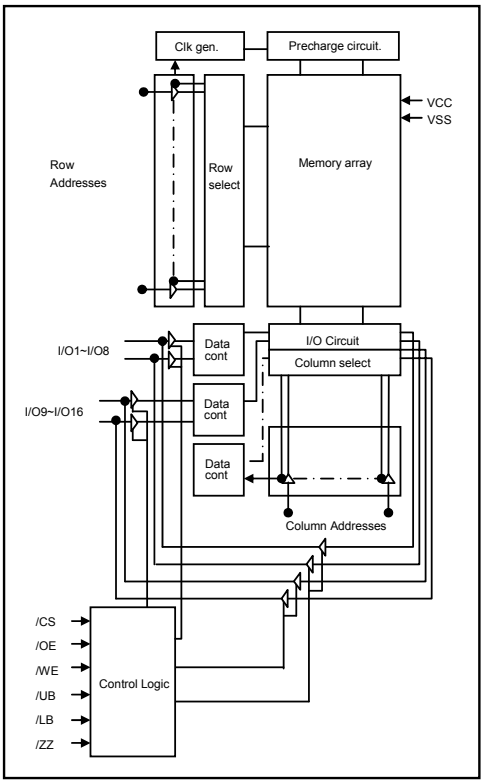
PIN DESCRIPTION



48-FBGA : Top View(Ball Down)

Name	Function	Name	Function
/ZZ	Low Power Modes	VCC	Core Power
/CS	Chip Select Input	VCCQ	I/O Power
/OE	Output Enable Input	VSS	Ground
/WE	Write Enable Input	/UB	Upper Byte(I/O9~16)
A0~A17	Address Inputs	/LB	Lower Byte(I/O 1~8)
I/O1~I/O16	Data Inputs/Outputs	DNU	Do Not Use
NC	No Connection		

FUNCTIONAL BLOCK DIAGRAM



PRODUCT LIST

Extended Temperature Products(-25~85'C)	
Part Name	Function
CMP0417AAx-F70E	48-FBGA, 70ns, VCC=3.0V, VCCQ=3.0V(2.5V,1.8V)

1. F=FBGA, G=FBGA(Pb-Free), H=FBGA(Pb-Free & Halogen Free), W=WAFER

FUNCTIONAL DESCRIPTION

/CS	/ZZ	/OE	/WE	/LB	/UB	I/O1-8	I/O9-16	Mode	Power
H	H	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	L	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	DPD[2]
H	L	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Low Power Modes[3]
X[1]	H	X[1]	X[1]	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X[1]	High-Z	High-Z	Output Disabled	Active
	H	H	H	X[1]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
				H	L	High-Z	Dout	Upper Byte Read	Active
				L	L	Dout	Dout	Word Read	Active
		X[1]	L	L	H	Din	High-Z	Lower Byte Write	Active
				H	L	High-Z	Din	Upper Byte Write	Active
				L	L	Din	Din	Word Write	Active

1. X means don't care.(Must be low or high state)
2. In case of CMP0417AA2 & CMP0417AA5 product
3. In case of CMP0417AA1 & CMP0417AA4 product

ABSOLUTE MAXIMUM RATINGS[1]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to Vcc+0.3V	V
Voltage on Vcc supply relative to Vss	Vcc	-0.2 to 3.6	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	'C
Operating Temperature	T_A	-25 to 85	'C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1]

Item	Symbol	CMP0417AA						Unit
		Min	Max	Min	Max	Min	Max	
Supply voltage	Vcc	2.7	3.3	2.7	3.3	2.7	3.3	V
I/O operating voltage (VCCQ ≤ VCC)	VCCQ	2.7	3.3	2.25	2.75	1.65	1.95	V
Ground	Vss	0	0	0	0	0	0	V
Input high voltage	V_{IH}	0.8VCCQ	VCC+0.2[2]	0.8VCCQ	VCC+0.2[2]	0.8VCCQ	VCC+0.2[2]	V
Input low voltage	V_{IL}	-0.2[3]	0.2VCCQ	-0.2[3]	0.2VCCQ	-0.2[3]	0.2VCCQ	V

Note :
1. T_A=-25 to 85'C, otherwise specified.
2. Overshoot : Vcc+1.0V in case of pulse width≤20ns.
3. Undershoot : -1.0V in case of pulse width≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1] (f=1MHz , T_A=25'C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	CIN	VIN=0V	-	8	pF
Input/Output capacitance	CIO	VIO=0V	-	8	pF

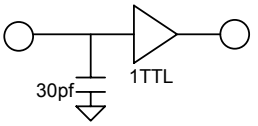
1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	ILI	VIN=VSS to VCC	-1	-	1	uA
Output leakage current	ILO	/CS=VIH, /ZZ=VIH, /OE=VIH or /WE=VIL, VIO=VSS to VCC	-1	-	1	uA
Average operating current	ICC1	Cycle time=1us, 100%duty, IIO=0mA, /CS≤0.2V, /ZZ=VIH, VIN≤0.2V or VIN≥VCC-0.2V	-	-	**3**	mA
	ICC2	Cycle time=Min, IIO=0mA, 100% duty, /CS=VIL, /ZZ=VIH, VIN=VIL or VIH	-	-	25	mA
Output low voltage	VOL	IOL=0.5mA			0.2VCCQ	V
Output high voltage	VOH	IOH=-0.5mA	0.8VCCQ			V
Standby Current(TTL)	ISB	/CS=VIH, /ZZ=VIH, Other inputs=VIH or VIL	-	-	0.3	mA
Standby Current(CMOS)	ISB1	/CS≥VCC-0.2V, /ZZ≥VCC-0.2V, Other inputs=0~VCC	-	-	70	uA
Deep Power Down Current[1]	ISB0	/ZZ≤0.2V, Other inputs=0~VCC, No refresh(DPD)	-	-	10	uA
Low Power Modes	ISB0a	/ZZ≤0.2V, Other inputs=0~VCC, ¼ refresh area selection	-	-	40	uA
	ISB0b	/ZZ≤0.2V, Other inputs=0~VCC, ½ refresh area selection	-	-	50	uA
	ISB0c	/ZZ≤0.2V, Other inputs=0~VCC, All refresh area selection	-	-	70	uA

1. CMP0817BA2 & CMP0817BA5 products support DPD(Deep Power Down) Current

AC OPERATING CONDITIONS



TEST CONDITIONS(Test Load and Input/Output Reference)
Input pulse level : 0.2 to VCC-0.2V
Input rising and falling time : 5ns
Input and output reference voltage : 0.5*VCCQ
Output load(see right) : CL=30pF+1TTL

AC CHARACTERISTICS(VCC=2.7V~3.3V, Extended product : T_A=-25 to 85'C)

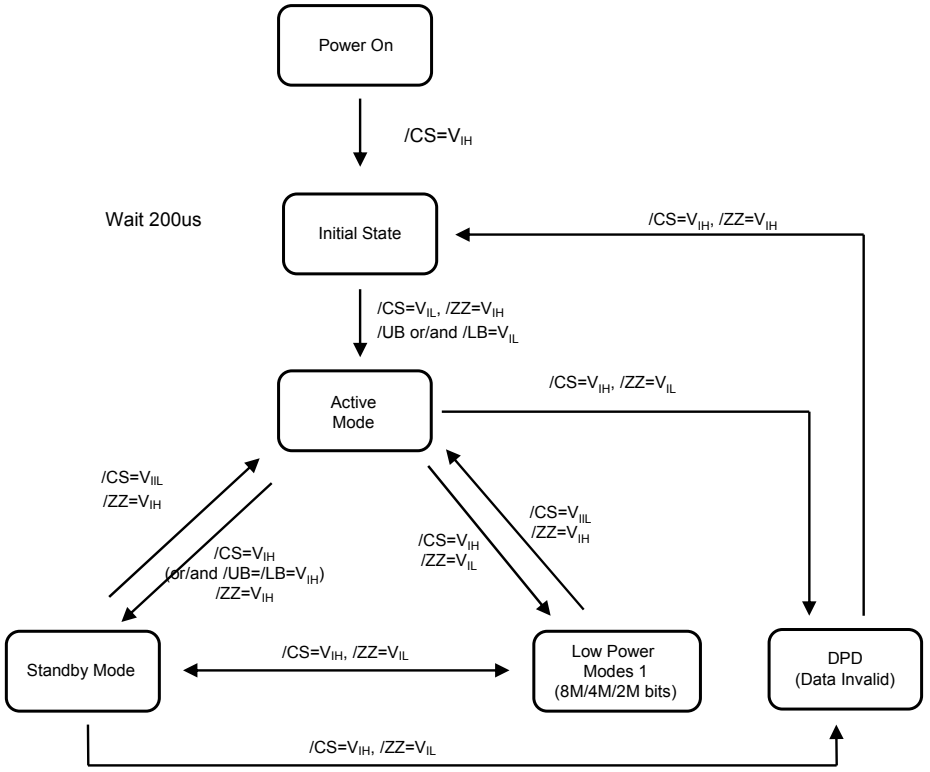
Parameter List		Symbol	70ns		Units
			Min	Max	
Read	Read Cycle Time	tRC	70	160k	ns
	Address Access Time	tAA	-	70	ns
	Chip Select to Output	tCO	-	70	ns
	Output Enable to Valid Output	tOE	-	25	ns
	/UB, /LB Access Time	tBA	-	70	ns
	Chip Select to Low-Z Output	tLZ	10	-	ns
	/UB, /LB Enable to Low-Z Output	tBLZ	10	-	ns
	Output Enable to Low-Z Output	tOLZ	5	-	ns
	Chip Disable to High- Z Output	tHZ	0	5	ns
	/UB, /LB Disable to High- Z Output	tBHZ	0	5	ns
	Output Disable to High- Z Output	tOHZ	0	5	ns
	Output Hold from Address Change	tOH	5	-	ns
Write	Write Cycle Time	tWC	70	160k	ns
	Chip Select to End of Write	tCW	60	-	ns
	Address Set-up Time	tAS	0	-	ns
	Address Valid to End of Write	tAW	60	-	ns
	/UB, /LB Valid to End of Write	tBW	60	-	ns
	Write Pulse Width	tWP	50	-	ns
	Write Recovery Time	tWR	0	-	ns
	Write to Output High-Z	tWHZ	0	5	ns
	Data to Write Time Overlap	tDW	20	-	ns
	Data Hold from Write Time	tDH	0	-	ns
	End Write to Output Low-Z	tOW	5	-	ns
Page	Page Mode Cycle Time	tPC	25	-	ns
	Page Mode Address Access Time	tPAA	-	25	ns
	Maximum Cycle Time	tMRC	-	160k	ns
/CS High Pulse Width[1)]		tCP	10	-	ns

1. /CS High Pulse Width is defined by /CS or (/UB and /LB) because /UB & /LB can make standby mode when /UB=High and /LB=High.

Power Up Sequence

1. Apply Power
2. Maintain stable power for a minimum of 200us with /CS=VIH

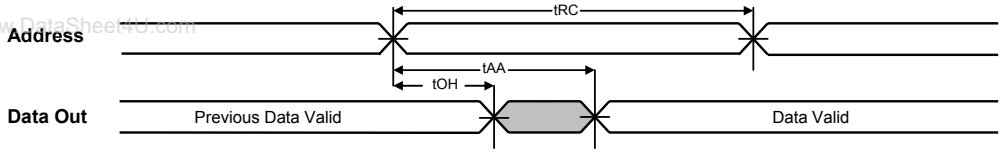
Standby Mode State machines



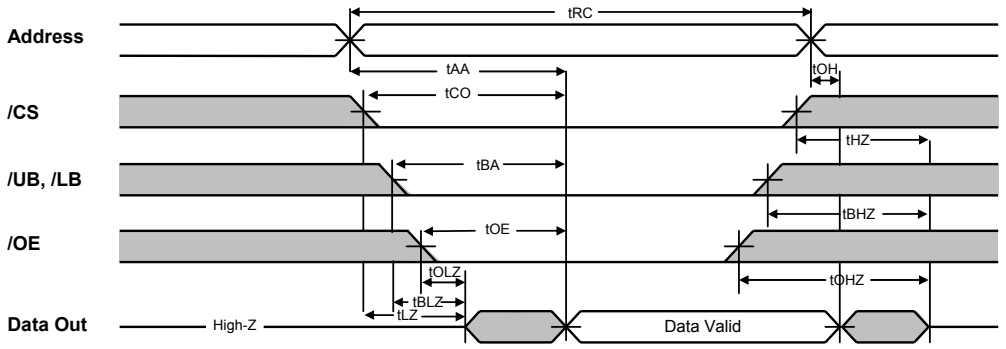
Standby Mode Characteristics

Mode	Memory Cell Data	Standby Current(uA)	Wait Time(us)
Standby	Valid	70 (ISB1)	0
Deep Power Down Mode	Invalid	10 (ISB0)	200
Low Power Modes	¼ valid	40 (ISB0a)	0
	½ valid	50 (ISB0b)	0
	valid	70 (ISB0c)	0

READ CYCLE (1) (Address controlled,/CS=/OE=VIL, /ZZ=/WE=VIH, /UB or/and /LB=VIL)

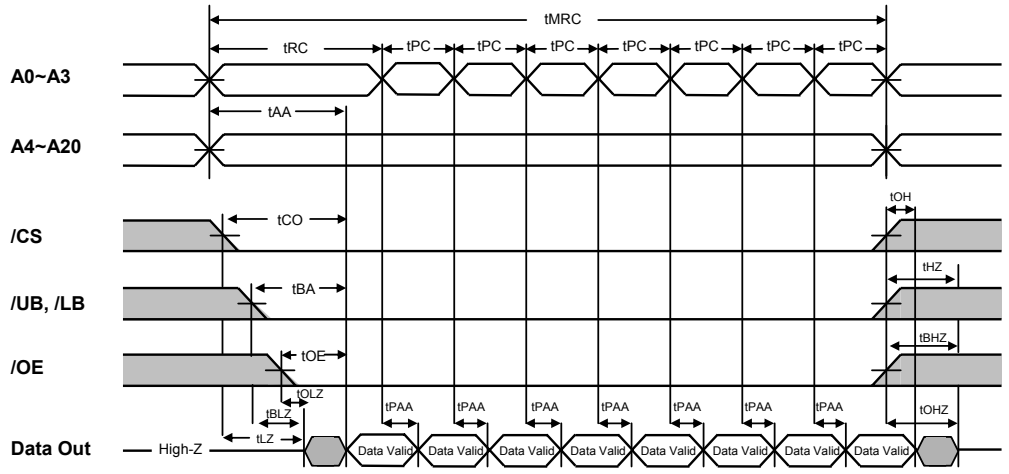


READ CYCLE (2) (/ZZ=/WE=VIH)



1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device interconnection.
3. Do not access device with cycle timing shorter than tRC(tWC) for continuous periods > 160us.

PAGE READ CYCLE (/ZZ=/WE=VIH, 16 words access)



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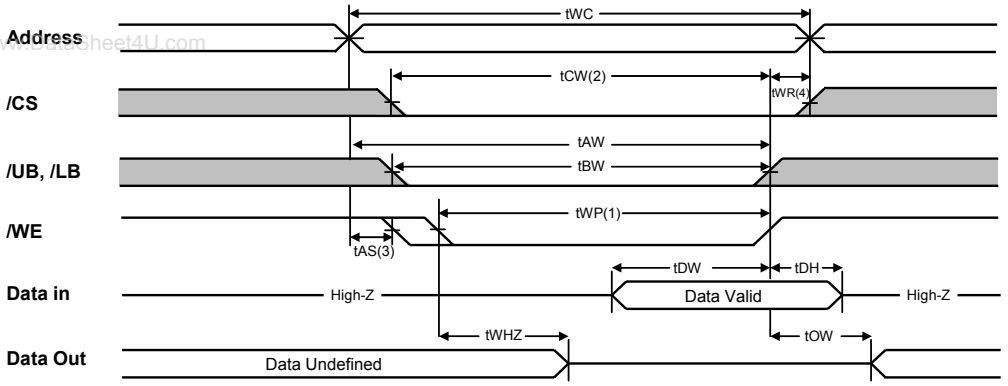
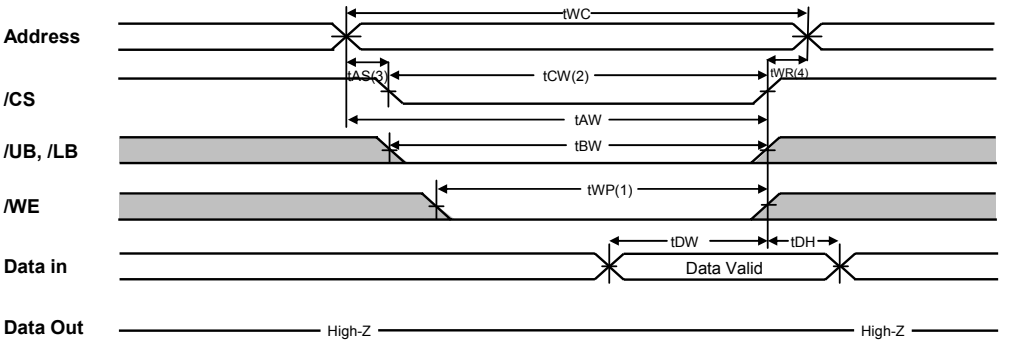
3. Do not access device with cycle timing shorter than tRC(tWC) for continuous periods > 160us.

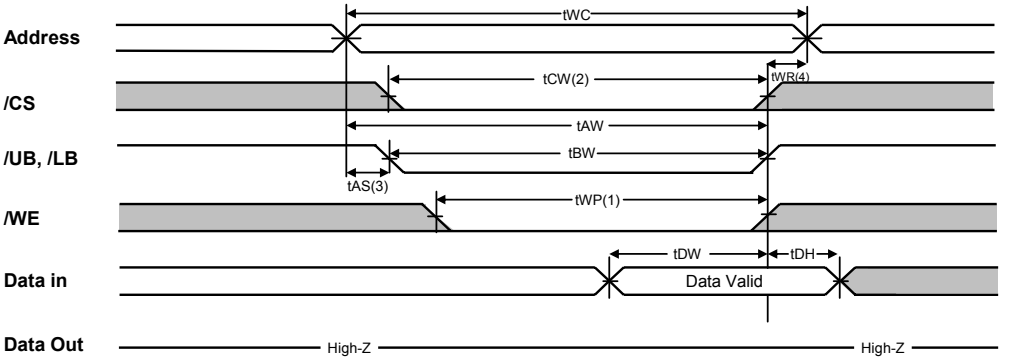
WRITE CYCLE (1) (/WE controlled, /ZZ=VIH)



WRITE CYCLE (2) (/CS controlled, /ZZ=/WE=VIH)

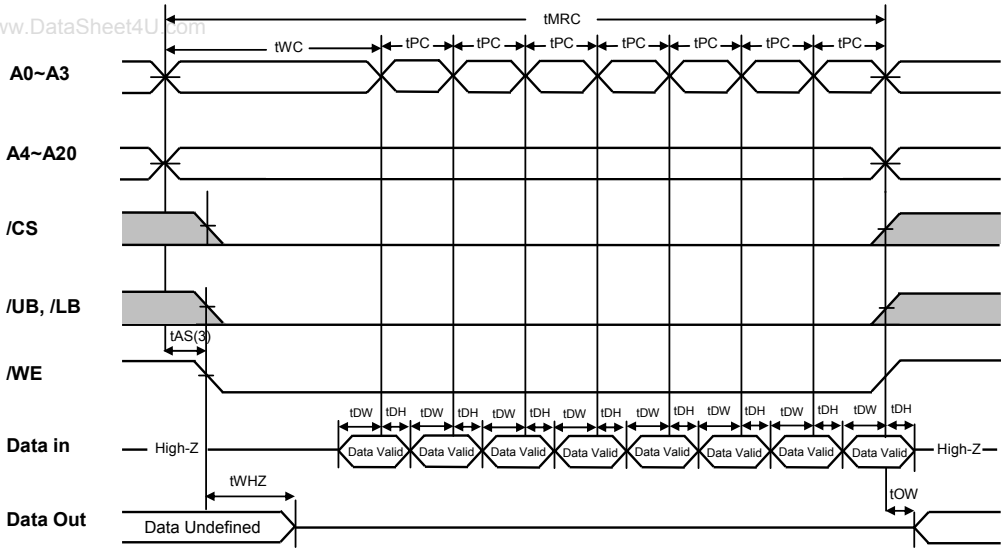


WRITE CYCLE (3) (/UB, /LB controlled, /ZZ=VIH)



1. A write occurs during the overlap (tWP) of low /CS and /WE. A write begins when /CS goes low and /WE goes low with asserting /UB or /LB for single byte operation or simultaneously asserting /UB and /LB for double byte operation. A write ends at the earliest transition when /CS goes high and WE goes high. The tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS or /WE going high.
5. Do not access device with cycle timing shorter than tRC(tWC) for continuous periods > 160us.

PAGE WRITE CYCLE (Address controlled, /ZZ=VIH)



1. A write occurs during the overlap (tWP) of low /CS and /WE. A write begins when /CS goes low and /WE goes low with asserting /UB or /LB for single byte operation or simultaneously asserting /UB and /LB for double byte operation. A write ends at the earliest transition when /CS goes high and /WE goes high. The tWP is measured from the beginning of write to the end of write.
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5. Do not access device with cycle timing shorter than tRC(tWC) for continuous periods > 160us.

LOW POWER MODES

1. Mode Register Set

A17 ~ A5	A4	A3	A2	A1	A0
0	1	Array On/Off on /ZZ	Half Selection	Array Refresh Area	

Array Refresh Area

A1	A0	Type
0	0	Full Array (Default)
0	1	RFU[1)]
1	0	½ Array
1	1	¼ Array

1. RFU : Reserved for the Future Use

Half Selection (Top / Bottom)

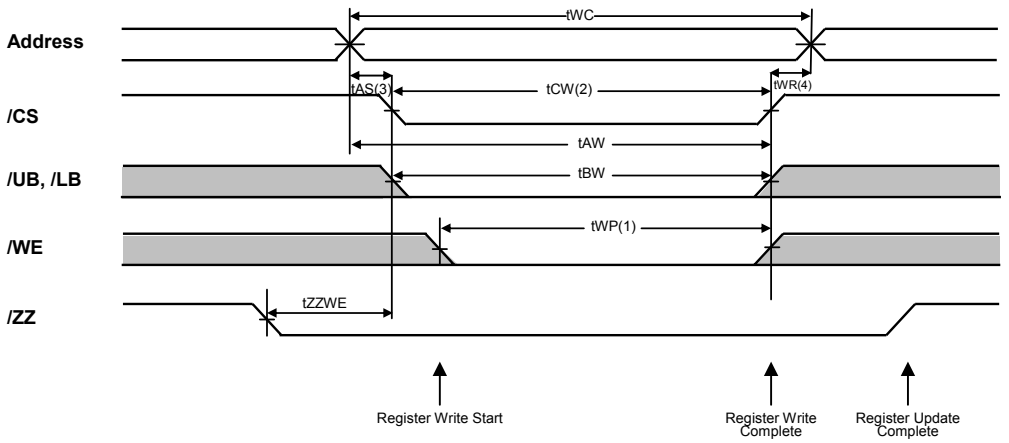
A2	Type
0	Bottom (Default)
1	Top

Array On/Off on /ZZ

A3	Type
0	Partial Array Refresh Mode (Default)
1	Reduced Memory Size Mode

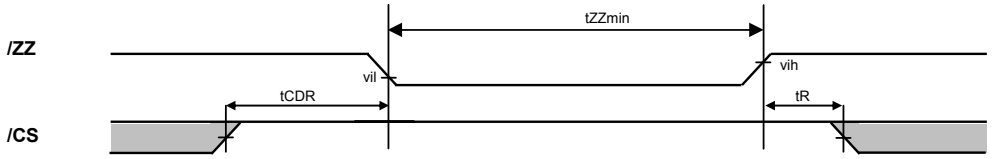
Note: The RMS(Reduced Memory Size) mode is enabled after /ZZ goes high and remains enabled after /ZZ goes high. To change to a different mode, the mode register will have to be rewritten.

2. MRS Update



The register update take place on the rising edge of /ZZ. Once the register is updated, the next time /ZZ goes low, without any updates to the register starting within the tZZWE max time of 1us, the part will refresh the array selected. The data bus is a don't care When /ZZ is low during the register updates.

3. Deep Power Down Mode Entry/Exit



Parameter	Description	Min	Max	Units
tCDR	Chip Deselect to ZZ Low	0	-	ns
tR(Deep Power Down Mode only)	Operation Recovery Time	200	-	us
tZZmin	Low Power Mode Time	10	-	us

4. Address Information

Partial Array Refresh Mode (A3=0, A4=1)

A2	A1,A0	Refresh Section	Address	Size	Density
0	10	1/2	00000h-1FFFFh	128Kbx16	2Mb
X	00	Full	00000h-3FFFFh	256Kbx16	4Mb
1	10	1/2	20000h-3FFFFh	128Kbx16	2Mb

Reduced Memory Size Mode (A3=1, A4=1)

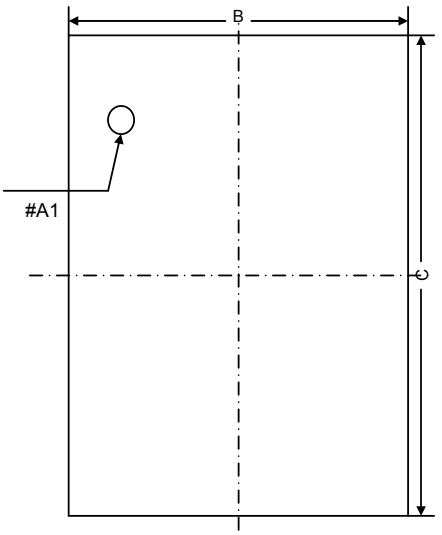
A2	A1,A0	Refresh Section	Address	Size	Density
0	10	1/2	00000h-1FFFFh	128Kbx16	2Mb
1	10	1/2	20000h-3FFFFh	128Kbx16	2Mb

PACKAGE DIMENSION

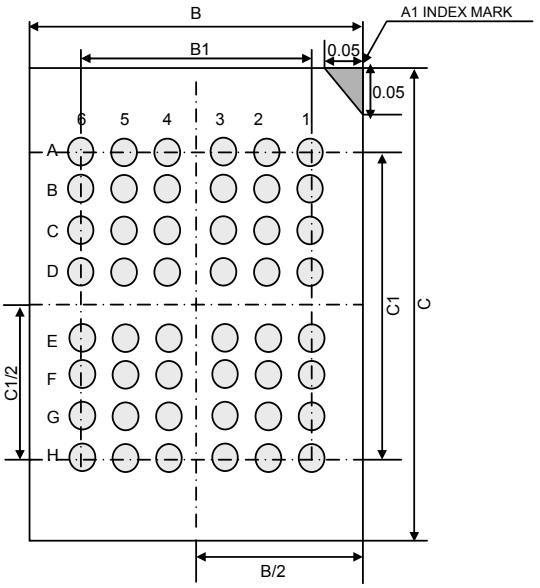
Unit : millimeters

48 BALL FINE PITCH BGA(0.75mm ball pitch)

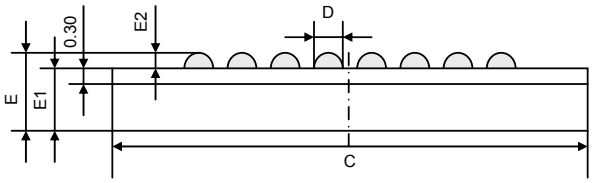
Top View



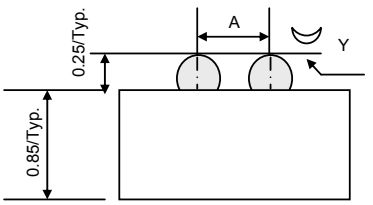
Bottom View



Side View



Detail A



-	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	1.00	-
E1	-	0.75	-
E2	0.20	0.25	0.30
Y	-	-	0.08

NOTES.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)