CMP60N03LD13

N-CHANNEL TRENCH MOSFET

APPLICATION

- Buck Converter High Side Switch
- Other Applications

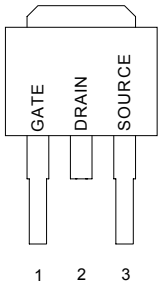
V_{DSS}	$R_{DS(ON)}$ Typ.	I_D
30V	10.8mΩ	55A

FEATURES

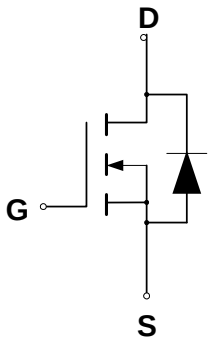
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- Inductive Switching Curves
- Improved UIS Ruggedness

PIN CONFIGURATION

TO-252
Front View



SYMBOL



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain to Source Voltage (Note 1)	V_{DSS}	30	V
Drain to Current — Continuous Tc = 25℃, V_{GS}@10V (Note 2)	I_D	50	A
— Continuous Tc = 100℃, V_{GS}@10V (Note 2)	I_D	Fig.3	
— Pulsed Tc = 25℃, V_{GS}@10V (Note 3)	I_{DM}	Fig.6	
Gate-to-Source Voltage — Continue	V_{GS}	±20	V
Total Power Dissipation	P_D	52	W
Derating Factor above 25℃		0.5	W/℃
Peak Diode Recovery dv/dt (Note 4)	dv/dt	3.0	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	℃
Single Pulse Avalanche Energy L=1.1mH,I_D=30 Amps	E_{AS}	500	mJ
Maximum Lead Temperature for Soldering Purposes	T_L	300	℃
Maximum Package Body for 10 seconds	T_{PKG}	260	℃
Pulsed Avalanche Rating	I_{AS}	Fig.8	

THERMAL RESISTANCE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
$R_{\theta JC}$	Junction-to-case			2.4	℃/W	Water cooled heatsink, P_D adjusted for a peak junction temperature of +150℃
$R_{\theta JA}$	Junction-to-ambient (PCB Mount)			50	℃/W	Minimum pad area, 2-oz copper, FR-4 circuit board, double sided
$R_{\theta JA}$	Junction-to-ambient			62	℃/W	1 cubic foot chamber, free air

ORDERING INFORMATION

Part Number	Package
CMP60N03LD13	TO-252

ELECTRICAL CHARACTERISTICS

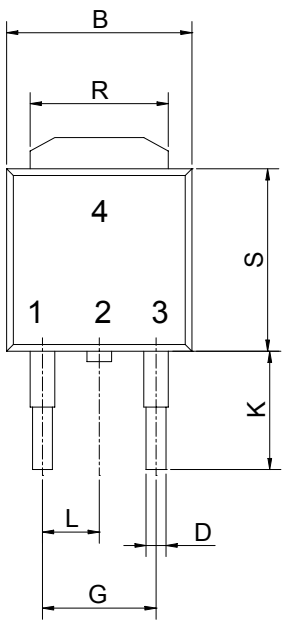
Unless otherwise specified, T_J = 25°C.

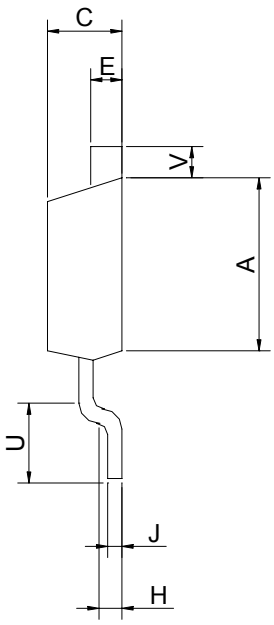
Characteristic		Symbol	CMP60N03LD13 Min	Typ	Max	Units
OFF Characteristics						
Drain-to-Source Breakdown Voltage (V_{GS} = 0 V, I_D = 250 μA)		V_{DSS}	30			V
Breakdown Voltage Temperature Coefficient,Fig.11 (Reference to 25°C, I_D = 250 μA)		$\Delta V_{DSS}/\Delta T_J$		27		mV/°C
Drain-to-Source Leakage Current (V_{DS} = 24 V, V_{GS} = 0 V, T_J = 25°C) (V_{DS} = 24 V, V_{GS} = 0 V, T_J = 125°C)		I_{DSS}			1 10	μA
Gate-to-Source Forward Leakage (V_{GS} = 20 V)		I_{GSS}			100	nA
Gate-to-Source Reverse Leakage (V_{GS} = -20 V)		I_{GSS}			-100	nA
ON Characteristics						
Gate Threshold Voltage,Fig.12 (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	1.0		3.0	V
Static Drain-to-Source On-Resistance, Fig.9,10 (Note 5) (V_{GS} = 10 V, I_D = 15A) (V_{GS} = 4.5 V, I_D = 12A)		$R_{DS(on)}$		 10.8 15.4	 12.5	mΩ
Forward Transconductance (V_{DS} = 15 V, I_D = 12A) (Note 5)		g_{FS}		28		S
Dynamic Characteristics						
Input Capacitance	(V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz) Fig.14	C_{iss}		1520		pF
Output Capacitance		C_{oss}		314		pF
Reverse Transfer Capacitance		C_{rss}		152		pF
Total Gate Charge (V_{GS} = 10 V)	(V_{DS} = 15 V, I_D = 12 A) (Note 6) Fig.15	Q_g		27.9	35	nC
Total Gate Charge (V_{GS} = 4.5 V)		Q_g		14	19	nC
Gate-to-Source Charge		Q_{gs}		4.9		nC
Gate-to-Drain Charge		Q_{gd}		4.3		nC
Resistive Switching Characteristics						
Turn-On Delay Time	(V_{DD} = 15 V, I_D = 12 A, V_{GS} = 10 V, R_G = 1.0Ω) (Note 6)	$t_{d(on)}$		10		ns
Rise Time		t_r		3.4		ns
Turn-Off Delay Time		$t_{d(off)}$		36		ns
Fall Time		t_f		6.0		ns
Turn-On Delay Time	(V_{DD} = 15 V, I_D = 12 A, V_{GS} = 4.5V, R_G = 1.0Ω) (Note 6)	$t_{d(on)}$		16		ns
Rise Time		t_r		7.2		ns
Turn-Off Delay Time		$t_{d(off)}$		34		ns
Fall Time		t_f		14		ns
Source-Drain Diode Characteristics						
Continuous Source Current (Body Diode Fig.16)	Integral pn-diode in MOSFET	I_S			50	A
Pulse Source Current (Body Diode)		I_{SM}			Fig.6	A
Forward On-Voltage	(I_S = 12 A, V_{GS} = 0 V)	V_{SD}			1.0	V
Forward Turn-On Time	(I_F = 12 A, V_{GS} = 0 V, d_i/d_t = 100A/μs)	t_{rr}		25	38	ns
Reverse Recovery Charge		Q_{rr}		31	46	nC

Note 1: T_J = +25℃ to 150℃
Note 2: Current is calculated based upon maximum allowable junction temperature.
Package current limitation is 30A.
Note 3: Repetitive rating; pulse width limited by maximum junction temperature.
Note 4: I_{SD} = 12.0A, di/dt ≤100A/μs, V_{DD} ≤ BV_{DSS}, T_J = +150℃
Note 5: Pulse width ≤ 250μs; duty cycle ≤ 2%
Note 6: Essentially independent of operating temerpature.

PACKAGE DIMENSION

TO-252





PIN 1: GATE
PIN 2: DRAIN
PIN 3: SOURCE

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	5.97	---	6.35	0.235	---	0.250
B	6.35	---	6.73	0.250	---	0.265
C	2.19	---	2.38	0.086	---	0.094
D	0.69	---	0.88	0.027	---	0.035
E	0.84	---	1.01	0.033	---	0.047
G	4.58BSC			0.180BSC		
H	0.87	---	1.01	0.034	---	0.040
J	0.46	---	0.58	0.018	---	0.023
K	2.60	---	2.89	0.102	---	0.114
L	2.29BSC			0.090BSC		
R	4.45	---	5.46	0.175	---	0.215
S	0.51	---	1.27	0.020	---	0.050
U	0.51	---	---	0.020	---	---
V	0.77	---	1.27	0.030	---	0.050

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

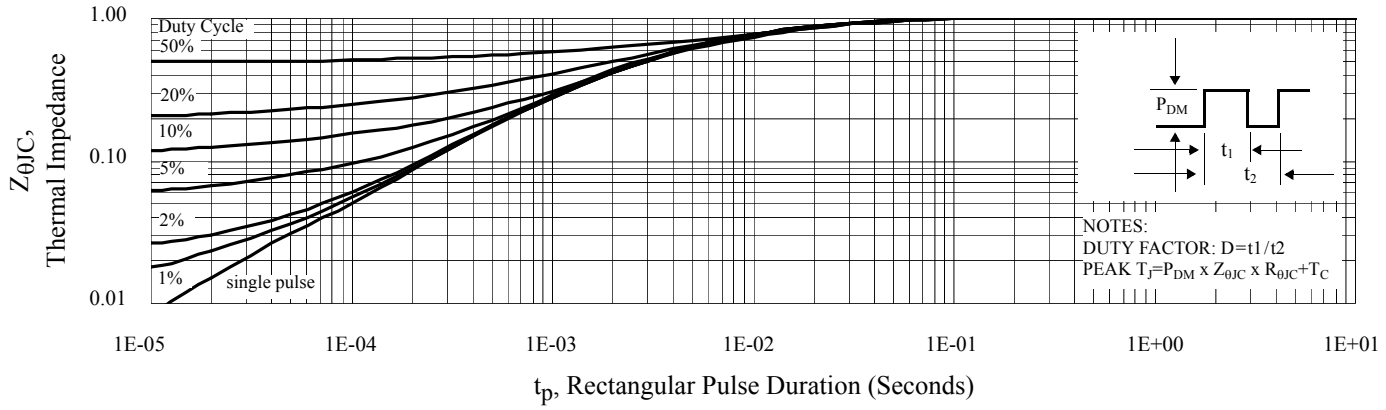


Figure 2. Maximum Power Dissipation vs Case Temperature

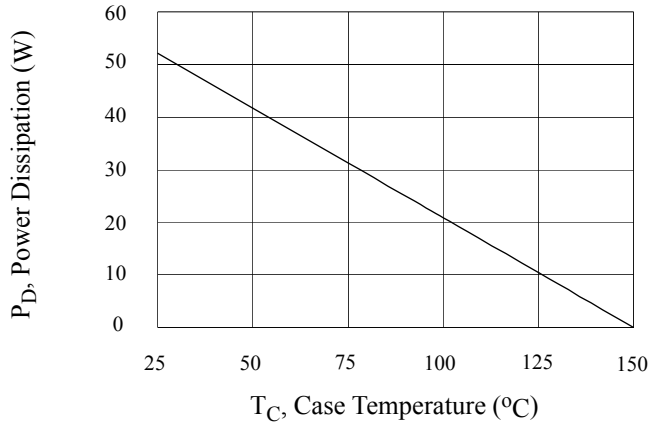


Figure 3. Maximum Continuous Drain Current vs Case Temperature

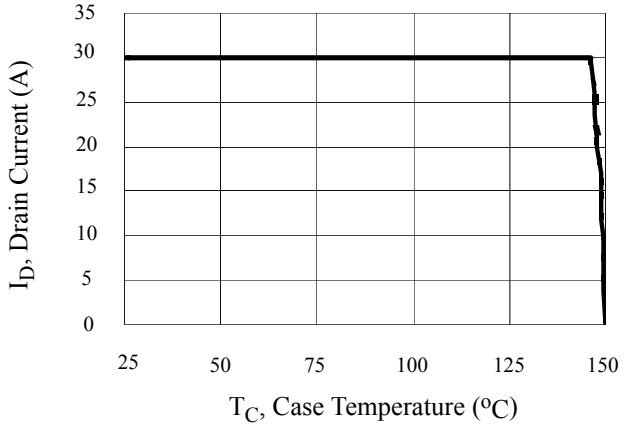


Figure 4. Typical Output Characteristics

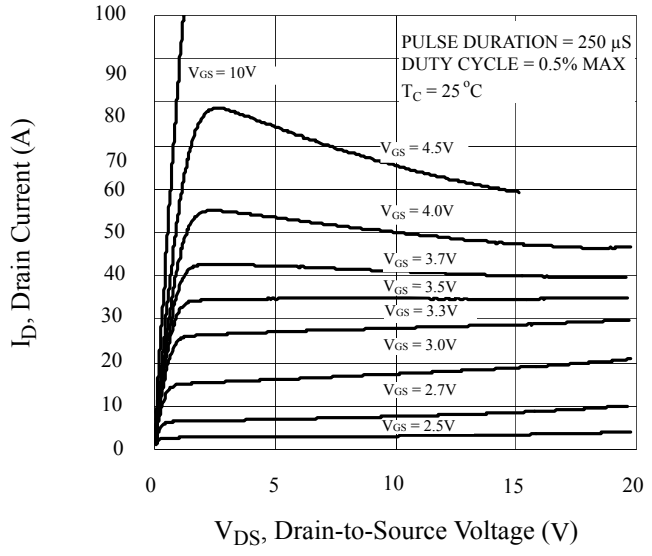


Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

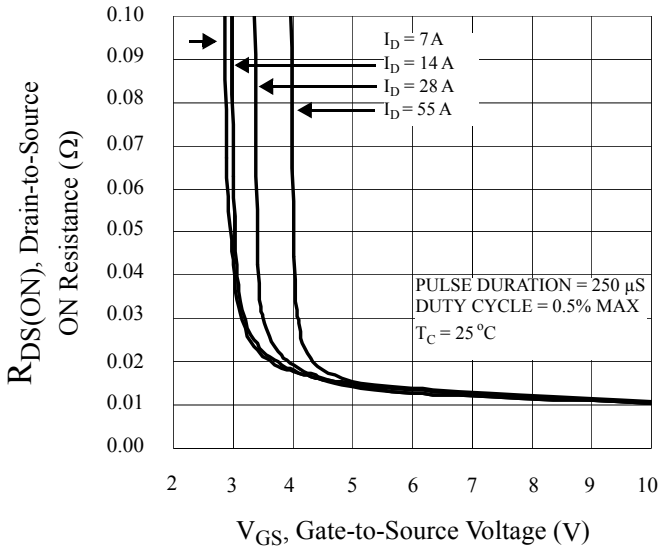


Figure 6. Maximum Peak Current Capability

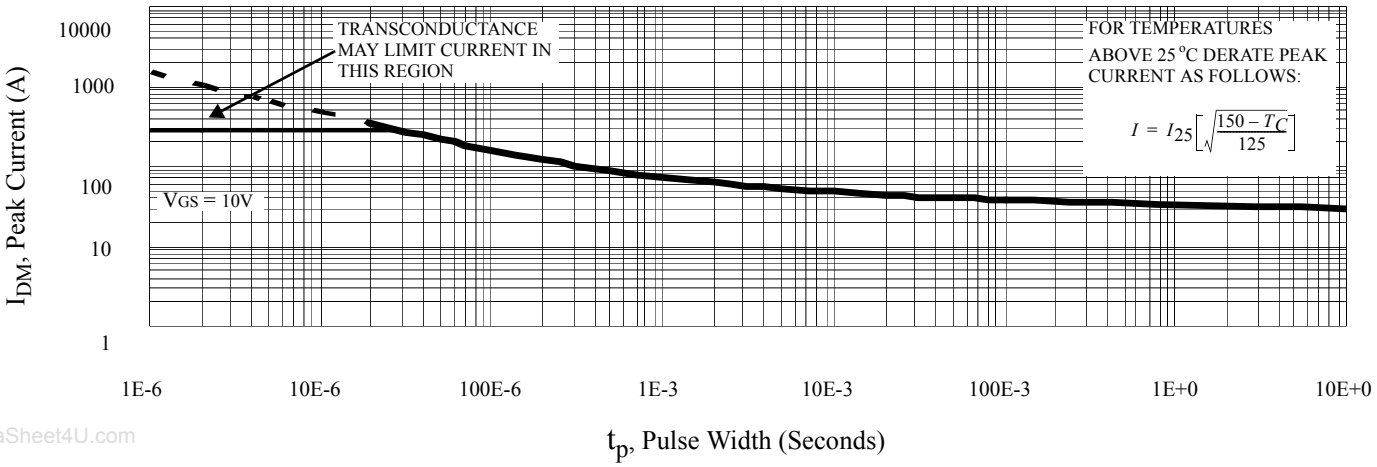


Figure 7. Typical Transfer Characteristics

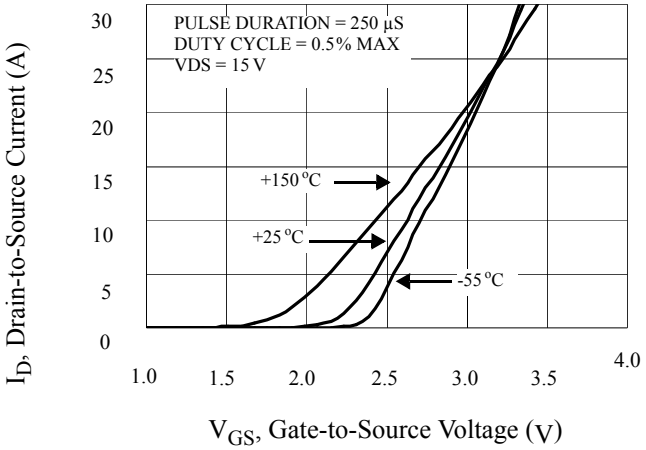


Figure 8. Unclamped Inductive Switching Capability

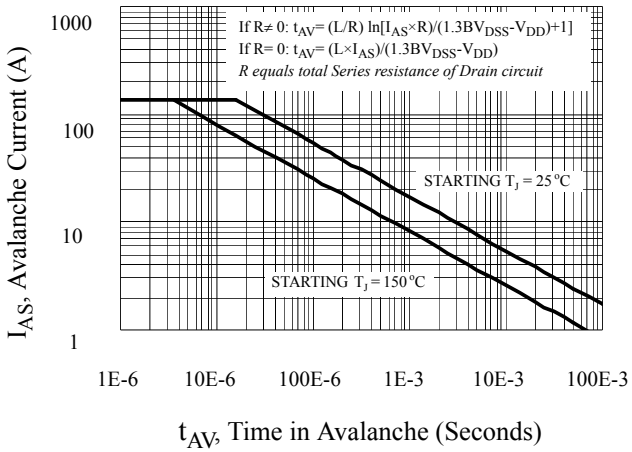


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

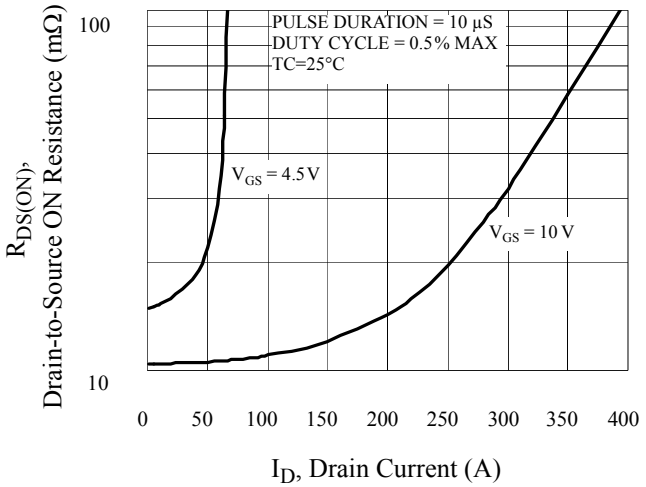


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

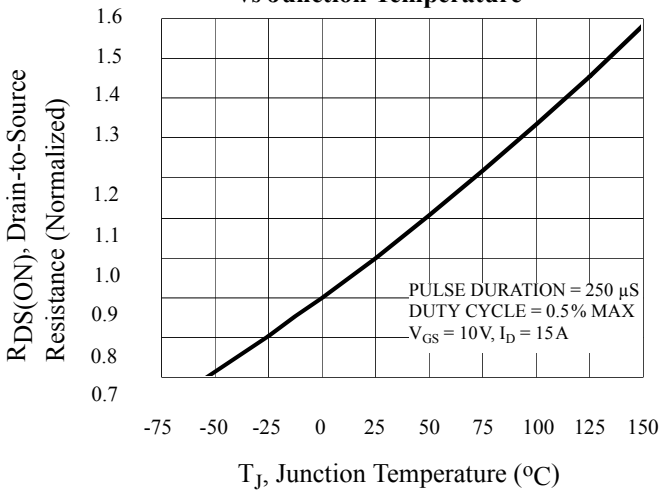


Figure 11. Typical Breakdown Voltage vs Junction Temperature

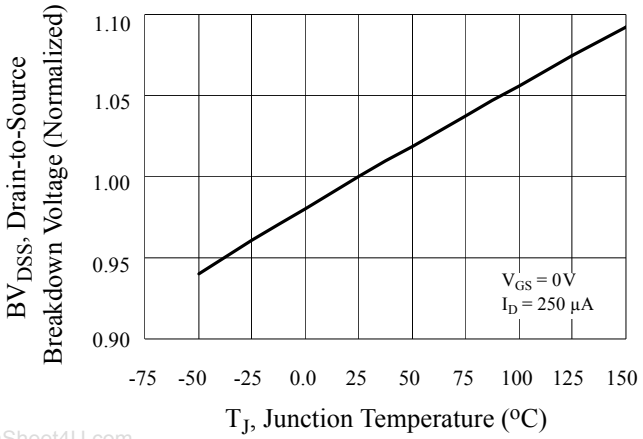


Figure 12. Typical Threshold Voltage vs Junction Temperature

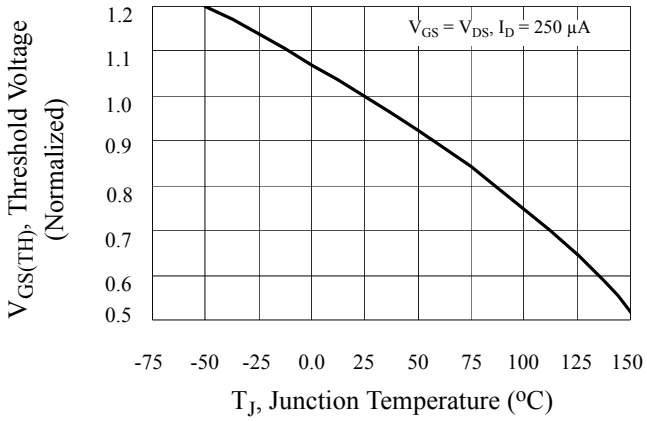


Figure 13. Maximum Forward Bias Safe Operating Area Area

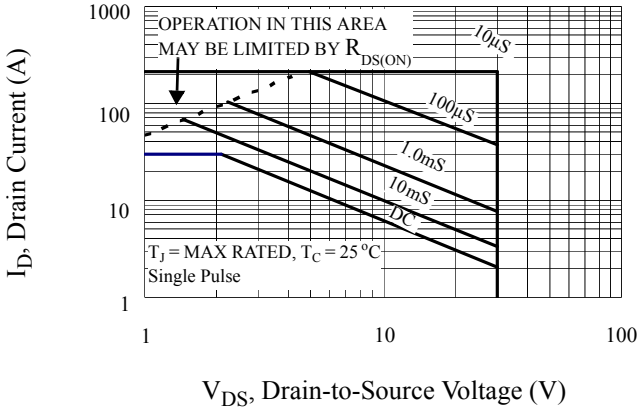


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

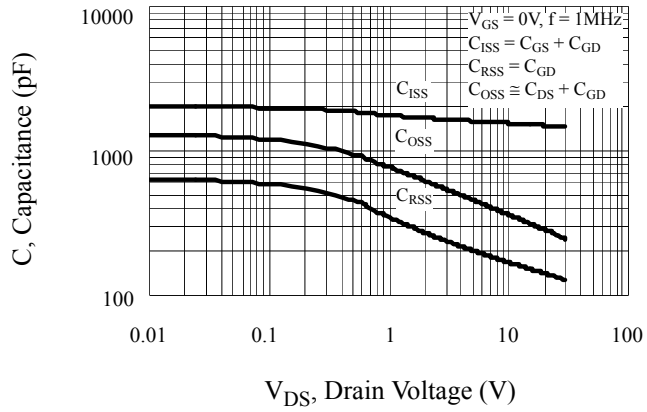


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

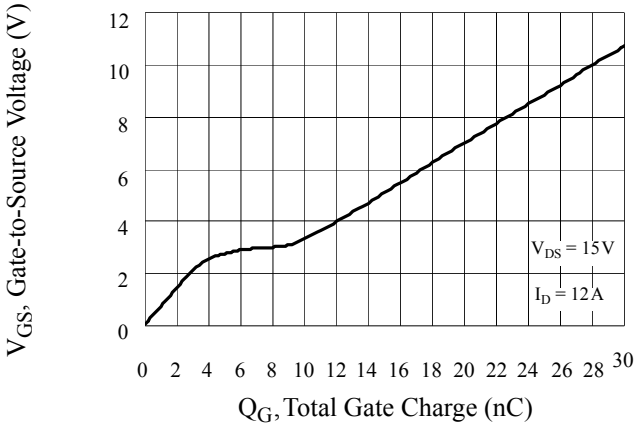
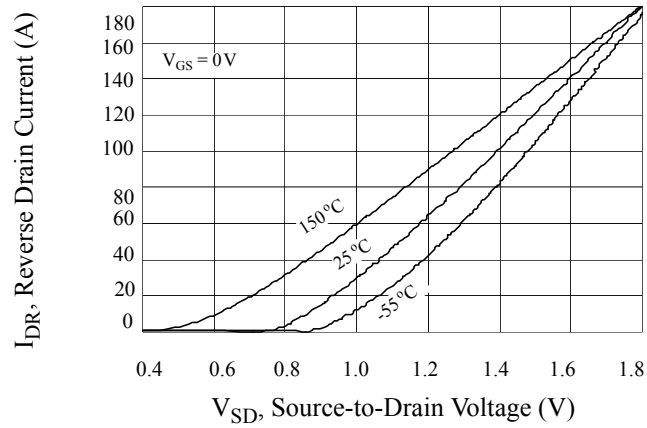


Figure 16. Typical Body Diode Transfer Characteristics



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