CMT-ANTARES DATASHEET

Version: 1.1

High-Temperature, 200mA, 5V Linear Voltage Regulator

General description

CMT-ANTARES is a high-temperature, high-reliability, 200mA adjustable linear voltage regulator suitable to generate from a +4.5V to +30V voltage source a regulated 5V voltage. The operating junction temperature ranges from -55°C to +175°C and can possibly go outside that range with some de-rating of the performance. The regulator is self-protected with a built-in current limiter and a thermal protection, the later becoming effective in the range 240°C to 260°C.

CMT-ANTARES brings unique benefits in applications where the ambient or operating temperature is high and above the temperature supported by traditional semiconductors, or in applications that run in standard 125°C or 150°C but require extended reliability; CMT-ANTARES allows also accelerated aging of the systems for qualification purposes as the device can support higher temperatures.

CMT-ANTARES is available in a standard 3-pins TO-263 plastic package which offers best trade-off between PCB area and thermal resistance. This 3-pins package makes it easy to integrate CMT-ANTARES in your design and allows a drop-in replacement of commercial voltage regulators.

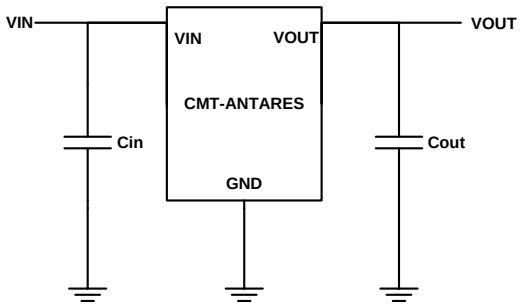
CMT-ANTARES offers a cost effective solution for temperature ranges that are not extreme but well above the temperature supported by traditional semiconductor solutions.

Applications

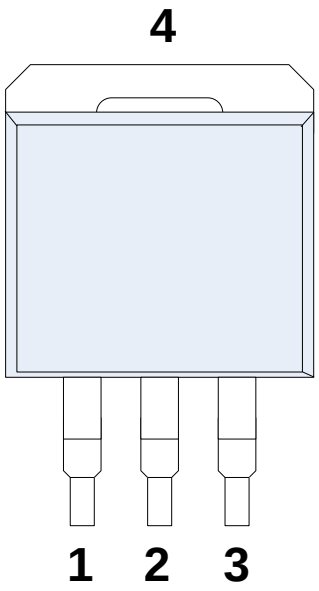
- Regulated power supplies for embedded electronics in automotive, industrial, aerospace and downhole systems.

Features

- Junction operating temperature
  - from -55°C to 175°C
- Input voltage: 5.5V to 30V
- Output voltage : 5V
- Output voltage total accuracy: ±5%
- Output current: 200mA max
- Min voltage dropout @ 100mA: 1.2V
- Line regulation: -1% max
- Load regulation: -0.4% typ
- C_{out}: min 1 µF
- Input ripple rejection:
  - 50dB typ (@ 100Hz)
- Quiescent current (no load, 175°C):
  - 1.3 mA typ.
- Thermal shutdown:
  - Active in the range 240°C to 260°C
- Current limitation: 340 mA typ.
- Latch-up free
- ESD HBM: > 6KV
- Available in TO-263 package
- Validated at 175°C for 2500 hours (and still on-going)
- For AEC-Q100 automotive qualification, please contact CISSOID



Pinout



Pin #	Pin Name	Pin Description
1	Vout	Output voltage
2	Vin	Positive power supply
3	GND	Negative power supply
4		Tab connected to Vin

Absolute Maximum Ratings

Supply Voltage Vin to GND	-0.5 to 40V
Peak output current	Internally limited
Junction Temperature(Tj)	200°C

ESD Rating

Human Body Model	> 6kV

Operating Conditions

Supply Voltage Vin to GND:	5.5V to 30V
Junction temperature	-55°C to +175°C
Continuous current	0 to 200 mA

CAUTION: *Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability.*
Permanent uses of the device in short-circuit state or in over-temperature state may affect long term reliability of the device.

Electrical Characteristics

Unless otherwise stated, T_j = 25°C, C_{in} = 4.7µF, C_{out}= 4.7µF . **Bold** figures point out values valid over the whole temperature range (T_j = -55°C to +175°C).

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Voltage	V_{in}		**5.5**		**30**	V
Dropout[1]	D_r	Iout = 200mA	**2.4**		**25**	V
Output current	I_{out}		**0**		**200**	mA
Output voltage total accuracy		Vin =[7.4-30]V Iout = [0 .. 200]mA	**Vout -5%**		**Vout +5%**	V
Output voltage temperature drift		Vin= 10V Iout = 0mA T_j = [25°C,175°C]		+1.4		%
Output voltage line regulation		Vin =[7-30]V Iout= 0mA			**-1**	%
Output voltage load regulation		Vin =[10V-30V] Iout = [0 .. 200]mA		**-0.4**[2]		%
Quiescent current	I_q	Vin= 10V Iout = 0 mA		**1.3**		mA
		Vin= 30V Iout = 0 mA		**1.34**		
Response to Line Transient		Vin from 10V to 12V (5V/µs) Iout = 50mA		+1.6		%
		Vin from 12V to 10V (5V/µs) Iout = 50mA		-1.6		%
Response to Load Transient		Vin = 10V Iout from 10mA to 200 mA (25mA/µs), T_j = 175°C		-6		%
		Vin = 10V Iout from 200 mA to 10 mA (25mA/µs), T_j = 175°C		+7		%
Power Supply Rejection Ratio (Vin=10V, Iout= [0..200mA])	PSRR	100Hz		**50**		dB
		1 KHz		**30**		dB
Output noise voltage		BW = [1Hz .. 10KHz]		100		μV_{RMS}
Current limit threshold	Isc	Vin = [7-30]V	**250**	340	**450**	mA
Over temperature protection threshold	TH_{OTP}			260		°C
Over temperature protection hysteresis	$Hyst_{OTP}$			10		°C
Junction–to-air thermal resistance[3]	$R_{\Theta JA}$	In free air Vertically mounted		61.6		°C/W
Junction–to-case thermal resistance	$R_{\Theta JC}$			4.6		°C/W

[1] Refer to Figure 11 for evolution of min dropout in function of required output current

[2] Load regulation measurements must be done in a way to avoid self-heating effect

[3] Please refer to graph on page 8 for information about thermal resistance evolution in function of PCB copper pad

Typical Performance Characteristics

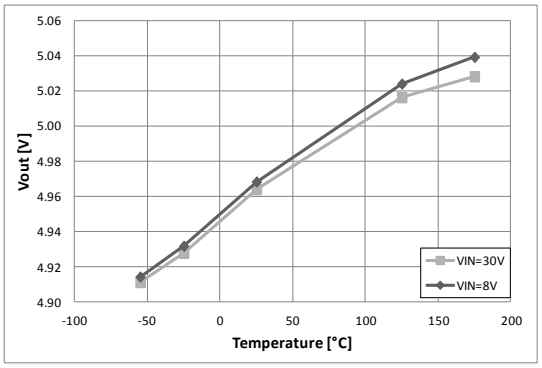


Figure 1: Output voltage temperature drift (Iout = 0 mA)

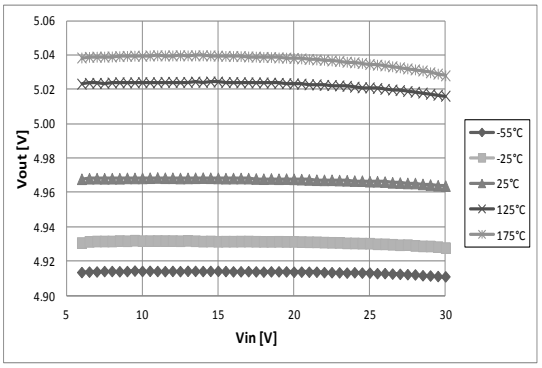


Figure 2: Output voltage line regulation (Iout = 0mA)

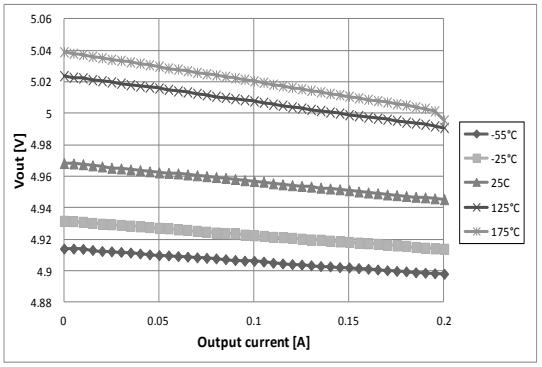


Figure 3: Output voltage load regulation (Vin = 7.4V)

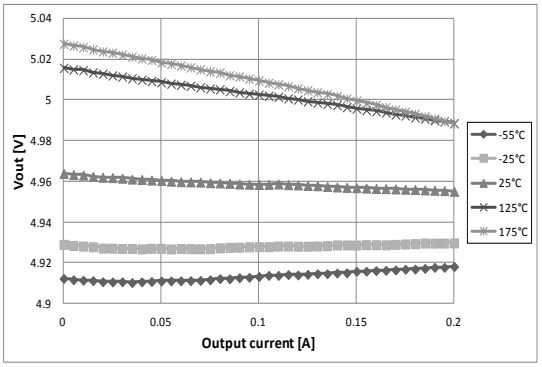


Figure 4: Output voltage load regulation (Vin = 30V)

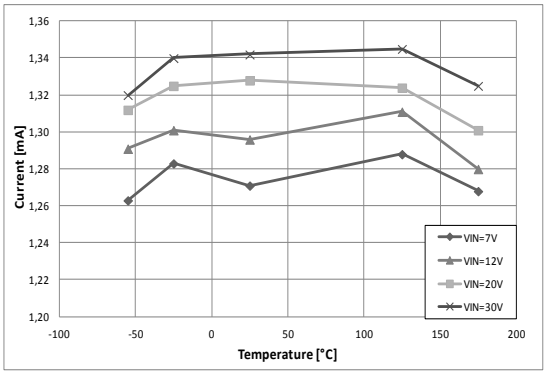


Figure 5: Quiescent current versus temp (Iout = 0 mA)

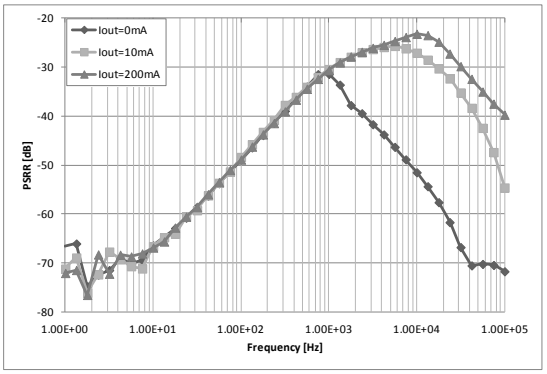


Figure 6: PSRR (Vin=10V, Cout= 4.7µF, Ta=25°C)

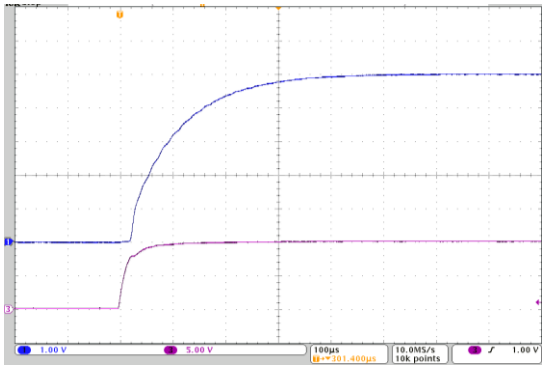


Figure 7: Start-up transient (Vin = 0 to 10V; Iout = 50mA,Ta = 175°C)(1:Vout,3:Vin)

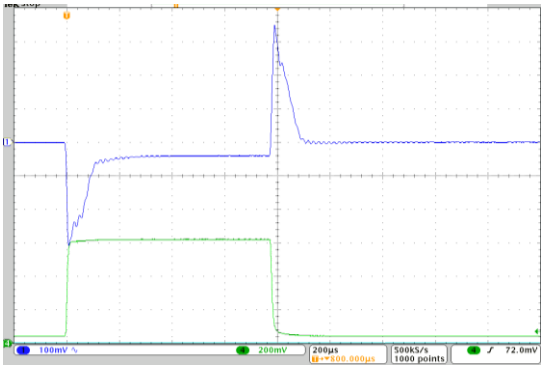


Figure 8: Response to load transient (10mA <-> 200 mA, 25mA/µs, Vin = 10V, Ta= 175°C, Cout = 4.7µF)

Typical Performance Characteristics (cnt'd)

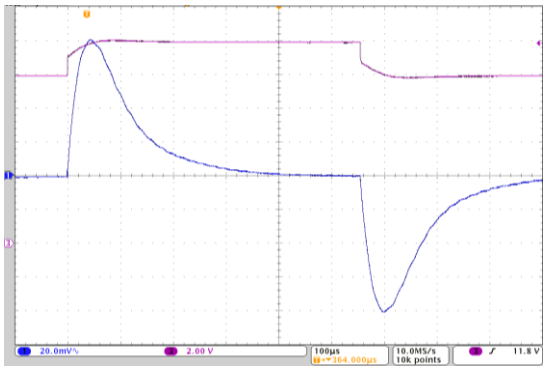


Figure 9: Response to line transient (Iout = 50 mA, Vin: 10 <-> 12V, 5V/µS, Ta= 175°C; Cout= 4.7µF) (1:Vout AC, 3:Vin)

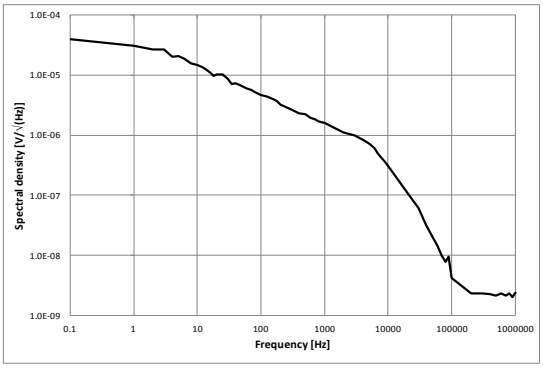


Figure 10: Output noise spectral density (Vin=8V, Iout= 0mA, Cout = 4.7 µF, Ta=25°C)

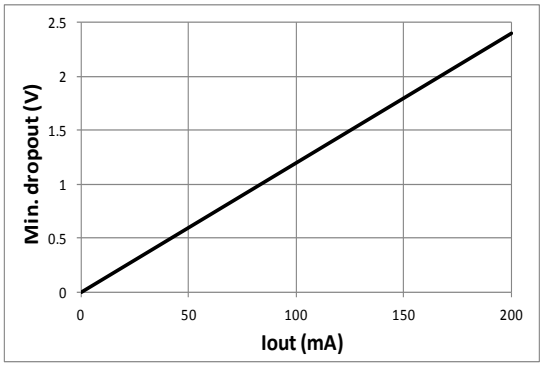


Figure 11: Dropout in function of output current (Tj=175°C)

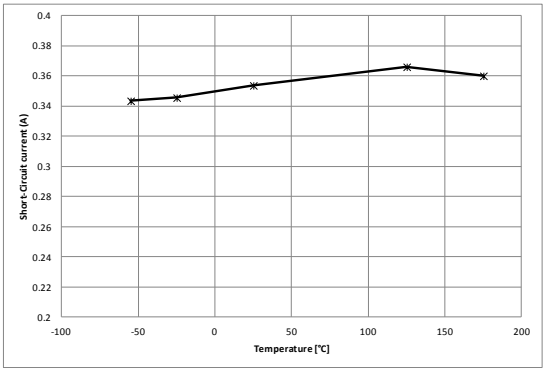
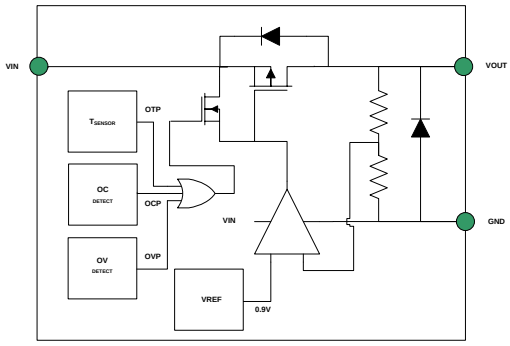


Figure 12: Current limit threshold in function of temperature (Vin = 7.4V)

Circuit Functionality

Functional Block diagram



A PMOS transistor controls the level of current flowing from Vin to Vout. An internal voltage reference of 0.9V (highly stable over the whole temperature range) provides the reference to which the voltage on the internal FB node is compared. The internal amplifier drives the gate of the PMOS and regulates Vout.

An on-chip temperature sensor with hysteresis monitors the die temperature; if this die temperature exceeds a predefined threshold, the PMOS transistor is disabled.

In addition, an overcurrent protection circuit is implemented which limits gracefully the output current to a pre-defined value.

In case of very fast load change (specifically a load decrease), the regulation loop might not regulate fast enough, leading to an output voltage increase. A specific overvoltage protection circuit clamps the output voltage to max 10% above the target output voltage.

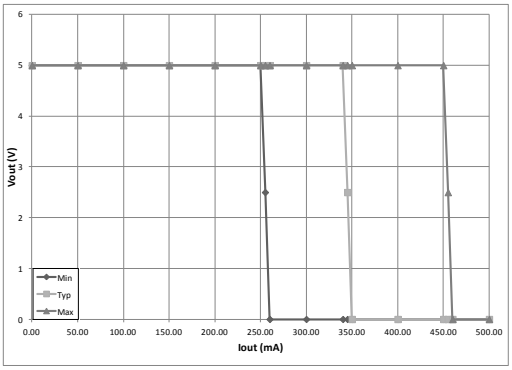
Input and output capacitance

CMT-ANTARES requires an output capacitor connected between Vout and GND to stabilize the internal control loop. The output capacitance value must be between 1 µF and 10 µF with ESR (equivalent series resistance) values between 0.01Ω and 1Ω.
Higher capacitor values offer improved behaviour in case of fast and high amplitude load transient.

There is no explicit requirement on the value of the input capacitance. Its size mainly depends on system aspects (impedance of the power source, distance between power source and CMT-ANTARES, amount and speed of the load transients ...). CISSOID recommends the use of a 1 µF input capacitance.

Current limit

In case the load connected to CMT-ANTARES would demand more than 200 mA current, the internal current limiter circuit will limit the maximum current delivered by CMT-ANTARES to 340mA (typical) whatever the output voltage (see graph below)



If the output current exceeds the recommended 200mA and depending on the conditions (dropout, junction-to-air thermal resistance), the internal thermal protection could get activated and CMT-ANTARES would then switch between 2 modes:

- Thermal protection active; no output current
- Thermal protection not active; output current internally limited.

In case of short-circuit, both current limiter and thermal protection will be activated and will protect the device. Endurance tests have been performed and showed that CMT-ANTARES did resist to a permanent short-circuit (Vin=30V) for at least 9 hours.

Safe operating area, power dissipation, and PCB layout considerations:

CMT-ANTARES requires adequate PCB layout in order to achieve efficient thermal dissipation, the minimization of the junction operating temperature, and maximizing the power dissipation taking advantage of the temperature behavior capability of CMT-ANTARES.

The junction-to-air overall thermal resistance of CMT-ANTARES in TO-263 package relies, to a large extend, on the implementation of the copper mounting pads that act as a heatsink for the integrated circuit. The design must take into consideration the size of the copper pad and its placement on either of the board surfaces, or both.

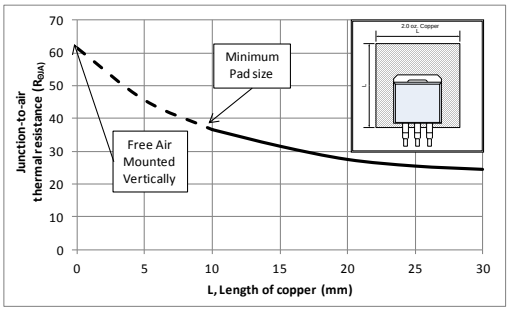
The maximum power dissipation is determined by the maximum junction temperature rating, the ambient temperature, and junction-to-ambient thermal resistance:

$$P_{DMAX} = (T_{JMAX} - T_A)/R_{\theta JA}$$

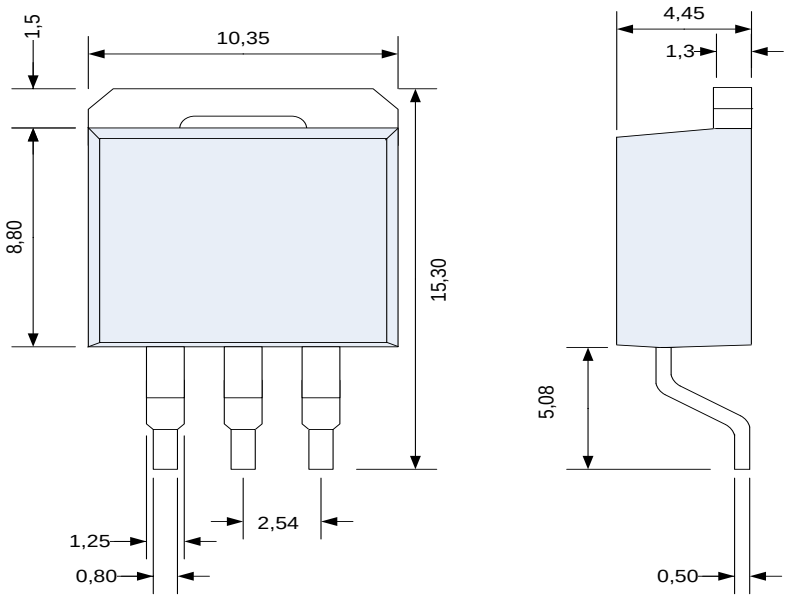
Where T_{JMAX}=175°C and $R_{\theta JA}=R_{\theta JC}+R_{\theta CA}$ with $R_{\theta JC}$=4.6°C/W and $R_{\theta CA}$ (to be determined) is function of the size of the copper mounting pad and thermal coupling to the TO-263.

The graph below indicates the junction-to-air thermal resistance of the TO-263 package mounted on PCB versus the surface of the copper thermal pads on the PCB.

The designer should refer to this graph when designing his PCB layout, taking into account his own operating configuration: expected power dissipation (calculated from maximum input voltage, the output voltage and the expected current flow thru CMT-ANTARES) and the maximum expected ambient operating temperature.



Package Dimensions



TO-263 physical dimensions (tolerance: +/- 0.2 mm)

Ordering Information

Product Name	Ordering Reference	Package	Marking
CMT-ANTARES	CMT-STA0389A-050-TO-263-T	TO-263	CMT-STA0389A-5V

Contact & Ordering

CISSOID S.A.

Headquarters and contact EMEA:	CISSOID S.A. – Rue Francqui, 3 – 1435 Mont Saint Guibert - Belgium T : +32 10 48 92 10 - F: +32 10 88 98 75 Email: sales@cissoid.com
Sales Representatives:	**Visit our website: http://www.cissoid.com**

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